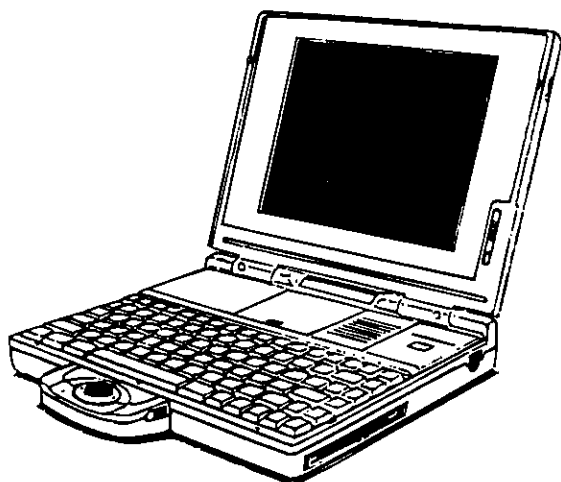


SHARP SERVICE MANUAL

CODE: 00ZPC8660SM1E



PERSONAL COMPUTER

MODEL PC-8660

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The PC-8660 is an upgrade version of the PC-8650, and differs from it in the following points:

- 1) LCD: 8.4 inch → 9.4 inch (1CCFT backlight)
- 2) CPU: 486DX-33MHz → 486DX2-50MHz
- 3) HDD: 200MB → 340MB
- 4) VGA controller: Made by Cirrus Made by Western Digital

This Service Manual describes only the differences. For the other points, refer to the Service Manual (Code: 00ZPC8650SM-E) of the PC-8650.

Parts marked with "△" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

[THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY.]

"BATTERY DISPOSAL"

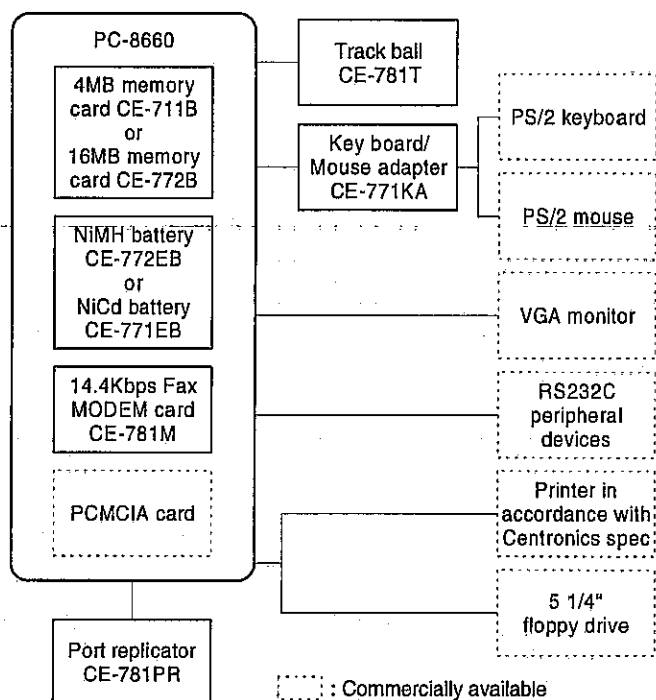
"CONTAINS NICKEL-CADMIUM RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

[THE FOLLOWING CAUTION IS APPLICABLE IN THE UNITED STATES ONLY.]

"BATTERY DISPOSAL"

"CONTAINS NICKEL-METAL HYDRIDE RECHARGEABLE BATTERY MUST BE RECYCLED OR DISPOSED OF PROPERLY. REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND DISPOSAL OPTIONS."

1. SYSTEM DIAGRAM



2.2 CRT CONTROLLER

The CRT Controller performs the following functions:

- Generates horizontal sync (HSYNC) and vertical sync (VSYNC) for the CRT display monitor
- Simultaneous CRT and dual flat panel display is performed using frame buffer architecture
- Hidden display timing registers meet the fixed display timing for the flat panel display
- CRT display screen refresh is maintained for the various display modes defined by the BIOS ROM resident firmware
- Performs video split screen refresh and screen size mapping

2.3 SEQUENCER

The Sequencer performs the following functions:

- Timing generator for the video memory cycles
- Character clock in the alphanumeric mode, and the dot clock in the graphics mode
- Arbitrates between the video display refresh, memory refresh, and CRT access of the video memory for CRT only, flat panel only, or simultaneous CRT and single panel displays
- Arbitrates between the video display refresh, frame buffer access, memory refresh, and CRT access of the video memory for simultaneous CRT and dual panel displays
- Arbitrates cursor pattern access to the off-screen display memory when the hardware cursor is activated
- Provides the write cache control for CPU memory write to the video display memory

FIGURE 2-1. SYSTEM BLOCK DIAGRAM

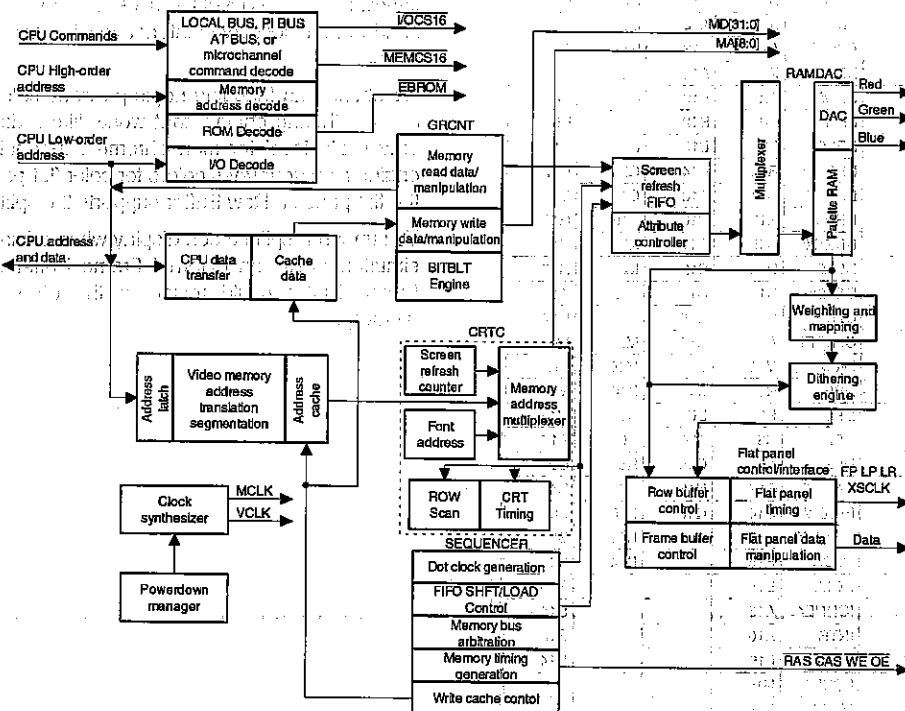
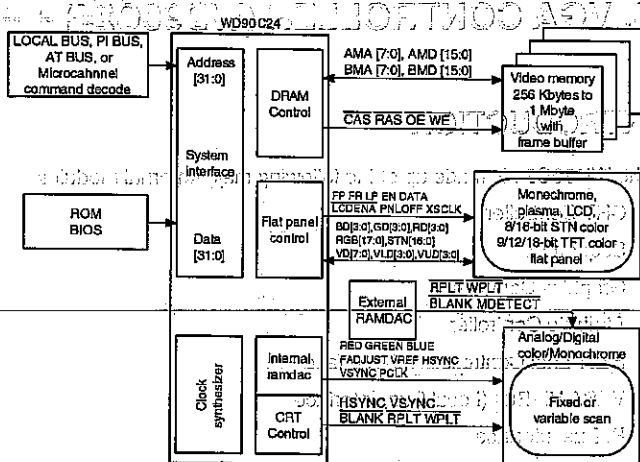
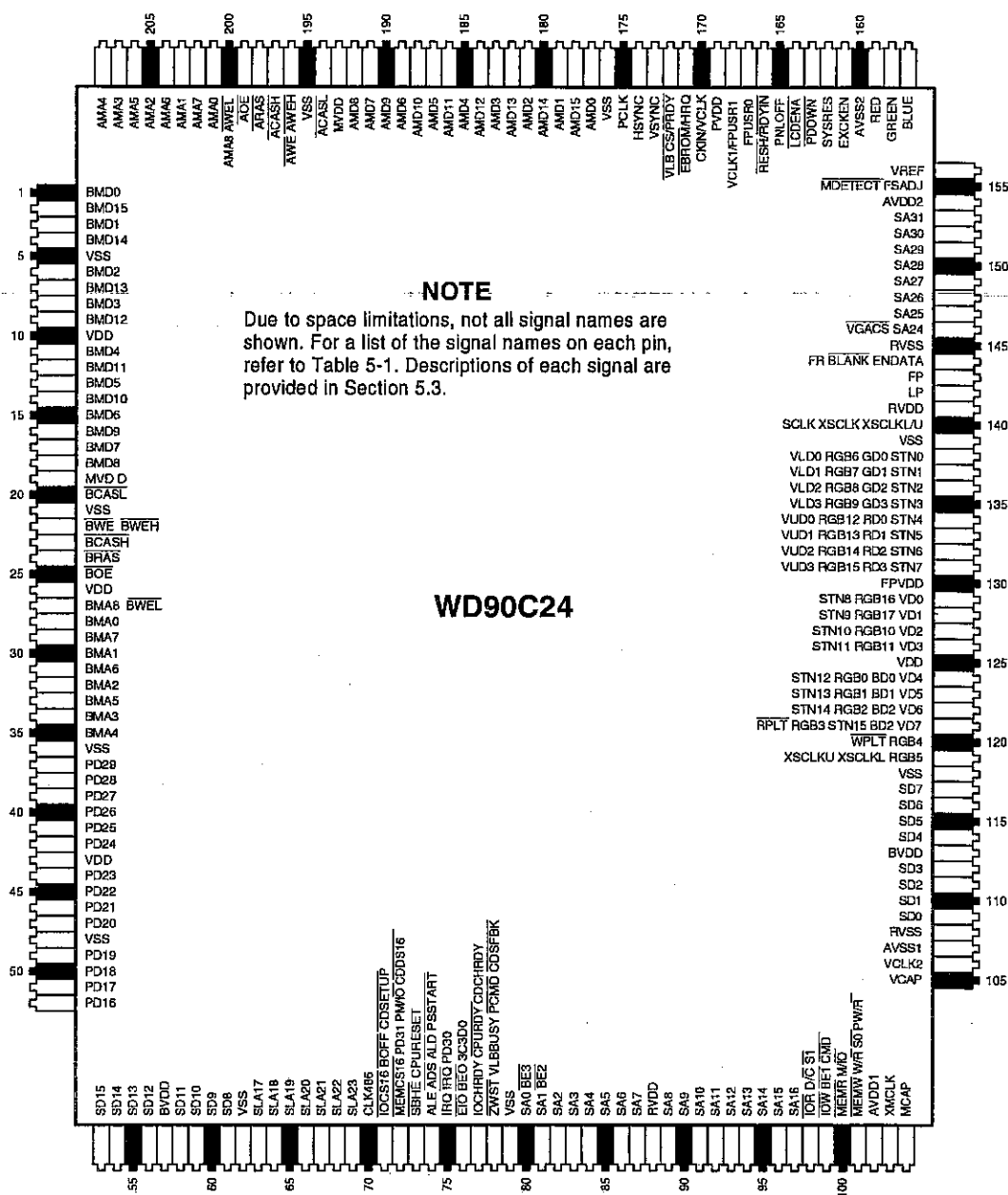


FIGURE 2-2. WE90C24 BLOCK DIAGRAM



5.3.1 Host Interface Pin Definitions

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
71	IOCS16	AT	Active Low Output	I/O Chip Select 16 In AT mode, this signal used to respond to the host to allow 16-bit access to the I/O bus.
		PI	Active Low Output	I/O Chip Select 16 In PI mode, since no 8-bit access will occur, this signal should be connected to VSS (ground) so it is always low.
	BOFF	LOC	Active Low Output	Bus Backoff Connects to the 80486 BOFF pin. When active low, the 80486 retracts its last cycle and enables other masters to control the local bus.
	CDSETUP	MC	Active Low Input	Card Setup This signal is driven by the host to individually select channel connector slots during system configuration.
72	MEMCS16	AT	Active Low Output	Memory Chip Select 16 Bits This line is used to respond to the host to enable 16-bit video memory data transfer.
	PM/I/O	PI	Active Low Input	PI Bus Memory or I/O Indicates the type of cycle currently executing on the PI bus. When high, the cycle is a memory operation, and when low the cycle is an Input/Output operation.
	PD31	LOC	Active High Input/Output	CPU Data Bus Bit 31 Provides bit 31 on the Local bus. This bit is combined with PD30 (pin 75), PD29: PD16, and SD15: SD0 to provide a 32-bit Local Data bus.
	CDDST16	MC	Active Low Output	Card Data Size 16 Bits Indicates that a 16-bit resource is available at the current address.
73	SBHE	AT PI MC	Active Low Input	System Byte High Enable Indicates a data transfer on the upper byte of the data bus (SD15:8).
	CPURESET	LOC	Active High Input	CPU Reset Local bus reset operation similar to AT bus RESET. This signal is used, primarily for the 386-based systems, to synchronize the divided-by-2 clock (internal working clock) on the Local Bus Interface between the WD90C24 and CPU. For 486-based systems this line should be tied to VSS (ground).

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
74	ALE	AT	Active High Input	Address Latch Enable Address bits SLA23:SLA17 are latched internally on the falling edge of the ALE.
	PSTART	PI	Active Low Input	PI Bus Start Signal Indicates the start of a PI bus cycle. This signal is used to latch the address bus and command lines PM/I/O, PWR, and VGACS.
	ADS	LOC	Active Low Input	Address Status Indicates the start of a Local bus cycle.
	ALD	MC	Active Low Input	Address Decode Latch In MicroChannel mode, this signal is not used and the line should be tied to VSS (ground).
75	IRQ	AT	Active High Output	Interrupt Request Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. When the end of Vertical Display occurs, this signal goes active, causing an interrupt. It stays active until CRTCl bit 4 clears it. In an AT system IRQ is usually not connected; but may be connected if desired.
		MC	Active Low Output	Interrupt Request Works similar to AT bus mode except that it is active low instead of active high.
	PD30	LOC	Active High Input/Output	CPU Data Bus Bit 30 Provides bit 30 on the Local bus. This bit is combined with PD31 (pin 72), PD29:PD16, and SD15:SD0 to provide a 32-bit Local Data bus.
	EIO	AT	Active Low Input	Enable I/O This signal is used to enable I/O address decoding and is connected directly to the system bus signal AE (address enable).
76	BE0	LOC	Active Low Input	Byte Enable 0 Byte enable for Local bus data bits SD7:SD0. BE3:BE1 are located on pins 80, 81, and 99, respectively.
	3C3D0	MC	Active High Input	Video Subsystem Enable Port When pulled high, this signal "wakes up" the WD90C24 in a manner identical to setting the Wake-up Register (3C3h) bit 0 to 1. This signal enables video memory and I/O address decoding.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
77	IOCHRDY	AT	Active High Output (Tristate)	I/O Channel Ready Indicates to the system processor that a memory access is completed. It is used to add wait states to the CPU bus cycles during video memory accesses. It may be pulled inactive by the WD90C24 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM.
	CPURDY	LOC	Active Low Output, (Tristate)	CPU Ready Ready signal to host processor or Local Bus controller for the termination of the current instruction cycles.
	CDCHRDY	MC	Active Low Output	Channel Ready This signal is normally active, and is driven not active by the WD90C24 to allow additional time to complete a channel cycle.
78	ZWST	AT	Active Low Output	Zero Wait State This signal can be used to generate zero wait states to the AT bus. This signal can be programmed by the PR33A register, bits 7, 6 in the following ways: A. $\overline{OWS} = 0$ if write cache is not full. B. $\overline{OWS} = 0$ if valid memory address decode AND write cache is not full. In this case $\overline{OWS} = 0$ should be ANDed externally with $\overline{MWR}$ to generate zero wait state strobe. C. $\overline{OWS} = 0$ if valid memory address decode AND write cache is not full, AND $\overline{MWR}$ is active. D. $\overline{OWS} = 0$ if valid memory address decode AND write cache is not full AND $\overline{MWR}$ is active, OR valid I/O address decode AND $\overline{IOW}$ is active.
	PCMD	PI	Active Low Input	PI Bus Cycle Command When asserted during write cycles, this signal indicates valid data on the PI bus, or that data bytes are ready to read. This signal must be asserted during read cycles to provide an output enable.
	VLBIBUSY	LOC	Active High Output, Tristate	VGA Local Bus Busy Signal Local bus interface busy signal.
	CDSFBK	MC	Active Low Output, (Tristate)	Card Selected Feedback Asserted by WD90C24 to acknowledge its selection. Cannot be asserted if $\overline{CDSETUP}$ is asserted.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
98	IOR	AT	Active Low Input	I/O Read I/O read strobe. This strobe signals an I/O read.
	D/C	LOC	Active High/Low Input	Data or Code Indicator Provides data or code indicator for the local bus.
	S1	MC	Active Low Input	S1 Cycle Decode MicroChannel status. Used with $\overline{S0}$, $\overline{M/I\overline{O}}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
	—	PI	Pulled Low	Pin not used
99	IOW	AT	Active Low Input	I/O Write I/O write strobe. This strobe signals an I/O write.
	BE1	LOC	Active Low Input	Byte Enable 1 Byte enable for Local bus data bits SD15:SD8. BE3, BE2, and BE0 are located on pins 80, 81, and 76, respectively.
	CMD	MC	Active Low Input	Command MicroChannel command. Used with $\overline{S0}$, $\overline{S1}$, and $\overline{M/I\overline{O}}$ to decode Microchannel bus cycles.
	—	PI	Pulled Low	Pin not used
100	MEMR	AT	Active Low Input	Memory Read This signal indicates that a memory read cycle is occurring. MEMR is internally gated with REFRESH.
	M/I $\overline{O}$	LOC	Active High/Low Input	Memory or I/O Cycle Local bus indicator for memory or I/O cycle. Low indicates I/O cycle and high indicates memory cycle.
	M/I $\overline{O}$	MC	Active High/Low Input	Memory or I/O Cycle MicroChannel memory or I/O cycle indicator. Low indicates I/O cycle; high indicates memory cycle. Used with $\overline{S0}$, $\overline{S1}$, and $\overline{CMD}$ to decode Microchannel bus cycles.
	—	PI	Pulled Low	Pin not used
101	MEMW	AT	Input	Memory Write This signal indicates that a memory write cycle is occurring. MEMW is internally gated with REFRESH.
	PW/R	PI	Active High/Low Input	Write or Read Cycle Indicates the type of access occurring on the PI bus. When high, the access is a write operation, and when low the access is a read operation.
	W/R	LOC	Active High/Low Input	Write or Read Cycle Indicates the type of access occurring on the Local bus. When high, the access is a write operation, and when low the access is a read operation.
	S0	MC	Active Low Input	S0 Cycle Decode MicroChannel status. Used with $\overline{S1}$, $\overline{M/I\overline{O}}$, and $\overline{CMD}$ to decode Microchannel bus cycles.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
162	RESET	AT, PI	Active High Input	Reset This signal resets the WD90C24. MCLK and VCLK should be connected to WD90C24 in order for the WD90C24 to initialize during Reset. Western Digital configuration bits are initialized at power-up reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors. The reset pulse width should be at least 10 MCLK periods.
	SYSRES	LOC	Active High Input	System Reset This signal resets the Local Bus Logic. Western Digital configuration bits are initialized at power-up/reset based on the logic level on the Display Buffer Memory bus as determined by pull-up/pull-down resistors.
	CHRESET	MC	Active High Input	Channel Reset Microchannel reset operation similar to AT bus RESET.
166	REFRESH	AT, PI, MC	Active Low Input	DRAM Refresh Initiates video buffer memory refresh. This signal must be inactive for memory reads or writes to occur.
	RDYIN	LOC	Active Low Input	Ready In This signal is used for synchronizing the local bus with the host processor.
171	EBROM	AT, MC	Active Low Output	Enable BIOS ROM This is an active low signal to enable BIOS ROM (C0000h - C7FFFh) if enabled by PR1(0). A write to WD90C24 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
	HRQ	LOC	Active High Input	Hold Request Indicates that a System Bus Request was received via a REFRESH, DMA, or MASTER signal. The host CPU responds by relinquishing the bus and asserting HOLD ACKNOWLEDGE.
172	PRDY	PI	Active Low Output	Bus Ready Terminates a PI-bus cycle. The PI bus default is not ready and a bus cycle continues until PRDY is asserted by holding it low until the rising edge of PCMD. The bus cycles is also terminated if PRDY is not asserted within a programmed time-out interval.
	VLBICS	LOC	Active Low Output, Tristate	Video Local bus Interface Chip Select Local bus chip select. This line is driven low only if the current cycle requires service by the Local bus interface. Otherwise, the line is tristated.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
153	SA31	LOC	Active High Input	Host System Address Bus (SA31 - SA25) These local address bits should be connected to the host CPU address bus. These bits are combined with SLA23:SLA17, SA24 and SA16:SA2 to provide a 30-bit Local Bus Address. Internal pullup resistors are provided on these pins.
152	SA30			
151	SA29			
150	SA28			
149	SA27			
148	SA26			Host System Address Bus (SA24) This bit is combined with SLA23:SLA17 and SA16:SA2 to provide a 30-bit Local Bus Address. An internal pullup resistor is provided on this pin.
147	SA25			
	VGACS	PI	Active Low Input	VGA Chip Select Indicates access to user-defined VGA memory address space. It is not asserted during I/O cycles.
69	SLA23	All	Active High Input	Host System/Latchable Address Bus (SLA23:SLA17) These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SA16:SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SA16:SA2 to provide a 30-bit Address Bus.
68	SLA22			
67	SLA21			
66	SLA20			
65	SLA19			
64	SLA18			Host System Address Bus (SA16 - SA2) These address bits should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, these bits are combined with SLA23:SLA17, SA1, and SA0 to provide a 24-bit address bus. For the Local bus interface, these bits are combined with SA31:SA24 and SLA23:SLA17 to provide a 30-bit Address Bus.
63	SLA17			
97	SA16	All	Active High Input	
96	SA15			
95	SA14			
94	SA13			
93	SA12			
92	SA11			
91	SA10			
90	SA9			
89	SA8			
87	SA7			
86	SA6			Host System Address bus (SA1) This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA0 to provide a 24-bit address bus.
85	SA5	AT, PI, MC	Active High Input	
84	SA4			
83	SA3			
82	SA2			Byte Enable 2 Local bus Byte Enable: for a 16-bit host CPU, BE2 = SA1; for a 32-bit host CPU, BE2 enables SD[23:16] BE3, BE1, and BE0 are located on pins 80, 99, and 76, respectively.
81	SA1			
	BE2	LOC	Active Low Input	

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
80	SA0	AT, PI, MC	Active High Input	Host System Address Bus (SA0) This address bit should be connected to the host CPU address bus. For the AT, PI, and MC bus interfaces, this bit is combined with SLA23:SLA17, SA16:SA2, and SA1 to provide a 24-bit address bus.
	BE3	LOC	Active Low Input	Byte Enable 3 Local bus Byte Enable: for a 16-bit host CPU, BE3 is tied to an external pullup resistor; for a 32-bit host CPU, BE3 enables SD[31:24]. BE2:BE0 are located on pins 81, 99, and 76, respectively.
53 54 55 56 58 59 60 61 117 116 115 114 112 111 110 109	SD15 SD14 SD13 SD12 SD11 SD10 SD9 SD8 SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0	All	Active High Input/Output	DATA BUS (SD15 - SD0) These bidirectional signals may be connected directly to a local data bus requiring less than 8 mA of source/sink, or may be connected through two external buffers. One external buffer for SD15:8 and the other external buffer for SD7:SD0. For the AT, PI, and MC bus interfaces, these bits provide a 16-bit system data bus. For the Local bus, these bits are combined with PD31 (pin 72), PD30 (pin 75), and PD29:PD16 to provide a 32-bit data bus.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

PIN NO.	MNEMONIC	BUS	TYPE	DESCRIPTION
37 38 39 40 41 42 44 45 46 47 49 50 51 52	PD29 PD28 PD27 PD26 PD25 PD24 PD23 PD22 PD21 PD20 PD19 PD18 PD17 PD16	LOC	Active High Input/Output	CPU Data Bus Bits (PD29:PD16) Provide bits 29:16 on the WD909C24 Local bus. These bits are combined with PD30 (pin 75), PD31 (pin 72), and SD15:SD0 to provide a 32-bit Local Data bus. The source/sink drive capability of these pins is 3 mA.
163	PDOWN	All	Active Low Input	Power-down Control This active low input signal is used to activate the various power-down modes in conjunction with system power management.

TABLE 5-2. HOST INTERFACE PIN SIGNAL DEFINITIONS

5.3.2 Display Buffer Memory Interface Pins

The display buffer memory interface is designed for connection of up to four 256Kx4 or one 256Kx16 fast-page-mode DRAMs. Also, memory data lines AMD[15:0] and BMD[15:0] are used to input configuration data (CNF[31:0]) at system power up and reset.

This section is divided into the following subsections,, which list the bus lines as follows:

- Bank A Video Memory Bus
- Bank B Video Memory Bus

5.3.2.1 Bank A Video Memory Bus

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK A VIDEO MEMORY DATA/CONFIGURATION BITS			
178	AMD15	I/O	Bank A Memory Data Bit 15:Configuration Bit CNF15
180	AMD14	I/O	Bank A Memory Data Bit 14:Configuration Bit CNF14
182	AMD13	I/O	Bank A Memory Data Bit 13:Configuration Bit CNF13
184	AMD12	I/O	Bank A Memory Data Bit 12:Configuration Bit CNF12
186	AMD11	I/O	Bank A Memory Data Bit 11:Configuration Bit CNF8
188	AMD10	I/O	Bank A Memory Data Bit 10:Configuration Bit CNF10
190	AMD9	I/O	Bank A Memory Data Bit 9:Configuration Bit CNF9
192	AMD8	I/O	Bank A Memory Data Bit 8:Configuration Bit CNF11
191	AMD7	I/O	Bank A Memory Data Bit 7:Configuration Bit CNF7
189	AMD6	I/O	Bank A Memory Data Bit 6:Configuration Bit CNF6
187	AMD5	I/O	Bank A Memory Data Bit 5:Configuration Bit CNF5
185	AMD4	I/O	Bank A Memory Data Bit 4:Configuration Bit CNF4
183	AMD3	I/O	Bank A Memory Data Bit 3:Configuration Bit CNF3
181	AMD2	I/O	Bank A Memory Data Bit 2:Configuration Bit CNF2
179	AMD1	I/O	Bank A Memory Data Bit 1:Configuration Bit CNF1
177	AMD0	I/O	Bank A Memory Data Bit 0:Configuration Bit CNF0
NOTE: AMD15 through AMD0 have internal 100 Kohm pullup resistors.			
BANK A VIDEO MEMORY ADDRESS BITS			
200	AMA8	Output	Bank A Memory Address Bit 8
	AWEL	Active Low Output	Write Enable Low Bank A Write Enable control for video memory buffer DRAM bank A. This signal is used in memory configurations Mode 4 and Mode 5.
202	AMA7	Output	Bank A Memory Address Bit 7
204	AMA6	Output	Bank A Memory Address Bit 6
206	AMA5	Output	Bank A Memory Address Bit 5
208	AMA4	Output	Bank A Memory Address Bit 4
207	AMA3	Output	Bank A Memory Address Bit 3
205	AMA2	Output	Bank A Memory Address Bit 2
203	AMA1	Output	Bank A Memory Address Bit 1
201	AMA0	Output	Bank A Memory Address Bit 0
NOTE: AMA8 through AMA0 form the primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			

TABLE 5-3. BANK A VIDEO MEMORY SIGNALS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK A VIDEO MEMORY CONTROL SIGNALS			
194	ACASL	Active Low Output	CAS Bank A Low Lower column address strobe for video memory buffer DRAM bank A.
196	AWE	Active Low Output	Write Enable Bank A Write Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used this is the DRAM write enable output.
	AWEH		Write Enable High Bank A Write Enable control for video memory buffer DRAM bank A. This signal is used in memory configurations Mode 4 and Mode 5.
197	ACASH	Active Low Output	CAS Bank A High Upper column address strobe for video memory buffer DRAM bank A.
198	ARAS	Active Low Output	RAS Bank A Row address strobe for video memory buffer DRAM bank A.
199	AOE	Active Low Output	Output Enable Bank A Output Enable control for video memory buffer DRAM bank A. When a 256Kx16 DRAM is used, this is the DRAM output enable strobe.

TABLE 5-3. BANK A VIDEO MEMORY SIGNALS

5.3.2.2 Bank B Video Memory Bus

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK B VIDEO MEMORY DATA BITS/CONFIGURATION BITS			
2	BMD15	I/O	Bank B Memory Data Bit 15: Configuration Bit CNF31
4	BMD14	I/O	Bank B Memory Data Bit 14: Configuration Bit CNF30
7	BMD13	I/O	Bank B Memory Data Bit 13: Configuration Bit CNF29
9	BMD12	I/O	Bank B Memory Data Bit 12: Configuration Bit CNF28
12	BMD11	I/O	Bank B Memory Data Bit 11: Configuration Bit CNF27
14	BMD10	I/O	Bank B Memory Data Bit 10: Configuration Bit CNF26
16	BMD9	I/O	Bank B Memory Data Bit 9: Configuration Bit CNF25
18	BMD8	I/O	Bank B Memory Data Bit 8: Configuration Bit CNF24
17	BMD7	I/O	Bank B Memory Data Bit 7: Configuration Bit CNF23
15	BMD6	I/O	Bank B Memory Data Bit 6: Configuration Bit CNF22
13	BMD5	I/O	Bank B Memory Data Bit 5: Configuration Bit CNF21
11	BMD4	I/O	Bank B Memory Data Bit 4: Configuration Bit CNF20
8	BMD3	I/O	Bank B Memory Data Bit 3: Configuration Bit CNF19
6	BMD2	I/O	Bank B Memory Data Bit 2: Configuration Bit CNF18
3	BMD1	I/O	Bank B Memory Data Bit 1: Configuration Bit CNF17
1	BMD0	I/O	Bank B Memory Data Bit 0: Configuration Bit CNF16

NOTE: BMD15 through BMD0 have internal 100 Kohm pullup resistors.

TABLE 5-4. BANK B VIDEO MEMORY SIGNALS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
BANK B VIDEO MEMORY ADDRESS BITS			
27	BMA8	Output	Bank Memory Address Bit 8
	BWEL	Active Low Output	Write Enable Low Bank B Write Enable control for video memory buffer DRAM bank B. This signal is used in memory configurations Mode 3, Mode 4, and Mode 5.
29	BMA7	Output	Bank B Memory Address Bit 7
31	BMA6	Output	Bank B Memory Address Bit 6
33	BMA5	Output	Bank B Memory Address Bit 5
35	BMA4	Output	Bank B Memory Address Bit 4
34	BMA3	Output	Bank B Memory Address Bit 3
32	BMA2	Output	Bank B Memory Address Bit 2
30	BMA1	Output	Bank B Memory Address Bit 1
28	BMA0	Output	Bank B Memory Address Bit 0
BANK B VIDEO MEMORY ADDRESS CONTROL SIGNALS			
20	BCASL	Active Low Output	CAS Bank B Low Lower column address strobe for video memory buffer DRAM bank B.
22	BWE	Active Low Output	Write Enable Bank B Write Enable control for video memory buffer DRAM bank B.
	BWEH		Write Enable High Bank B Write Enable control for video memory buffer DRAM bank B. This signal is used in memory configurations Mode 3, Mode 4, and Mode 5.
23	BCASH	Active Low Output	CAS Bank B High Upper column address strobe for video memory buffer DRAM bank B.
24	BRAS	Active Low Output	RAS Bank B Row address strobe for video memory buffer DRAM bank B.
25	BOE	Active Low Output	Output Enable Bank B Output Enable control for video memory buffer DRAM bank B.

TABLE 5-4. BANK B VIDEO MEMORY SIGNALS

5.3.3 RAMDAC/CRT Interface Pins

Internal RAMDAC interface pins are described in the following table.

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
155	FSADJ	Analog Input	Full Scale Adjust A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DACs. FSADJ if PR18, bit 7 = 0 (internal RAMDAC mode). CAUTION: Do not ground this pin.
	MDETECT	Active Low Input	Monitor Detect When PR18, bit 7 = 1 (external RAMDAC mode), this pin is used as a monitor detect input. The result of this input is read from 3C2h bit 4. MDETECT if PR18, bit 7 = 1 (external RAMDAC mode).
156	VREF	Analog Input	Voltage Reference Input An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC.
157	BLUE	Analog Output	Blue Current Output High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
158	GREEN	Analog Output	Green Current Output High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.

TABLE 5-6. CLOCK GENERATION INTERFACE PIN TABLE

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
159	RED	Analog Output	Red Current Output High impedance current source can directly drive a double-terminated 75-Ohm coaxial cable.
173	VSNC	Active High Output	CRT Vertical Sync VSNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register (3C2h).
174	HSNC	Active High Output	CRT Horizontal Sync HSNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register (3C2h).
175	PCLK	Active High Input/ Output	Pixel Clock Video pixel clock output used by the external RAMDAC to latch pixel data from the WD90C24 controller's video output bus into an external RAMDAC or panel interface. Pixel data from the WD90C24 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or panel interface by the falling edge of PCLK. In Auxiliary Video Extender (AVE) Mode, this pin provides the input for the internal RAMDAC PCLK signal. (PR66 bit 7 is set to 1.)

TABLE 5-5. INTERNAL DAC INTERFACE PINS

5.3.4 Clock Generation Interface Pins

Clock generation interface pins are described in the following table.

PIN	MNEMONIC	TYPE	DESCRIPTION
70	CLK486	Input	CPU Clock Provides the clock input for the Local bus. This pin has an internal 100 Kohm pulldown resistor.
103	XMCLK	Input	External Memory Clock In external clock mode, this signal is the MCLK input. In internal clock mode this pin is used for test.
104	MCAP	Analog Input	Analog Input Connects to discrete filter network.
105	VCAP	Analog Input	Analog Input Connects to discrete filter network.
106	VCLK2	Input/ Output	Video Clock 2 In external PCLK clock mode, VCLK2 is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types. When CNF3 is set to 1, this pin outputs either 3C2h bit 3 or PR2 bit 1. In internal clock mode this pin is used for test.
161	EXCKEN	Active High Input	External Clock Enable Asserted to select external clock mode

TABLE 5-6. CLOCK GENERATION INTERFACE PIN TABLE

PIN	MNEMONIC	TYPE	DESCRIPTION
168	VCLK1	Input/ Output	Video Clock 1 In external PCLK clock mode, VCLK1 is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types. When CNF3 is set to 1, this pin outputs either 3C2h bit 2 or the external PCLK latch enable signal.
	FPUSR1	Output	User Programmable Output 1 In internal PCLK mode, VCLK1 is an output configured as FPUSR1. FPUSR1 is a panel interface signal that can be programmed by the user to initiate or confirm an action.
170	CKIN	Input	System Clock Input In internal PCLK mode, CKIN provides the CPU clock (14.318 MHz), which is the default mode. This pin has an internal 100 Kohm pulldown resistor.
	VCLK	Input	External Video Clock In external PCLK clock mode, VCLK is one of three possible video clock inputs to the WD90C24. The three clock inputs (VCLK, VCLK1, and VCLK2) are internally selected to provide video shift clock rates for various screen formats and display types.

TABLE 5-6. CLOCK GENERATION INTERFACE PIN TABLE

5.3.5 Panel Interface Pins

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
119	XSCKL	Active High Output	External Shift Clock Lower Used for 8-bit STN color LCD (Seiko)
	XSCKU		External Shift Clock Upper Used for 8-bit STN color LCD (Sharp)
	XSCLK		External Shift Clock Used for 16-bit STN color LCD
	RGB5		Red Green Blue Bit 5 Data bit 5 for 18-bit TFT color LCD
120	WPLT	Active Low Output	Write Palette If not configured for a TFT 18-bit interface, WPLT is the write pulse to the external RAMDAC or equivalent circuit.
	RGB4	Active High Output	Red Green Blue Bit 4 Data bit 4 for 18-bit TFT color LCD
121	RPLT	Active Low Output	Read Palette If not configured for TFT or color STN interface, RPLT is the active low read pulse to the external RAMDAC or equivalent circuit.
	RGB3	Active High Output	Red Green Blue Bit 3 Data bit 3 for 18-bit TFT color LCD
	STN15		Super Twisted Nematic Bit 15 Data bit 15 for 16-bit STN color LCD, single panel
	BD3		Blue Data Bit 3 Data Bit 3 for 12-bit TFT color LCD
	UD7		Upper Video Data Bit 7 Data bit 7 for the upper 8-bits of a 16-bit STN color LCD, dual panel

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
122	RGB2	Active High Output	Red Green Blue Bit 2 Data bit 2 for 18-bit TFT color LCD
	STN14		Super Twisted Nematic Bit 14 Data bit 14 for 16-bit STN color LCD, single panel
	BD2		Blue Data Bit 2 Data Bit 2 for 9-bit and 12-bit TFT color LCD
	UD6		Upper Video Data Bit 6 Data bit 6 for the upper 8-bits of a 16-bit STN color LCD, dual panel
123	RGB1	Active High Output	Red Green Blue Bit 1 Data bit 1 for 18-bit TFT color LCD
	STN13		Super Twisted Nematic Bit 13 Data bit 13 for 16-bit STN color LCD, single panel
	BD1		Blue Data Bit 1 Data Bit 1 for 9-bit and 12-bit TFT color LCD
	UD5		Upper Video Data Bit 5 Data bit 5 for the upper 8-bits of a 16-bit STN color LCD, dual panel
124	RGB0	Active High Output	Red Green Blue Bit 0 Data bit 0 for 18-bit TFT color LCD
	STN12		Super Twisted Nematic Bit 12 Data bit 12 for 16-bit STN color LCD, single panel
	BD11		Blue Data Bit 0 Data Bit 0 for 3-bit, 9-bit, and 12-bit TFT color LCD
	UD4		Upper Video Data Bit 4 Data bit 4 for the upper 8-bits of a 16-bit STN color LCD, dual panel
126	RGB11	Active High Output	Red Green Blue Bit 11 Data bit 11 for 18-bit TFT color LCD
	STN11		Super Twisted Nematic Bit 11 Data bit 11 for 16-bit STN color LCD, single panel
	UD3		Upper Video Data Bit 3 Data bit 3 for the upper 8-bits of a 16-bit STN color LCD, dual panel
127	RGB10	Active High Output	Red Green Blue Bit 10 Data bit 10 for 18-bit TFT color LCD
	STN10		Super Twisted Nematic Bit 10 Data bit 10 for 16-bit STN color LCD, single panel
	UD2		Upper Video Data Bit 2 Data bit 2 for the upper 8-bits of a 16-bit STN color LCD, dual panel
128	RGB17	Active High Output	Red Green Blue Bit 17 Data bit 17 for 18-bit TFT color LCD
	STN9		Super Twisted Nematic Bit 9 Data bit 9 for 16-bit STN color LCD, single panel
	UD1		Upper Video Data Bit 1 Data bit 1 for the upper 8-bits of a 16-bit STN color LCD, dual panel
129	RGB16	Active High Output	Red Green Blue Bit 16 Data bit 16 for 18-bit TFT color LCD
	STN8		Super Twisted Nematic Bit 8 Data bit 8 for 16-bit STN color LCD, single panel
	UD0		Upper Video Data Bit 0 Data bit 0 for the upper 8-bits of a 16-bit STN color LCD, dual panel

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
131	RGB15	Active High Output	Red Green Blue Bit 15 Data bit 15 for 18-bit TFT color LCD
	RD3		Red Data Bit 3 Data bit 3 for 12-bit TFT color LCD
	STN7		Super Twisted Nematic Bit 7 Data bit 7 for 8-bit and 16-bit STN color LCD, single panel
	LD7		Lower Video Data Bit 7 Data bit 7 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD7		Video Data Bit 7 Data bit 7 for the 8-bit external RAMDAC interface
	VUD3		UPPER PANEL DATA BIT 3 In a monochrome dual-panel LCD interface, VUD3 through VUD0 are used for the upper panel data bus. In a monochrome single panel LCD interface these pins also provide video data to the panel. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits of pixel video outputs to the RAMDAC. Fourth Pixel VUD3 Pin 131 Third Pixel VUD2 Pin 132 Second Pixel VUD1 Pin 133 First Pixel VUD0 Pin 134
	P7		In Auxiliary Video Extender (AVE) Mode, this pin provides the P7 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)
132	RGB14	Active High Output	Red Green Blue Bit 14 Data bit 14 for 18-bit TFT color LCD.
	RD2		Red Data Bit 2 Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN6		Super Twisted Nematic Bit 6 Data bit 6 for 8-bit and 16-bit STN color LCD, single panel
	LD6		Lower Video Data Bit 6 Data bit 6 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD6		Video Data Bit 6 Data bit 6 for the 8-bit external RAMDAC interface
	VUD2		Upper Panel Data Bit 2 Refer to VUD3, pin 131
	P6	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P6 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)
133	RGB13	Active High Output	Red Green Blue Bit 13 Data bit 13 for 18-bit TFT color LCD.
	RD1		Red Data Bit 1 Data bit 1 for 9-bit and 12-bit TFT color LCD
	STN5		Super Twisted Nematic Bit 5 Data bit 5 for 8-bit and 16-bit STN color LCD, single panel
	LD5		Lower Video Data Bit 5 Data bit 5 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD5		Video Data Bit 5 Data bit 5 for the 8-bit external RAMDAC interface
	VUD1		Upper Panel Data Bit 1 Refer to VUD3, pin 131
	P5	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P5 input for the internal RAMDAC. (PR66 bit 7 is set to 1.)

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
134	RGB12	Active High Output	Red Green Blue Bit 12 Data bit 12 for 18-bit TFT color LCD
	RD0		Red Data Bit 0 Data Bit 0 for 9-bit and 12-bit TFT color LCD
	STN4		Super Twisted Nematic Bit 4 Data bit 4 for 8-bit and 16-bit STN color LCD, single panel
	LD4		Lower Video Data Bit 4 Data bit 4 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD4		Video Data Bit 4 Data bit 4 for the 8-bit external RAMDAC interface
	VUD0		Upper Panel Data Bit 0 Refer to VUD3, pin 131
	P4	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P4 input for the internal RAMDAC.
135	RGB9	Active High Output	Red Green Blue Bit 9 Data bit 9 for 18-bit TFT color LCD.
	GD3		Green Data Bit 3 Data bit 3 for 12-bit TFT color LCD
	STN3		Super Twisted Nematic Bit 3 Data bit 3 for 8-bit and 16-bit STN color LCD, single panel
	LD3		Lower Video Data Bit 3 Data bit 3 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD3		Video Data Bit 7 Data bit 7 for the 8-bit external RAMDAC interface
	VLD3		Lower Panel Data Bit 3 In a dual-panel LCD interface, VLD3 through VLD0 are used for the lower panel data bus. In a 4-bit plasma interface, they are reserved. In an 8-bit plasma interface they provide the second pixel of video data to the panel. In a CRT interface, they are the lower four bits of pixel video outputs to the RAMDAC.
	P3	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P3 input for the internal RAMDAC.
136	RGB8	Active High Output	Red Green Blue Bit 8 Data bit 8 for 18-bit TFT color LCD.
	GD2		Green Data Bit 2 Data bit 2 for 9-bit and 12-bit TFT color LCD
	STN2		Super Twisted Nematic Bit 2 Data bit 2 for 8-bit and 16-bit STN color LCD, single panel
	LD2		Lower Video Data Bit 2 Data bit 2 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD2		Video Data Bit 2 Data bit 2 for the 8-bit external RAMDAC interface
	VLD2		Lower Panel Data Bit 2 Refer to VLD3, pin 135
	P2	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P2 input for the internal RAMDAC.

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
137	RGB7	Active High Output	Red Green Blue Bit 7 Data bit 7 for 18-bit TFT color LCD.
	GD1		Green Data Bit 1 Data bit 1 for 9-bit and 12-bit TFT color LCD
	GD0		Green Data Bit 0 Data bit 0 for 3-bit TFT color LCD
	STN1		Super Twisted Nematic Bit 1 Data bit 1 for 8-bit and 16-bit STN color LCD, single panel
	LD1		Lower Video Data Bit 1 Data bit 1 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD1		Video Data Bit 1 Data bit 1 for the 8-bit external RAMDAC interface
	VLD1		Lower Panel Data Bit 1 Refer to VLD3, pin 135
138	P1	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P1 input for the internal RAMDAC.
	RGB6	Active High Output	Red Green Blue Bit 6 Data bit 6 for 18-bit TFT color LCD.
	GD0		Green Data Bit 0 Data bit 0 for 9-bit and 12-bit TFT color LCD
	STN0		Super Twisted Nematic Bit 0 Data bit 0 for 8-bit and 16-bit STN color LCD, single panel
	LCD0		Lower Video Data Bit 0 Data bit 0 for the lower 8-bits of a 16-bit STN color LCD, dual panel
	VD0		Video Data Bit 0 Data bit 0 for the 8-bit external RAMDAC interface
	VLD0		Lower Panel Data Bit 0 Refer to VLD3, pin 135
140	P0	Active High Input	In Auxiliary Video Extender (AVE) Mode, this pin provides the P0 input for the internal RAMDAC.
	XSCLK	Active High Output	X Driver Shift Clock In a single or dual panel interface, this signal is used to shift the data into the X-driver.
	XSCLKL		External Shift Clock Lower Used for 8-bit STN color LCD (Sharp)
	XSCLKU		External Shift Clock Upper Used for 8-bit STN color LCD (Seiko)
142	SCLK	Active High Output	Shift Clock In a single panel interface, this signal is used to shift the panel data into the display drivers.
	LP		Latch Pulse The LP output is intended to be used by a panel to latch all the current panel data into the current scan line of the panel.
	FP		Frame Pulse FP is output as an indication to attached panels that a frame has begun.

TABLE 5-7. PANEL INTERFACE PINS

PIN NO.	MNEMONIC	TYPE	DESCRIPTION
144	FR	Active High Output	Frame Rate Whenever the WD90C24 is operating in any panel mode, FR is a free-running clock, which is intended to be connected to FR inputs on some LCD panels. Frequency of its signal is programmable and is controlled by setting PR62.
	BLANK	Active Low Input/Output	Blanking Control BLANK is the standard analog VGA RAMDAC blanking signal. This signal is an output when the WD90C24 is operating in any CRT modes. In Auxiliary Video Extender (AVE) Mode, this pin provides the BLANK input for the internal RAMDAC.
	ENDATA	Active High Output	Enable Data This is a data enable output for panels such as TFT. In a plasma interface, it is an "enable video" signal.
164	LCDENA	Active Low Output	LCD Panel Enable Provides the power off signal to the bias supply circuit of an LCD panel. The LCDENA signal is used as a power enable/disable to the high voltage bias inverter of a panel, and is tied to the WD90C24 controller's power management circuit. The WD90C24 sequences this signal as part of the panel power-on/power-off procedures designed to protect panel power circuit. A high at this output indicates power-off to the panel and a low power-on.
165	PNLOFF	Active High Output	Panel Power Off PNLOFF can be used to control the power supply for the attached panel. When a panel is enabled (PR19 bit 4 is set to 1), setting PR57 bit 2 to 0 causes the PNLOFF signal to be driven low. Setting PR57 to 1 causes a high level to appear at PNLOFF.
167	FPUSR0	Output	User Programmable Output 0 This line can be programmed by the user to initiate or confirm an action.
168	FPUSR1	Output	User Programmable Output 1 This line can be programmed by the user to initiate or confirm an action. NOTE: In external PCLK mode, FPUSR1 is configured as VCLK1.

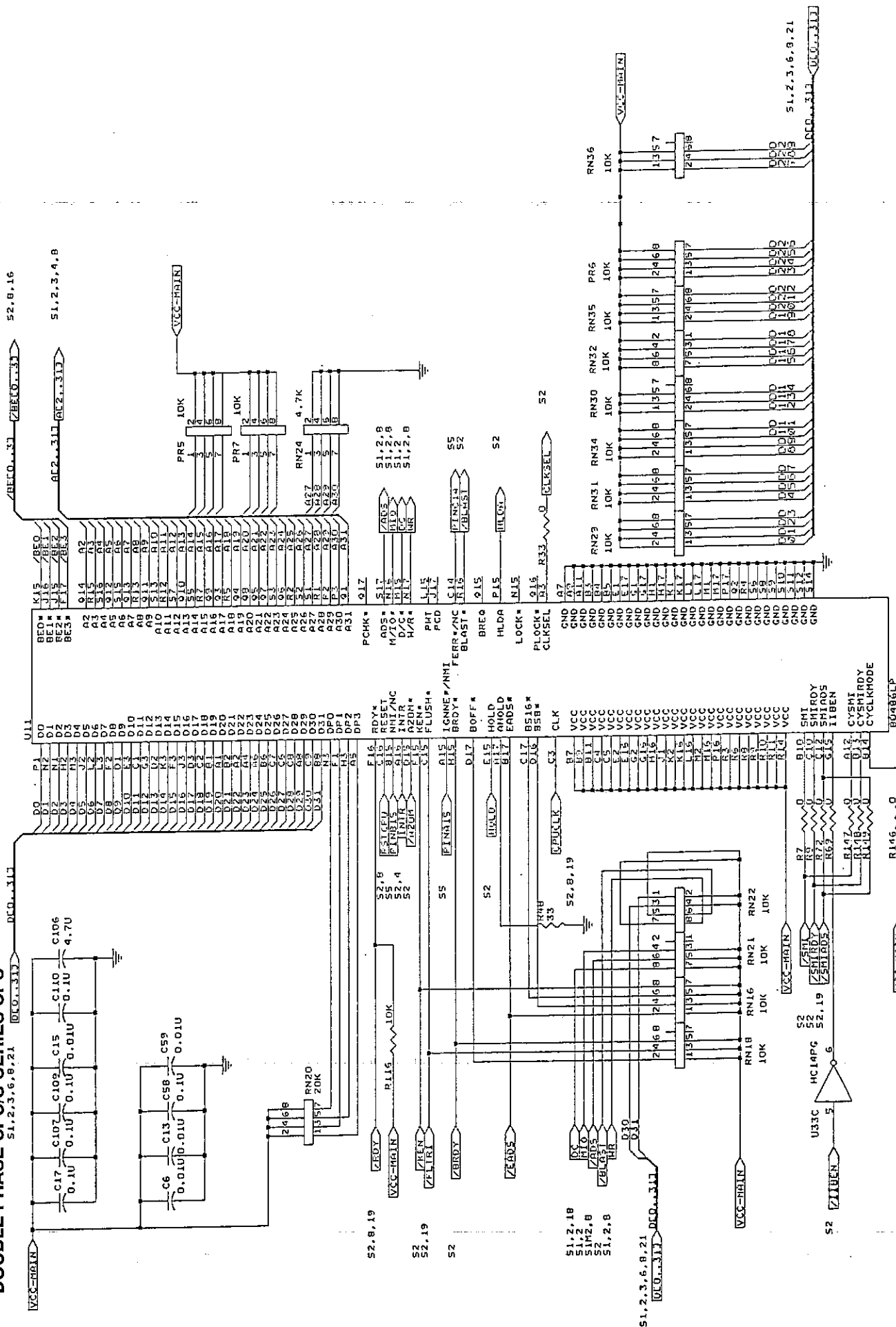
TABLE 5-7. PANEL INTERFACE PINS

5.3.6 Power and Ground Pins

PIN NO.	MNEMONIC	DESCRIPTION
5, 21, 36, 48, 62, 79, 118, 139, 176, 195	VSS	Ground VSS=0V
10, 26, 43, 125	VDD	Main VDD Power to Core Logic
19, 193	MVDD	Memory Interface VDD Supply
57, 113	BVDD	System Bus Interface VDD Supply
88, 141	RVDD	RAM Filtered Palette VDD Supply
108, 145	RVSS	RAM Palette VSS Ground
102	AVDD1	PCLK Analog Power
107	AVSS1	PCLK Analog Ground
130	FPVDD	Panel Interface VDD Supply
154	AVDD2	RAMDAC Analog Power
160	AVSS2	RAMDAC Analog Ground
169	PVDD	Power-Down Section VDD Supply

TABLE 5-8. POWER AND GROUND SIGNAL DEFINITIONS

5. CIRCUIT DIAGRAM DOUBLE PHASE CPU/S-SERIES CPU



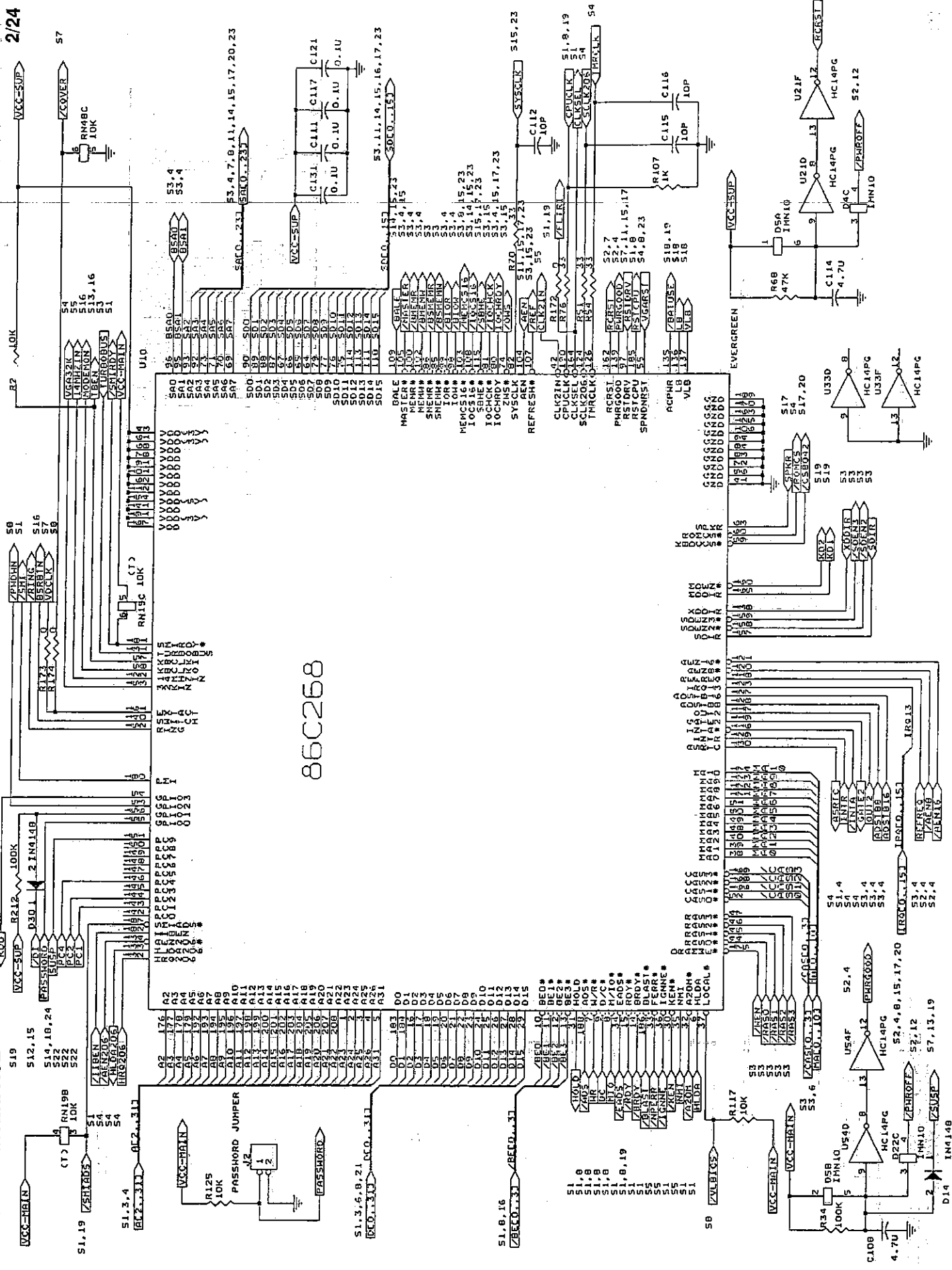
INTEL 5 SERIES : R7, R9, 69, R72 INSTALLED CYEOX 5 SERIES :

R149, R147, R148 INSTALLED

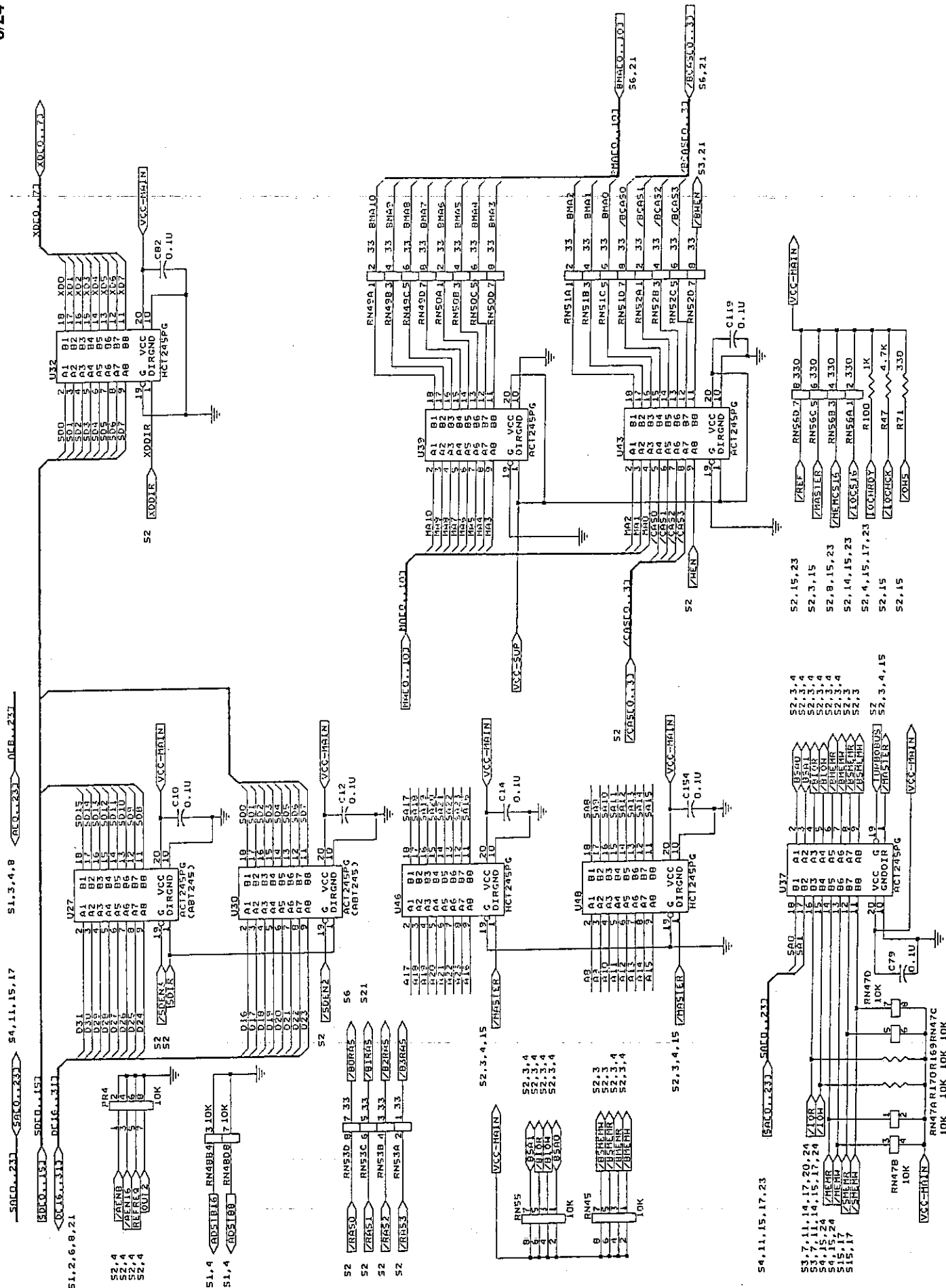
R8 NOT INSTALLED

R146 INSTALLED FOR OVERDRIVE CPU

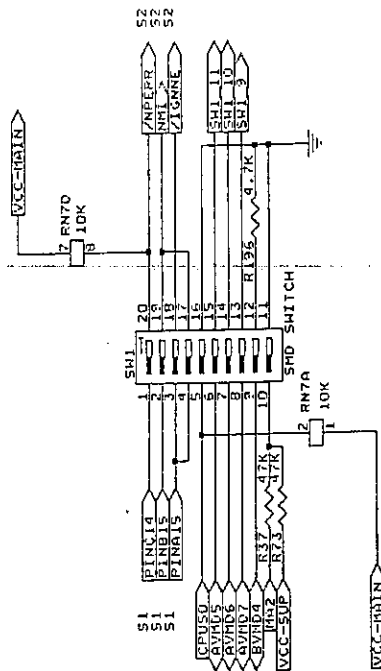
EVERGREEN INTERFACE



51.3,4,8







CPUS0	CPUS1	CPUS2	CPUCLK2(PIN16)
1	0	1	66.66M
0	0	1	50M

SYSTEM DRAM

EMACO...102 EMACO...103 53,21

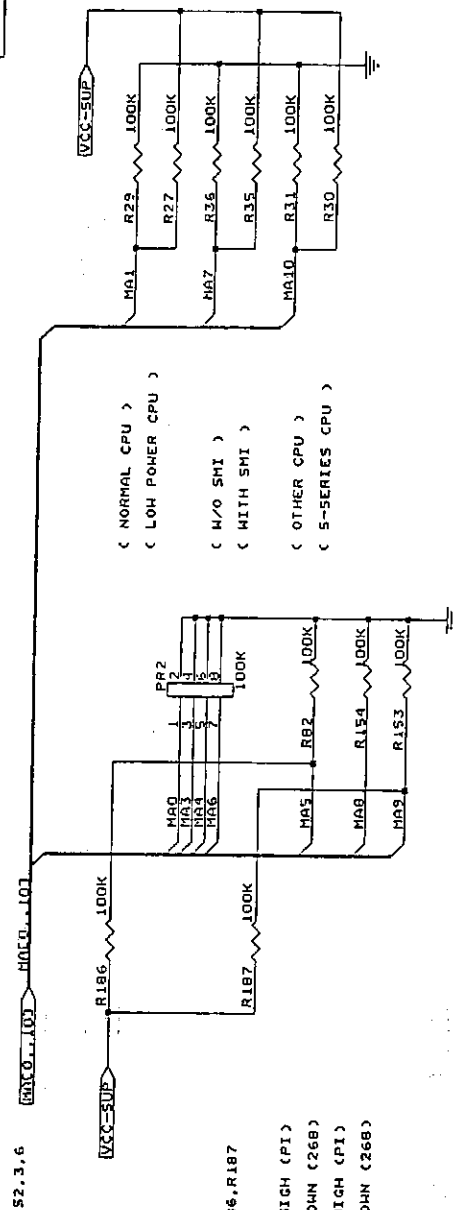
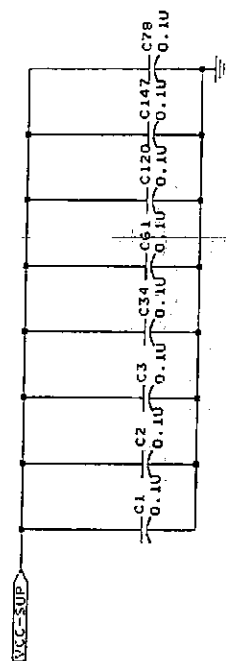
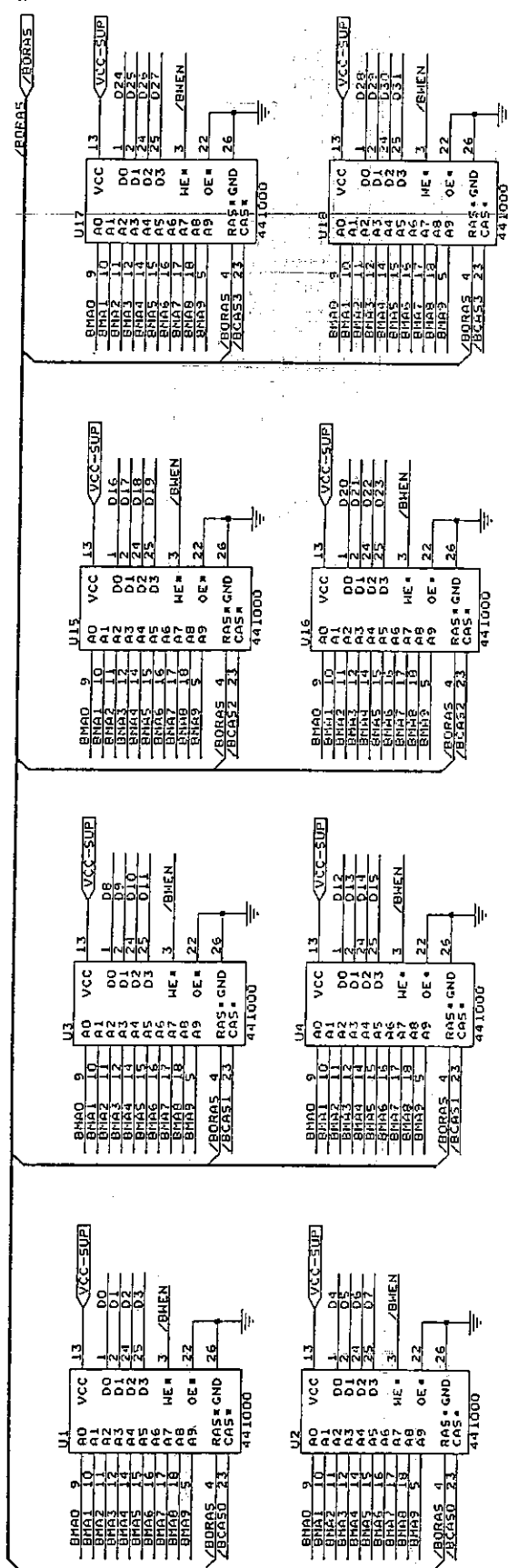
53,21

/BCASCO..37

050...317 050...317 51,2,3,8,21

53,21

✓ROEAS ✓BORAS S3



NO MOUNT : R186, R187

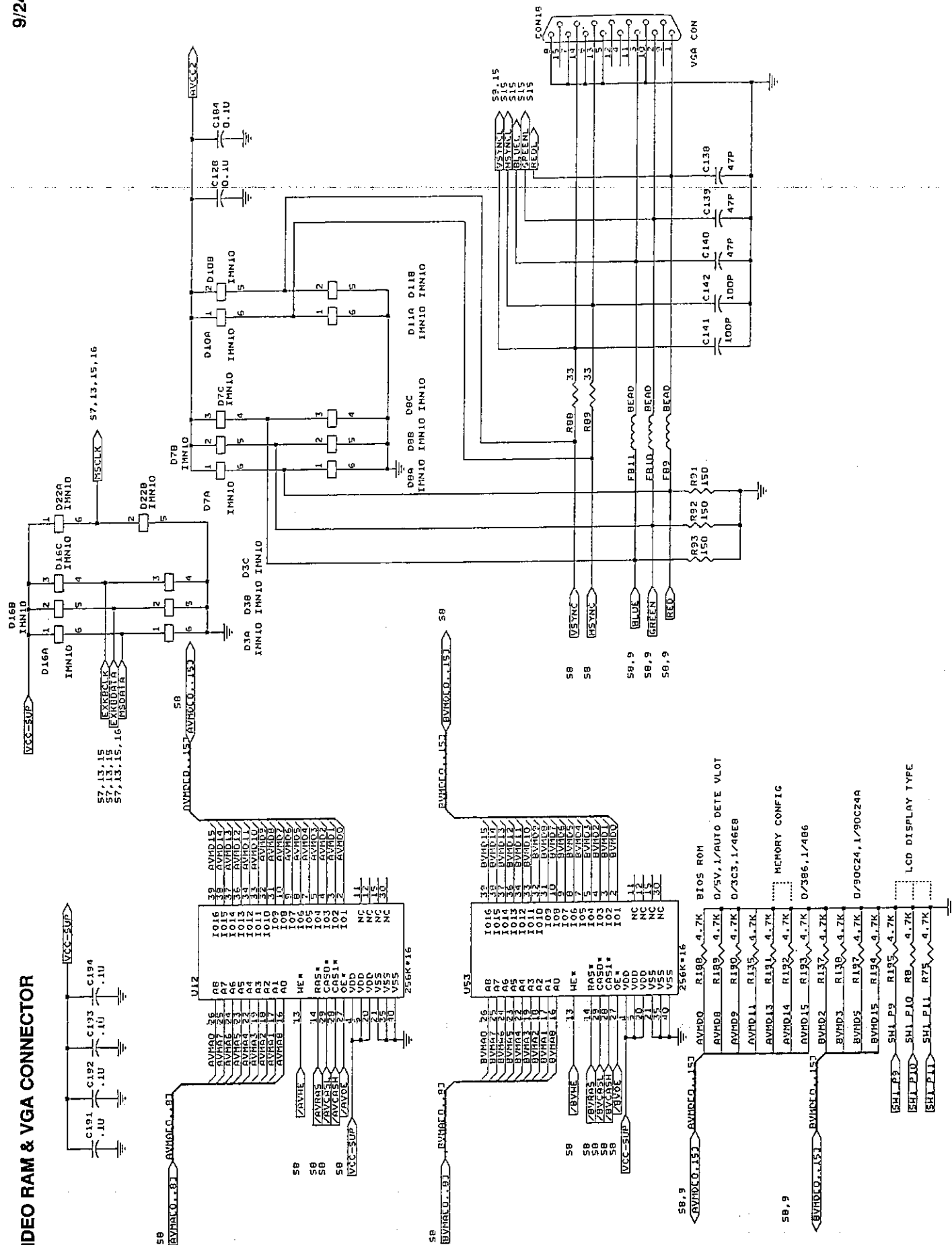
NOTE :

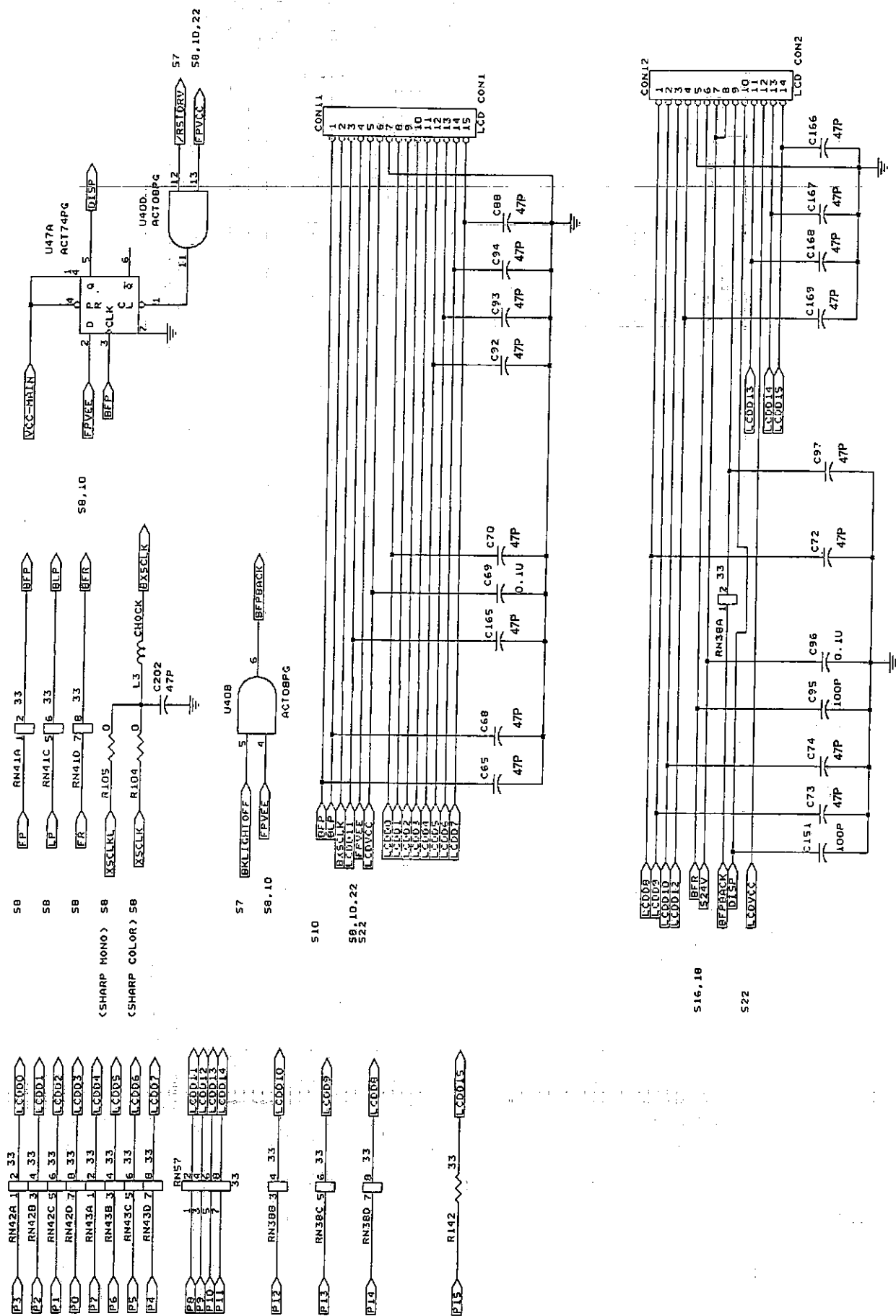
1. PULL HIGH (PI)
PULL DOWN (26B)

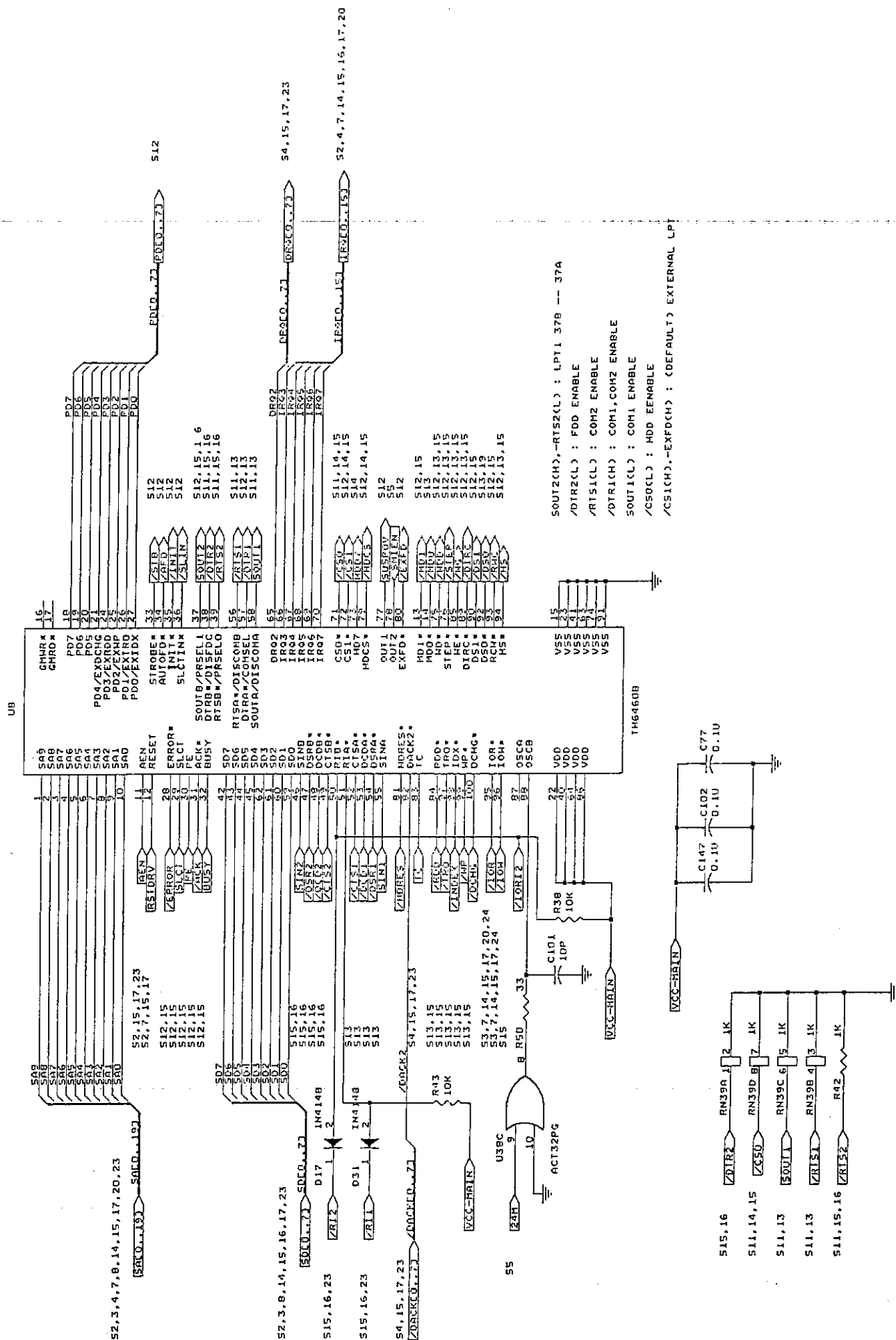
2. PULL HIGH (PI)
PULL DOWN (268)





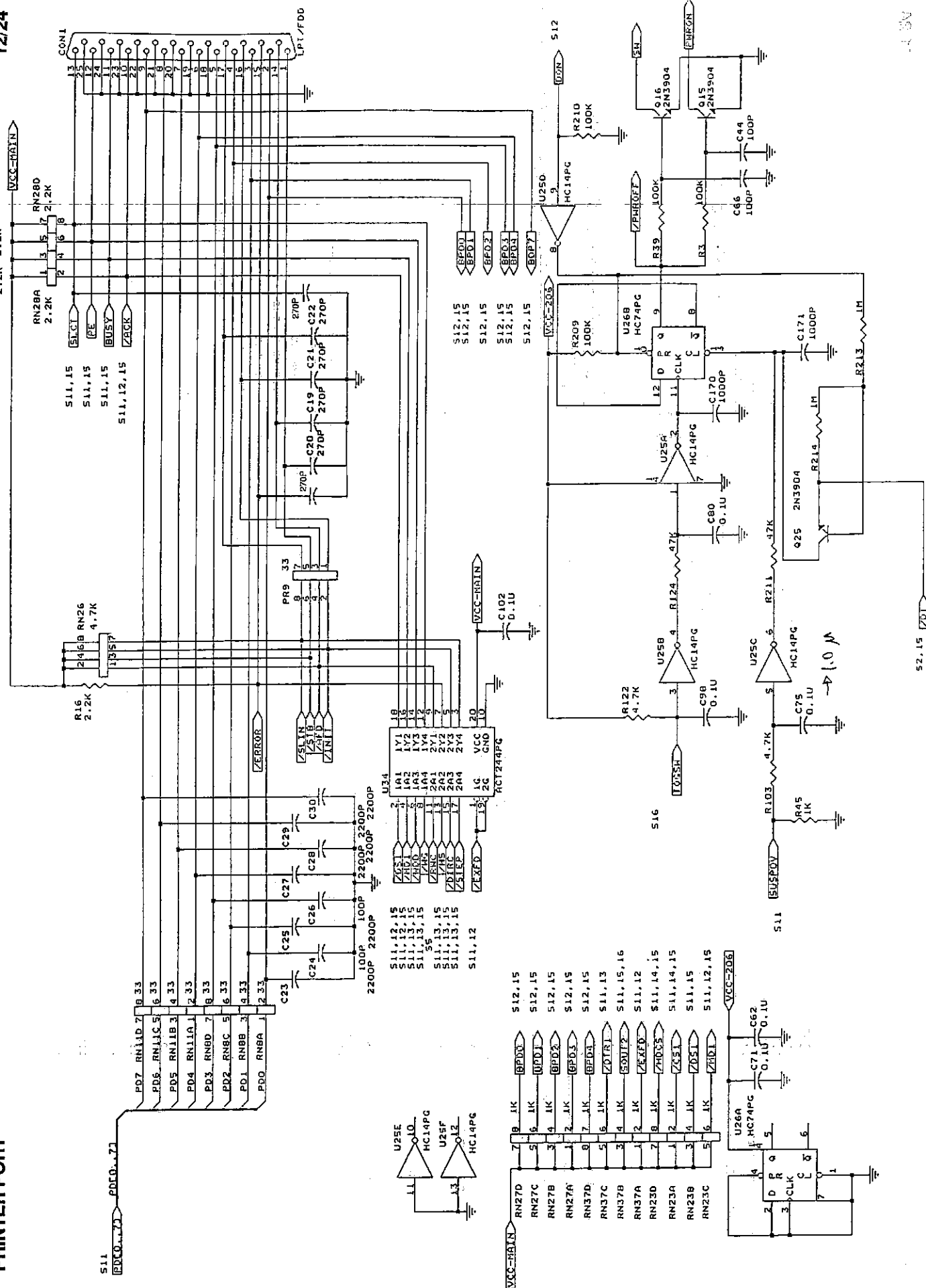


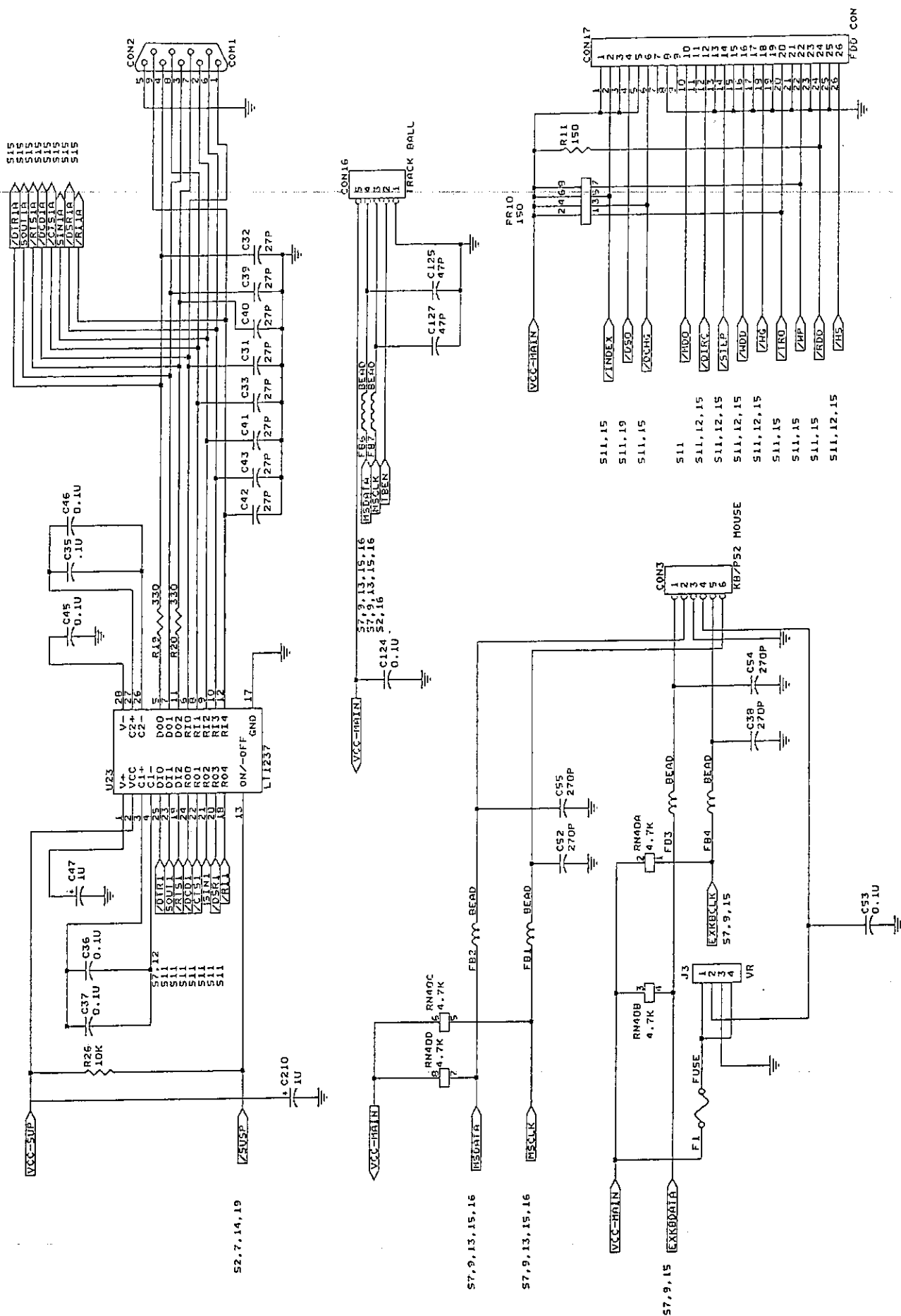




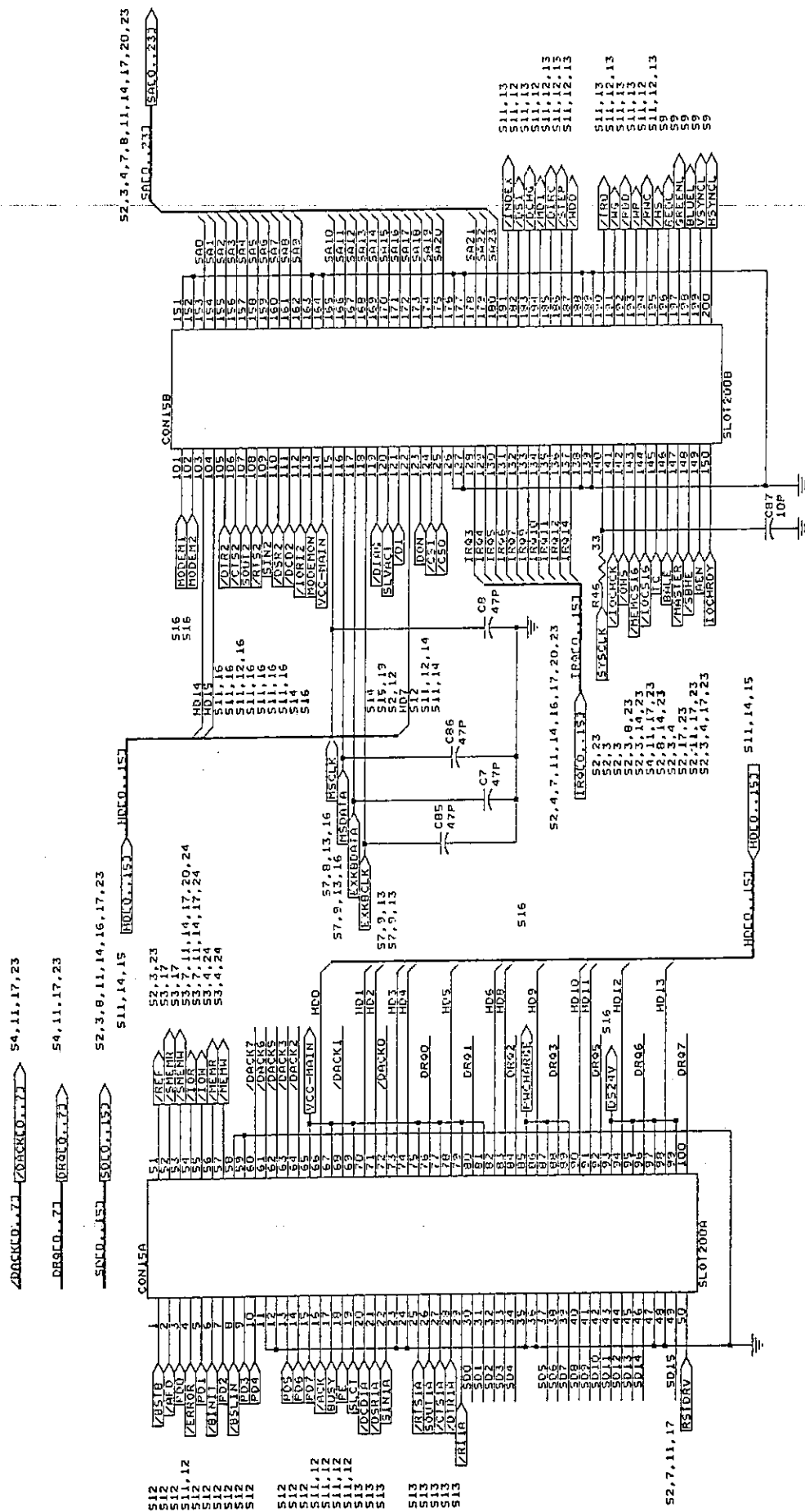
RN28B RN28C

2.2K 2.2K



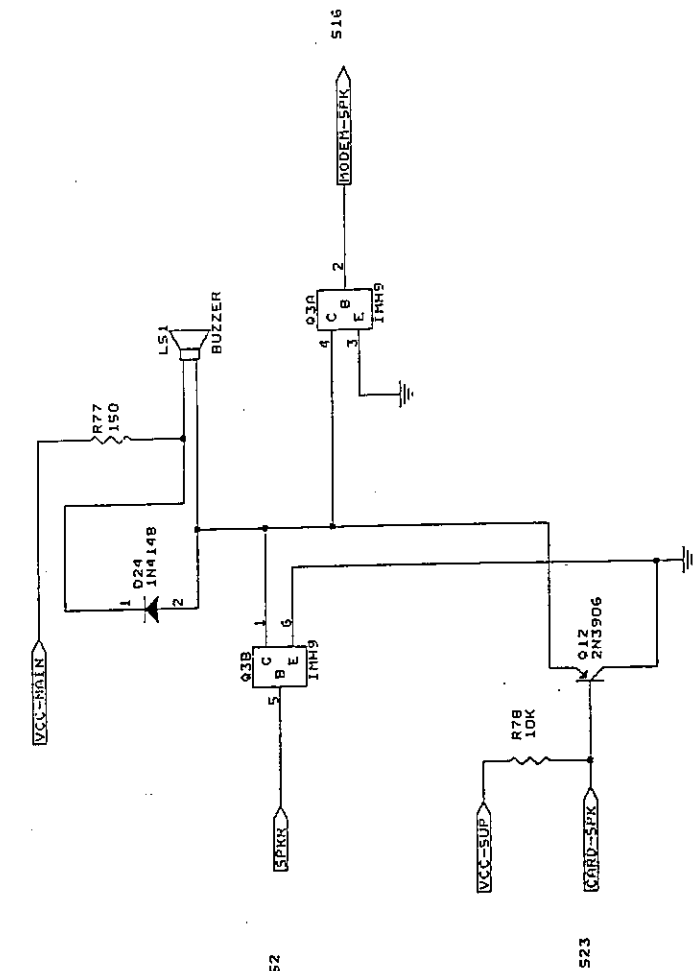
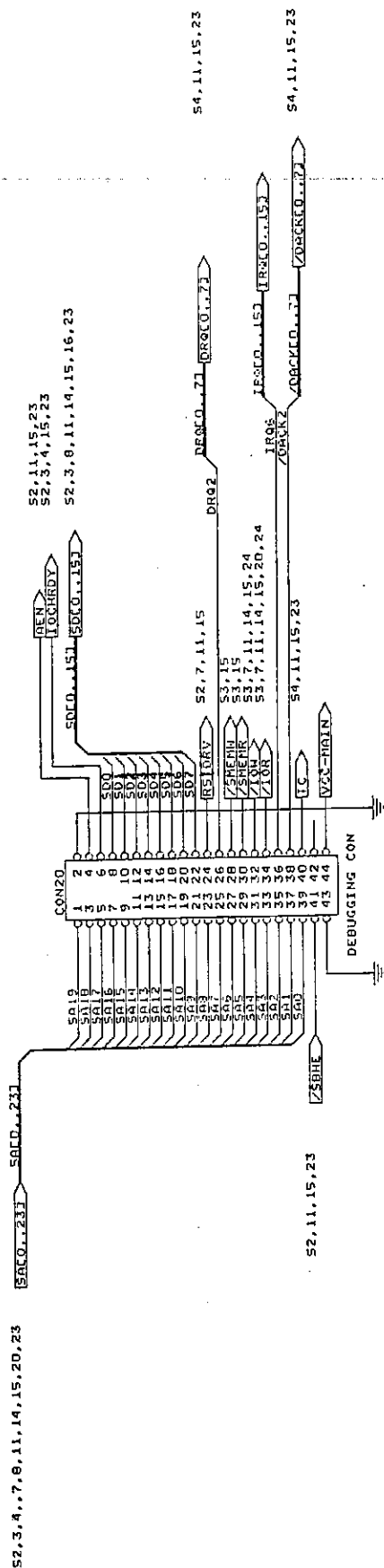








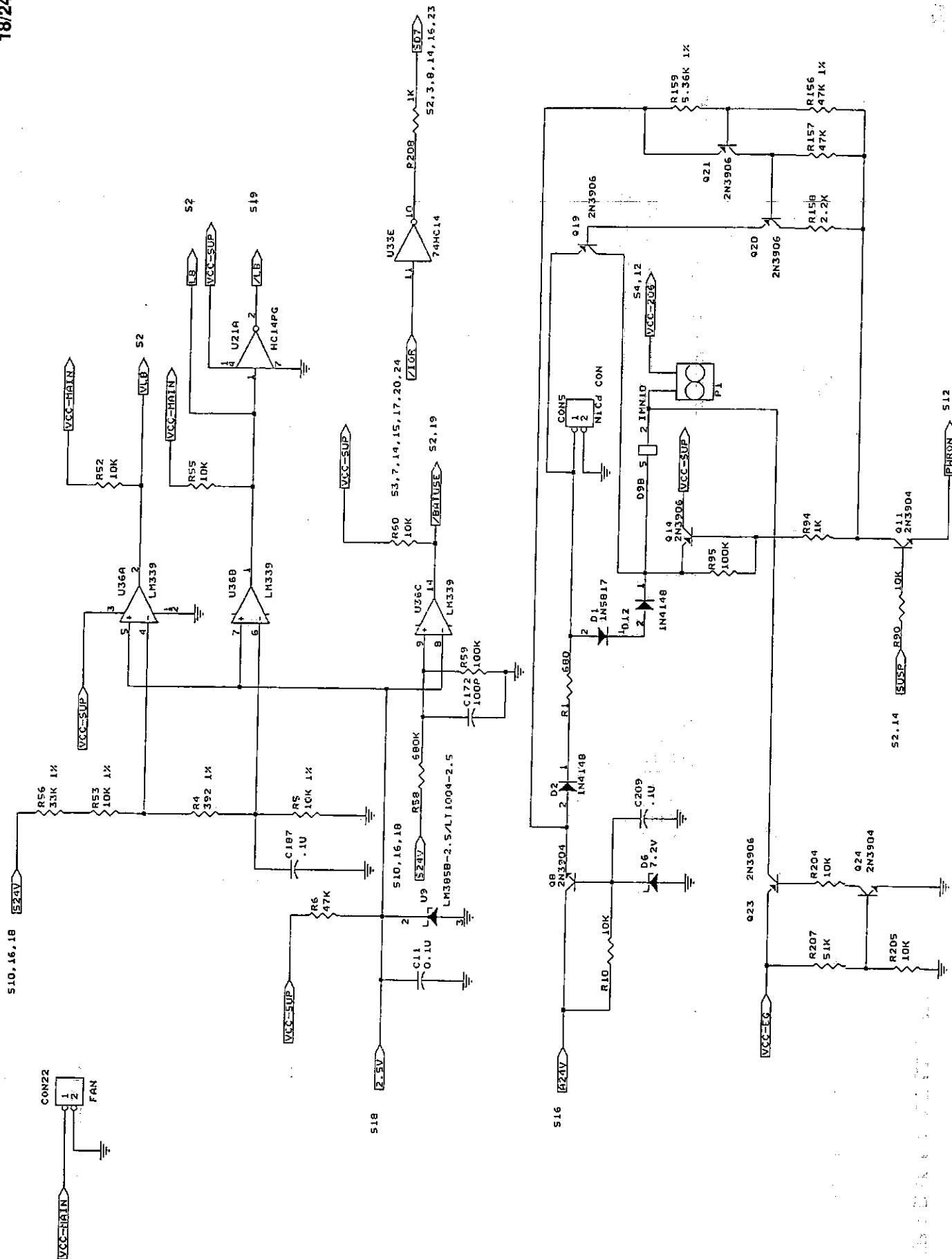
BUZZER & BATTERY LEVEL SIGNALS



206 POWER & BATTERY STATUS

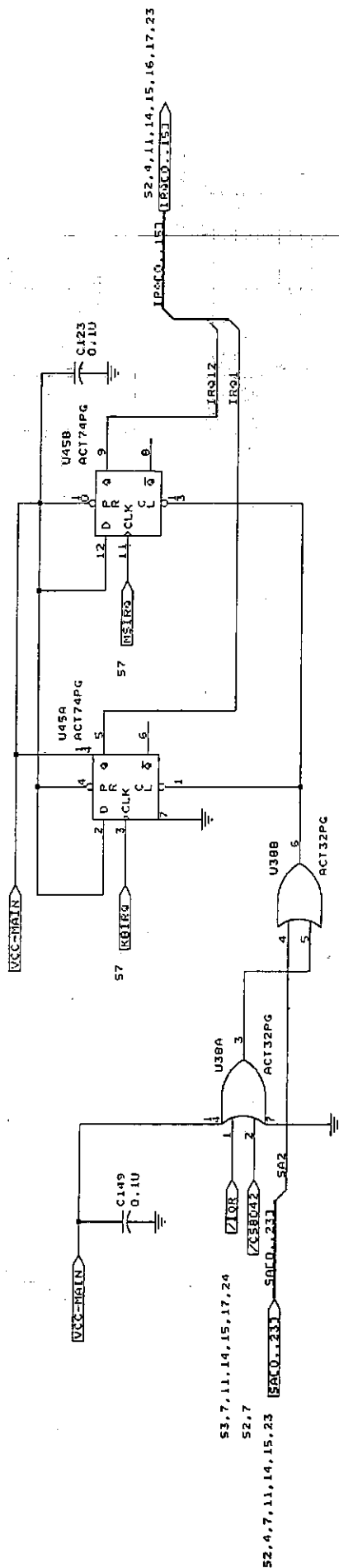
18/24

PC-8660

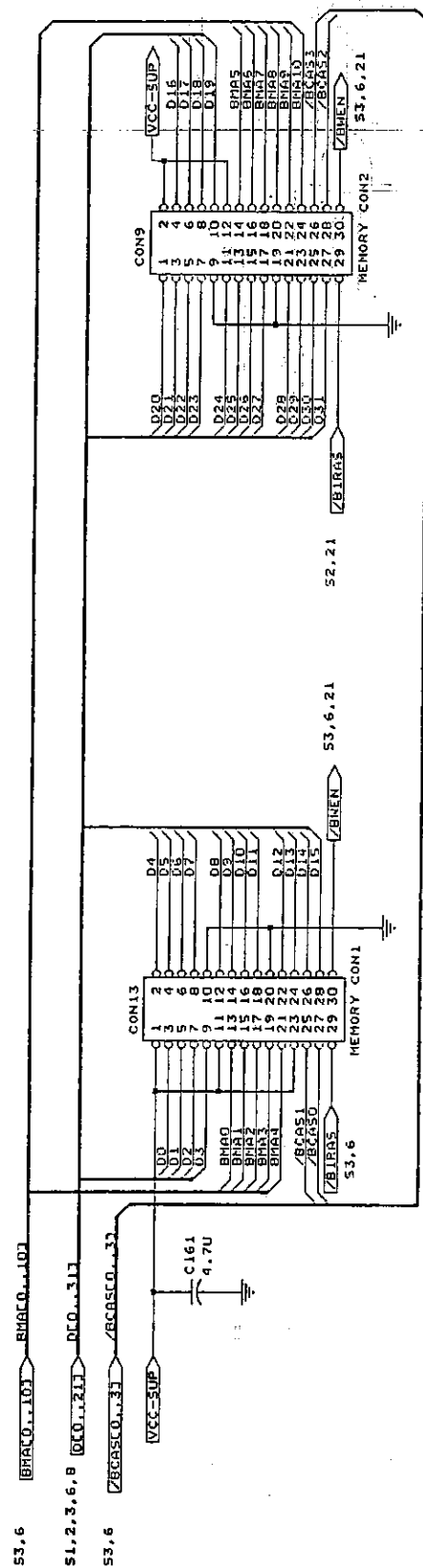


19/24





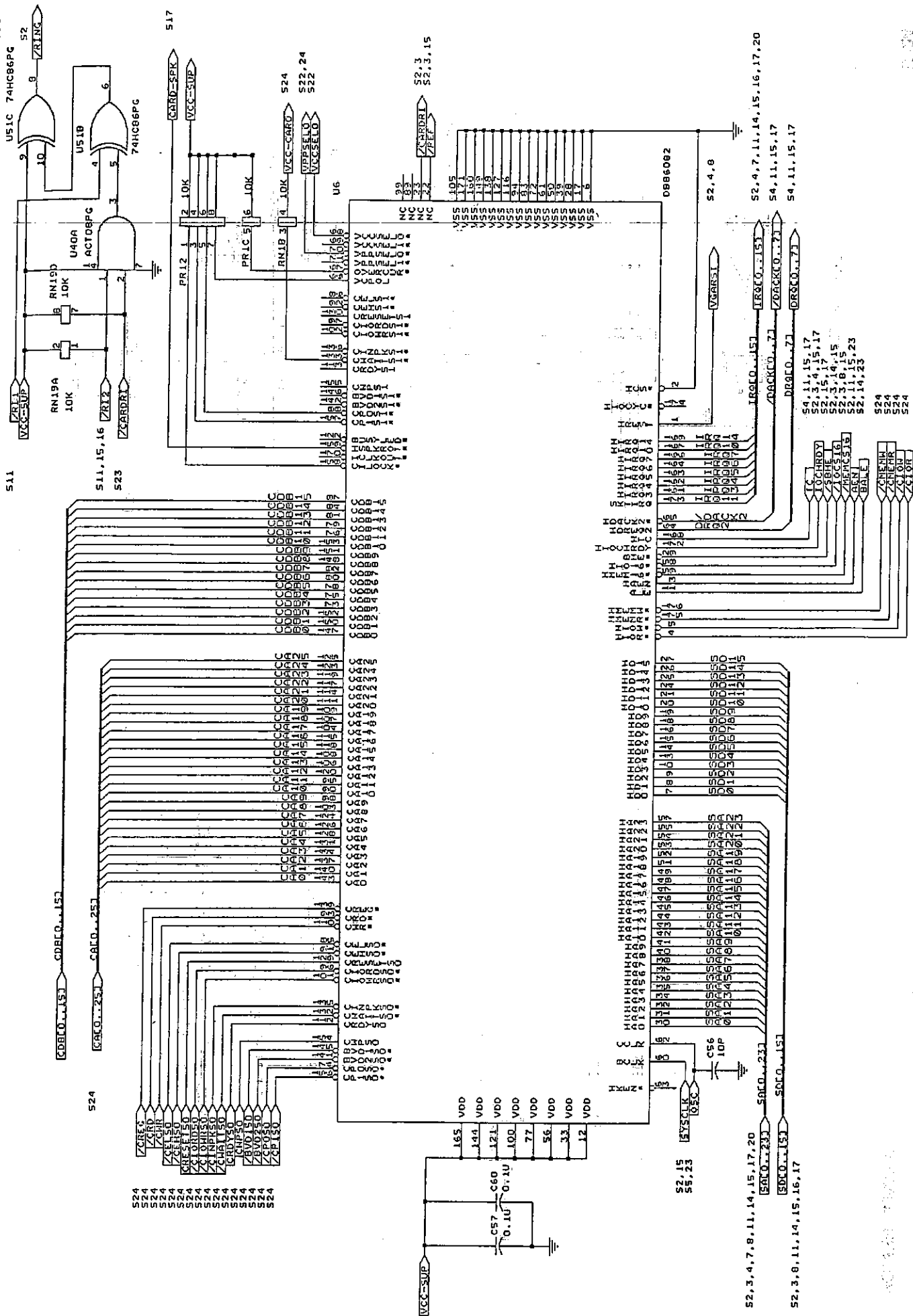
MEMORY CONNECTOR



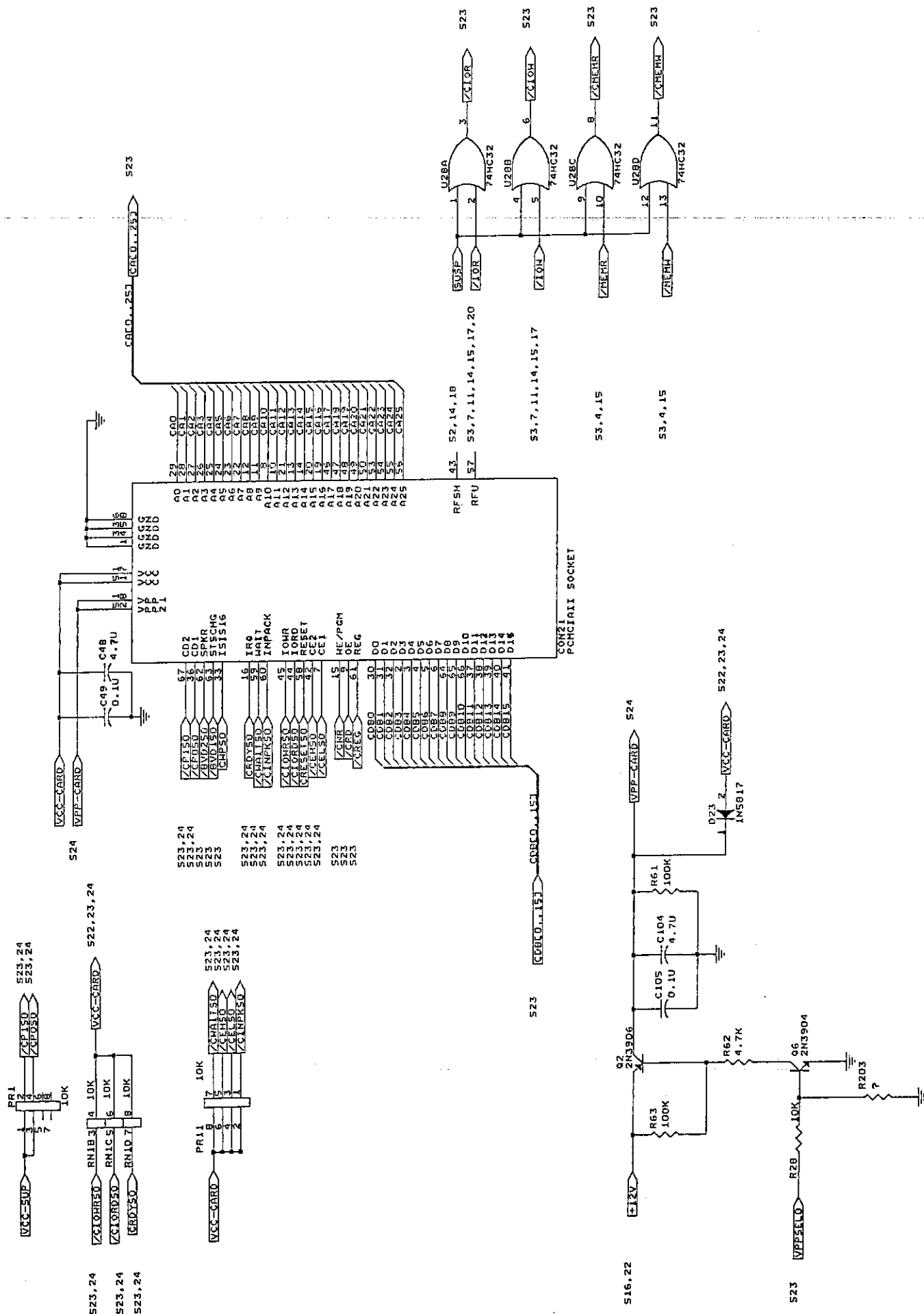
PCMCIA II CONTROLLER

23/24

PC-8660



PCMCIA II SOCKET



COMPONENT LOCATION

PV-486W COMPONENT LOCATION :

1/1

C1 : 6	C81 : 12	CON1 : 12	F1 : 13	PR1 : 23	R1 : 18	Q1 : 5	RN1 : 23, 24	U1 : 5	U1 : 6
C2 : 1	C82 : 13	CON2 : 13	F2 : 13	PR2 : 6	R2 : 12	Q2 : 7	RN2 : 7	U2 : 16	U2 : 6
C3 : 1	C83 : 14	CON3 : 14	F3 : 14	PR3 : 3	R3 : 18	Q3 : 1	RN3 : 1	U3 : 1	U3 : 6
C4 : 1	C84 : 15	CON4 : 15	F4 : 15	PR4 : 1	R4 : 18	Q4 : 1	RN4 : 1	U4 : 1	U4 : 6
C5 : 1	C85 : 16	CON5 : 16	F5 : 16	PR5 : 1	R5 : 18	Q5 : 1	RN5 : 1	U5 : 1	U5 : 6
C6 : 1	C86 : 17	CON6 : 17	F6 : 17	PR6 : 1	R6 : 18	Q6 : 1	RN6 : 1	U6 : 1	U6 : 6
C7 : 1	C87 : 18	CON7 : 18	F7 : 18	PR7 : 1	R7 : 18	Q7 : 1	RN7 : 1	U7 : 1	U7 : 6
C8 : 1	C88 : 19	CON8 : 19	F8 : 19	PR8 : 1	R8 : 18	Q8 : 1	RN8 : 1	U8 : 1	U8 : 6
C9 : 1	C89 : 20	CON9 : 20	F9 : 20	PR9 : 1	R9 : 18	Q9 : 1	RN9 : 1	U9 : 1	U9 : 6
C10 : 1	C90 : 21	CON10 : 21	F10 : 21	PR10 : 1	R10 : 18	Q10 : 1	RN10 : 1	U10 : 1	U10 : 6
C11 : 1	C91 : 22	CON11 : 22	F11 : 22	PR11 : 1	R11 : 18	Q11 : 1	RN11 : 1	U11 : 1	U11 : 6
C12 : 1	C92 : 23	CON12 : 23	F12 : 23	PR12 : 1	R12 : 18	Q12 : 1	RN12 : 1	U12 : 1	U12 : 6
C13 : 1	C93 : 24	CON13 : 24	F13 : 24	PR13 : 1	R13 : 18	Q13 : 1	RN13 : 1	U13 : 1	U13 : 6
C14 : 1	C94 : 25	CON14 : 25	F14 : 25	PR14 : 1	R14 : 18	Q14 : 1	RN14 : 1	U14 : 1	U14 : 6
C15 : 1	C95 : 26	CON15 : 26	F15 : 26	PR15 : 1	R15 : 18	Q15 : 1	RN15 : 1	U15 : 1	U15 : 6
C16 : 1	C96 : 27	CON16 : 27	F16 : 27	PR16 : 1	R16 : 18	Q16 : 1	RN16 : 1	U16 : 1	U16 : 6
C17 : 1	C97 : 28	CON17 : 28	F17 : 28	PR17 : 1	R17 : 18	Q17 : 1	RN17 : 1	U17 : 1	U17 : 6
C18 : 1	C98 : 29	CON18 : 29	F18 : 29	PR18 : 1	R18 : 18	Q18 : 1	RN18 : 1	U18 : 1	U18 : 6
C19 : 1	C99 : 30	CON19 : 30	F19 : 30	PR19 : 1	R19 : 18	Q19 : 1	RN19 : 1	U19 : 1	U19 : 6
C20 : 1	C100 : 31	CON20 : 31	F20 : 31	PR20 : 1	R20 : 18	Q20 : 1	RN20 : 1	U20 : 1	U20 : 6
C21 : 1	C101 : 32	CON21 : 32	F21 : 32	PR21 : 1	R21 : 18	Q21 : 1	RN21 : 1	U21 : 1	U21 : 6
C22 : 1	C102 : 33	CON22 : 33	F22 : 33	PR22 : 1	R22 : 18	Q22 : 1	RN22 : 1	U22 : 1	U22 : 6
C23 : 1	C103 : 34	CON23 : 34	F23 : 34	PR23 : 1	R23 : 18	Q23 : 1	RN23 : 1	U23 : 1	U23 : 6
C24 : 1	C104 : 35	CON24 : 35	F24 : 35	PR24 : 1	R24 : 18	Q24 : 1	RN24 : 1	U24 : 1	U24 : 6
C25 : 1	C105 : 36	CON25 : 36	F25 : 36	PR25 : 1	R25 : 18	Q25 : 1	RN25 : 1	U25 : 1	U25 : 6
C26 : 1	C106 : 37	CON26 : 37	F26 : 37	PR26 : 1	R26 : 18	Q26 : 1	RN26 : 1	U26 : 1	U26 : 6
C27 : 1	C107 : 38	CON27 : 38	F27 : 38	PR27 : 1	R27 : 18	Q27 : 1	RN27 : 1	U27 : 1	U27 : 6
C28 : 1	C108 : 39	CON28 : 39	F28 : 39	PR28 : 1	R28 : 18	Q28 : 1	RN28 : 1	U28 : 1	U28 : 6
C29 : 1	C109 : 40	CON29 : 40	F29 : 40	PR29 : 1	R29 : 18	Q29 : 1	RN29 : 1	U29 : 1	U29 : 6
C30 : 1	C110 : 41	CON30 : 41	F30 : 41	PR30 : 1	R30 : 18	Q30 : 1	RN30 : 1	U30 : 1	U30 : 6
C31 : 1	C111 : 42	CON31 : 42	F31 : 42	PR31 : 1	R31 : 18	Q31 : 1	RN31 : 1	U31 : 1	U31 : 6
C32 : 1	C112 : 43	CON32 : 43	F32 : 43	PR32 : 1	R32 : 18	Q32 : 1	RN32 : 1	U32 : 1	U32 : 6
C33 : 1	C113 : 44	CON33 : 44	F33 : 44	PR33 : 1	R33 : 18	Q33 : 1	RN33 : 1	U33 : 1	U33 : 6
C34 : 1	C114 : 45	CON34 : 45	F34 : 45	PR34 : 1	R34 : 18	Q34 : 1	RN34 : 1	U34 : 1	U34 : 6
C35 : 1	C115 : 46	CON35 : 46	F35 : 46	PR35 : 1	R35 : 18	Q35 : 1	RN35 : 1	U35 : 1	U35 : 6
C36 : 1	C116 : 47	CON36 : 47	F36 : 47	PR36 : 1	R36 : 18	Q36 : 1	RN36 : 1	U36 : 1	U36 : 6
C37 : 1	C117 : 48	CON37 : 48	F37 : 48	PR37 : 1	R37 : 18	Q37 : 1	RN37 : 1	U37 : 1	U37 : 6
C38 : 1	C118 : 49	CON38 : 49	F38 : 49	PR38 : 1	R38 : 18	Q38 : 1	RN38 : 1	U38 : 1	U38 : 6
C39 : 1	C119 : 50	CON39 : 50	F39 : 50	PR39 : 1	R39 : 18	Q39 : 1	RN39 : 1	U39 : 1	U39 : 6
C40 : 1	C120 : 51	CON40 : 51	F40 : 51	PR40 : 1	R40 : 18	Q40 : 1	RN40 : 1	U40 : 1	U40 : 6
C41 : 1	C121 : 52	CON41 : 52	F41 : 52	PR41 : 1	R41 : 18	Q41 : 1	RN41 : 1	U41 : 1	U41 : 6
C42 : 1	C122 : 53	CON42 : 53	F42 : 53	PR42 : 1	R42 : 18	Q42 : 1	RN42 : 1	U42 : 1	U42 : 6
C43 : 1	C123 : 54	CON43 : 54	F43 : 54	PR43 : 1	R43 : 18	Q43 : 1	RN43 : 1	U43 : 1	U43 : 6
C44 : 1	C124 : 55	CON44 : 55	F44 : 55	PR44 : 1	R44 : 18	Q44 : 1	RN44 : 1	U44 : 1	U44 : 6
C45 : 1	C125 : 56	CON45 : 56	F45 : 56	PR45 : 1	R45 : 18	Q45 : 1	RN45 : 1	U45 : 1	U45 : 6
C46 : 1	C126 : 57	CON46 : 57	F46 : 57	PR46 : 1	R46 : 18	Q46 : 1	RN46 : 1	U46 : 1	U46 : 6
C47 : 1	C127 : 58	CON47 : 58	F47 : 58	PR47 : 1	R47 : 18	Q47 : 1	RN47 : 1	U47 : 1	U47 : 6
C48 : 1	C128 : 59	CON48 : 59	F48 : 59	PR48 : 1	R48 : 18	Q48 : 1	RN48 : 1	U48 : 1	U48 : 6
C49 : 1	C129 : 60	CON49 : 60	F49 : 60	PR49 : 1	R49 : 18	Q49 : 1	RN49 : 1	U49 : 1	U49 : 6
C50 : 1	C130 : 61	CON50 : 61	F50 : 61	PR50 : 1	R50 : 18	Q50 : 1	RN50 : 1	U50 : 1	U50 : 6
C51 : 1	C131 : 62	CON51 : 62	F51 : 62	PR51 : 1	R51 : 18	Q51 : 1	RN51 : 1	U51 : 1	U51 : 6
C52 : 1	C132 : 63	CON52 : 63	F52 : 63	PR52 : 1	R52 : 18	Q52 : 1	RN52 : 1	U52 : 1	U52 : 6
C53 : 1	C133 : 64	CON53 : 64	F53 : 64	PR53 : 1	R53 : 18	Q53 : 1	RN53 : 1	U53 : 1	U53 : 6
C54 : 1	C134 : 65	CON54 : 65	F54 : 65	PR54 : 1	R54 : 18	Q54 : 1	RN54 : 1	U54 : 1	U54 : 6
C55 : 1	C135 : 66	CON55 : 66	F55 : 66	PR55 : 1	R55 : 18	Q55 : 1	RN55 : 1	U55 : 1	U55 : 6
C56 : 1	C136 : 67	CON56 : 67	F56 : 67	PR56 : 1	R56 : 18	Q56 : 1	RN56 : 1	U56 : 1	U56 : 6
C57 : 1	C137 : 68	CON57 : 68	F57 : 68	PR57 : 1	R57 : 18	Q57 : 1	RN57 : 1	U57 : 1	U57 : 6
C58 : 1	C138 : 69	CON58 : 69	F58 : 69	PR58 : 1	R58 : 18	Q58 : 1	RN58 : 1	U58 : 1	U58 : 6
C59 : 1	C139 : 70	CON59 : 70	F59 : 70	PR59 : 1	R59 : 18	Q59 : 1	RN59 : 1	U59 : 1	U59 : 6
C60 : 1	C140 : 71	CON60 : 71	F60 : 71	PR60 : 1	R60 : 18	Q60 : 1	RN60 : 1	U60 : 1	U60 : 6
C61 : 1	C141 : 72	CON61 : 72	F61 : 72	PR61 : 1	R61 : 18	Q61 : 1	RN61 : 1	U61 : 1	U61 : 6
C62 : 1	C142 : 73	CON62 : 73	F62 : 73	PR62 : 1	R62 : 18	Q62 : 1	RN62 : 1	U62 : 1	U62 : 6
C63 : 1	C143 : 74	CON63 : 74	F63 : 74	PR63 : 1	R63 : 18	Q63 : 1	RN63 : 1	U63 : 1	U63 : 6
C64 : 1	C144 : 75	CON64 : 75	F64 : 75	PR64 : 1	R64 : 18	Q64 : 1	RN64 : 1	U64 : 1	U64 : 6
C65 : 1	C145 : 76	CON65 : 76	F65 : 76	PR65 : 1	R65 : 18	Q65 : 1	RN65 : 1	U65 : 1	U65 : 6
C66 : 1	C146 : 77	CON66 : 77	F66 : 77	PR66 : 1	R66 : 18	Q66 : 1	RN66 : 1	U66 : 1	U66 : 6
C67 : 1	C147 : 78	CON67 : 78	F67 : 78	PR67 : 1	R67 : 18	Q67 : 1	RN67 : 1	U67 : 1	U67 : 6
C68 : 1	C148 : 79	CON68 : 79	F68 : 79	PR68 : 1	R68 : 18	Q68 : 1	RN68 : 1	U68 : 1	U68 : 6
C69 : 1	C149 : 80	CON69 : 80	F69 : 80	PR69 : 1	R69 : 18	Q69 : 1	RN69 : 1	U69 : 1	U69 : 6
C70 : 1	C150 : 81	CON70 : 81	F70 : 81	PR70 : 1	R70 : 18	Q70 : 1	RN70 : 1	U70 : 1	U70 : 6
C71 : 1	C151 : 82	CON71 : 82	F71 : 82	PR71 : 1	R71 : 18	Q71 : 1	RN71 : 1	U71 : 1	U71 : 6
C72 : 1	C152 : 83	CON72 : 83	F72 : 83	PR72 : 1	R72 : 18	Q72 : 1	RN72 : 1	U72 : 1	U72 : 6
C73 : 1	C153 : 84	CON73 : 84	F73 : 84	PR73 : 1	R73 : 18	Q73 : 1	RN73 : 1	U73 : 1	U73 : 6
C74 : 1	C154 : 85	CON74 : 85	F74 : 85	PR74 : 1	R74 : 18	Q74 : 1	RN74 : 1	U74 : 1	U74 : 6
C75 : 1	C155 : 86	CON75 : 86	F75 : 86	PR75 : 1	R75 : 18	Q75 : 1	RN75 : 1	U75 : 1	U75 : 6
C76 : 1	C156 : 87	CON76 : 87	F76 : 87	PR76 : 1	R76 : 18	Q76 : 1	RN76 : 1	U76 : 1	U76 : 6
C77 : 1	C157 : 88	CON77 : 88	F77 : 88	PR77 : 1	R77 : 18	Q77 : 1	RN77 : 1	U77 : 1	U77 : 6
C78 : 1	C158 : 89	CON78 : 89	F78 : 89	PR78 : 1	R78 : 18	Q78 : 1	RN78 : 1	U78 : 1	U78 : 6
C79 : 1	C159 : 90	CON79 : 90	F79 : 90	PR79 : 1	R79 : 18	Q79 : 1	RN79 : 1	U79 : 1	U79 : 6
C80 : 1	C160 : 91	CON80 : 91	F80 : 91	PR80 : 1	R80 : 18	Q80 : 1	RN80 : 1	U80 : 1	U80 : 6

NOTE : * : VCC-MAIN VOLTAGE
 * : VCC-SUP VOLTAGE
 * : VCC-206 VOLTAGE

PC-8660 difference points from PC-8650 service manual (00ZPC8650SM-E)

1. Page 58 on PC-8650 service manual

Jumper & Switch Setting

(1) SW1

CPU	486DX/DX2	486SX
Switch		
SW1	ON	OFF
SW2	ON	OFF
SW3	ON	OFF
SW4	OFF	ON

CPU SPEED

Frequency	50M	66M
Switch		
SW5	ON	OFF

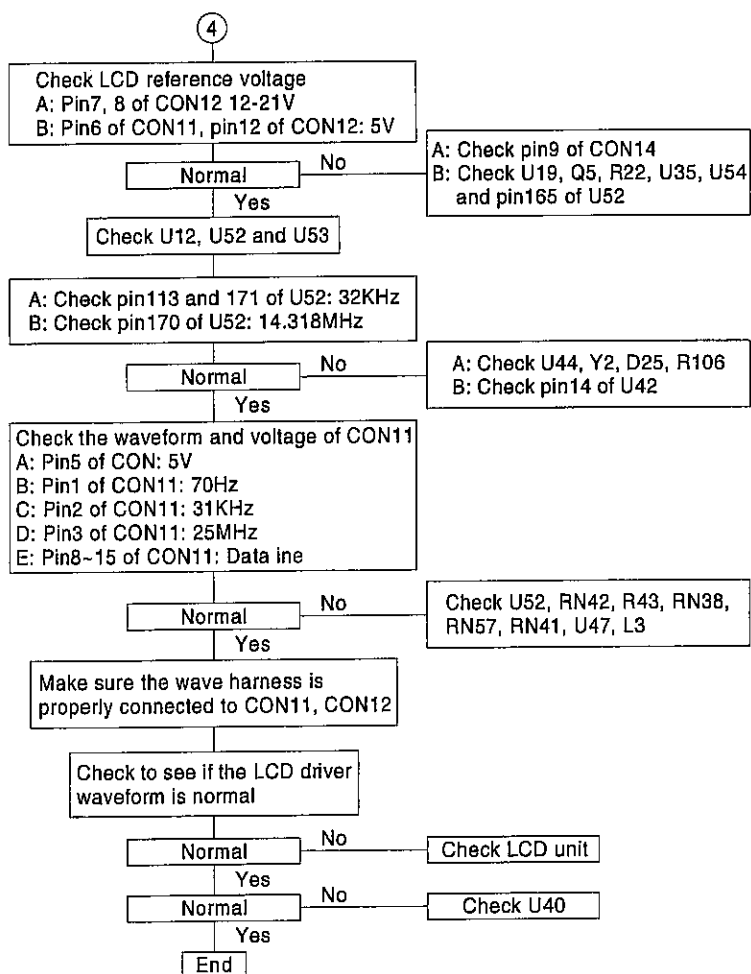
PANEL TYPE

	TFT 9 bit
SW6	OFF
SW7	OFF
SW8	OFF

CPU TYPE

	1X
SW9	ON
SW10	ON

2. Page 60 on PC-8650 service manual



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