

SHARP SERVICE MANUAL

CODE: 00ZPC6881SM/E



PERSONAL COMPUTER

MODEL PC-6881

OPTION: CE-671B
CE-672B
CE-671NK
CE-671EB

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CHAPTER 1. OUTLINE OF THE PC-6800

1. General

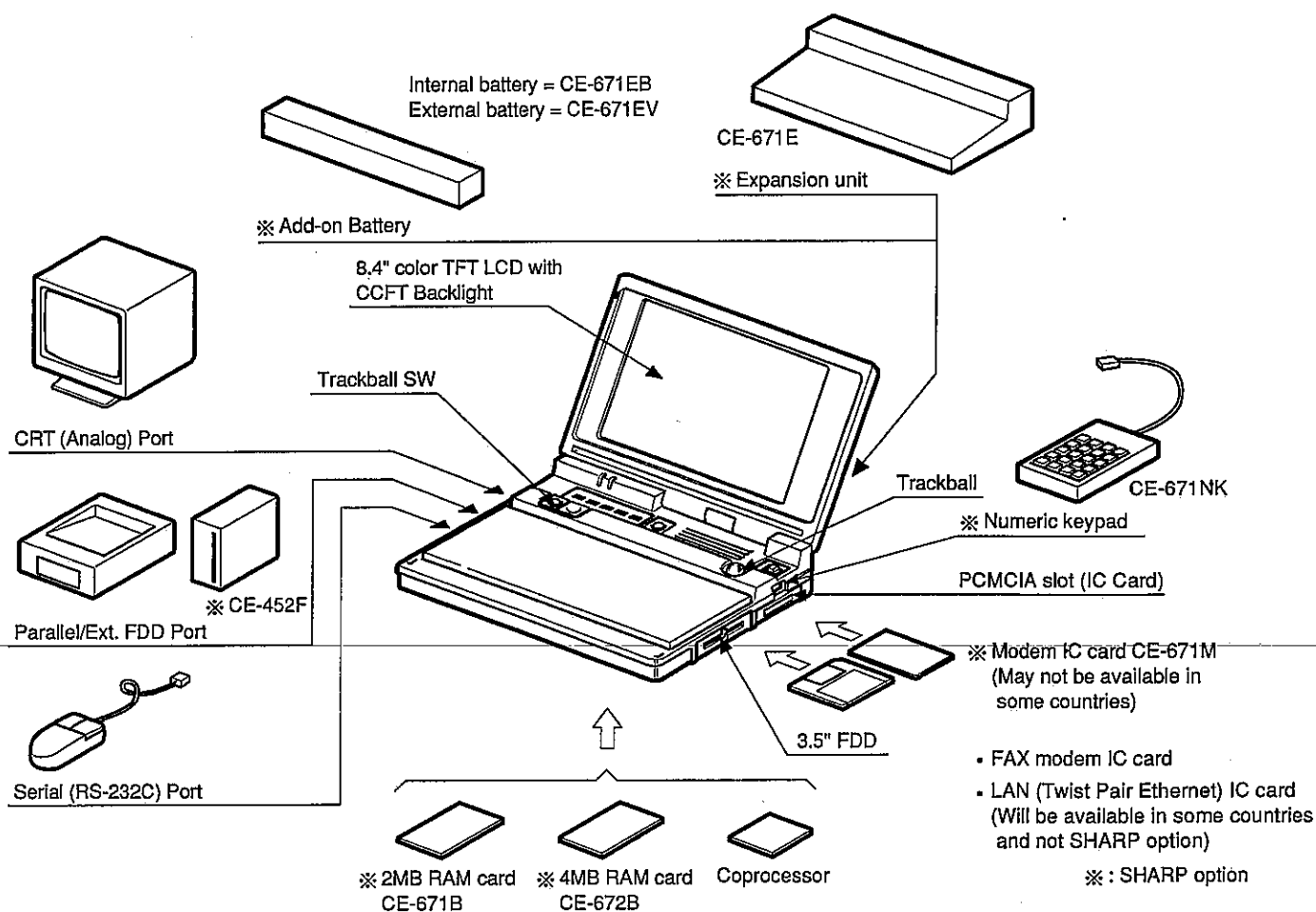
1-1. Product Concept

- High performance and advanced battery power management.
- PCMCIA standard IC card available.
- Letter size fits in your briefcase.
- 3.5" floppy disk drive & hard disk drive standard.
- IBM PC/AT compatible.

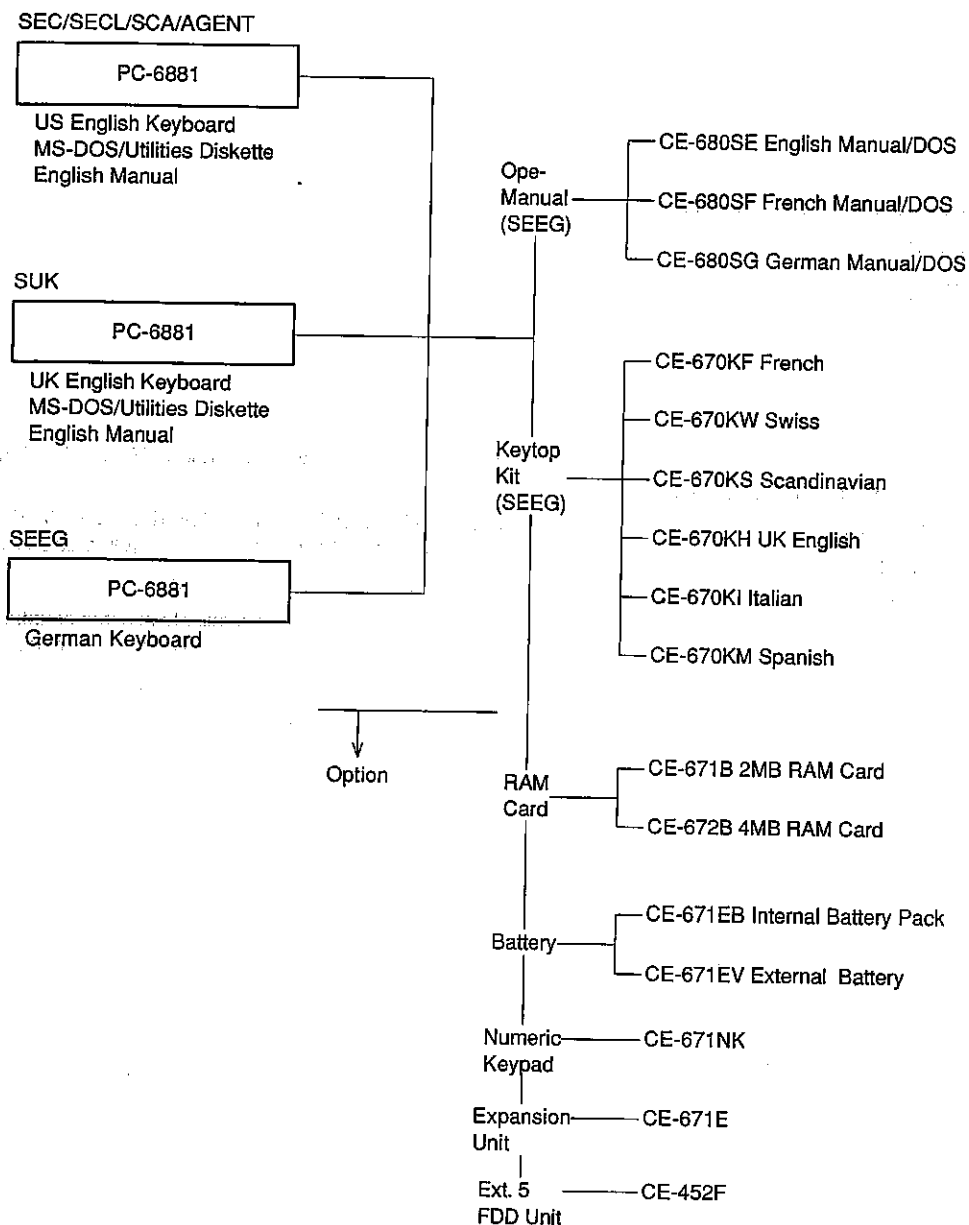
1-2. Feature Highlights

- 32 bits 25MHz-386SL microprocessor.
- 4-way set associative cache control and 16KB cache memory.
- Auto power saving control by system BIOS.
- Supporting 4 levels of power saving states.
 - Local Standby State (Device control)
 - Global Standby State (CPU and system control)
 - Suspend/Resume State
 - Saved-off/Resume State (Loading memory and register values to hard disk, and the power turns off automatically.)
- Letter size (8.5x11x1.9").
- 3.5" 1.44MB floppy disk drive and 80MB hard disk drive is standard.
- Micro trackball, which is a pointing device, is standard. It is effective under applications supporting GUI (Graphical User Interface).
- One PCMCIA IC card slot is standard.
- Optional Modem IC card is available in some countries. Optional FAX-modem and LAN IC card will be available.
- Standard 2MB RAM. Expandable up to 8MB on the system board.
- MS-DOS 5.0 supporting GUI like 'Windows'.

1-3. Outside Figure



1-4. System Diagram (Main Unit)



1-5. Options

1) RAM Cards

CE-671B

2MB RAM card

Extended or EMS support

Size: 50 mm (W) × 27 mm (D) × 7.5 mm (H)
2.0" (W) × 1.1" (D) × 0.3" (H)

Weight: 6 g (0.013 lbs)

CE-672B

4MB RAM card

Extended or EMS support

Size: 50 mm (W) × 38 mm (D) × 7.5 mm (H)
2.0" (W) × 1.5" (D) × 0.3" (H)

Weight: 9 g (0.020 lbs)

2) Floppy Disk Drive Unit

CE-452F

5.25-inch 360 KB 2D

Size: 118 mm (W) × 331 mm (D) × 189 mm (H)
4.6" (W) × 13.0" (D) × 7.4" (H)

Weight: 5.1 kg (11.3 lbs)

3) Internal Battery Pack

CE-671EB

Ni-Cd battery pack with carrying case

Size: 280 mm (W) × 34 mm (D) × 27 mm (H)
(including cover)
11" (W) × 1.4" (D) × 1.1" (H)

Weight: Approx. 350 g (0.8 lbs) (including cover)
Capacity: 1800 mAh

4) Expansion Unit

CE-671E

Size: 373 mm (W) × 428 mm (D) × 120 mm (H)
(including cover)

16.9" (W) × 14.7" (D) × 4.7" (H)

Weight: Approx. 5.0 kg (11.0 lbs)

5) Numeric Keypad

CE-671NK

Size: 91 mm (W) × 160 mm (D) × 35 mm (H)
3.6" (W) × 6.3" (D) × 1.4" (H)

Weight: Approx. 180 g (0.4 lbs)

CHAPTER 2. SPECIFICATION

1. Hardware

Processor:	386SL (5/10/25MHz) - Clock speed can be changed by 'Set Up Program' or following key combination after the power is on. - Ctrl-Alt-'↑' (Up arrow): 5→10→25MHz - Ctrl-Alt-'↓' (Down arrow): 25→10→5MHz - Following beep sounds when the clock speed is changed by the key combination. 5MHz: Low-pitched beep 10MHz: Middle-pitched beep 25MHz: High-pitched beep - The above key combinations, however, may not work in certain applications or system software. In case, use the 'Set Up Program'. - If application software uses the above key combination, end user can use the key combination of the application software by disabling this function by the 'Set Up Program'. - Supporting real time clock/calendar. (CMOS backup memory) - Bus speed: 8MHz	- Memory configuration is as follows: 2M byte: Standard RAM 4M byte: Standard RAM + 2M byte RAM card 6M byte: Standard RAM + 4M byte RAM card 8M byte: Standard RAM + 2M byte RAM card + 4M byte RAM card 8000K byte: User's memory 192K byte: Reserved
Coprocessor:	Socket for 387SX (25MHz) 387SX: User Option - End user buys 387SX in the market and inserts it to the IC socket by himself by removing the RAM card cover on the bottom panel of the computer.	Supporting 'Expanded (Max. 7360K byte)' and 'Extended (Max. 7360K byte)' memory. 'Expanded' and 'Extended' memory can be assigned by 'Set Up Program'.
ROM:	2M bit Flash-ROM x 1 pc. - System BIOS: IPL, Power management, Set up program, AT BIOS, Battery Watcher etc. (Phoenix Technologies Ltd.) - VGA BIOS (Phoenix Technologies, Ltd.) Supporting 82C456A VGA controller. - BIOS version up grade can be done by IC card or floppy diskette	'Expanded' memory can be used as 'LIM/EMS 4.0' memory by using the device driver 'PEMM.SYS' including the diag diskette.
Cache:	16K byte standard High speed 16K byte cache delivers zero wait state processing.	Data storage: 2.5 inch 80M byte hard disk drive x 1 - Average access time: Typical 16.5ms - Supporting auto head parking function to avoid damage the damage when the power is turned off.
RAM:	2M byte standard 512K byte (1M bit x 4) DRAM x 4 pcs. - Access time: 100ns - Without parity 1856K byte: User's memory (640K byte for conventional, 1216K byte for expanded or extended memory) 192K byte: reserved (128K byte: Shadow RAM, 64K byte: Power Management RAM) - Supporting LIM/EMS 4.0 - Bus width: 16 bit Expandable up to 8M byte by installing the optional RAM cards. (CE-671B/672B) - Optional 2M byte (CE-671B) and 4M byte (CE-672B) RAM cards can be installed by end-user by removing the RAM card cover on the bottom panel of the computer.	3.5 inch 1.44M byte floppy disk drive x 1 - Can read/write both 1.44M byte and 720K byte diskettes. Display: Color TFT (Thin Film Transistor) LCD with CCFT (Cold Cathode Fluorescent Tube) backlight - Resolution: 640 x 480 pixels, bit-mapped graphics 256 colors out of 262144 colors - Viewing area: 8" x 6" - Aspect ratio: 1 : 1 - Dot pitch: 0.27 mm - Response speed: Rise 30mS, Decay 50mS - Contrast ratio: 60 : 1 - Backlight: two CCFT - Life of CCFT: 10,000h (until the brightness becomes half.) Display Mode - VGA controller: 82C456A - VGA compatible. - Supporting 'Backward Compatibility'. (EGA/CGA/MDA/HGC) - Selectable VGA/EGA/CGA/MDA/HGC by 'Set Up Program'. 'HGC' is available on CRT only. - LCD screen and CRT display can be used simultaneously. Safety Function - Supporting the micro switch which enters this system 'Suspend State' automatically when the display is shut during power on. When the display is opened, the previous state is resumed. Display Unit 0 - 155 degrees tilt angle adjustment. - Latch x 2 (on the left and right side) - Not detachable - CCFT backlight unit can be replaced by service man. (service parts.) - LCD backlight brightness is adjustable by the setup.

Keyboard:	• 'Display Timeout': Time is selectable by the 'Set Up Program'. - IBM 101/102 like keyboard layout • 79 keys (US layout) • 80 keys (UK and German layout) • Realizing full compatibility with IBM enhanced keyboard (101/102 keys) according to the combination with 'Fn' special function key. (ex. 'Fn' + 'Insert') • Integrated numeric keypad (combination with 'Fn' key or 'Num Lock': On) • Separate 4 cursor keys • 'Set Up' key for 'Set Up Program' • 'Fn' key for special function • 12 programmable function keys • 19mm pitch (typewriter key part), 2mm stroke with soft click mechanism • No step-sculptured and very thin keyboard (9.5mm) • Cylindrical and very thin key top (3.7mm) • Green LEDs for Num Lock, Caps Lock, and Scroll Lock • Selectable 'On/Off' of 'Num Lock', 'Caps Lock' and 'Scroll Lock' by 'Set Up Program'. 'On' enables them during boot. 'Off' disables them during boot.	• Selectable 'Parallel' or 'Ext. FDD' by hardware switch. • Can define this port as LPT1 – LPT3 by 'Set Up Program'. • Selectable 'Disable' by 'Set Up Program'. • This port is 'Bi-directional' port. • With interface connector cover (Open/Close door style, plastic)
	European layout • Change from 'German' to the following layout by using the optional keytop kit. French, Swiss, Scandinavian (Swedish/Finnish, Danish, Norwegian), Italian, UK English, Spanish	Numeric keypad x 1 • Small 10 pin connector • With interface connector cover (Open/Close door style, plastic) Expansion bus x 1 • For the optional expansion unit • AT bus • Bus speed: 8MHz • With interface connector cover (Detachable type, plastic)
Trackball:	Micro trackball • Compatible with Microsoft serial mouse. • 2 click buttons. (Left: Main, Right: Sub) • Trackball should be operated by right hand. • Click buttons should be operated by left hand.	Internal slot: 1 slot for PCMCIA IC card • IC card: user option • Optional Modem IC cards can be installed. (Available in some countries) • Optional LAN IC card (Twist Pair Ethernet) and FAX modem IC card can be installed. (Intel brand will be available) • PCMCIA cards in the market are available. • With eject button • With interface connector cover (Open/Close shutter style, plastic) 2 slots for 2M byte and 4M byte RAM cards • RAM card: user option • 2MB RAM Card: CE-671B • 4MB RAM Card: CE-672B • With cover (plastic) • End user can open the cover and install them easily.
Interface:	Serial (RS-232C) x 1 • D-sub 9 pin male connector • Can define this port as COM1 – COM4 by 'Set Up Program'. • Selectable 'Disable' by 'Set Up Program'. • Selectable initial baud rate, data bits, stop bits and parity by 'Set Up Program'. • With interface connector cover (Open/Close door style, plastic) CRT (Analog) x 1 • D-sub 15 pin female connector • Analog RGB output • VGA compatible • Selectable LCD/CRT, CRT mode by hardware switch when the power turns on. • LCD and CRT can not be used simultaneously. • With interface connector cover (Open/Close door style, plastic) Parallel (Centronics)/Ext. FDD x 1 • D-sub 25 pin female connector	1 socket for the optional coprocessor • Coprocessor: user option • With cover (plastic; same as RAM cover) • End user can open the cover (same as RAM cover) and install it easily. Power supply: Ni-Cd battery pack • Rechargeable and removable battery pack (without cables) • Output: 7.2 V DC, 1.8 Ah, 12.96 Wh • Supporting 'Battery Status' gage. The estimated battery status for the selected configuration will be displayed. The battery status should reflect the 'Battery Watch' CMOS value. • Supporting 'Quick charging mode' when the power is off. It takes approx. 1.5 – 2.0 hours from 'Low Battery' (BATTERY indicator turns red) to 'Full Battery' (BATTERY indicator turns green).

- Supporting 'Standard changing mode' which can charge while operating. It takes approx. 8 hours from 'Low Battery' (BATTERY indicator turns red) to 'Full Battery' (BATTERY indicator turns green).
- End user can open the battery cover and remove/replace the pack easily.
- Extra Battery pack is option.
- The nature of all Ni-Cd batteries requires periodic discharging, then recharging to preserve their operating features. User should discharge and recharge the battery approximately every a few weeks.

AC adaptor

- Input: 100-240VAC, 50/60Hz, auto sensing
- Universal AC adaptor
- Output: 12.9 V
- Cable length: 150cm (AC adaptor's cable)
- AC cord is detachable from AC adaptor.

CMOS backup battery:

Ni-Cd battery

- Backup the set-up information and the password data. If end user changes the internal battery, the backup data will not be lost.

Battery life:

Approx. 1 hour (continuous operation time from 'Full Charge' (BATTERY indicator illuminates green) to 'Low Battery' (BATTERY indicator turns red))

- Condition is as follows:
Options: No option,
Power saving mode: On

Battery management:

1st-step:

When the power switch turns on, POWER indicator illuminates green.
When the battery is charged more than 90%, The BATTERY indicator illuminates green.

- In the case of the AC adaptor being connected, the BATTERY indicator illuminates orange. (Standard charging mode)
- In the case of the AC adaptor not being connected and the battery being discharged from 90% to 10%, The BATTERY indicator does not illuminate.

2nd-step:

When the battery is discharged the energy of more than roughly 90%, BATTERY indicator turns red and the alarm beeps for about 15 seconds. When the battery comes up to 'Low' level, the system enters 'Suspend State' automatically, when "Suspend Battery Low" section is set to Enabled.

3rd-step:

When the system enters into the 'Suspend State' or 'Stand-by State', The POWER indicator blinks (green) and the BATTERY indicator does not illuminate.

4th-step:

After the BATTERY indicator begins to blink (red) and the alarm beeps for about 15 seconds simultaneously, the system will shut off automatically. If the 'Saved-off' mode is on, the system enters the 'Saved-off State' automatically.

5th-step:

When the system enters the 'Saved-off State' or the power switch is turns off, both POWER and BATTERY indicators will not illuminate.

Power management:

BIOS supports following functions:

- Power saving for devices and options
Local standby state
- Power saving for CPU and system
Global standby state
- Suspend/Resume function
Suspend state
(Besides the power needed to backup memory, the power is cutted.)
Saved-off state
(After all memory and register values are saved to hard disk, the power turns off automatically.)

Parameters of power management can be specified by 'Set Up Program'.

Power consumption:

13 watts

Security:

Power-on password

- Input or delete of the password can be done by using the password utility.
- When end-user forgets the password or the unknown password is inputted, the password must be deleted to operate the computer. It is possible to delete the password refer to "Password function in 7-1. This action should be done by a service man.

2. Mechanical

Connectors:

External connectors

- Serial port: D-sub 9 pin male connector
- CRT port: D-sub 15 pin female connector
- Parallel/EXT. FDD port:
D-sub 25 pin female connector
- Numeric keypad: Small 10 pin
- Expansion bus: 120 pin
- AC adaptor: 2 conductor phone jack

Internal connectors

- PCMCIA Card: 68 pin connector
- RAM Card: 50 pin connector

Switches:

Power switch (slide switch)

- On/Off

Suspend/Resume button

Display shut alarm switch (micro switch)

DIP Switches:

Selection of 'Parallel' or 'Ext. FDD' I/F Selection of 'LCD and CRT' or 'CRT only'
Speaker volume ('On' or 'Off', 'High' or 'Low')

Connector Covers:

One open/close door style cover for the serial, CRT, parallel/ext. FDD connector and the DIP switches. (not detachable)

One open/close door style cover for the numeric keypad. (not detachable)

One detachable cover for the expansion bus.

One detachable cover for add-on battery.

One cover for the expansion RAM cards and coprocessor. (not detachable)

LEDs: Outside (Even if LCD screen is shut, the following indicators can be seen.)

- Power indicator (green)
- Battery indicator (green/orange/red)

Inside (When LCD screen is shut, the following indicators cannot be seen.)

- FDD indicator (green)
- HDD indicator (green)
- Caps lock indicator (green)
- Num lock indicator (green)
- Scroll lock indicator (green)

Dimensions: Letter size
8.5"(D) x 11.0"(W) x 1.9"(H)
216mm(D) x 279mm(W) x 48.2mm(H)

Weight: Less than 6.6 pounds (Approx. 3.0kg)
(Including battery, excluding AC adaptor)

3. Software

Operating System: MS-DOS 5.0

- Supplied by three 3.5" diskettes.
- Language: English, French, German
- SEEG: Option (CE-680DE/F/G)

Diagnostics: • Diagnostics software is supplied by one 3.5" diskette.
• Language: English only

4. Operational and storage range

Operational range: 50 to 95 degrees F
10 to 35 degrees C
20 to 80% humidity (Non-condensing)

Storage range: -4 to 140 degrees F
-20 to 60 degrees C
10 to 90% humidity (Non-condensing)

Shock: 5 G (Operating)
60 G (Non-operating)

Vibration: 5-200 Hz (0.5 G peak to peak) (Operating)
5-200 Hz (5 G peak to peak) (Non-operating)

5. MTBF

Target MTBF: 5,000 H

6. DOCUMENTATION

Operation Manual: • Including MS-DOS quick reference.
• Language: English, French, German
• SEEG: Option (CE-680SE/F/G)

7. BIOS

7-1. Outline

The PC-6800 is a notebook-type personal computer having the following features realized through enhanced BIOS functions.

- Use of BIOS (LAP386SL BIOS) for 386 SL made by Phoenix Ltd. (U.S.A.) (386SL CPU register and memory environment initialization and setting)
- Memory roll over function
- Hardware EMS
- Cache memory support (High-speed memory access)
- Pass word function support
- Enhanced set-up functions (4 set-up functions)
 - ① ROM version set-up (Incorporated in BIOS ROM)
 - ② Disk version set-up (SETUP.EXE)
 - ③ Master program (MASTER.EXE)
Set-up utility of pop-up type by hot key
Selection of various screen settings
Power management parameter selection
 - ④ System manager (SYSMAN.EXE: Windows 3.0 application set-up utility)
Power management parameter selection
- Enhanced power management function
Power-saving function by SMI (System Management Interrupt)
Local standby function (Power saving function of each device)
Global standby function (Power saving function of whole system)
Suspend/Resume functions and SUSPEND TO DISK function (2 kinds of SUSPEND/RESUME functions)
Power management by CPU clock (MISER.EXE)
Battery watch (BW.EXE) (Battery remaining capacity monitoring)
- Micro-track ball support (Track ball equivalent to serial mouse is assigned to an RS232C port.)
- IC card conforming to PCMCIA version 2.0 supported.
- FLASH BIOS supported.
BIOS version up grade and efficient writing of FLASH ROM (ROM contents can be changed by software) (Improving serviceability)
- PASSWORD function
Password setting is performed by password utility (PASSWORD.EXE).
Password disappears when the battery is exhausted and the set-up information is lost.
When password is forgotten, make it invalid as follows:
 - ① Remove the rear cabinet.
 - ② Install the IC card which is equipped with Password remover.
 - ③ Turn on the power.
 - ④ Press the red switch described below.

For details about "IC card equipped with Password remover, refer to the service checker manual (separately attached.).

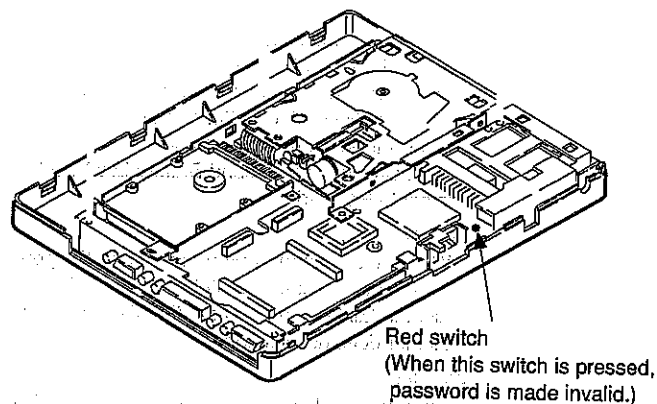


Figure of the system board bottom surface

7-2. BIOS rewriting

The PC-6800 BIOS is stored in the flash ROM and easily rewritten.

(1) BIOS up-date

If FDD works perfectly, BIOS can be rewritten from FDD. The tool (utility) for that purpose is included in the service checker.

For details, refer to the service checker manual (separately attached).

(2) BIOS writing from IC card

If the flash ROM contents are cleared and FDD does not work, the above procedure cannot be performed.

In this case, use the following procedures and rewrite the BIOS using the IC card.

- ① Remove the rear cabinet.
- ② Install the IC card which is equipped with BIOS.
- ③ Turn on the power.
- ④ Press the red switch described in the "Password function".

For details about IC card equipped with BIOS, refer to the service checker manual (separately attached).

7-3. Power-On BIOS message

(1) BIOS Messages

Power-on self tests are the system tests and component initialization processes performed by IBM AT-compatible ROM BIOS in the computer. The main portions of hardware are tested and initialized first. Proper functioning of the main portion is required before further system tests can be run. In general, a failure in a test of the system board or its components will sound a beep, and halt the system. A failure in add-on boards or memory is reported on the screen.

There are two types of messages displayed if the computer fails one of the power-on tests:

- Error messages indicating a failure in either the hardware, software or firmware.
- Informational messages about the power-on and booting processes.

Power-on messages are listed below, with possible causes and solutions.

1) Power-On Self Test Error Messages

Diskette drive (X) failure

Possible cause The floppy disk drive has failed.

Solution Run the diagnostics program to check the floppy disk drive.

Diskette read failure

Possible cause The diskette is either not formatted or defective.

Solution Replace with a formatted diskette.

Fixed disk configuration error

Possible cause The setting on the setup screen is wrong.

Solution Run the setup program and enter the correct values.

Fixed disk failure

Fixed disk controller failure

Solution Reboot. If this does not work, run the diagnostics program to check the hard disk drive.

Fixed disk read failure

Possible cause The hard disk is defective.

Solution Reboot. If that does not work, run the diagnostics program to check the hard disk.

Gate A20 failure

Possible cause The system board is defective.

Solution Check 80386SL and 82360SL

Invalid configuration information-run SETUP program

Possible causes

- Memory size is incorrectly configured.

- Display adaptor is incorrectly configured.

- Incorrect number of disk drives.

Solution Check the settings in the setup program.

I/O card parity interrupt at xx

Possible causes

- The I/O card is improperly inserted.

- The system board is defective.

- The I/O card is defective.

Solution Reinsert the I/O card. If the problem continues, contact the dealer of the I/O card.

Keyboard clock/data line failure

Possible cause The keyboard data line is defective.

Solution Check keyboard controller (80C51SL) and surrounding circuit.

Keyboard failure

Keyboard controller failure

Solution Reboot. If this does not work, run the diagnostics program to check the keyboard.

Keyboard stuck key failure

Possible cause One or more keys were pressed during the power-on self test.

Solution Avoid pressing any keys during the power-on self test except the **Space Bar** to terminate the memory test.

No boot device available

Possible cause Either a floppy disk drive, the hard disk, or the diskette itself is defective.

Solution Reboot. If this does not work, replace the floppy diskette. If the hard disk is faulty, run the diagnostics program.

No boot sector on fixed disk

Possible cause The hard disk is not formatted.

Solution Format the hard disk. Remember this will erase the contents of the hard disk.

Not a boot diskette

Possible cause The diskette in the floppy disk drive is not formatted as a bootable diskette.

Solution Replace the diskette with a bootable diskette and reboot.

Time-of-day not set-run SETUP program

Possible cause The RTC time-of-day clock chip has failed.

Solution Reset the time and data in the setup program.

2) Power-On Self Test informational Messages

XXX Conventional Memory, XXXXXK Extended

Meaning This message indicates the amount of memory that has tested successfully.

Memory tests terminated by keystroke

Meaning This message indicates that you have pressed the **Space Bar** while the memory tests were running. This stops the memory tests.

Press F1 to retry boot, F2 for SETUP program

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows the system to attempt to boot, and pressing **F2** brings you to the setup screen.

Press the F1 key to continue, F2 to run the SETUP program

Meaning This message indicates that an error was found during the power-on tests. Pressing **F1** allows you to start the system, ignoring the error, and pressing **F2** brings you to the setup screen.

7-4. Setup

(1) Setup Program

When using the computer for the first time or after installing options, you must specify your hardware and software configurations. In addition, you can customize many of the settings of your system so that your computer will always start up with those settings. The setup program can specify the hardware and the software configurations by making selections on four pages of the setup program (System Parameters screen, Hardware Device Configuration screen, Feature Configuration screen, and Power Management Feature Control screen).

1) Running the Setup Program

The setup program can be run in three ways:

Power-On Message When you turn on the computer for the first time or after adding an option, the following message will appear on the screen:

Press F1 to continue, F2 to run the SETUP program

This message indicates that the settings on the setup program do not match the actual hardware and software configurations you are using. Press F2 to display the setup program.

Pressing F1 will bypass the message and allow you to start MS-DOS, although you will still have to set your new configurations later.

Accessing the Setup Program from MS-DOS Enter the SETUP command. To execute the SETUP command, the SETUP.EXE file must be in the current directory on the hard disk or within the current path.

Note: Some application programs, such as Microsoft Windows, have a SETUP.EXE file as their setup or installation program. If the directories of these application programs precede the DOS directory in the path, their SETUP.EXE will execute. In this case, enter the full path (\DOS\SETUP) to run the Sharp setup program.

Accessing the Setup Program Directly This method does not rely on having MS-DOS running. Pressing Fn-F1 (Set Up) enables you to access the setup program even while you are in an application program.

Caution: Some application programs allow you to run the setup program even if the application is running, by pressing Fn-F1 (Set Up). However, this is NOT recommended, because the computer will restart when it exits the setup program and you will lose the contents of memory.

2) Making Selections

Guidance for available keys on the setup screens are displayed on the bottom of each setup screen.

→/↓ Moves the cursor forward through each item

←/↑ Moves the cursor backward through each item

PgDn (Fn-↓) Moves to the next page

PgUp (Fn-↑) Moves to the previous page

Space Bar/+/- Selects a value for the highlighted item. The space Bar or + key moves forwards through the selection list while the -key moves backwards. If there are only two selection in the list, all three keys (Space Bar, + and-) act as toggles

Note: Some items require direct keyboard input.

F1 Displays an on-line help message for the current (highlighted) item.

Note: On-line help is only available when you run the setup program using the SETUP command.

F2 Displays system information.

Note: System Information is only available you run the setup program using the SETUP command.

F3 Reinitialize the settings of all the items on each setup screen to their default values.

Pressing the Esc key displays the Exit/Save Menu.

Esc Returns to the setup program to make more selections.

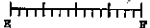
F4 Exits the setup program with all the updated settings you made.

F6 Simply aborts the setup program without updating any of the settings you made.

The selections you make on the setup program are stored in a special memory area which is backed up by the built-in clock battery. All selections are maintained even when the power is turned off. If the system has not been used for an extended period of time, however, the clock battery may become discharged. When using the computer for the first time after a long period without use, run the setup program and use F3 to reset the settings if necessary.

Each category on the program is described below

System Parameters Screen (Page 1)

SHARP PERSONAL COMPUTER SETUP PROGRAM (Version 1.00) (c) Phoenix Technologies Ltd. 1985, 1991 All Rights Reserved			
MOBILE		**System Parameters** Page 1/4	
System Time:	11:38:51	Password:	Disabled
System Date:	Wed, Oct 02, 1991	Hard Disk Size:	80 MB
Time/Date Format:	24 hour (US)	CPU Speed:	20 MHz
Battery		Display Adaptor:	Internal VGA
		Display Mode:	VGA
Setup Configuration:	Mobile	Conventional Memory:	640 KB
Quick Boot:	Off	Expanded Memory:	OKB
Suspend Mode:	Suspend/Resume	Extended Memory:	1024 KB
Scroll Lock:	Off	IC Card Memory:	0 KB
Caps Lock:	Off		
Num Lock:	Off	Total Extended Memory:	1024 KB
Cursor Type:	Underline	Memory Available:	1664 KB
ESC EXIT/SAVE		F3 Defaults	F4 Field
		Sp/+/- Value3	FgUp/Dn Page

System Time This field specifies the current time. Time is set either in a 12-hour or a 24-hour clock format depending on the format specified in the Time/Date Format field. Press the Space Bar or the + key to increase the time, or the -key to decrease it. This also resets the seconds to 00.

System Date This field specifies the current date. The date is set either in the month-day-year or the day-month-year order depending on the format specified in the Time/Date Format field. The day of the week (Mon, Tue, Wed, etc.) is set automatically after the date is entered.

Time/Date Format This field specifies the Time and Date format.

The Time can be set either in a 12-hour or 24-hour format, and the Date can be set in either a U.S. style (month-day-year) or European style (day-month-year). The possible settings are: 12 hour (US), 12 hour (Euro.), 24 hour (US) and 24 hour (Euro.).

Battery This field displays the estimated remainder of the battery charge in a fuel gauge format. The battery status is based on the latest information available to the Battery Watch utility.

Note: The battery gauge appears only when you install the Battery Watch program.

Setup Configuration This field specifies the level of the power savings. The possible settings are: Mobile or Docking Station. The system remembers the values of any other relevant fields, especially the settings on the Power Management Feature Control screen. The current setting of this field is always shown in the upper left corner of all setup screens. The system starts up with the Mobile setting when the optional expansion unit is not connected, and with the Docking Station setting when the expansion unit is connected.

Quick Boot This field selects quick loading of the system. When this field is set to On, the system bypasses some of the power-on self checks (including memory check) when starting up. The possible settings are: On or Off.

Suspend Mode This field specifies what happens when a Suspend event occurs. Suspend events are:

- Auto System Suspend (See Power Management Feature Control Screen for details.)

- Suspend Battery Low (See Power Management Feature Control Screen for details.)
- Suspend Button
- Screen Close (See Feature Configuration Screen for details.)

The possible settings are: Suspend/Resume or Suspend to Disk. If Suspend/Resume is selected, a "suspend event" causes the system to enter the Suspend mode. A "resume event" returns the system to exactly where it was when the suspend occurred. Resume events are:

- Suspend Button
- Screen Open (See Feature Configuration Screen for details.)
- Resume on Modem Ring (See Power Management Feature Control Screen.)
- Resume Time-of-Day (See Power Management Feature Control Screen.)

If Suspend to Disk is selected, a "suspend event" causes the system to save any data in memory to the special partition on the hard disk and turns off the system power. To return from this state, the power switch must be turned off and back on.

Note: To activate the Suspend-to-Disk function, the hard disk must have the Suspend-to-Disk partition adequate for the memory size.

Caution: The Suspend-to-Disk function will provide you with a substantial amount of protection against loss of data in many situations, although there are some situations where data loss may occur. As above-mentioned, your system will automatically save data in the memory to the hard disk, in a dangerously low battery condition. This procedure will require the hard disk to be operating. If the machine is jarred or struck during the save procedure, data loss may occur.

Scroll Lock Specifies the default state of the **Scr LK** key. Possible settings are: On or Off

Caps Lock Specifies the default state of the **Caps Lock** key. Possible settings are: On or Off.

Num Lock Specifies the default state of the **Num Lk** key. Possible settings are: On or Off.

Cursor Type The shape of the cursor can be changed to one of the following settings: Underline, Underbar, or Block.

Password This field allows the user to enable or disable the password you set using the PASSWORD utility. The possible settings are: Enabled or Disabled. When Enabled is selected, the system prompts you to enter the password each time you start the system, displaying a key mark (on) on the top of the screen. At this prompt only, you can change the password by typing the current password followed by a slash (/), a new password and then Enter. To delete the password, enter the password followed by a slash, or set the Password field to Disabled. When the system resumes from the Suspend mode, you are also required to enter the password (the indicators on the upper left of the keyboard blink in sequence).

Hard Disk Size This field shows the size of the hard disk in MB.

CPU Speed These fields specify the CPU speed used when the system is booted. The possible settings are: 25 MHz, 10 MHz, or 5 MHz.

Note: CPU Speed may be changed from the keyboard using Ctrl-Alt-↑ to increase the speed and Ctrl-Alt-↓ to decrease the speed. See the Speed Switch Key field on the Feature Configuration Screen.

Display Adaptor This field specifies the type of display adaptor used by the computer. The possible settings are: Internal VGA, CGA40, CGA80, Mono, or Others. Unless you use a display adaptor card inserted in the optional expansion unit, set this field to Internal VGA.

Display Mode This field specifies the mode of the internal VGA controller. The possible settings are: VGA, EGA, CGA, MDA, HGC or SVGA. The HGC and SVGA (Super VGA-800x600x16 colors) modes are effective only for an external CRT monitor. Typically, this field should be set to VGA Mode. The internal VGA display adaptor will automatically emulate the display mode of your application software configuration. (Either text or graphics mode will be selected). If the screen displays improperly, refer to your application program manual for instructions on how to set the display mode.

Conventional Memory This field always shows 640 KB.

Expanded Memory This field display the amount of internal expanded memory.

Extended Memory This field displays the amount of internal extended memory.

IC Card Memory This field displays the amount of extended memory on the IC card inserted in the IC card slot.

Total Extended Memory This field display the total amount of internal extended memory and any IC card memory that is set to extended memory.

Memory Available This field displays the total amount of memory in the system.

Hardware Device Configuration Screen (Page 2)

SHARP PERSONAL COMPUTER SETUP PROGRAM (Version 1.00)									
(c) Phoenix Technologies Ltd. 1985, 1991 All Rights Reserved									
MOBILE **Hardware Device Configuration ** Page 2/4									
Hard Disks: Cyl Hd Pre IX Sec Size									
Internal Hard Disk1: C: Type 10 965 10 -1 965 17 80									
External Hard Disk2: - Not Installed									
Floppy Drives and IC Card:									
Device 1 (DriveA): Internal Floppy Disks: 3.5", 1.44 MB									
Device 2 (DriveB): Not Installed									
Device 3 (Other): Not Installed									
Serial Ports DOS Name I/O IRQ Parallel Port DOS Name I/O IRQ									
COM Port: COM1 03F8h 4 Printer Port: LPT1 03BCh 7									
Track Ball: COM2 02F8h 3									
Esc Exit/Save				F3 Defaults		←→ Field		Sp/+/- Value	
								Pg/Dn Page	

Hard Disks

This category specifies the type of the hard disk.

Internal Hard Disk 1 This field assigns the drive letter to the internal hard disk and specifies its type. According to the specified drive type, the following information is displayed:

- number of cylinders
- number of heads
- precompensation
- landing zone
- number of sectors per track
- disk size (capacity)

External Hard disk 2 This field assigns the drive letter to the external hard disk and specifies its type. Normally, set this field to Not Installed.

Floppy Drives and IC Card

This category specifies the type of floppy disk drives and IC card.

Device 1 (Drive A) This field specifies drive A assignment. The possible settings are: Internal Floppy Disk, External Floppy Disk, IC Card RAM Disk or Not Installed. You can also specify the size and capacity.

Device 2 (Drive B) This field specifies drive B assignment. The possible settings are: Not Installed, Internal Floppy Disk, External Floppy Disk or IC Card RAM Disk. You can also specify the size and capacity.

Device 3 (Other) This field specifies the way the computer is to use the IC card. The possible settings are: Not Installed, IC Card Extended Memory or IC Card COM Port. You can also specify the amount of memory and COM port number.

Serial Ports

This category specifies the port number of the serial interfaces. When the port number is specified, the I/O address and IRQ number for that port is displayed on the right.

Note: If you install an IC card which has a serial port, set the port number in the Device 3 (Other) field in the previous category.

Note that some applications support only two serial port, COM1 and COM2.

COM Port This field specifies the port number of the serial RS-232C port. The possible settings are: COM1, COM2, COM3, COM4 or Disabled.

Trackball This field specifies the port to which the trackball is connected. The possible settings are: COM1, COM2, COM3, COM4 or Disabled.

Parallel Port

This category specifies the port number of the parallel port. When the port number is specified, the I/O address and IRQ number for that port is displayed on the right.

Printer Port This field specifies the port number of the parallel printer port of the computer. The possible settings are: LP1, LP2, LP3 or Disable.

Feature Configuration Screen (Page 3)

SHARP PERSONAL COMPUTER SETUP PROGRAM (Version 1.00)			
(c) Phoenix Technologies Ltd. 1985, 1991 All Rights Reserved			
MOBILE	**Feature Configuration**		Page 3/4
Shadow BIOS ROM:	Enabled	EMS Memory Size:	Disabled
Shadow Video ROM:	Enabled	EMS PageFrame:	Disabled
Cache:	Enabled	Key Repeat Rate:	Fast
Cache BIOS ROM:	Enabled	Parallel Port:	Bidirectional
Cache Video ROM:	Enabled	Speed Switch Key:	Enabled
640-1024 KB Relocation:	Disabled	Screen Close Switch:	Disabled
Vertical Stretching	Off		
Backlight brightness:	High		
Esc Exit/Save F3 Defaults ←F1→ Field Sp/+/= Value Fg/Dn Page			

Shadow BIOS ROM This field enables or disables shadowing of the BIOS ROM. When enabled, the contents of the BIOS ROM is copied to memory between 640 KB and 1024 KB for faster execution.

Shadow Video ROM This field enables or disables shadowing of the Video ROM. When enabled, the contents of the Video ROM is copied to memory between 640 KB and 1024 KB for faster execution.

Cache This field specifies whether to enable or disable cache. The BIOS ROM and Video ROM cannot be cached unless option is enabled.

Note: This computer has 16 KB of high speed cache memory used to access data quickly.

Cache BIOS ROM This field specifies whether to enable or disable caching of the BIOS ROM.

Cache Video ROM This field specifies whether to enable or disable caching of the Video ROM.

640-1024 KB Relocation This field enables or disables the relocation of the memory between 640 KB and 1024 KB. When enabled, this feature causes the unused (i.e. not shadowed) memory between 640 KB and 1024 KB to be relocated to above the 1MB boundary and addressed as extended memory, except when PEMM.SYS is loaded. When PEMM.SYS is loaded, the memory can be used as logical pages.

EMS Memory Size This field specifies the amount of memory to be used as expanded memory, in 512 KB increments. Select Disabled if there is no memory to be used as expanded memory.

Note: This cannot exceed the total amount of extended memory on the system. The size specified here is displayed on the System Parameters screen (page 1/4).

EMS Page Frame This field displays the location of the EMS page

frame when EMS memory is defined. This will always be C000h-D3FFh.

Key Repeat Rate This field specifies the keyboard repeat rate. Possible settings are: Fast or standard.

Parallel Port This field specifies how the internal parallel port is to be configured, as unidirectional or bidirectional. The possible settings are: Unidirectional or Bidirectional.

Speed Switch Key This field lets you change the CPU clock speed from the keyboard. If you set this field to Enabled, you can change the CPU clock speed using the Ctrl-Alt-↑ or Ctrl-Alt-↓ key combination on the keyboard while using the computer. Ctrl-Alt-↑ increases the CPU speed step by step in the 5 MHz-10 MHz-25 MHz order, and Ctrl-Alt-↓ slows down the CPU speed step by step in the 25 MHz-10 MHz-5MHz order. The possible settings are: Enabled or Disabled.

You will hear a high-pitched beep when pressing Ctrl-Alt-↑, and a lower pitched beep when pressing Ctrl-Alt-↓. A middle tone results from the middle (10MHz) CPU speed.

When the maximum speed is reached, the Ctrl-Alt-↑ key combination does nothing, and when the minimum speed is reached, the Ctrl-Alt-↓ key combination does nothing.

Note: In some cases, the key functions of Ctrl-Alt-↑ and Ctrl-Alt-↓ may not be effective even when Enabled in the setup program. In this case, change the CPU Speed in the setup program.

Screen Close Switch This field specifies whether or not to activate the screen close switch function. The possible settings are Suspend or Disabled. When Suspend is selected, closing the screen panel causes the system to enter either the Suspend or Suspend-to-Disk mode depending on what was specified in the Suspend Mode field on the System Parameters screen. When Disabled is selected, closing the screen panel turns off the LCD.

Vertical Stretching This field specifies whether or not to activate the display expand function.

The possible settings are Full or Off.

When Full is selected, display is fully expanded in vertical even if the display mode has less resolution than 480 pixels (such as CGA, MDA, EGA).

When Off is selected, display expansion is not performed.

Backlight Brightness This field specifies the backlight brightness. The possible settings are High or Low.

Power Management Feature Control Screen (Page 4)

SHARP PERSONAL COMPUTER SETUP PROGRAM (Version 1.00)			
(c) Phoenix Technologies Ltd. 1985, 1991 All Rights Reserved			
MOBILE	**Power Management Feature Control**		Page 4/4
Global Power Management: Enabled			
Global Standby Timer:	10 minutes	Hard Disk Motor Timeout:	1 minute
Auto System Suspend:	20 minutes	CRT/LCD Panel Timeout:	5 minutes
Suspend Warning tone:	Disabled	Minimum Backlight:	Disabled
Suspend Battery Low:	Enabled	Printer Port Timeout:	5 minutes
Resume Battery Low:	Disabled	Printer Port Timeout:	4 seconds
Resume Modem Ring:	Disabled	Serial Port Timeout:	4 seconds
Resume time-of-Day:	Disabled	IC Card:	Enabled
Resume Time: 00:00			
Esc Exit/Save F3 Defaults ←F1→ Field Sp/+/= Value Fg/Dn Page			

Global Power Management This field specifies whether or not to activate the power management functions. The possible settings are: Enabled, Disabled or AC Disable. When set to Enabled, all settings on this screen are effective. When set to Disabled, no power management occurs regardless of the values specified for the other options. When set to AC Disable, all power management is disabled except Backlight Timeout, CRT/LCD Panel Timeout and Suspend on button/screen close, when the computer is operating on AC power.

Global Standby Timer After a specified period of inactivity, the system automatically enters the Global Standby mode. Pressing any key on the keyboard returns the system to the normal active mode. The possible settings are: 8 seconds, 32 seconds, 1 minute, 3 minutes, 5 minutes, 7 minutes, 10 to 50 minutes (in 5-minute increments) or Disabled. When set to Disabled, the Auto System Suspend feature does not work, either.

Auto System Suspend After a specified period from when the system enters the Global Standby mode, the system automatically moves from Global Standby mode to Suspend or Suspend-to-Disk mode depending on the selection in the Suspend Mode field on the System Parameters screen. The possible settings are: 8 seconds, 32 seconds, 1 minute, 3 minutes, 5 minutes, 7 minutes, 10 to 50 minutes (in 5-minute increments) or Disabled.

Note: The Global Standby Timer must be enabled for the Auto Suspend feature to work.

Suspend Warning Tone This field specifies whether or not to sound a beep when the system enters the Suspend mode. The possible settings are: Enabled or Disabled.

Suspend Battery Low This field specifies whether or not to enter the Suspend or Suspend-to-Disk mode, depending on the selection in the Suspend Mode field on the System Parameters screen, at the time of low battery. The possible settings are: Enabled or Disabled.

Resume Battery Low This field specifies whether or not to resume full operation from the Suspend mode on Modem Ring or Time-of-Day at the time of low battery. The possible settings are: Enabled or Disabled.

Resume Modem Ring The system returns to the normal active mode from the Suspend mode on detection of a modem ring. The possible settings are: Enabled or Disabled.

Resume Time-of-Day This field enables or disables the Resume Time-of-Day feature. The resume date timer may be set to any time within 24 hours, as described below. If the resume timer is set, the system returns to full power when the specified time is reached.

Resume time The system automatically returns to the normal active mode from the Suspend mode at the specified time. Specify the time in the hh:mm:ss format. This subfield is effective only when the Resume Time-of-Day field is set to Enabled.

Note: Although you can set any time resume time in the subfield, within 24 hours after the system enters the Suspend mode, the Suspend state lasts a maximum of 14 hours if the AC adaptor is not connected. (The battery will be fully discharged.)

Hard Disk Motor Timeout After a specified period with no access to the hard disk, the hard disk drive motor is automatically turned off. The time from the last access until the motor is turned off can be set. The possible settings are: 10 seconds, 1 to 20 minutes (in 1-minute increments) or Disabled.

CRT/LCD Panel Timeout After a specified period of inactivity, the system automatically shuts off the power to the CRT or LCD panel. Pressing any key on the keyboard turns the CRT or LCD panel back on. The backlight is also turned off when the LCD panel is turned off. The possible settings are: 8 seconds, 1 to 16 minutes (in 1-minute increments) or Disabled.

Minimum Backlight When this feature is enabled, the backlight is turned down to "low intensity" if there is no activity for half (1/2) of the time specified in the Backlight Timeout option. If there continues to be no activity for the remaining half of the Backlight Timeout, the backlight is turned off. Pressing any key on the keyboard returns the backlight to full intensity. The possible settings are: Enabled or Disabled. When Backlight Brightness is set to Low, this function will not work.

Backlight Timeout After a specified period of inactivity, the system automatically turns off the backlight. Pressing any key on the keyboard turns the backlight back on. The possible settings are: 8 seconds, 1 to 16 minutes (in 1-minute increments) or Disabled.

Printer Port Timeout After a specified period of inactivity to the parallel printer port, the power to the parallel printer port is automatically shut off. The possible settings are: 4 seconds to 1 minute (in 4-second increments) or Disabled.

Serial Port Timeout After a specified period of inactivity to the serial RS-232C port, the power to the serial RS-232C port is automatically shut off. The possible settings are: 4 second to 1 minute (in 4-second increments) or Disabled.

IC Card This field determines whether or not to provide power to the IC card slot at all times. When Enabled is selected, power is provided to the IC card slot at all times. When Disabled is selected, power is provided to the IC card slot only when a card is inserted into the slot. The possible settings are: Enabled or Disabled.

7-5. POST (Power On Self Test) ERROR CODE LIST

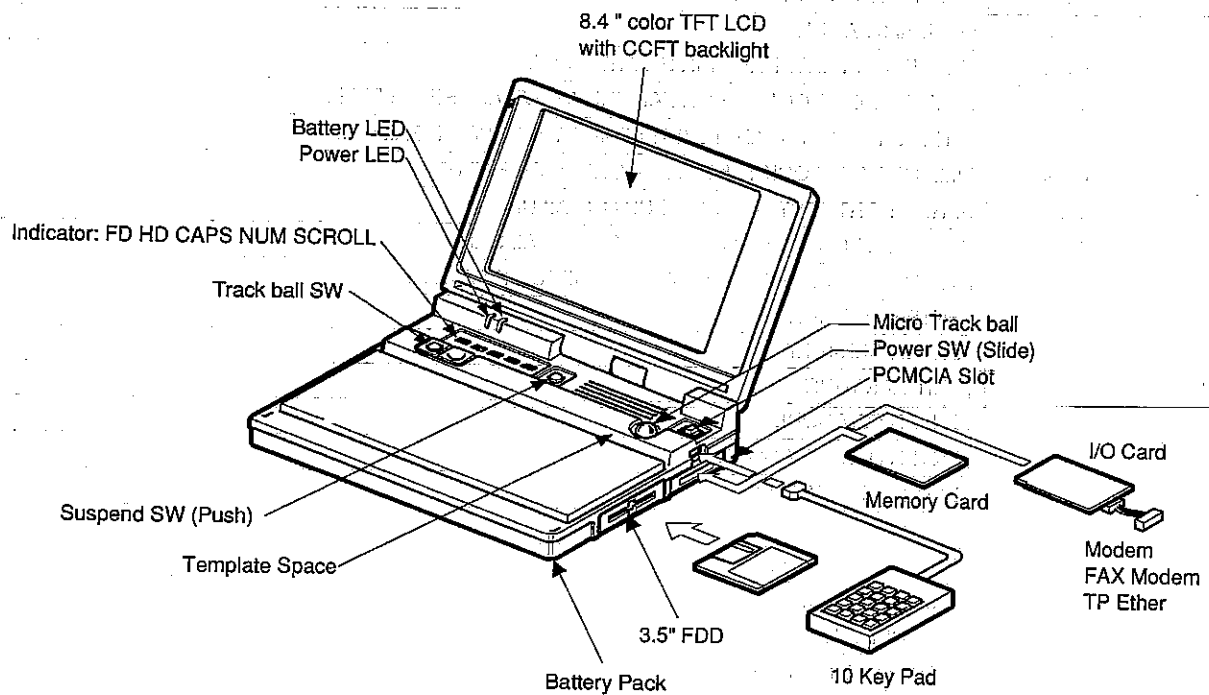
When the system has any hardware problem that prevent booting up, following Diag code is output to MFG port (I/O Address 80H), and Beep Code sounds.

DIAGNP OUTPUT	BEEP CODES	DESCRIPTION OF TEST OR FAILURE
01H		80386 REGISTER TEST IN PROGRESS
02H	1-1-3	CMOS WRITE/READ TEST IN PROGRESS OR FAILURE
03H	1-1-4	BIOS ROM CHECKSUM IN PROGRESS OR FAILURE
04H	1-2-1	PROGRAMMABLE INTERVAL TIMER TEST IN PROGRESS OR FAILURE
05H	1-2-2	DMA INITIALIZATION IN PROGRESS OR FAILURE
06H	1-2-3	DMA PAGE REGISTER WRITE/READ TEST IN PROGRESS OR FAILURE
08H	1-3-1	RAM REFRESH VERIFICATION IN PROGRESS OR FAILURE
09H		1ST 64K RAM TEST IN PROGRESS
0AH	1-3-3	1ST 64K RAM CHIP OR DATA LINE FAILURE MULTI BIT
0BH	1-3-4	1ST 64K RAM ODD/EVEN LOGIC FAILURE
0CH	1-4-1	1ST 64K RAM ADDRESS LINE FAILURE
0DH	1-4-2	1ST 64K RAM PARITY TEST IN PROGRESS OR FAILURE
0EH	1-4-3	FAIL-SAFE TIMER TEST IN PROGRESS
0FH	1-4-4	SOFTWARE NMI PORT TEST IN PROGRESS
10H	2-1-1	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 0
11H	2-1-2	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 1
12H	2-1-3	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 2
13H	2-1-4	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 3
14H	2-2-1	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 4
15H	2-2-2	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 5
16H	2-2-3	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 6
17H	2-2-4	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 7
18H	2-3-1	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 8
19H	2-3-2	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT 9
1AH	2-3-3	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT A
1BH	2-3-4	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT B
1CH	2-4-1	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT C
1DH	2-4-2	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT D
1EH	2-4-3	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT E
1FH	2-4-4	1ST 64K RAM CHIP OR DATA LINE FAILURE – BIT F
20H	3-1-1	SLAVE DMA REGISTER TEST IN PROGRESS OR FAILURE
21H	3-1-2	MASTER DMA REGISTER TEST IN PROGRESS OR FAILURE
22H	3-1-3	MASTER INTERRUPT MASK REGISTER TEST IN PROGRESS OR FAILURE
23H	3-1-4	SLAVE INTERRUPT MASK REGISTER TEST IN PROGRESS OR FAILURE
25H		INTERRUPT VECTOR LOADING IN PROGRESS
27H	3-2-4	KEYBOARD CONTROLLER TEST IN PROGRESS OR FAILURE
28H		CMOS POWER FAIL AND CHECKSUM CHECKS IN PROGRESS
29H		CMOS CONFIG INFO VALIDATION IN PROGRESS
2BH	3-3-4	SCREEN MEMORY TEST IN PROGRESS OR FAILURE
2CH	3-4-1	SCREEN INITIALIZATION IN PROGRESS OR FAILURE
2DH	3-4-2	SCREEN RETRACE TESTS IN PROGRESS OR FAILURE
2EH		SEARCH FOR VIDEO ROM IN PROGRESS
30H		SCREEN BELIEVED OPERABLE:
30H		SCREEN BELIEVED RUNNING W/ VIDEO ROM
31H		MONOCHROMATIC SCREEN BELIEVED OPERABLE
32H		40-COLUMN COLOR SCREEN BELIEVED OPERABLE

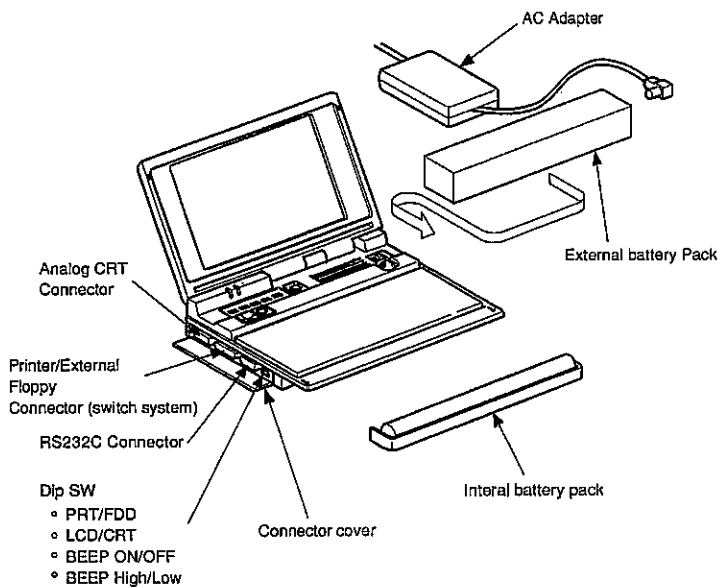
DIAGNP OUTPUT	BEEP CODES	DESCRIPTION OF TEST OR FAILURE
33H		80-COLUMN COLOR SCREEN BELIEVED OPERABLE
34H	4-2-1	TIMER TICK INTERRUPT TEST IN PROGRESS OR FAILURE
35H	4-2-2	SHUTDOWN TEST IN PROGRESS OR FAILURE
36H	4-2-3	GATE A20 FAILURE
37H	4-2-4	UNEXPECTED INTERRUPT IN PROTECTED MODE
38H	4-3-1	RAM TEST IN PROGRESS OR FAILURE ABOVE ADDRESS 0FFFFH
3AH	4-3-3	INTERNAL TIMER CHANNEL 2 TEST IN PROGRESS OR FAILURE
3BH	4-3-4	TIME OF DAY CLOCK TEST IN PROGRESS OR FAILURE
3CH	4-4-1	SERIAL PORT TEST IN PROGRESS OR FAILURE
3DH	4-4-2	PARALLEL PORT TEST IN PROGRESS OR FAILURE
3EH	4-4-3	MATH COPROCESSOR TEST IN PROGRESS OR FAILURE
C0H		; ENTER CSET INIT
C1H		; ENTER GENIO INIT
C2H		; EXIT GENIO INIT
C3H		; ENTER FCM CODE
C4H		; ENTER DYN MEM CODE
C5H		; EXIT DYM MEM CODE
C6H		; EXIT FCM CODE
C7H		; ENTER RCM CODE
C8H		; EXIT RCM CODE
C9H		; EXIT CSET INIT
CAH		; ENTER CSET BFR VIDROM
CBH		; ENTER CSET BFR SIZEMEM
CCH		; ENTER CSET AFT MTEST
CDH		; ENTER CSET AFT CMCFG
CFH		; EXIT CSET BFR OPROM

CHAPTER 3. STRUCTURES AND PARTS IDENTIFICATION

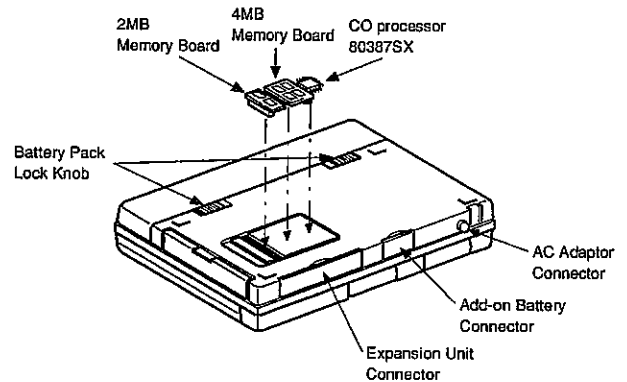
1. External view (1)



2. External view (2)

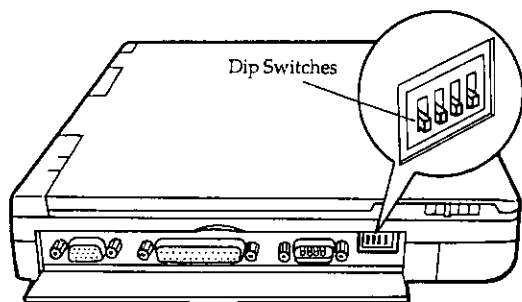


3. External view (3)



4. Switches

- ① **Power switch (slide switch)**
 OFF: Complete power OFF
 ON: Power ON, suspend, or SAVED OFF power OFF. (In SAVED OFF, the power is turned off by the software. The power is OFF though the power switch is ON.)
- ② **Suspend/resume double switch**
 Pushing during normal operation with power ON: Enters into the suspend state.
 Pushing during suspend state with power ON: Resume
 Pushing with power OFF: Invalid
- ③ **DIP Switches**
 To the right of the parallel/external FDD port connector is a group of four DIP switches that control the functions described below. The DIP switches are easily set with a pointed object, such as a pen point.
 For SW3 and SW4, new settings are normally only effective at the next power on.



SW1 Speaker On/Off Switch DIP switch 1 turns the speaker on and off.

Up Speaker Off
 Down Speaker On (default)

SW2 Speaker Volume Switch DIP switch 2 sets the speaker volume to high or low.

Up Speaker Volume Low
 Down Speaker Volume High (default)

SW3 Parallel/External FDD Switch DIP switch 3 specifies the function of the port as either a parallel (Centronics) port (for a parallel printer, for example), or an external floppy disk drive port.

Up External FDD
 Down Parallel Port (default)

SW4 LCD/CRT only Switch DIP switch 4 specifies either a simultaneous display on both the LCD and the external CRT or a display on only the external CRT.

In the simultaneous display mode, the CRT displaying method is the same as that of the LCD. If you use an external monitor which requires a CRT-specific signal, set DIP switch 4 to the up position.

Up CRT only
 Down LCD/CRT simultaneously (default)

- ④ **Boot switch and back-up reset switch**
 Not pushed: Normal operation
 Push: IC card boot and RTC backup reset
 IC card boot

When this switch is pushed with the power ON, BIOS mapping is swapped into the IC memory card of special specifications. Then BIOS in the IC card restarts to change and write the BIOS in the unit again.

5. LED

- ① **Power LED (green)**
 ON: Power ON
 Blink: Suspend
 OFF: Power OFF
- ② **Battery LED (red, green, orange)**
 Green ON: Completion of charging of built-in & add-on batteries
 Green blink: During quick charging of built-in & add-on batteries
 Red ON: Built-in & add-on batteries charge request
 Red blink: Built-in & add-on batteries operation critical state
 Orange ON: AC adaptor connected.
 Depending on the system, standard charging is made. (When standard charging is completed, the green lamp will light on though the AC adaptor is connected.)
 Orange OFF: Built-in & add-on batteries are ready to operate, and the charging circuit is in standby state.
- ③ **HDD LED (Green)**
 ON: Hard disk access
 OFF: Hard disk standby
- ④ **FDD LED (Green)**
 ON: Standard/external FDD access
 OFF: FDD standby
- ⑤ **NumLock (Green)**
 ON: NumLock ON
 OFF: NumLock OFF
- ⑥ **CapsLock (Green)**
 ON: CapsLock ON
 OFF: CapsLock OFF
- ⑦ **ScrollLock (Green)**
 ON: ScrollLock ON
 OFF: ScrollLock OFF

CHAPTER 4. DISASSEMBLY AND ASSEMBLY

This chapter describes the disassembly procedure for the PC-6881 device.

The assembly procedure is not provided in this chapter, since the device can be assembled by reversely performing the disassembly procedure. The procedure steps specific to assembly, however, will be provided as "Notes for Assembly" if necessary.

The procedure exclude the description for the unit/part replacement when the replacement does not require a specific complicated procedure.

Tool	Hex wrench	I.D. 5.5mm
------	------------	------------

1. Precautions

1. Before starting disassembly of the device, remove all the optional units (ex. expanded memory module) and the AC adapter.
2. Use a Phillips screwdriver of an appropriate size to remove the screws.
3. Many parts will be removed during disassembly of the device. Disassemble the device on a neat table in order not to lose any of the removed parts.
4. Plug/unplug connectors by holding both sides of the connector. Do not unplug connectors by pulling on the cables to avoid line breakage.

2. Disassembly and Assembly

(1) Removing display unit

Disassembly (See Fig. 1)

1. Remove left damper cover ①, right damper cover ②, and cable cover ③.
2. Unplug connectors ④, ⑤ and ⑩.
3. Remove screws ⑥ and ⑦ to remove display unit ⑧.
4. Remove screw ⑨.

[Note for Assembly]

- When attaching display unit 8, align edges A and C of the dampers to respective edges B and D of the upper cabinet to screw the damper onto the upper cabinet.

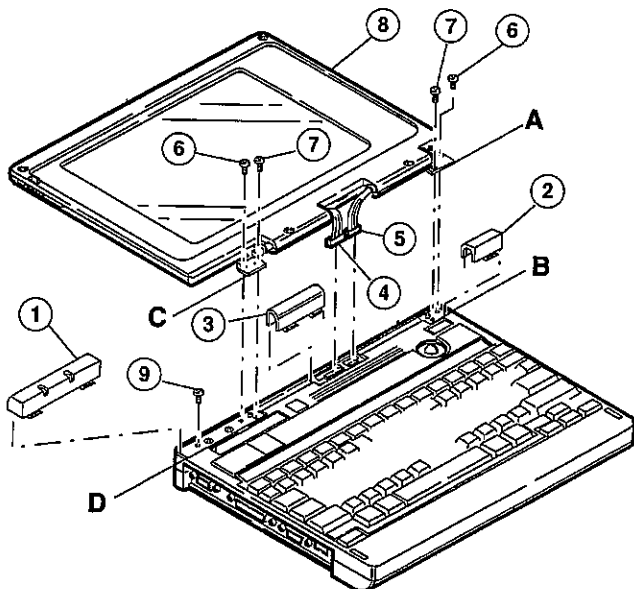


Fig. 1

(2) Disassembling upper and lower cabinets

Disassembly (See Fig. 2, 3)

1. Turn over the device.
2. Remove battery cover ① and battery ②.
3. Remove two rubber legs ③.
4. Remove screw ④ and eject button ⑤.
5. Open cover ⑥ to remove six screws ⑦.

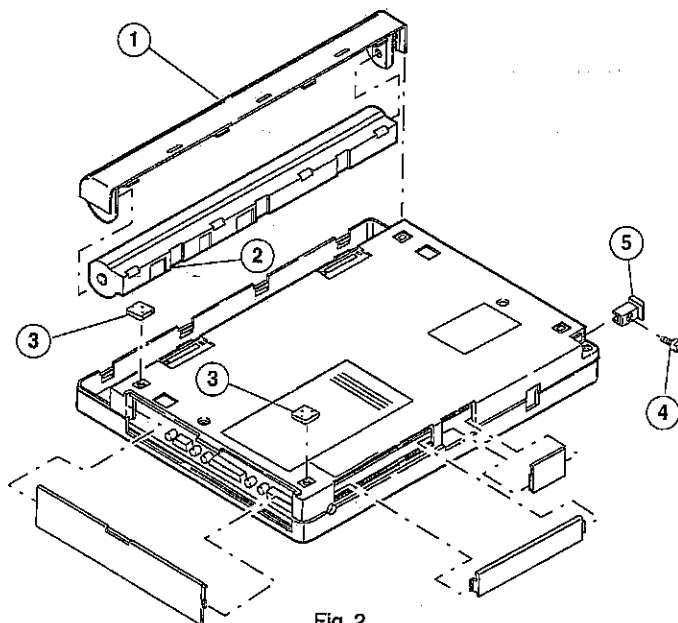


Fig. 2

6. Remove lower cabinet ⑧ from upper cabinet ⑨ by lifting the lower cabinet from B side.
7. Remove connector cover ⑩.

[Notes for Assembly]

1. When attaching the upper and lower cabinets, be sure that the four projections on the A side fit properly.
2. When attaching connector cover ⑩, align and fit the projections of the connector cover into the holes on upper cabinet ⑨.

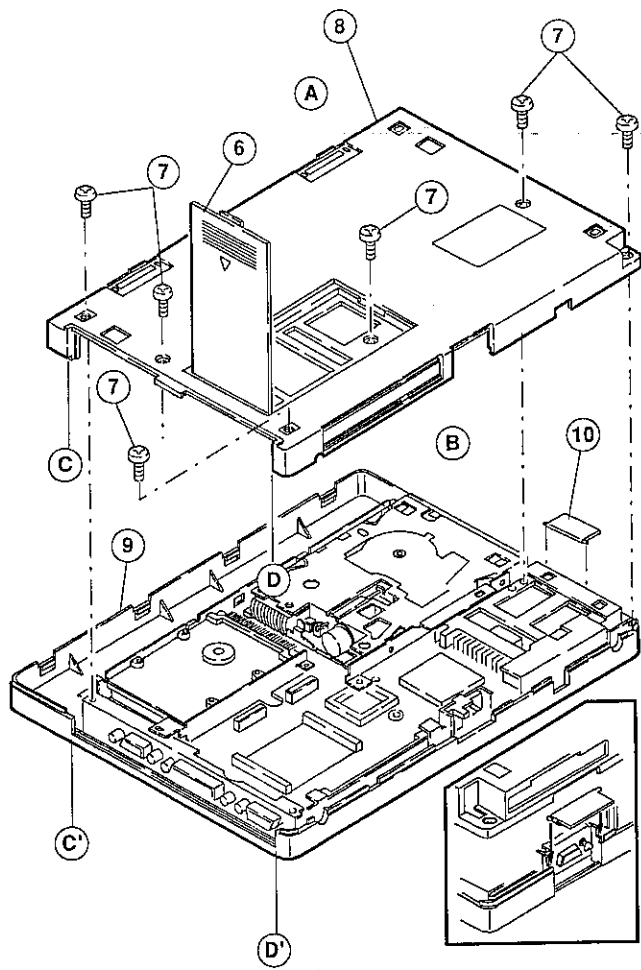


Fig. 3

(3) Removing keyboard

Disassembly (See Fig. 4)

1. Remove screws ①, screw ② ~ ⑥, through ⑦ and ⑧.
2. Remove connector FPCs ⑨ and ⑩ from the board.
3. Remove board unit ⑪ from upper cabinet ⑫.
4. Remove two screws ⑬.
5. Remove keyboard ⑭ from upper cabinet ⑫.

[Notes for Assembly]

1. When attaching a HDD/FDD unit, tighten the screws ⑥ through ①, starting from screw A to F.
2. When attaching keyboard ⑭ onto upper cabinet ⑫, first make sure the three projections of keyboard ⑭ are fitted in the three holes ⑭' of upper cabinet ⑫.

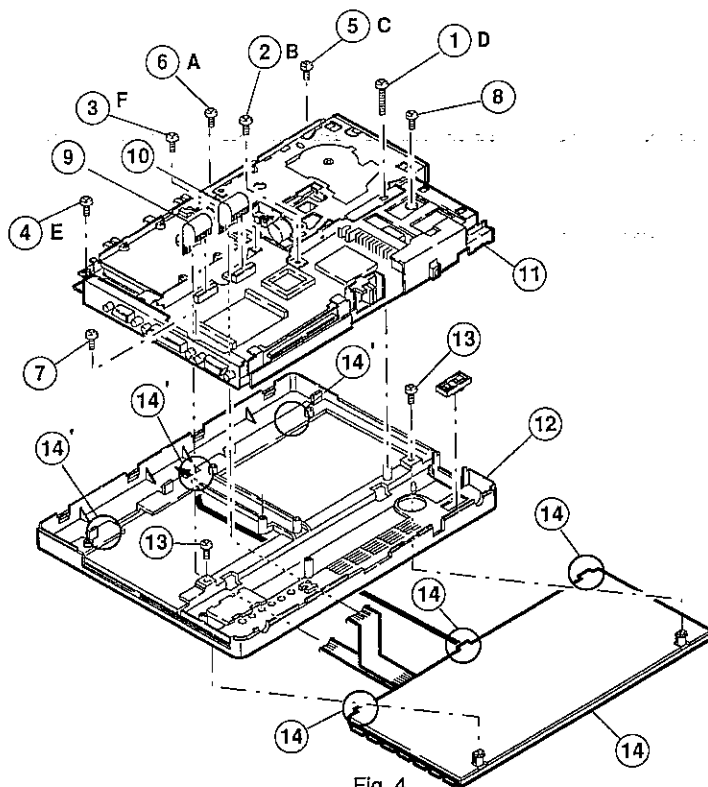


Fig. 4

(4) Replacing HDD/FDD units

Be careful when handling the HDD/FDD units. These precision-made devices are liable to be damaged by static electricity or vibration when they are removed from the main unit.

Disassembly (See Fig. 5, 6)

1. Remove two screws ①.
2. Remove connector ② to remove PWB battery unit ③.
3. Remove FD FPC ④ and HD FPC ⑤ from the board.

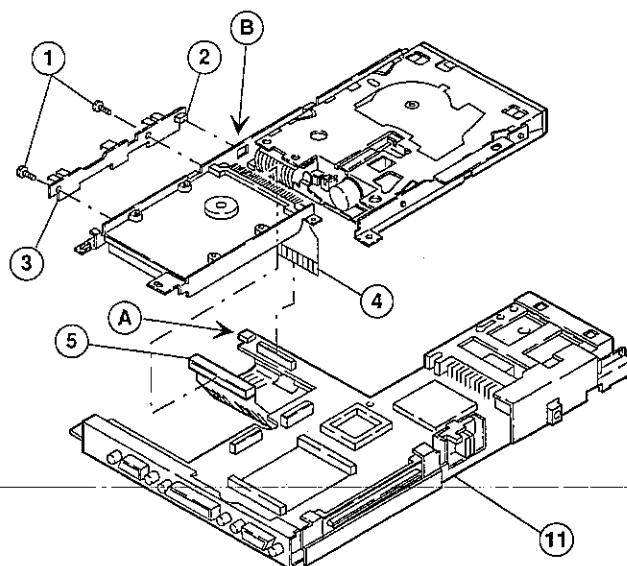


Fig. 5

4. Remove two screws ⑥ to remove HDD unit ⑦ from FD/HD angular bar ⑧.
5. Remove two screws ⑨ to remove FD/HD angular bar ⑧ from FDD unit ⑩.

[Note for Assembly]

- Make sure connector A on PWB battery unit ③ is fitted in square hole B.

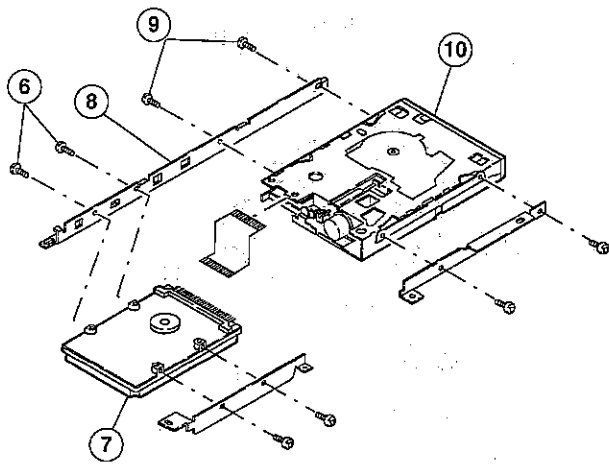


Fig. 6

(5) Replacing board and power unit

Disassembly (See Fig. 7)

1. Turn over the board unit.
2. Remove connector ① and two screws ② to remove LCD I/F FPC ③.
3. Remove screw ④ to remove 10 key board ⑤.
4. Remove screws ⑥ and ⑦ to remove main chassis C ⑧.
5. Remove six hexagon-head screws ⑨ to remove main chassis B ⑩ by using a hex wrench tool (ref. to top of this chapter).
6. Remove screw ⑪ to remove video board ⑫.
7. Remove screw ⑬ and MTB I/F cable ⑭ to remove MTB unit ⑮.
8. Remove screw ⑯ and ⑰ to remove main chassis D ⑱.
9. Remove power unit ⑲ from main board ⑳.

[Note for Assembly]

- When attaching power unit ⑲ and 10 key board ⑤ onto main board ⑳, do not press or distort the IC card socket.

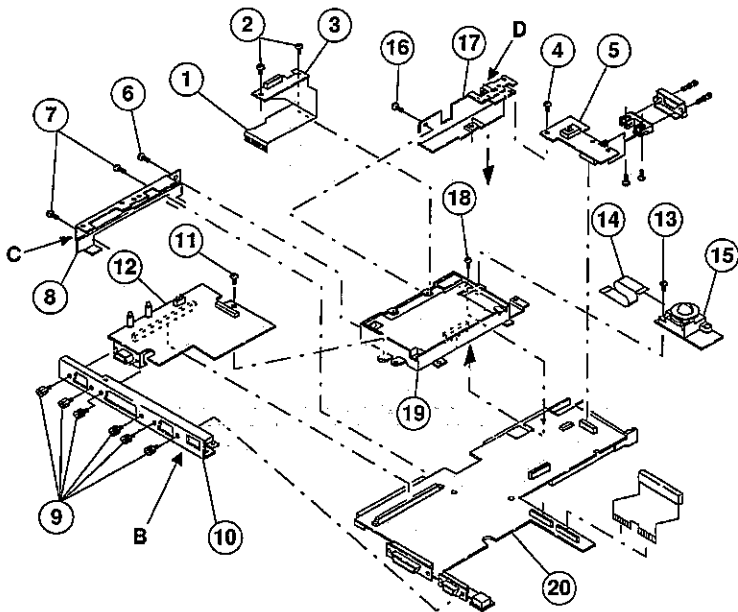


Fig. 7

(6) Display unit removal

Disassembly (Refer to Fig. 8.)

1. Remove four rubber legs ①.
2. Remove four screws ②.
3. Remove display front cabinet ③ from display rear cabinet ④.

[Note]

- When removing display front cabinet ③, remove pawl ⑬ and lift it through the square hole.

[Note for Assembly]

- When reassembling display front cabinet ③, engage pawls ①, ②, ---, and ⑬ in this sequence.

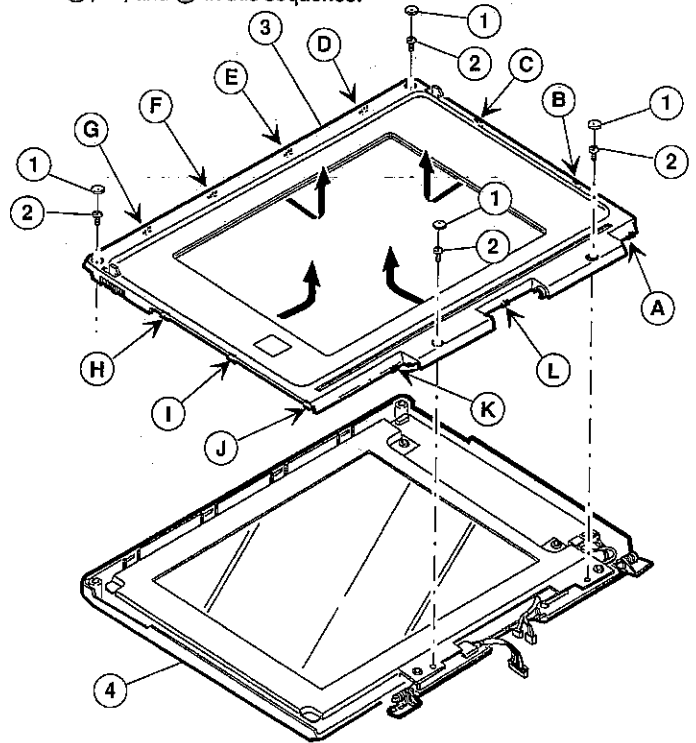


Fig. 8

(7) Inverter unit removal

Disassembly (Refer to Fig. 9.)

1. Remove two screws ①.
2. Lift inverter unit ② and pull out connectors ③, ④, ⑤, and ⑥, and remove inverter unit ② from display rear cabinet ⑦.

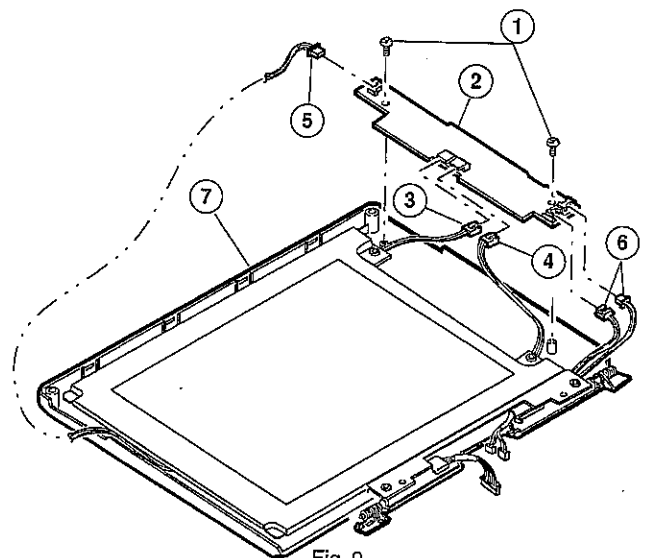


Fig. 9

(8) LCD unit removal

Disassembly (Refer to Fig. 10.)

1. Remove four screws ①.
2. Lift LCD unit ②, disconnect cables ③ and ④, and remove LCD unit ② from display rear cabinet ⑤.
3. Remove two screws ⑥, and remove dumper support angle ⑦.
4. Remove dumper L ⑧ and dumper R ⑨, then remove cable ⑩.

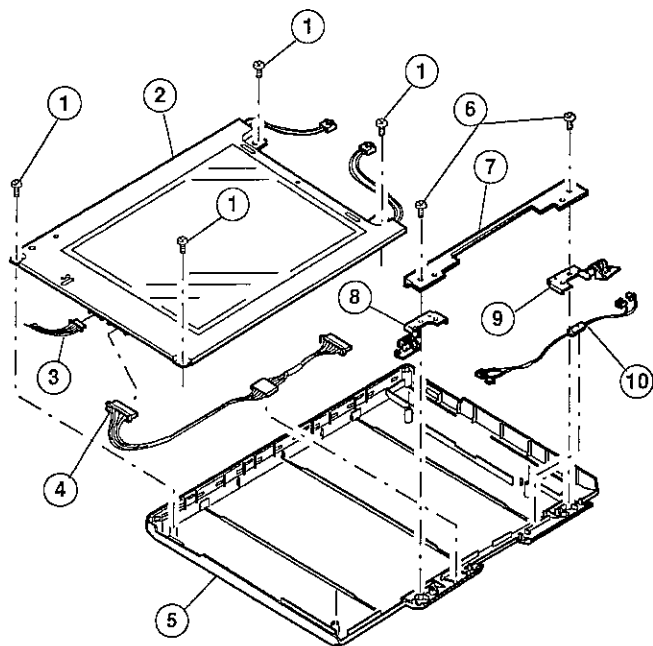


Fig. 10

[Note for Assembly]

- When connecting inverter cable ⑩ and LCD cable ④, adjust so that the tubes of the cables are at the center as shown in Fig. 11.

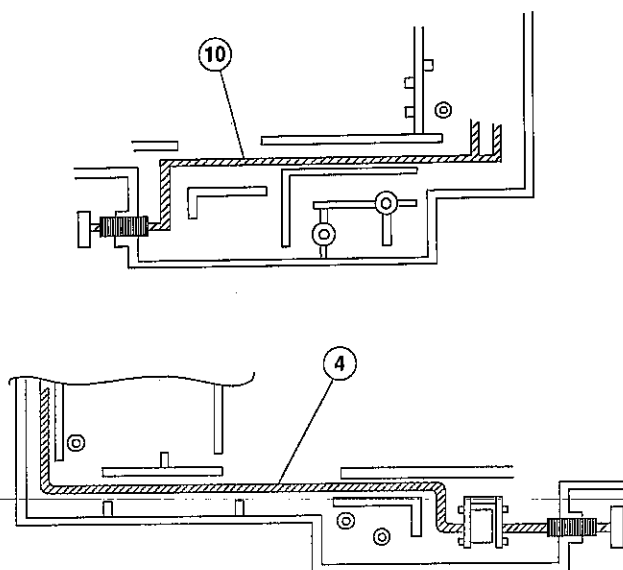


Fig. 11

CHAPTER 5. HARDWARE DESCRIPTION

1. OUTLINE

(1) System block diagram

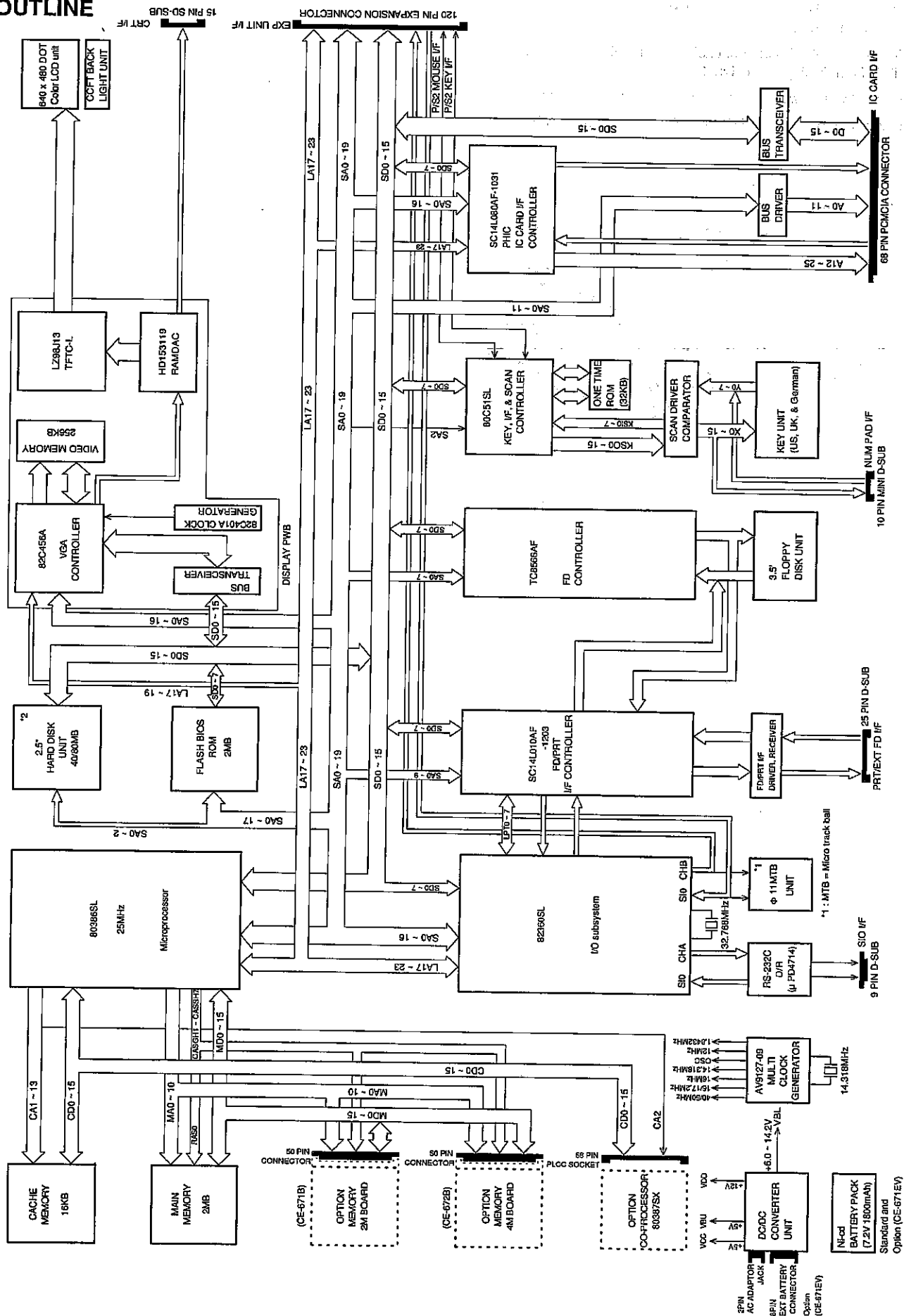


Fig. 5-1

(2) Memory map

FE0000H – FFFFFFFH	: System and Video BIOS ROM
FC0000H – FFFFFFFH	: Device Drivers, Power Management ROM
800000H – FBFFFFFFH	: Optional (undefined) *
400000H – 7FFFFFFH	: 4MB DRAM Option
200000H – 3FFFFFFH	: 2MB DRAM Option
100000H – 1FFFFFFH	: 1MB DRAM on motherboard
F0000H – FFFFFH	: System BIOS
E0000H – EFFFFH	: Video BIOS
D0000H – DFFFFH	: DRAM (can be rolled above option DRAM), FLASH window, PMaccess window
C0000H – CFFFFH	: DRAM (can be rolled above option DRAM)
B0000H – BFFFFH	: Video RAM (system DRAM used as PM RAM)
A0000H – AFFFFH	: Video RAM (system DRAM rolled)
0H – 9FFFFH	: DRAM
30000H – 3FFFFFFH	: PM RAM when in power Management Mode)

interrupt handler

* PCMCIA will likely map into this area.

(3) I/O address map

I/O address	Used device	Remark
000-01F	DMA controller 1 (Slave)	8 bit DMA
020-021	Interrupt controller 1 (Master)	
022-023	Special feature	CPU speed control
024-025	Configuration register	System control
040-043	Timer 1	
048-04B	Timer 2	
060-064	Key controller, port B	
070-07F	RTC, backup RAM, NMI, MASK	
080-08F	DMA page register	
092	Port 92	
0A0-0AF	Interrupt controller 2 (Slave)	
0C0-0DF	DMA controller 2 (Master)	16 bit DMA
0EE-0EF	Special features	
0F0-0F1	Co-processor busy clear, Reset	
0F4-0FB	Special features	
102	Printer port setting	
110-1EF	<Expansion slot>	
1F0-1F7	Hard disk controller	
200-277	<Expansion slot>	
278-27F	Printer board 2	Note 1
280-2F7	<Expansion slot>	
2F8-2FF	RS232C port 2	Note 2
370-377	Floppy disk controller (Secondary)	
378-37F	Printer port 1	Note 1
3B0-3DF	VGA & printer port 3 (3BC-3BF)	Note 2
3F0-3F7	Floppy disk controller	
3F8-3FF	RS232C port 1	Note 2

Note 1: Selectable between port 1 and port 2 by setup.

Note 2: Selectable among port 1, port 2, and port 3 by setup.

(4) Interruption map

Interruption request input	Specification device
IRQ0	System timer
IRQ1	Keyboard
IRQ2	Slave interruption controller (IRQ8 - 15)
IRQ3	RS232C port 2
IRQ4	RS232C port 1
IRQ5	Printer port 2
IRQ6	Floppy disk drive
IRQ7	Printer port 1
IRQ8	Real time clock
IRQ9	VGA V-SYNC
IRQ10	Expansion slot
IRQ11	Expansion slot
IRQ12	Expansion slot
IRQ13	Co-processor
IRQ14	Hard disk drive
IRQ15	Expansion slot
SMI	Power management

2. CLOCK GENERATOR (AV9127)

The AV9127 of AVASEM Co., Ltd. is used as the clock generator. The AV9127 is an LSI which can output several kinds of necessary frequencies simultaneously to the system circuit by oscillating one frequency of 14.31818MHz.

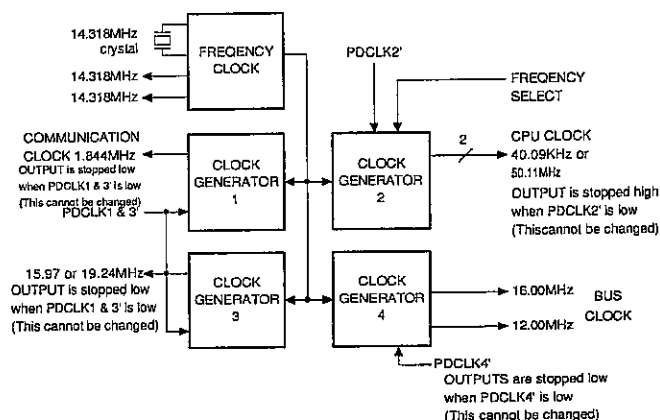


Fig. 5-2. Block diagram of AV9127-09

- Reference clock
Oscillates the basic clock of 14MHz for the clock generator. This clock is powered down when all CLK1 - 4 are powered down.
- Serial clock, floppy clock
Outputs 1.8432MHz for RS232C, and 16MHz and 19.2MHz for floppy. For the clock for floppy, the transmission rate becomes 300K only when making access to 2D diskette with 5" 2HD disk drive. 19.2MHz is outputted by switching. These two clocks are powered down simultaneously by PDCLK1&3, which becomes "0" when 360SL output SMOUT4 is "0", which shows the standby state of RS232C port, and FDC output FDCSTB is "1" which shows standby state of FDC.

PDCLK1&3	CLK3SEL	CLK1	CLK3
1	0	1.84MHz	16MHz
	1	1.84MHz	16MHz
0	X	0	0

- CPU clock

Outputs CPU operation clock of 50MHz. This clock can be switched to 40MHz. It can be powered down by the control of PDCLK2. Since local memory is refreshed even in the suspend mode, clock must be always inputted, therefore this clock is not powered down.

PDCLK2	CLK2SEL	CLK2
1	0	40MHz
	1	50MHz
0		1

- Bus clock, keyboard clock

Outputs clock of 16MHz for ISA bus and clock of 12MHz for keyboard controller 80C51SL. In the suspend mode, PDCLK4 is controlled to fix the output to "0" and to power down.

PDCLK4	CLK4-1	CLK4-2
1	16MHz	12MHz
0	0	0

Essentially, all of the components needed to build an ISA bus compatible personal computer have been combined within just two components: the 386 SL central processor and memory control system, and the 82360SL ISA peripheral and power management subsystem. The only other components needed for a complete, working PC are the main DRAM or optional static memory subsystem, optional cache SRAM and a graphics controller. In fact, the 82760SL Graphics Subsystem is fully compatible with the IBM VGA and earlier standards, and the SL SuperSet. A minimal amount of commodity Small Scale Integration (SSI) logic or Medium Scale Integration (MSI) logic buffers may also be required for design-specific interface to peripheral devices on the ISA bus.

3. 386™ SL MICROPROCESSOR SUPERSET

386 Microprocessor CPU Core with Integrated Cache Controller, Memory Controller and Bus Controller

Single-Chip ISA Peripheral System, with Power Management

Fully-Static Intel CHMOS-IV Technology

(1) Product Highlights

- **386 CPU Core**
Runs MS-DOS*, WINDOWS*, OS/2* and UNIX**
Object Code Compatible with Intel 8086, 80286 and 386 Microprocessors
- **Integrated Cache Controller and Tag RAM**
No-Glue Cache SRAM Interface
16K, 32K, or 64K-byte Cache Size
Direct, 2- or 4-way Set Associative Organization
- **Transparent Power-Management System Architecture**
Architecture extension for truly compatible systems
Transparent to operating systems and application programs
Programmable hardware supports custom power-control methods
Integrated Power Management Unit manages power-events safely
- **Programmable Memory Control**
No-Glue, Page-mode DRAM Interface
SRAM Support for lowest power
- **Complete ISA System, with Extended Support**
Full ISA Bus Control, with full 24 mA Drive
Compatible Peripherals integrated
System Interfaces, decoding and support integrated
New idea Port Interface for hardware expansion

(2) Product Description

The SL SuperSet combines an ISA compatible personal computer's microprocessor, memory controller, cache controller and peripheral subsystem into just two Very Large Scale Integration (VLSI) devices. Contained in these two components is all of the critical circuitry needed to build a range of complete ISA compatible personal computers. The product's high-integration and power conservation features reduce the size and power consumption typically associated with fully IBM compatible systems. In addition, new expandability and flexibility features offer the capability for continued innovation in battery-operated, space-constrained systems. The SL SuperSet brings 100% ISA-bus compatibility to system designs ranging from the smallest palm-top and notebook PCs, to expandable lap-top systems.

The SL SuperSet is an extremely flexible pair of components. Included in the pair are a 386 architecture central processing unit, several memory subsystem controllers, address translation and remapping logic, an optional cache memory controller, and an extensive collection of ISA-bus compatible peripheral functions.

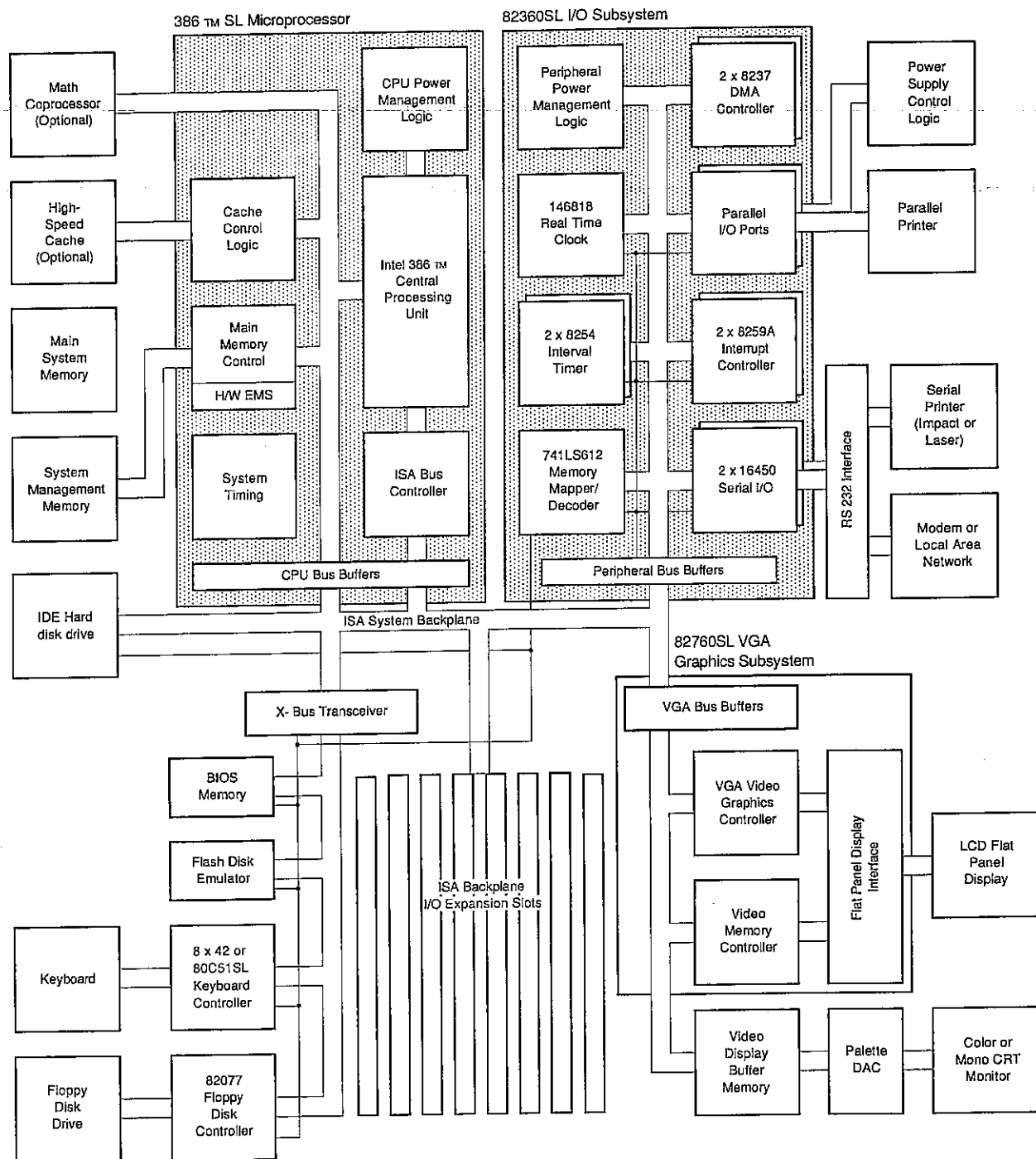


Fig 3-1. Example of SL SuperSet System

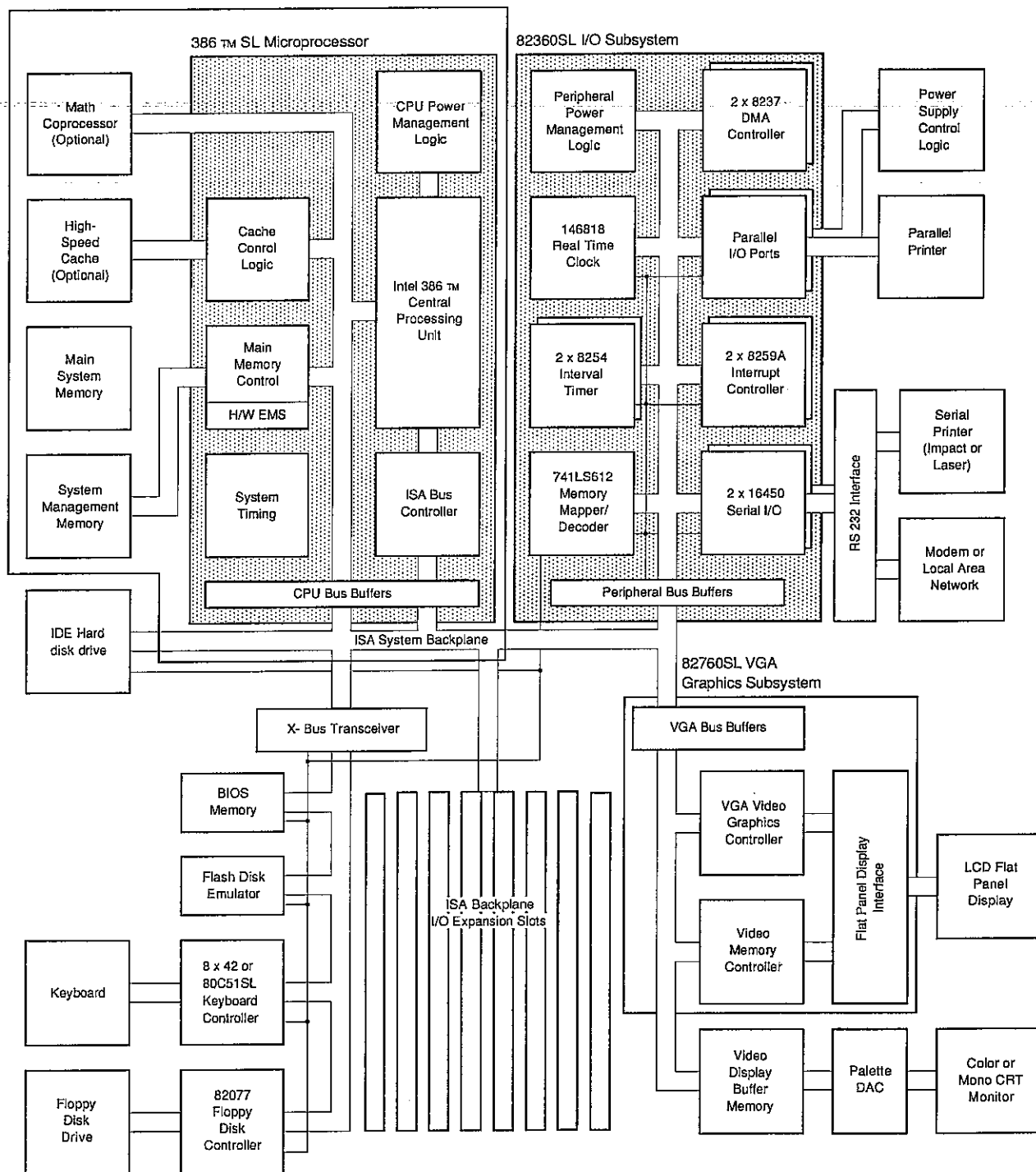


Fig 3-2. 386™ SL Microprocessor Functions

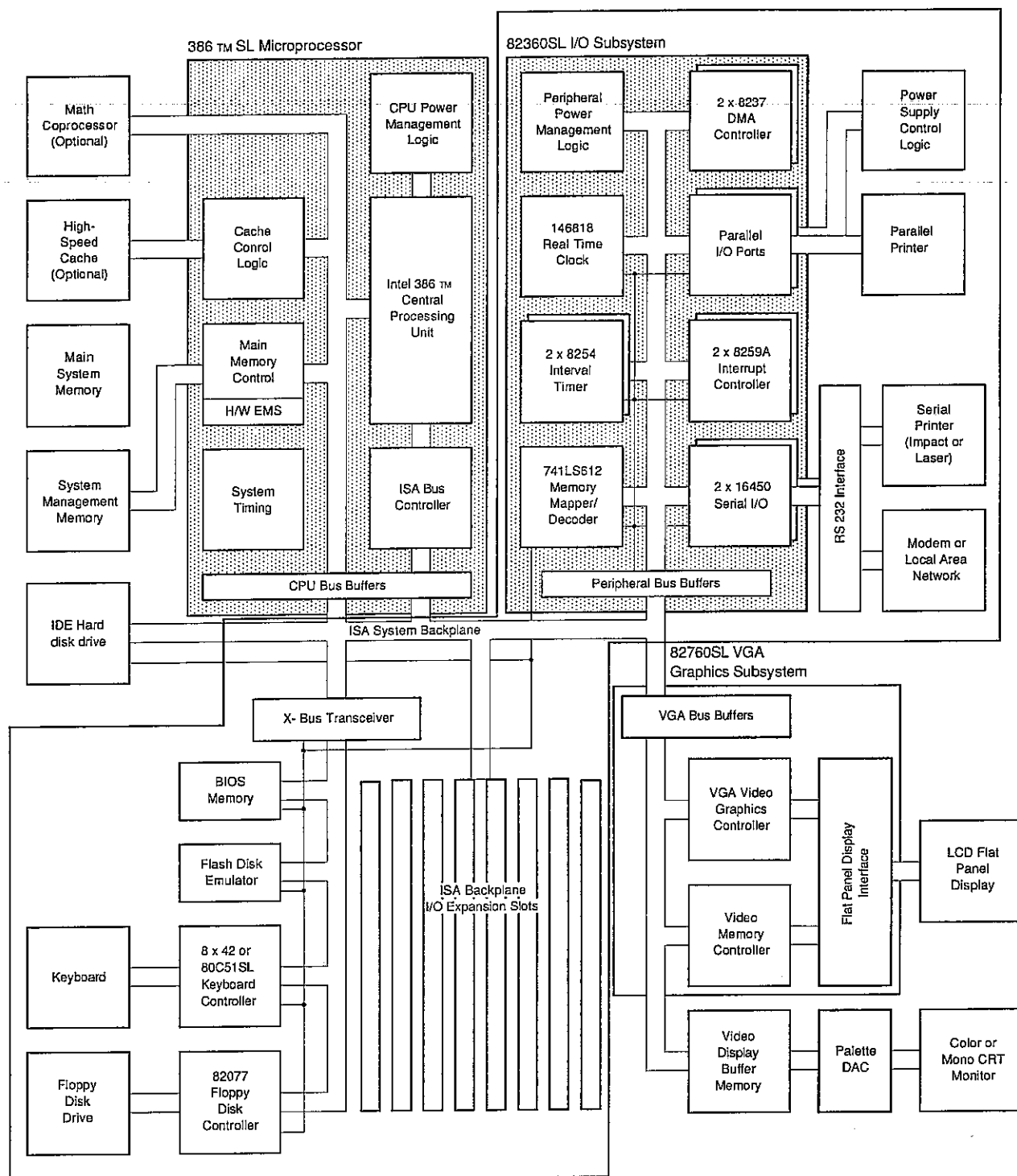


Fig 3-3. 82360SL I/O Subsystem Functions

4. MATH COPROCESSOR INTERFACE

The 386™ SL CPU includes an interface that directly supports a 387™ SX math coprocessor (MCP).

4-1 MCP INTERFACE FEATURES

The 386 SL CPU math coprocessor interface:

- Directly supports a 387 SX MCP
- Provides a programmable slow MCP clock — clock speed can be divided by 1, 2, 4, 8, or 16
- Automatically slows the MCP clock when the MCP is idle
- Supports ISA-style numeric control, including I/O ports 0F0H and 0F1H
- Automatically detects presence of 387 SX MCP

The 386 SL CPU provides a coprocessor clock output derived from the EFI clock input. When the MCP is executing numeric instructions, the MCP clock runs at the current CPU clock frequency. When the MCP is idle, the 386 SL CPU automatically divides the MCP clock by the value programmed in bits [13-11] of the CPUPWRMODE register. This saves power when the MCP is not in use. The MCP clock frequency can never be greater than the CPU clock frequency.

Two 386 SL CPU write-only registers at I/O addresses 0F0H and 0F1H support ISA-style clear BUSY and coprocessor reset functions respectively. If the 386 SL CPU ERROR# signal is activated (low), the 386 SL CPU internally holds the BUSY# signal low to prevent further coprocessor instruction execution. When the 82360 SL ERROR# signal is activated, the 82360 SL generates an INT 13 interrupt. An I/O write to port 0F0H clears the BUSY# input. An I/O write to 0F1H resets the MCP.

Upon reset, the 386 SL CPU checks for the presence of an MCP by sampling the ERROR# input. If the ERROR# input is sampled low, an MCP present is detected and the MCP interface functions as described. If the ERROR# signal is sampled high, an MCP is not detected and the MCP clock is stopped.

4-2 MCP INTERFACE SIGNALS

The 386 SL CPU MCP interface contains the following data signals and control signals:

• Data Signals

Cache Data (CD[15:0]). These signals transfer data between the 386 SL CPU and the 387 SX, and between the 386 SL CPU and cache memory.

• Control Signals

Processor Extension REQuest (PEREQ). This active high 386 SL CPU input is generated by the MCP to indicate that it has data for the 386 SL CPU to transfer.

BUSY (BUSY#). This active low 386 SL CPU input indicates that the MCP is busy executing a numeric instruction.

ERROR (ERROR#). This active low 82360 SL input indicates when a math coprocessor error has occurred. It is also used to detect the presence of a math coprocessor upon reset.

Numeric ReaDY (NPXRDY#). This active low 386 SL CPU input terminates a math coprocessor bus cycle.

Numeric Address Strobe (NPXADS#). This active low 386 SL CPU output indicates the start of a numeric data transfer cycle. This pin is floated during a Suspend operation.

Numeric Write or Read (NPXW/R#). This 386 SL CPU output indicates the type of data transfer taking place between the 386 SL CPU and the math coprocessor. This pin is floated during a Suspend operation.

Numeric RESET (NPXRESET). This active high 386 SL CPU output resets the math coprocessor. This pin is floated during a Suspend operation.

Numeric CLoCK (NPXCLK). This 386 SL CPU output drives the math coprocessor clock input. This pin is floated during a Suspend operation.

Fig. 4-1 shows the 386 SL CPU to 387 SX connections.

4-3 MCP BUS OPERATIONS

The 386 SL CPU math coprocessor interface supports both read and write MCP bus operations. Fig. 4-2 depicts a math coprocessor read cycle. Fig. 4-3 depicts a math coprocessor write cycle.

Interaction between the 386 SL CPU and the MCP can be initiated by either device. The 386 SL CPU initiates coprocessor operation during the execution of a coprocessor (ESC) instruction. This initiation occurs under program control. The coprocessor initiates interaction by activating the PEREQ signal. This signal requests that the 386 SL CPU transfer operands to or from memory.

When the 386 SL CPU executes an ESC instruction that requires the transfer of operands to or from the coprocessor, the CPU automatically sets an internal memory address base register, memory address limit register, and direction flag. The coprocessor then requests operand transfers by driving PEREQ active. These requests can occur only when BUSY# is active, indicating the coprocessor is executing an instruction.

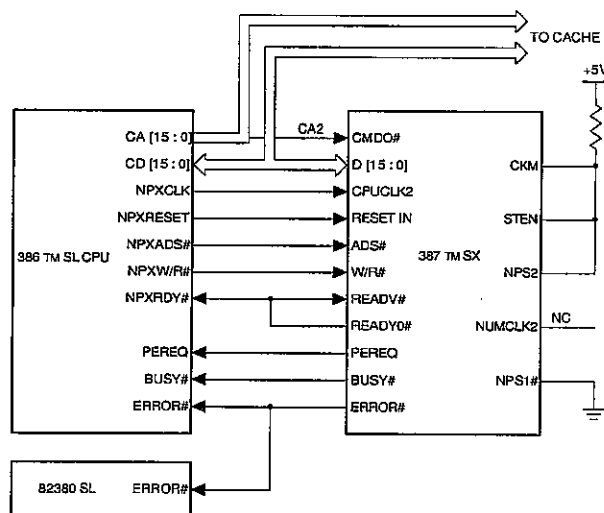


Fig 4-1. Math Coprocessor Interface

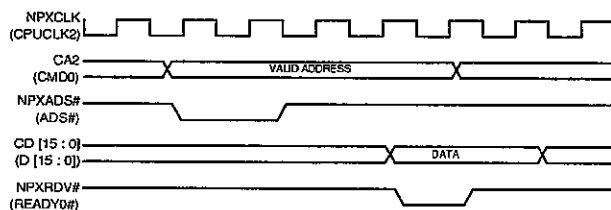


Fig 4-2. Math Coprocessor Read Cycle

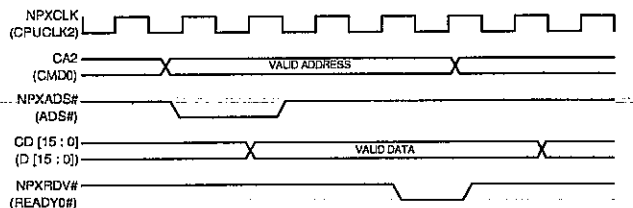


Fig 4-3. Math Coprocessor Write Cycle

Each operand transfer may require two, three, four, or five bus cycles. These cycles include one coprocessor cycle plus on of the following:

- One memory cycle for an aligned operand
- Two memory cycles for a misaligned operand
- Two or three memory cycles for misaligned 32-bit operands in 16-bit memory
- Four or five memory cycles for misaligned 64-bit operands in 16-bit memory

Data transfers for coprocessor bus cycles have the same bus priority as programmed data transfers.

5. CACHE INTERFACE

A cache is a fast and relatively small memory located between the processor and the larger main memory. An SRAM cache system makes all of the large main memory (typically DRAM) appear to respond as fast as the high-speed SRAMs in the cache respond, thereby providing the performance of SRAMs at a cost approaching that of DRAMs.

The SL SuperSet provides an on-chip cache controller unit that cost-effectively saves board space, reduces power consumption, and achieves zero-wait-state memory access speeds. The on-chip cache control unit and its interface are shown in Fig. 5-1.

5-1 SL SUPERSET CACHE CONTROL FEATURES

The SL SuperSet cache controller has the following features:

- 16-, 32- or 64-Kbyte cache sizes
 - Complete cache can be implemented with one or two SRAMs
 - No external buffers required
 - 64-Kbyte four-way set-associative cache required only two SRAMs

- Direct, two-way or four-way set-associative cache mapping options
 - Efficient Least Recently Used (LRU) cache replacement algorithms for two and four-way set associative mapping
- On-chip cache tags for fast cache hit/miss determination
 - Zero wait-state operation for most read hits
- Saves system power
 - Can reduce DRAM power consumption up to 50%
 - Cache address, data, and control signals active only when needed
- Cache coherency maintained
 - Write-through main memory updating
 - Bus snooping on DMA and master cycles
 - Affected tags flushed on EMS page change
 - User-flushable tags
 - Programmable, non-cacheable address space regions
- Programmable cache disable option

(1) DIRECT MAPPING

With direct mapping, each location in main memory can be mapped into only one cache location. The advantage of this is that when the processor makes a memory access, only one entry of the cache must be checked to determine if the desired information is stored there (a cache hit). The disadvantage is that for certain types of program behavior, accesses may alternate between memory locations that map into the same cache location, causing a sequence of cache misses and poor performance. This repeated replacement of a cache line if called "thrashing", which can be alleviated by either of the other two mapping options.

(2) TWO-WAY SET ASSOCIATIVE MAPPING

With two-way set associative mapping, each location in main memory can be mapped into either of two locations in the cache. The controller chooses one of the two locations based on a Least Recently Used (LRU) algorithm. In general, the location with the newest data is retained and its companion location is replaced. This design is less subject to thrashing than direct mapped cache, but two cache locations must be checked on every access instead of one.

(3) FOUR-WAY SET ASSOCIATIVE MAPPING

With four-way set associative mapping, each location in main memory can be mapped into any of four locations in the cache. This design is even more efficient than two-way mapping, but requires that four cache locations be checked on each access.

(4) On-Chip Tag RAM

The cache controller organizes main memory into lines and blocks. A cache line in the Intel386 SL CPU is two bytes (one word), and represents the unit of data transfer between main memory and the cache. When a word is not in the cache, the cache controller moves the needed word from main memory into the cache. A block contains 16 lines (32 bytes). A cache tag always addresses one block.

The Intel386 SL CPU has on-chip RAM capable of storing 2K tags, each containing 30 bits. Tag organization and use depend on cache size and type of mapping. A 16-Kbyte cache uses 512 tags, a 32-Kbyte cache uses 1K tags and a 64-Kbyte cache uses 2K tags. A direct mapped cache has one set of tags, a two-way set associative cache has two sets, and a four-way set associative cache has four sets.

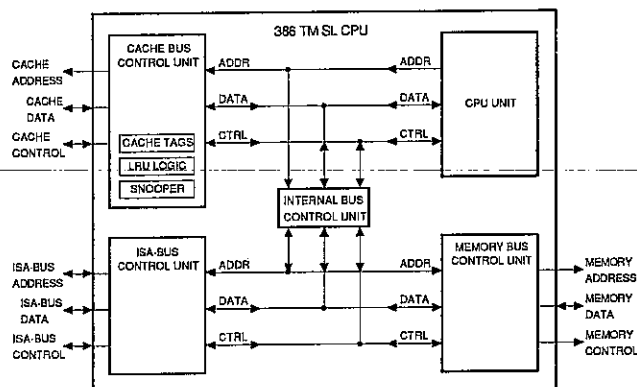


Fig 5-1. Cache Unit Block Diagram

5-2 CACHE INTERFACE SIGNALS

The SL SuperSet cache interface includes control, data, and address signals. These are listed and described below.

• Control Signals

Cache Write Enable (CWE#). This active low output indicates a write access to the cache SRAMs. This signal connects to the write enable signal of both the high and low byte cache SRAMs.

Cache Output Enable (COE#). This active low output indicates a read access to the cache SRAMs. It enables the SRAM output buffers. This signal connects to the output enable signals of both the high and low byte cache SRAMs.

Cache Chip Select High (CCSH#). This active low output enables the upper byte of the cache SRAMs. It connects to the high byte cache SRAM chip-select input.

Cache Chip Select Low (CCSL#). This active low output enables the low byte of the cache SRAMs. It connects to the lower byte cache SRAM chip-select input.

• Data

Cache Data Bus (CD[15:0]). These signals form the data bus used to transfer data between the cache SRAMs and the Intel386 SL CPU. This bus is also shared with the math coprocessor.

• Address

Cache Address Bus (CA[15:1]). These signals form the address bus used to select the memory cell in cache memory. They are driven by the Intel386 SL CPU.

5-3 CACHE BUS OPERATIONS

The SL SuperSet system has the following four types of cache bus operations, each of which is described in more detail below:

- Cache read hit cycle
- Cache read miss cycle
- Cache write hit cycle
- Cache write miss cycle

The cache controller provides all necessary cache SRAM control signals. It is also responsible for updating the cache during a read miss, 16-bit write, or 8-bit write hit. An 8-bit write hit causes a main memory update and updates the corresponding cache data byte without affecting the cache tag. 8-bit write misses are ignored by the cache controller.

The COE#, CWE#, CCSH#, and CCSL# signals are provided to enable SRAM read and write operations. Both 8-bit and 16-bit accesses are made possible by providing separate chip-select lines for high and low bytes.

A standard sequence of events for a cache access is as follows:

- The cache is enabled.
- The Intel386 SL CPU internal bus unit generates an address corresponding to a cacheable address region.
- The tag controller signals the interface controller that either a cache hit or a cache miss cycle is in progress. This signal is also recognized by the internal bus controller and a memory access cycle is initiated for a read miss or a write cycle.
- At the end of a memory access, an internal READY signal is asserted by the internal bus controller to signal termination of the present cycle.

(1) Cache Read Hit Cycle

For a cache read cycle, the cache address bus CA[15:1], COE#, CCSH# and CCSL# are asserted. When the internal cache controller returns a ready signal to the CPU core, data is latched by the Intel386 SL CPU from the cache data bus CD[15:0]. A cache read hit cycle following an idle or write cycle requires no wait states. A cache read hit cycle immediately following a read miss cycle requires one wait state. Fig. 5-2 shows cache read hit cycles following an idle cycle. Fig. 5-3 shows a cache read hit cycle following a read miss cycle.

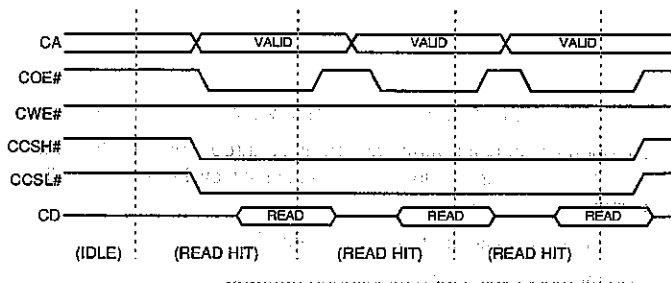
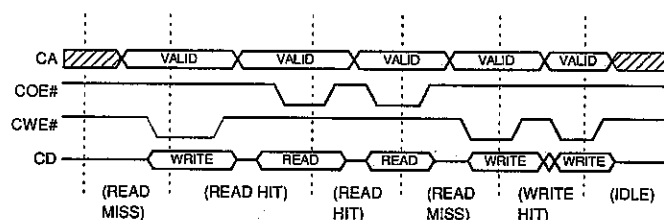


Fig 5-2. Cache Read Hit Cycles After Idle Cycle



NOTES:

1. A READ HIT AFTER A READ MISS ALWAYS GENERATES ONE WAIT STATE.
2. THE NUMBER OF WAIT STATES INSERTED IN READ MISS AND WRITE CYCLES IS CONTROLLED BY MAIN MEMORY TIMING.

Fig 5-3. Cache Read/Write Hit Cycles Following Read Miss

(2) Cache Read Miss Cycle

If a cache read miss occurs, the address to be updated is placed on the cache address bus and the CCSH# and CCSL# signals are asserted. At the same time, a local memory read access is initiated by the internal bus controller. When the local memory access is completed, the data is put on the cache data bus and held valid during a cache write cycle. The cache bus cycle is terminated when the internal READY signal from the internal bus unit is detected by the CPU core.

(3) Cache Write Cycle

The Intel386 SL CPU updates the cache on 8-bit write hit, all 16-bit write, and all read miss cycles. Because write-through is supported, local memory is also updated for all write cycles. For 8-bit write hits, the tag is unaffected and the byte is written to both the local memory and cache. 8-bit cache write misses are ignored by the cache controller. For a 16-bit write hit the cache data line is updated and the tag is unaffected. A 16-bit write miss in which the address matched but the valid bit was cleared causes the data line to be updated, and sets the tag and line valid bits. A 16-bit write miss with no address match causes the data line and tag address to be updated, sets the tag and line valid bits, and clears all other line valid bits for the block.

When a cache write occurs, address lines CA[15:1] are asserted. For an 8-bit write, either the CCSH# signal or the CCSL# signal is asserted. For a 16-bit write, both signals are asserted. Data is then put on the CD[15:0] data bus. At the same time, a local memory write cycle is initiated. Fig. 5-4 shows cache write hit/miss cycles.

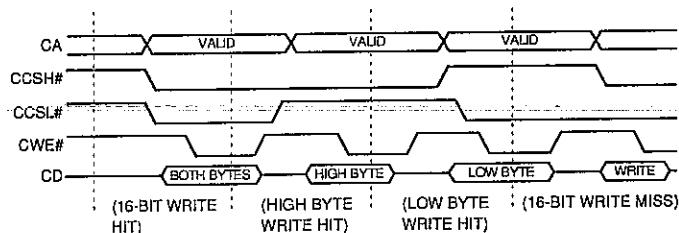


Fig 5-4. Cache Write Hit/Miss Cycles

5-4 CACHE HARDWARE OPTIONS

The cache directory, management logic, and glue logic for interfacing to external cache SRAMs are all integrated into the Intel386 SL CPU. Thus, cache subsystem design is simpler than a discrete approach. Typical SL SuperSet cache designs are straightforward and require only two 32Kx8 SRAMs for a 64-Kbyte cache system, two 8Kx8 SRAMs for a 16-Kbyte cache system, or one 16Kx16 SRAM for a 32-Kbyte cache system.

Fig. 5-5 shows a 16-Kbyte cache system.

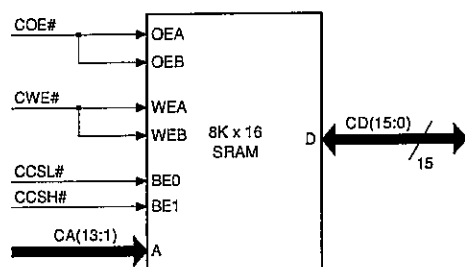


Fig 5-5. 16-Kbyte Cache Design

6. MEMORY INTERFACE

Memory in a microprocessing system is used for program and data storage. Because the majority of bus operations in a typical microprocessing system are operations to or from memory, overall system performance in a high-performance microprocessing system is linked very closely with the performance of its memory subsystems.

In an SL SuperSet system, all the logic needed to support a local memory (also called main or on-board memory) subsystem is embedded in the Intel386 SL CPU. Local memory is non-cache RAM located on the motherboard. Since external glue logic is not required, the SL SuperSet can achieve higher performance, simplify memory interface design, and save board space. Fig. 6-1 shows a block diagram of the SL SuperSet memory controller unit. This chapter describes the Intel386 SL CPU memory control features.

6-1 SL SUPERSET MEMORY CONTROLLER FEATURES

The SL SuperSet memory controller includes the following features:

- DRAM or SRAM can be used for local memory, with support for up to 32 Mbytes
- 4-, 16-, and 64-Kbyte memory access control granularity
 - Read/write, read-only, write-only, and disable control of high memory blocks
- Hardware support for LIM 4.0 EMS
 - 4 sets of EMS page registers
 - 768-Kbytes addressable memory per EMS register set
- Hardware shadowing of EPROM address space, with 4-Kbytes granularity
- Roll-over address mapping; allows use of otherwise "hidden" high memory RAM
- Memory auto-scan register; simplifies dynamic memory sizing
- "Smart hit" bus controller; saves power

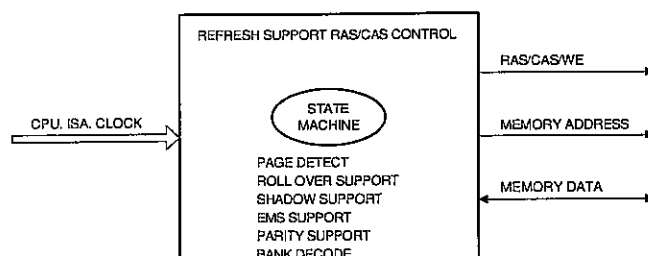


Fig 6-1 Memory Controller Functional Block Diagram

6-1-2 Memory Access Control

The memory controller has several registers that control accesses to the lower 1 Mbyte of memory. Fig. 6-2 depicts this memory access control granularity. The low memory area (0 - 640 Kbytes) can be disabled or enabled in 64-Kbyte blocks. The high memory area (640 - 1024 Kbytes) has four different memory access modes: read/write, read-only, write-only, and disable. These access modes can be set in 16-Kbyte blocks between 640 and 896 Kbytes, and in 4-Kbyte blocks between 896 and 1024 Kbytes.

Read/write is the standard access mode for local memory. Read-only and write-only modes are used for shadow RAM and are described in that section below. Memory disabling is useful for several purposes including roll-over addressing and opening a window for an external EMS mapper. When a memory block is disabled, all accesses to that memory block are directed to the ISA-bus or PI-bus.

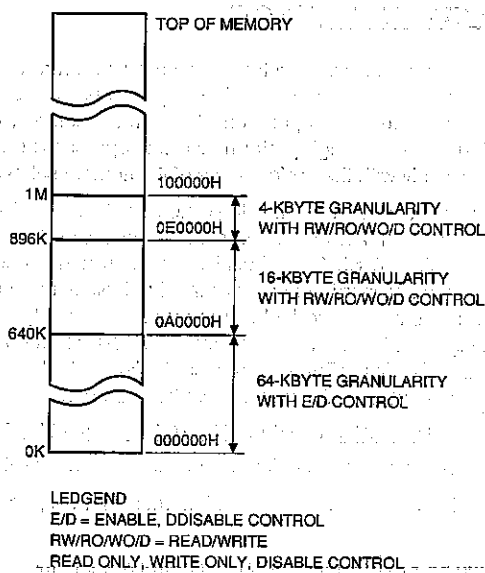


Fig 6-2. Memory Access Control Granularity

6-1-3 EMS Mapper

The EMS Mapper of the memory controller unit contains hardware support for the LIM 4.0 EMS specification. It can remap system addresses from 0 to 1 Mbyte, except 0A0000h-0BFFFFh and 0E0000h-0FFFFh which are reserved, to an EMS address from 0 to 32 Mbytes with minimal performance impact. Most EMS cycles execute with zero extra wait states.

The EMS mapping hardware provides four sets of EMS page registers. Each set allows addressing of 768 Kbytes. Either internal or external EMS support can be easily implemented during system initialization.

(1) INTERNAL EMS SUPPORT

The EMS mapper consists of an EMS Control register and four sets of 64 EMS Page registers, 16 of which are reserved. Each register represents a 16-Kbyte block of memory. Each EMS memory page can be mapped to any location in the entire 32 Mbytes of the Intel386 SL CPU memory controller address space. Physical memory should be present, however, wherever EMS addresses are mapped.

6-1-4 Shadow Memory Support

System EPROMs normally reside in the reserved memory space between 640 and 1024 Kbytes. If RAM is present at the same address range as an EPROM, the SL SuperSet allows the EPROM to be shadowed by the local memory. This means the contents of the EPROM are copied into the RAM at the same address and subsequent EPROM accesses are directed to the RAM copy.

Shadowing increases system performance for applications that access EPROM code such as the system BIOS. Shadowed BIOS code is executed at memory-controller speeds (RAM memory and CPU speeds with close to zero-wait-state performance) instead of EPROM speeds (ISA-bus speeds with wait states).

After the EPROM content is copied to local memory, the shadowed region can be set to read-only mode. This mode protects the RAM copy of the EPROM from corruption. Thereafter, all normal EPROM accesses (read cycles within the selected EPROM area) come from the shadowed RAM. All write accesses to EPROM address space are directed to the ISA-bus and effectively discarded.

6-1-5 Roll-Over Memory Support

Local memory located in the same address range as system EPROM (between 640 and 1024 Kbytes) cannot normally be used because the accesses are directed to the EPROM via the ISA-bus. The SL SuperSet allows up to six 64-Kbyte blocks to be relocated to addresses above the top of all physical memory. Accesses to these blocks are then directed to the unused RAM in the 640- to 1024-Kbyte region. This is called memory roll-over. Memory roll-over does not induce any performance degradation.

Up to six 64-Kbyte blocks of memory can be rolled. Each is disabled by the on-board memory controller unit before being rolled. Once a block of memory is rolled, it is no longer accessed at its original address range. It responds instead to an address assigned to it by the memory controller that is somewhere above the address specified by the roll-over base register.

Since the original memory block was marked as disabled, accesses to the original address range are directed to the ISA-bus unless they are in the range of an enabled EMS page.

6-1-6 Auto Memory Bank and Size Enabling

The memory controller configuration registers unit contains two registers that support memory bank/size determination and enabling. The memory Controller Auto-scan Register (MCASR) is used to place the memory controller in a test mode that allows physical on-board memory to be easily sized. The Memory controller Bank Size Register (MCBSR) stores the current bank size configuration information.

The MCASR register allows selective enabling of memory banks. After enabling a single bank of memory, memory size can easily be determined by writing to areas of it separated by the block size of memory.

6-2 LOCAL DRAM INTERFACE

The Intel386 SL CPU memory controller ensures optimal performance from DRAM main memory configurations. It provides all the signals necessary to drive up to 20 Mbytes of DRAM. The controller supports several memory configurations and memory mapping options, making system design flexible and ensuring efficient performance.

6-2-1 Local DRAM Features

When the memory controller is configured for a DRAM main memory subsystem, it supports the following features:

- 1, 2, 3, or 4 banks of DRAM with DRAM size mixing
- Page-interleaving in 2 bank DRAM subsystems
- Support for High Speed Fast Page Mode (F1), Fast Page Mode (F2), or Page Mode (P1) DRAMs
- CAS# before RAS# refresh with staggered refresh in a multiple bank configuration
- Suspend Refresh
- Programmable refresh rates for both normal and suspend refresh operations
- Parity generation and checking

(1) PAGE-INTERLEAVING FOR MULTI-BANK CONFIGURATIONS

To optimize memory subsystem performance, the memory controller uses a page-interleaving scheme for multi-banked systems. A page is a block of memory having the same row address. In this scheme, similar-sized banks are interleaved per page. Because a bank-miss cycle requires fewer wait states than a page-miss-bank-hit cycle, banks are interleaved so that bank-miss accesses are more likely to occur than page-miss-bank-hit accesses. Fig. 6-3 shows how page-mode bank interleaving is accomplished for one, two, three, and four banks of memory.

When two banks have the same DRAM size, they are interleaved on page boundaries. This means that a page-miss-bank-hit cycle only occurs when a back-to-back access is made from bank 0 page 0 to bank 0 page x (x represents any page). Thus, to cross an effective page boundary, an address jump two times greater than the page size would have to occur.

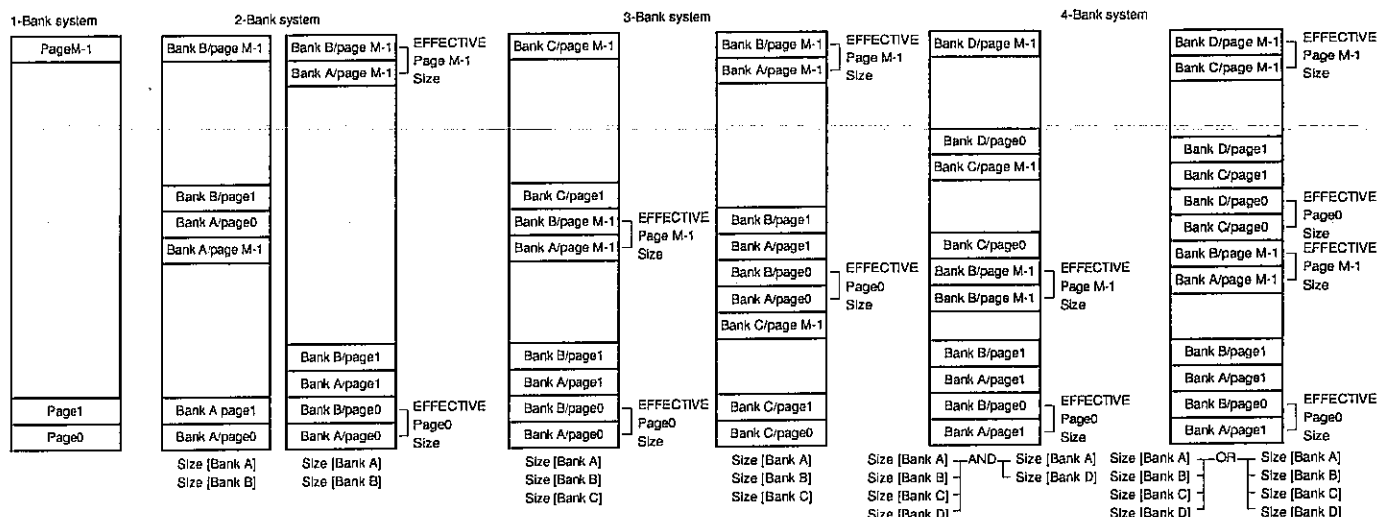


Fig 6-3. Bank Interleaving

(2) HIGH-SPEED FAST-PAGE MODE, FAST-PAGE MODE, AND PAGE-MODE DRAM SUPPORT

The SL SuperSet memory controller can be configured to drive high-speed fast-page mode DRAMs (F1), fast-page mode DRAMs (F2), or page-mode DRAMs (P1). The Memory Controller DRAM Mode register (MCDRAMMD) specifies the DRAM type. Table 6-1 shows the recommended DRAM speeds for the various DRAM types.

For most bus operations, H.S. Fast-Page Mode (F1) improves performance by reducing the number of wait states. Table 6-2 shows how High-Speed Fast-Page Mode, Fast-Page Mode, and Page Mode DRAMs affect the number of wait states for various bus cycles.

The Fast-Page Mode (F2) bus cycle is similar to the H.S. Fast Page mode DRAM bus cycle except that the first access into a page requires one wait-state.

CPU Speed	DRAM Speed
Memory Mode	
H.S. fast page mode (F1)	—
Fast page mode (F2)	80
Page mode (p1)	80

NOTE: All DRAM speed values are in nanosecond.

Table 6-1. DRAM Speed Requirement for Different DRAM Modes

Memory Mode	Bus Cycle			
	Read/Write cycle after idle cycle	Page-Miss Bank-Miss (PM-BM)	Page-Miss Bank-Hit (PM-BH)	Page Hit
H.S. Fast Page Mode (F1)	1	0	2	0
Fast Page Mode (F2)	2	1	3	0
Page Mode (P1)	2	1	3	1

Table 6-2. Wait States Inserted for Each Bus Operation for Each DRAM Mode

The Page Mode (P1) bus cycle is very similar to the Fast Page Mode DRAM bus cycle except that the CAS# timing is modified in Page Mode to support slower DRAMs. The first access into a page requires one wait-state. CAS# is activated about one EFl clock late to allow zero wait-state operation for the page-hit read cycle.

(3) POWER SAVING REFRESH OPTIONS

① CAS# Before RAS# Refresh with Staggered Refresh Type

The memory controller in DRAM mode supports CAS# before RAS# refresh. CAS# is brought active first, followed by RAS#. To prevent current surges, multiple DRAM banks are refreshed in a staggered sequential order starting with bank 0. A CAS# before RAS# refresh requires less power than a RAS# only refresh.

② Suspend Refresh

The Intel386 SL CPU supports a very low power mode called Suspend. In this mode, power can be removed from the entire system except for the Intel386 SL CPU, 82360SL, and possibly the memory subsystem. The Intel386 SL CPU maintains DRAM content with the suspend refresh mechanism. When system power is restored, the application resumes where it left off. The suspend refresh mechanism is controlled through the resumes where it left off. The suspend refresh mechanism is controlled through the On-board Memory Suspend Refresh register (OMSR) in the Internal Bus Unit configuration space.

The Memory Controller Refresh Configuration register (MCRF) specifies the refresh interval for the Normal Refresh and Suspend Refresh operations. The refresh rate can be programmed to match the ISA-bus refresh controller rate (typically, once every 15.6 microseconds) or a division of that rate by 2, 4, 8, 16, 32, or 64 support newer DRAMs with slower refresh rates.

The refresh mechanism is switched by the 82360 SL when the refresh mode is changed from normal refresh to suspend refresh.

(4) PARITY SUPPORT

The Intel386 SL CPU provides on-chip, parity-support logic for the memory controller in DRAM mode. But PC6800 does not support this feature.

6-2-2 DRAM Signal Overview

The memory interface signals for DRAM mode are:

• Control Signals

Turbo. This active high input tells Intel386 SL CPU when to enter "Turbo Mode." In Turbo Mode, the CPU executes at full speed, the default speed for the system. When this signal is forced inactive (low), the Intel386 SL CPU executes from a divide-by-two or a divide-by-four clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is high, the CPU executes from a clock defined by the Fast CPU clock field in the CPUPWRMODE register.

REFresh Request (REFREQ). This active high input from the 82360 SL indicates that the Intel386 SL CPU should execute a DRAM refresh cycle for local memory.

Parity ERROR (PERR#). This active low output tells an external device that the Intel386 SL CPU memory controller unit has detected a memory parity error.

PARity Low byte (PARL). This multiplexed pin is an extension of the lower data byte when the memory controller unit is programmed for DRAM mode. It is used by the Intel386 SL CPU to read or write the low byte DRAM parity bit.

PARity High byte (PARH). This multiplexed pin is an extension of the upper data byte when the memory controller unit is programmed for DRAM mode. It is used by the Intel386 SL CPU to read or write the high byte DRAM parity bit.

Column Address Strobe Low byte (CASL[3:0]#). These output signals qualify the column address of the lower bytes in each of the four DRAM banks.

Column Address Strobe High byte (CASH[3:0]#). These output signals qualify the column address of the upper bytes in each of the four DRAM banks.

Row Address Strobe (RAS[3:0]#). These output signals qualify the row address for each of the four DRAM banks.

Write Low Enable (WLE#). This active low output indicates that a write access to the lower byte of the Intel386 SL CPU memory bus is occurring. This output can be directly connected to the write enable input of the lower byte on the DRAM subsystem.

Write High Enable (WHE#). This active low output indicates that a write access to the upper byte of the Intel386 SL CPU memory bus is occurring. This output can be directly connected to the write enable input of the upper byte on the DRAM subsystem.

- Data

Memory Data Bus (MD[15:0]). These signals form the data bus for the memory controller unit. All accesses generated by the Memory Controller Unit transfer data between the Intel386 SL CPU and DRAM through this bus.

- Address

Multiplexed Memory Address Bus (MA[10:0]). These signals form the address bus for the Memory Controller Unit. An 18-, 20-, or 22-bit address is output in a multiplexed row/column sequence.

6-2-3 DRAM Bus Cycles

Memory read, write and refresh bus cycles of High Speed Fast-Page Mode DRAMs, Fast-Page Mode DRAMs, and Page-Mode DRAMs are discussed in the following sections.

(1) MEMORY READ CYCLES

Read cycle timing for various page/bank hit/miss combinations is shown in Fig. 6-4, 6-5, and 6-6. In a read cycle, the memory row address becomes active first, followed by RAS#, which latches the row address. With High-Speed Fast-Page Mode DRAMs,

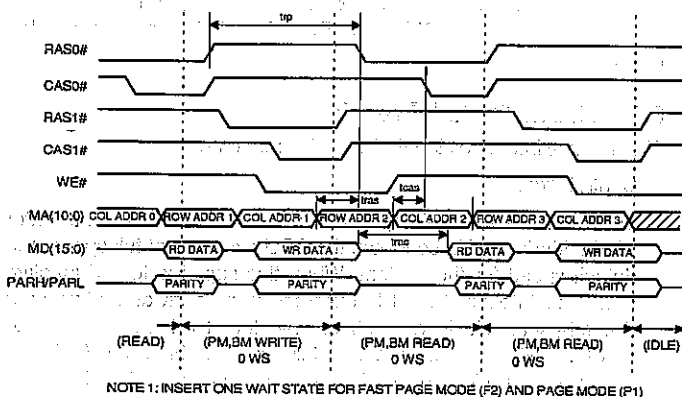


Fig 6-4. H.S. Fast Page Mode DRAM Timing
(Read, PM BM Write, PM BM Read)

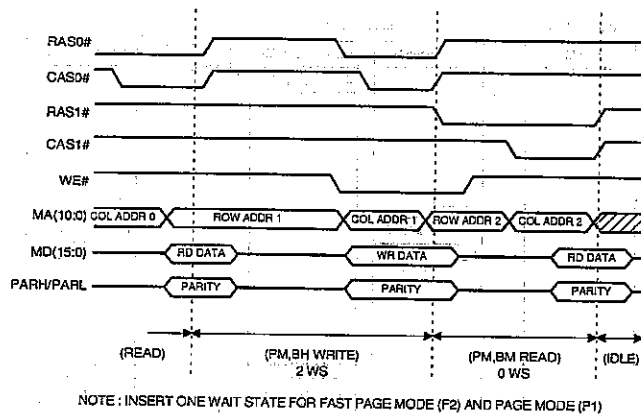


Fig 6-5. H.S. Fast Page Mode DRAM Timing
(Read, PM BH Write, PM BM Read)

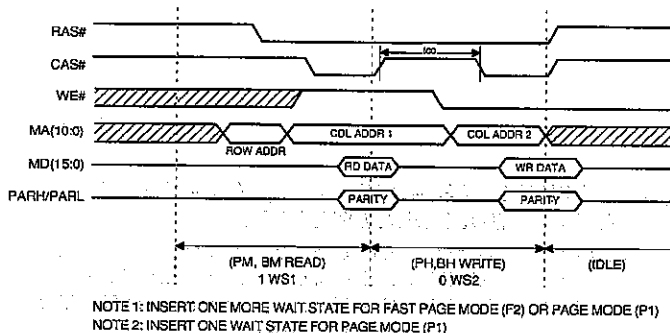


Fig 6-6. H.S. Fast Page Mode DRAM Timing (Idle, PM BM Read)

CAS# then goes active latching the column address. Valid data is output from DRAM after an access delay and is latched by the Intel386 SL CPU at the end of the read cycle.

(2) MEMORY WRITE CYCLES

Write cycle timing is very similar to that for read cycles, as depicted in Fig. 6-4, 6-5, and 6-6. WE# is activated at about the same time the column address is asserted and valid data is output by the Intel386 SL CPU.

Note that the Page-Miss-Bank-Miss cycle in Fig. 6-4 is shorter than the Page-Miss-Bank-Hit cycle in Fig. 6-5. This illustrates the advantage of bank interleaving done by the SL SuperSet memory controller. Page Mode (P1) and Fast Page Mode (F2) DRAMs require insertion of one extra wait-state for page miss cycles.

(3) REFRESH CYCLES

Refresh cycles are initiated by activation of the REFREQ signal from 82360 SL. The Intel386 SL CPU memory controller detects this signal and begins the CAS# before RAS# refresh cycle. In a multiple-bank DRAM system, CAS0# is activated for the specified period (the CAS0# setup time) before RAS0# becomes active. CAS1# then activates before RAS1# goes active. This refresh cycle pattern is repeated for all populated DRAM banks. Fig. 6-7 depicts DRAM refresh cycles using staggered refresh methods in a multiple-bank memory subsystem.

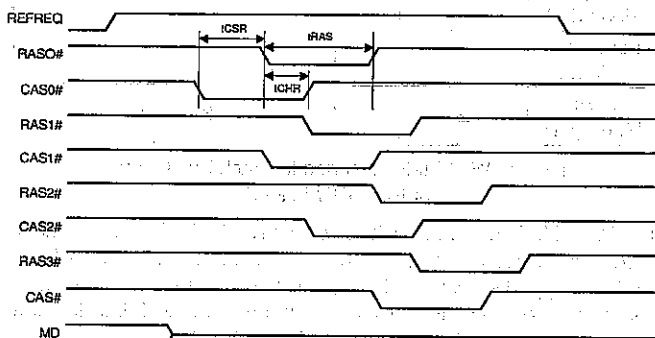


Fig 6-7. DRAM Refresh Cycles with Staggered Refresh

7. PARALLEL INTERFACE

Parallel interface is contained in the 82360SL. It is connected to printer connector through multiplexer in the ASIC. This parallel port interfaces with parallel printer and plotters.

This circuit consists of the printer data register, printer status port and printer control register.

The print data register stores to be sent to the printer. The contents of this register can be read by the CPU. The printer status port reads status information sent from the printer. The printer control register stores control codes to be sent to the printer. Bit 4 of this register determines whether the ACK# signal from the printer makes enable or disable as the CPU interrupt signal. When this bit is HIGH, interruption is disabled. The contents of this register can be read by the CPU.

This parallel port can be configured to both unidirectional mode which supports the ISA style parallel port and bi-directional mode which supports the PS/2 style parallel port.

This can be disabled or configured as LPT1:, LPT2:, or LPT3:.

(1) Base Address and Interrupt Request Levels for Different Parallel Port Modes

Mode	Parallel Port	Base Address	Interrupt Used
PS/2	LPT1:, LPT2: and LPT3:	378H, 278H, 3BCH	IRQ7
ISA	LPT2:	378H	IRQ7
ISA	LPT3:	278H	IRQ5
ISA	LPT1:	3BCH	IRQ7

(2) I/O address definition

I/O Address	Bit	Write	Read
378/	0	Print Data 0(LSB)	Print Data 0(LSB)
278/	1	1	1
3BC	2	2	2
	3	3	3
	4	4	4
	5	5	5
	6	6	6
	7	Print Data 7(MSB)	Print Data 7(MSB)

I/O Address	Bit	Write	Read
379/	0	—	1
279/	1	—	1
3BD	2	—	1
	3	—	ERROR
	4	—	SLST
	5	—	PE
	6	—	ACK
	7	—	BUSY

I/O Address	Bit	Write	Read
37A/	0	STROBE	STROBE
27A/	1	AUTOFEED	AUTOFEED
3BE	2	INITIALIZE#	INITIALIZE#
	3	SELECT	SELECT
	4	ENABLE IRQ	ENABLE IRQ
	5	—	1
	6	—	1
	7	—	1

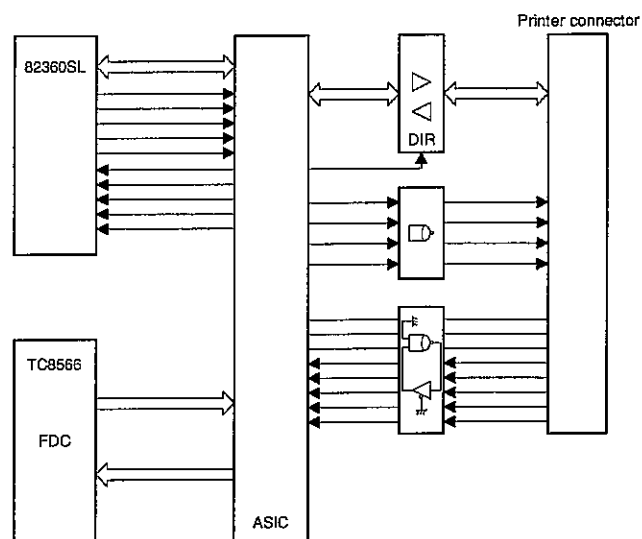
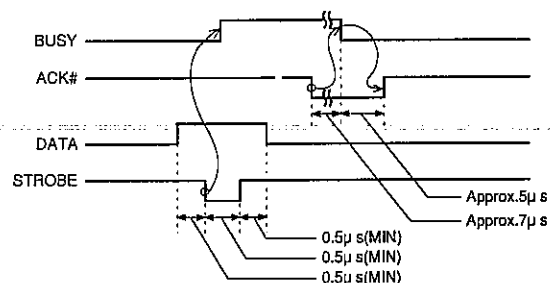


Table 7-1 lists the states of registers indicated at each I/O address, and Table 7-2 lists the bit assignment of each register.

I/O Address	A2	A1	A0	XIOR	XIOW	DLAB	
3F8	L	L	L	L	H	0	Receive buffer register
3F8	L	L	L	H	L	0	Transmit holding register
3F8	L	L	L	*	*	1	Divisor latch LSB
3F9	L	L	H	*	*	1	Divisor latch LSB
3F9	L	L	H	*	*	X	Interrupt enable register
3FA	L	H	L	L	H	X	Interrupt identification register
3FB	L	H	H	*	*	X	Line control register
3FC	H	L	L	*	*	X	Modem control register
3FD	H	L	H	*	*	X	Line status register
3FE	H	H	L	*	*	X	Modem status register

*: XIOR becomes LOW at read operation

XIOW becomes LOW at write operation

X: Not applicable.

Table 7-1 Register Status

I/O Address	Bit	Description
3F9 Interrupt enable register	0	H: Enable data
	1	H: Enable TX holding register empty interrupt
	2	H: Enable receive line status interrupt
	3	H: Enable modem status interrupt
	4-7	Always LOW
3FA Interrupt identification register	0	H: No interrupt pending
	1	Interrupt identification bit 0
	2	Interrupt identification bit 1
	3-7	Always LOW
3FB Line control register	0	Word length select bit 0
	1	Word length select bit 1
	2	Number of stop bit
	3	Parity enable
	4	Even parity select
	5	Stuck parity
	6	Set break
	7	Divisor latch access bit (DLAB)
3FC Modem control register	0	Data terminal ready (DTR)
	1	Request to send (RTS)
	2	Out 1
	3	Out 2
	4	Loopback
	5-7	Always LOW
3FD Line status register	0	Data ready (DR)
	1	Overrun error (OR)
	2	Parity error (PE)
	3	Framing error (FE)
	4	Break interrupt (BI)
	5	Transmit holding register empty (THRE)
	6	TX Shift empty (TSRE)
	7	Always LOW
3FE Modem status register	0	Delta clear to send (DCTS)
	1	Delta data set ready (DDSR)
	2	Trailing edge ring indicator (TERI)
	3	Delta data carrier detect (DDCD)
	4	Clear to send (CTS)
	5	Data set ready (DSR)
	6	Ring indicator (RI)
	7	Delta carrier detect (DCD)

Table 7-2 Register bit assignment

8. SERIAL PORT INTERFACE (RS-232C)

The 82360 SL has two internal ISA-compatible serial port controllers. These controllers give SL SuperSet the flexibility to interface with modems, serial printers, plotters, pointing devices such as a mouse, and other serial peripherals. Fig. 8-1 shows a block diagram of the 82360 SL internal serial controllers.

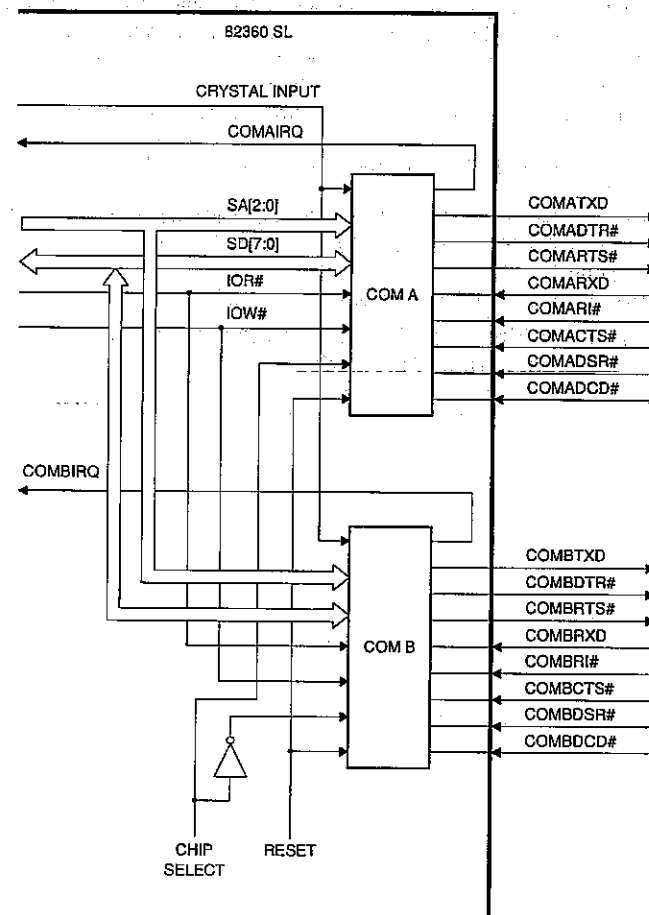


Fig 8-1. Block diagram of the 82360 SL Internal Serial Controllers

8-1 SERIAL PORT INTERFACE FEATURES

The 82360 SL serial port interface has the following features:

- Two 16450-compatible serial port controllers
- Baud rate programmable from 50-56000 bps
- One or both serial ports deselectable
- Programmable base address
- Modem connection does not require external buffering
- Internal baud rate generator works with direct crystal input
- Associated interrupt lines can be software selected

To maintain ISA-compatibility, the 82360 SL provides the functionality of two 16450 serial controllers. These support a large number of transmission rates. Table 8-1 shows the byte values to program into the Divisor Latch registers to achieve various baud rates and the percentage error associated with each.

The PS/2 architecture uses a serial controller that incorporates an internal FIFO. To support this architecture, the serial controllers in the 82360 SL can be disabled and external controllers used instead.

Table 8-1. Baud Rates Achievable Using a 1.8432-MHz Oscillator

Desired Baud Rate	Divisor Value in Registers		% Error
	DIV_LATCH_MSB	DIV_LATCH_LSB	
50	09H	00H	0
75	06H	09H	0
110	04H	17H	0.026
150	03H	00H	0
300	01H	80H	0
600	00H	C0H	0
1200	00H	60H	0
1800	00H	40H	0
2000	00H	3AH	0.690
2400	00H	30H	0
3600	00H	20H	0
4800	00H	18H	0
7200	00H	10H	0
9600	00H	0CH	0
19200	00H	06H	0
28400	00H	03H	0
56000	00H	02H	2.860

The base addresses of the serial ports can be changed to allow external serial ports to be addressed in the standard ISA serial port address space. The base address is changed by setting the base address program bits in the CFGR3 register and then loading new base addresses into the COM(A,B)BAL and COM(A,B)BAH registers. (For details on register programming consult the 386™ SL Microprocessor Programmer's Reference Manual.)

If the serial port is connected to a modem chip with TTL input levels (such as the 89C024), no external buffers are necessary. No external timer is required for baud rate generation either. A crystal or oscillator tuned to 1.8432 MHz can be directly connected to the 82360 SL.

Any two of the free ISA-bus interrupt lines can be selected for the serial port interrupts to the 386 SL CPU. This allows the standard serial port interrupts to be used by external controllers that may require them, with the SL SuperSet serial ports using non-standard interrupts. Thus, a total of four serial ports can be supported.

8-2 SERIAL PORT INTERFACE SIGNALS

The serial port control and data signals are described below.

• Control Signals

Data Carrier Detect (COMADCD#, COMBD CD#). These active low signals are inputs to the 82360 SL. Each indicates that the modem or data set detected a data carrier.

Data Terminal Ready (COMADTR#, COMBDTR#). These active low signals are outputs from the 82360 SL. Each notifies the modem or data set that the controller is ready to communicate.

Data Set Ready (COMADSR#, COMBDSR#). These active low signals are inputs to the 82360 SL. Each indicates that the modem or data set is ready to establish the communication link.

Request To Send (COMARTS#, COMBRTS#). These active low signals are outputs from the 82360 SL. Each notifies the modem or data set that the 82360 SL is ready to send data.

Clear To Send (COMACTS#, COMBCTS#). These active low signals are inputs to the 82360 SL. The modem or data set asserts this signal when it is ready to accept data for transmission. A change in the state of this signal generates a modem status interrupt.

Ring Indicator (COMARI#, COMBRI#). These active low signals are inputs to the 82360 SL. The modem or data set asserts this signal to indicate that it has detected a telephone ring. A change in the state (either from high to low or from low to high) of this signal generates a modem status interrupt. Assertion of this signal causes the 82360 SL to wake the 386 SL CPU from a Suspend state if modem ring is enabled as a wake-up event.

• Data

Serial data transmission (COMATXD, COMBTXD). These 82360 SL outputs are used for asynchronous serial data transmission. Fig. 8-2 depicts transmission of one 7-bit character with parity. Character length can be programmed to be from five to eight bits. There is always one start bit. The least significant data bit is transmitted first. The number of stop bits is programmable. If the STB bit of the Line Control register is cleared, one stop bit is added. If the STB bit is set to one, 1 1/2 stop bits are added for a 5 bit character and 2 stop bits are added for 6-, 7- and 8-bit characters. For more information about character format control, see the description of the Line Control register in the SL SuperSet Programmer's Guide.

Serial data Receive (COMARXD, COMBRXD). These inputs are used for serial data input to the 82360 SL. Character control settings are the same as for data transmission.

8-3 SERIAL PORT OPERATIONS

The 82360 SL serial controllers support full duplex serial asynchronous operation. Both controllers are identical.

The serial controller control signals execute the protocol used to ensure proper information transfer. Some of the signals are specifically designed for modem control. However, they may be used by other peripherals in a manner appropriate to the operation of the connected devices. For more details about serial controller operation, consult an MS16C450 Data Sheet.

8-3-1 SERIAL PORT DESIGN OPTIONS

The options of disabling the serial ports for PS/2 compatibility and moving the base addresses of the internal serial ports to allow use of two external serial ports were discussed in Section 8-1. Several other 82360 SL serial port interface design options are discussed in the following section.

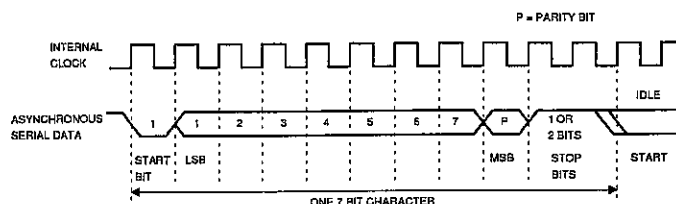


Fig 8-2. Serial Data Transmission

8-3-2 SERIAL PORT BUFFER OPTION

To buffer and to convert from the 82360 SL serial COMA port signal to the RS232C ± 12 volt signal, UPD4714 is used that combine high density and low power dissipation. It makes buffers with up to 3 drivers and 5 receivers on one chip using a 5 volt power supply.

To interface the COMB port to MTB(Micro Track Ball), no buffer is added.

The 82360 SL serial port signals are capable of directly driving TTL loads such as modem signals. However, for long distance communications, various standards such as RS232C or RS422 may be used. Each of these standards specifies different buffering requirements.

RS232C — This standard defines a ± 12 volt signal swing. TTL level signals need to be buffered and converted to this voltage level. Fig. 8-3 shows the buffering required. A number of very compact external buffer solutions are available.

Conventional 1488/1489 buffers have the advantage of easy availability and low price. The 1488 is a quad line driver and the 1489 is a quad line receiver. Both are available in 14-pin DIP configurations. This configuration has the disadvantage of requiring a +12 volt power supply. Each chip dissipates about 1/2 Watt. Use of 14C88 and 14C89 CMOS buffers instead will reduce power consumption to about 50 milliwatts per chip.

Buffers are now available that combine high density and low power dissipation. For example, Maxim makes buffers with up to 5 drivers and 5 receivers on one chip using a 5 volt power supply. In addition, some of these chips feature a low power shutdown mode consuming less than 5 microwatts. In continuous operation, the dissipation is about 1/2 Watt. Another example is the 145406, which has three drivers and three receivers in one package.

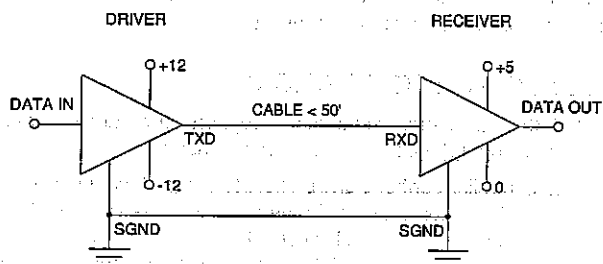


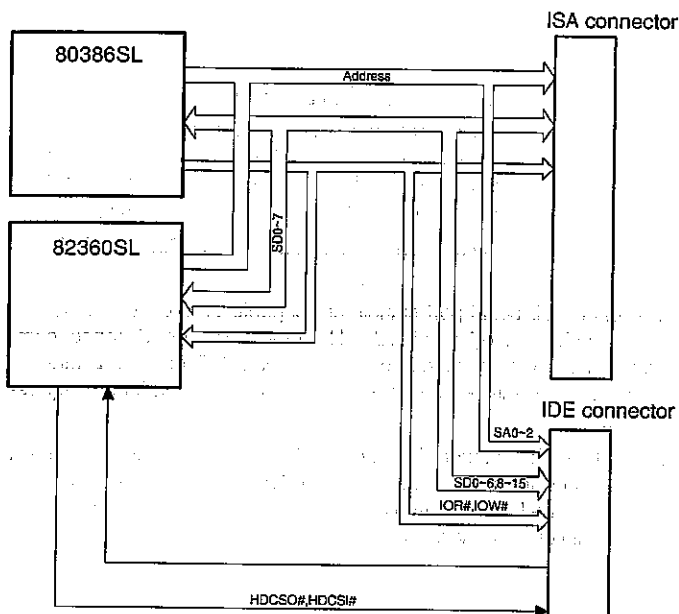
Fig 8-3. RS232C Driver/Receiver Diagram

9. 2.5" Hard Disk Interface

PC6800 supports the IDE(Integrated Device Electronics) type hard disks.

The PC AT hard disk I/O addresses (01F0H-01F7H and 03F6H-03F7H) have become the industry standard. The 82360SL internally decodes accesses to these I/O addresses and generates two hard disk chip select signals (HDCS0# and HDCS1#).

The I/O address 03F7H is shared between the hard disk and floppy disk in the PC AT architecture. An I/O read from address 03F7H returns six data bits from the hard disk and one data bit from the floppy disk. The 82360SL supports this industry standard with a separately buffered and controlled hard disk data bit (HD7) and X-bus (XD7).



10. REAL TIME CLOCK INTERFACE (RTC)

The SL SuperSet Real Time Clock (RTC) is a hardware implementation of a time-of-day clock and calendar. In addition, a small amount of CMOS RAM is provided. The purpose of this hardware is twofold:

1. Relieve the software of time keeping duties
2. Provide a method of maintaining system time, date and a small amount of system setup information in RAM, even when the computer is off.

The SL SuperSet also provides the option of connecting an external RTC to the 82360 SL.

The RTC is powered from the system supply when the system is fully on or in Suspend state, and from a small 3 to 5 volt battery when the system is powered off. As long as the battery retains its charge, the internal registers and the CMOS RAM of the RTC are nonvolatile.

10-1 RTC INTERFACE FEATURES

The SL SuperSet RTC provides the following features:

- Addressing through standard ISA index and data ports
- 256 bytes of CMOS RAM available in the internal RTC
- A PS/2-style password system can be implemented
- Controls are provided for an external RTC
- RTC alarm wakeup from Suspend capability is available

Selection of either an external or internal RTC is made by strapping the RTCEN# pin. RTCEN# is connected to ground to enable the internal RTC. RTCEN# is strapped to Vcc to enable an external RTC.

The RTC (internal or external) is accessed through ports 70H and 71H. RTC register addresses are written to the index register located at port 70H. Data is then written to the selected register (or RAM location) by writing to port 71H.

The standard ISA RTC contains 128 bytes of CMOS RAM, which can be used to store system configuration data. The 82360 SL RTC provides an extra 128 bytes of CMOS RAM. This extended RAM is accessed through ports 74H and 76H. The address of the extended RAM location is written to the 82360 SL EXTRTCIDX register through port 74. Data is then written into the selected location by writing into the EXTRTCDATA register through port 76H.

The SL SuperSet provides an optional password protection scheme. Eight bytes of the RTC RAM (38H-3FH) can contain the system password. When the 82360 SL is reset by PWRGOOD, the password security lock bit (PSS_LK; port 92H, Bit 3) is cleared. The system initialization code can then read the password and compare it with the code entered by the operator. If the correct password has been entered, the initialization code can set the security lock bit PSS_LK to one and boot the system. The password location cannot be written to or read by the system after this bit has been set.

Fig. 10-1 is a block diagram of the connections for the internal RTC. Note the use of diode isolators for the battery and supply voltage.

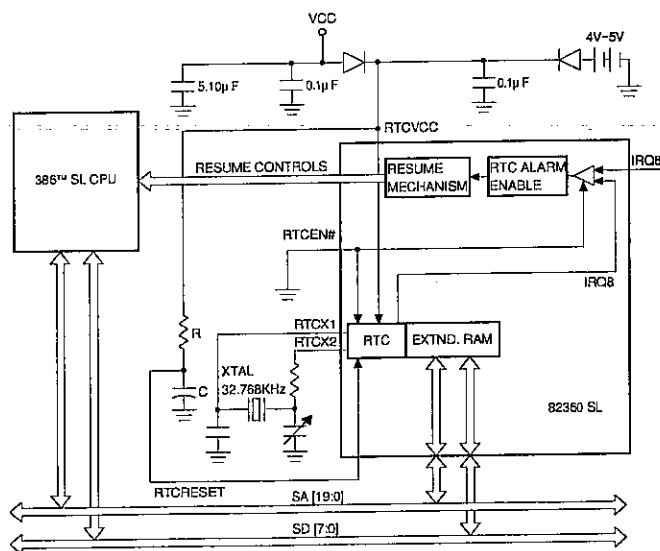


Fig 10-1. Internal RTC Block Diagram

An RTC can be programmed to provide an alarm at a certain date and time. The internal RTC alarm is hardwired to IRQ8. During a Suspend condition, an RTC alarm can be enabled to wake up the system. If this alarm is enabled, IRQ8 remains enabled during a Suspend condition, while all other IRQs are disabled. When IRQ8 is asserted, the 82360 SL deactivates the SUS_STAT# signal and normal operation is resumed. If an external RTC is used, its IRQ output should be connected to the IRQ8 pin on the 82360 SL if the RTC alarm is to wake the SL SuperSet from a Suspend condition.

10-2 RTC INTERFACE SIGNALS

The RTC signals are grouped into three categories: those affecting the internal RTC, those affecting an external RTC, and those common to both.

• Internal RTC

RTC Crystal oscillator input and output pins (RTCX1, RTCX2). The RTCX1 input and RTCX2 output should be connected to an external oscillator or crystal. This oscillator generates a timing clock for the RTC and system management state machines. The input frequency should be 32.768 KHz.

RTC input Voltage (RTCVCC). This 82360 SL input is a separate power supply for the internal RTC. It should be connected to a 3 to 5 volt battery when the system is fully off and to a 5 volt power source during active or Suspend operation.

Internal RTC RESET input (RTCRESET#). This 82360 SL input is used to reset the internal RTC after its battery has been changed.

• Common RTC Signals

• Control

Interrupt ReQuest 8 (IRQ8). This 82360 SL interrupt input is triggered by the wakeup alarm from the RTC. Either the internal or an external RTC can drive this interrupt.

RTC ENable (RTCEN#). This 82360 SL input is externally strapped low for an internal RTC or high for an external RTC.

• Data

X-bus Data (XD[7:0]). The X data bus is used to transfer both address and data to an external RTC.

10-3 RTC BUS CYCLES

The SL SuperSet uses the standard ISA method for accessing the RTC. With this method, only two of the internal registers of the RTC are externally accessible. Data written into the internal address register is latched and used as an index into RTC registers. Data subsequently written to the internal data register is written to the CMOS RAM memory location pointed to by the internal address register. This organization is shown in Fig. 10-2.

10-3-1 Internal RTC Bus Cycles

The internal RTC is accessed by initiating standard ISA 8-bit bus cycles to ports 70H and 71H. (For information about 8-bit I/O bus cycles, see Chapter 7.) The first cycle is a write directed to port 70H. The 82360 SL decodes this port address from the system address bus and directs the access to the internal RTC address register NMIRTCIDX.

The second cycle is a read or write from/to port 71H. The 82360 SL decodes this port address from the system address bus and directs the access to the internal RTC data register RTCDATA. For read cycles, the 82360 SL puts data from the memory location pointed to by NMIRTCIDX onto the system-data bus (SD[7:0]). For write cycles, the 82360 SL puts data from SD[7:0] into the RTCDATA register, thereby updating the CMOS memory location pointed to by NMIRTCIDX.

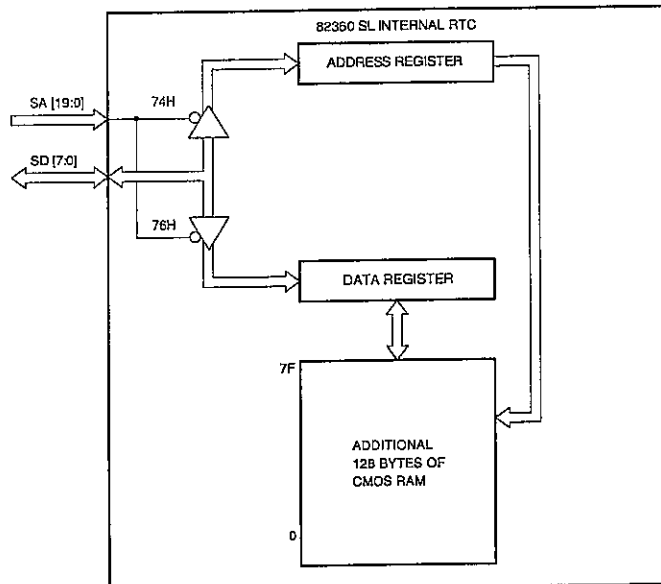


Fig 10-2. Indexed Addressing Inside the 82360 SL RTC

10-3-2 Extended CMOS RAM Accesses

The extended CMOS RAM is accessed in the same manner as the internal RTC. However, the internal address register is accessed through port 74H and the internal data register is accessed through port 76H.

11. NMI, INTR and SMI

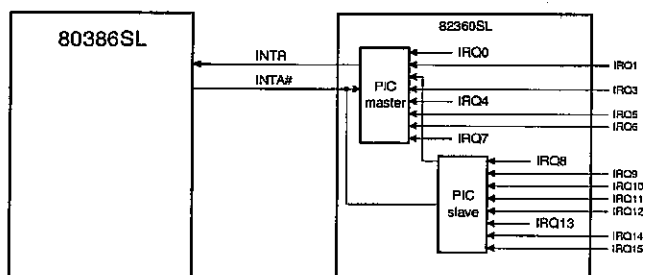
The 80386SL in PC6800 has three interrupt terminals; one is the System Management interrupt(SMI), Non-Maskable interrupt(NMI), the others is the Maskable interrupt(INTR).

The NMI terminals is used to detect a malfunction of I/O devices connected to the optional board.

The INTR signal is controlled by two PICs (PIC Master and PIC slave) connected in cascade. The INT terminal of the PIC Slave is connected to the IRQ2 terminal of the PIC Master; therefore, the PIC Master acts as a master PIC and the PIC Slave acts as a slave PIC. When the CPU is interrupted at the INTR terminal, it returns the interrupt acknowledge status. When the 386SL receives this status, it recognizes that the CPU could enter the interrupt acknowledge cycle, and the 386SL asserts the INTA signal to the master PIC in the 360SL. The PIC sends the preassigned vector address corresponding to the I/O device to the CPU via the data bus. Table 11-1 lists the assignment of the IRQ0 to IRQ15 signals.

LEVEL	FUNCTION
PIC#1 PIC#2	
IRQ0	Time output
IRQ1	Keyboard interface (output buffer full)
IRQ2	interrupt from PIC#2
IRQ3	Micro Track Ball
IRQ4	Serial Port 1
IRQ5	Parallel port 2 or ISA slot
IRQ6	Floppy Disk Controller
IRQ7	Parallel port 1
IRQ8	Realtime clock interrupt (RTC)
IRQ9	VGA chip (WD90C20, C&T82C456 or etc.)
IRQ10	ISA slot
IRQ11	ISA slot
IRQ12	ISA slot
IRQ13	NPX (Coprocesor)
IRQ14	Hard Disk
IRQ15	ISA slot

Table 11-1 Assignment of the IRQ0~15



The SMI (System Management Interrupt) allows system management routines to execute transparently to applications, the operating system, the BIOS and the mode of the processor. The system management routines can be resident in device drivers that are shipped with the system or in the system BIOS. This permits systems to utilize the SL SuperSet system management features directly with standard operating systems such as DOS, OS/2, Windows, and UNIX without requiring any modification. Only the SL SuperSet provides true software transparent system management through the SMI. The SMI is a new non-maskable interrupt that has been added as an extension to the 386 architecture. The SMI is similar to the NMI in that it is not affected by the interrupt enable bit in the 386 CPU flag register, and it does not generate interrupt acknowledge cycles.

SMI source

- Software Request
- Hardware Request
 - Auto Power Off Request
 - Battery Low Suspend Request
 - Suspend-Resume Button request
- Global Standby Request
- Local Standby Request
 - Device0 Standby Request
 - Device1 Standby Request
 - Device2 Standby Request
 - Device3 Standby Request
 - Device4 Standby Request
 - Device5 Standby Request
- Local Trap Request 2
 - Device0 Trap Request
 - Device1 Trap Request
 - Device2 Trap Request
 - Device3 Trap Request
 - Device4 Trap Request
 - Device5 Trap Request
- Software Request
- External SMI Request

12. DMA

Two DMACs in the 80360SL are utilized to provide fast, efficient transfer of data from the I/O device to memory, or memory to I/O device, without intervention by the CPU. (The CPU is held in the hold cycle while the DMA operation is performed.) The DMACs are linked in a master/slave relationship, with the master and the slave, by connecting the hold request (HOLD) terminal of the slave DMAC with the service request input (DRQ4) terminal of the master DMAC, and the hold acknowledge input (HLDA) terminal of the slave with the DMA acknowledge (DACK4#) terminal of the master DMAC. The master DMAC controls DMA channels 4 through 3. Channel 4 is used to connect the slave DMAC in cascade. The master DMAC is used to perform a word-by-word data transfer, and the slave DMAC is related to a byte-by-byte data transfer.

DMA channel assignments

- | | |
|--------|---------------------|
| Slave | 0 Option board |
| | 1 Option board |
| | 2 FDC option |
| | 3 Option board |
| Master | 4 Cascade for slave |
| | 5 Option board |
| | 6 Option board |
| | 7 Option board |

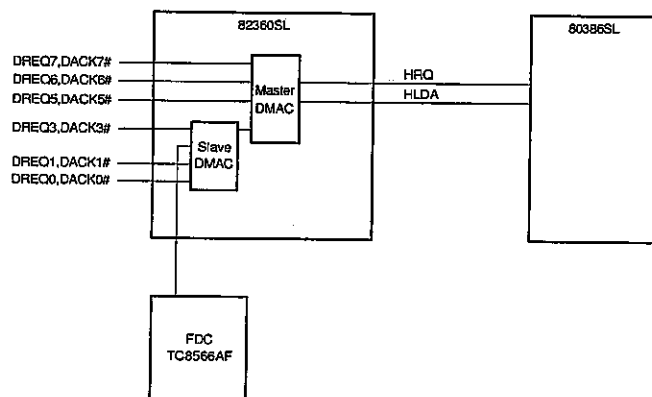


Fig. 12-1 DMA Block diagram

13. TIMER

Timer circuit has the following functional features:

- * Generates an interruption signal when the predetermined timer becomes active.
- * Determines the frequency of a signal to be sent to the buzzer. (Counter 2)

These operations are based on 1.19 MHz of clock signal which is obtained by dividing 14.31818 MHz signal. The PIT has three 16-bit counters. The timer output signal sends an interruption request to the CPU via PIC when the predetermined timer counting has been completed. Another timer output sends audio frequency signal to the speaker according to the requirements of the software. This signal is connected to the speaker drive circuit in the Sub PCB.

Command signals related to the speaker are output by writing data to the latch assigned at the I/O address 61H. Similarly, these states can be read from the buffer assigned at the I/O address 61H. Table 13-1 lists data loading and reading for each counter.

Table 13-1 Counter assignment

I/O Address	A1	A0	RD-	WR-0	
0040	L	L	L	H	Read counter No.0
0040	L	L	H	L	Load counter No.0
0041	L	H	L	H	Read counter No.1
0041	L	H	H	L	Load counter No.1
0042	H	L	L	H	Read counter No.2
0042	H	L	H	L	Load counter No.2
0043	H	H	L	H	No-operation (3-state)
0043	H	H	H	L	Write control word

14. POWER MANAGEMENT

14-1. General

The 386SL provides a powerful means of managing system operation in a manner completely transparent to the operating system and applications software. This capability is built around the following unique 386SL Features.

An SMI is a non-maskable interrupt that can be triggered in a number of user-defined ways. System management RAM stores the SMI handler code and the state of the system at the time of an SMI and allows complete restoration of the system state at the time of the interrupt. The IdeaPort consists of fourteen pins and their associated signals that can be used to control external devices in whatever manner is specified in the SMI handler. Example uses are for a power failure fail-safe mechanism, a fast on/off switch, system access control and ASIC control.

The 386SL goes beyond current power management methods achieving power savings, software compatibility and performance unattainable in other system. The 386SL includes the following power management

features:

- * Programmable automatic global standby control.
- * Programmable suspend and resume control.
 - Automatic suspend timer available.
 - Supports suspend/resume button.
 - Suspend refresh.
- * Dedicated hardware system management interrupt (SMI#) for true transparent power management.
- * Separate system management address space protects power management code and data.
 - Implicit SMI interrupt vector always jumps to SMI code.
- * Programmable clock speed control.
 - Divide CPU clock by 1, 2, 4, 8, or stop.
 - Divide math coprocessor clock by 1, 2, 3, 4, 8, and 16.
 - Divide key board clock by 2, 4, or stop.
 - 8-MHz, 4-MHz, or stop DMA clocks.
- * Programmable system management output signals can power-down devices.
 - Six independent SMOUT signals.
 - Programmable timeout control for each SMOUT signal.
- * System suspend status signal.
 - Can automatically power-down selected peripherals and system components during suspend.
- * Battery monitoring signals.

14-2. ARCHITECTURE OF THE POWER MANAGEMENT SYSTEM

Power management on the SL SuperSet is a joint effort between software and hardware. Together, they form a power management system. The power management system can be viewed as existing at two layers: the control layer and the physical layer. The interface between the two layers is provided by the system management interrupt. An example architecture of a power management system is depicted in Fig. 14-1.

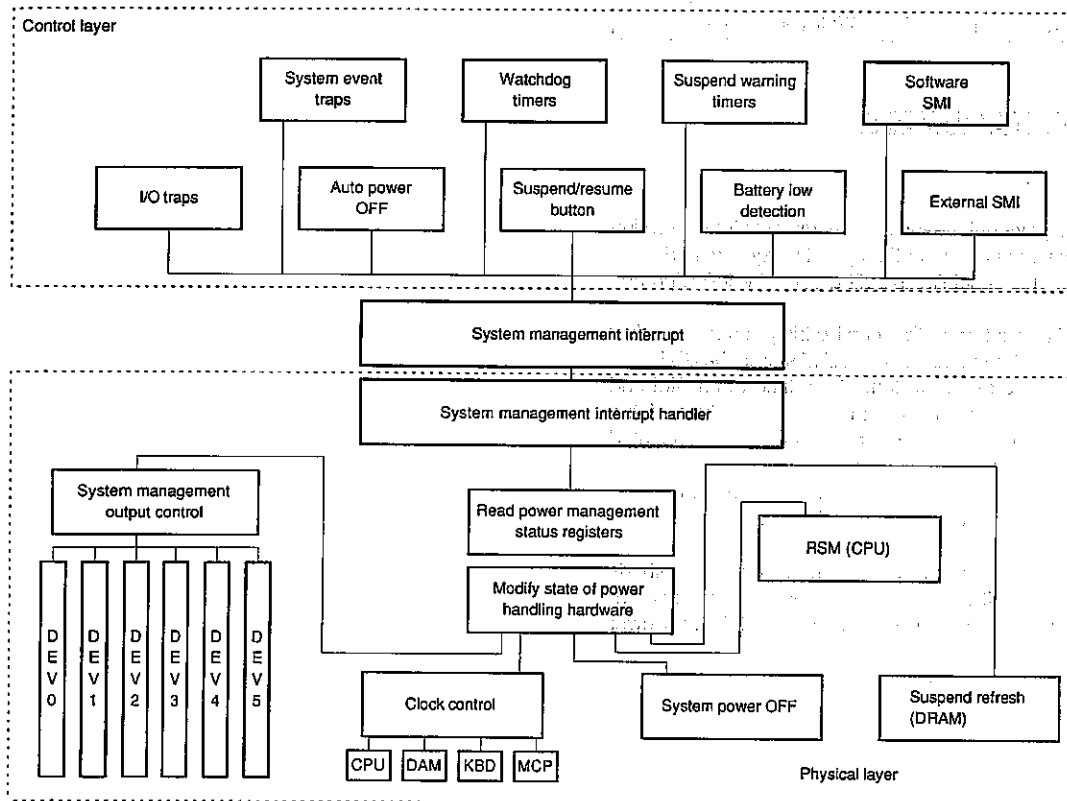


Fig. 14-1. Architecture of a Power Management System

At the top of the power management system is the control layer. Its prime function is specification of power management strategy, i.e., how the power management hardware should work. This is accomplished by enabling the desired power management features, selecting which devices to monitor, and initializing the corresponding power management timers. In addition, the control layer monitors the system activities that trigger power management functions. If action is required, a power management service request is sent to the physical layer.

The physical layer communicates directly with physical devices to execute the power management service requests generated by the control layer. Everything done in the physical layer is transparent to the application software. The SMI handler associated with the physical layer determines what caused a power management service request and directs the power management hardware in the physical layer to act accordingly.

The hardware in the physical layer includes clock control circuitry to slow down or stop the clock to a component, device power control circuitry to turn power off to devices, system power control circuitry to turn power off to the entire system, circuitry to generate slow refresh of DRAM during suspend, request status flag registers to identify the type of power management service request, and hardware support for resuming operation from the Suspend state.

15. KEYBOARD INTERFACE

15-1. General

This interface of the standard PC employs two one-chip microprocessors, one is called "Command Processor" and the other is called "Scan Processor". The 80C51SL is the processor combined these function into one-chip and it has the following feature;

- Fully compatible 8042-style host interface
- Extended Command Set
- Directly supports local 16x8 keyboard switch matrix
- Supports both scanned and serial keyboard
- Supports PS/2 style mouse
- Five high-drive LED outputs
- Optional hardware acceleration of Gate A-20

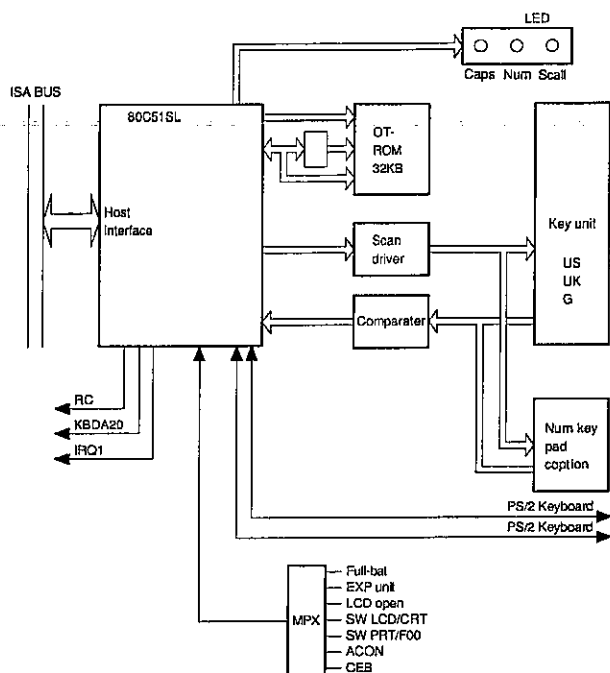


Fig. 15-1 Block diagram

IRQ1;	A one-byte data sent from the keyboard makes this terminal active, indicating that the output buffer in the keyboard interface is full. This signal is sent to the IRQ1 terminal of the PIC, requesting that the CPU reads these data.
KBDA20;	When this signal becomes LOW, the A20 signal on the address bus is forced to LOW.
RC#;	When the CPU requires a change in its operation mode from protect mode to real mode, it sends certain commands to make the terminal HIGH. The RC signal is sent to the 82360SL and the CPURESET signal is generated. Finally, the CPU is reset and thus returns to the real mode.
Full-BAT	If the external battery is not connected, when the internal battery is charged full, this signal is active. If the external battery is connected, when both internal and external battery is charged full, this signal is active.
EXPUNIT	When the expansion unit is connected, this signal is active.
LCDOPEN	When the LCD unit is open, this signal is active.
SW LCD/CRT	When sw4 of the Dip-switch is on, this signal is low and it select the CRT display only mode.
SWPRT/FDD	When sw3 of the Dip-switch is on, this signal is low and it select the external FDD interface mode
ACON	When the AC adapter is connected, this signal is active.
CEB	When the External Battery is connected, this signal is active.

15-2. 80C51SL Low-Power Keyboard Controller

The 80C51SL, based on Intel's industry-standard MCS-5 microcontroller family, is especially well suited for laptop and notebook computers with attached keyboards. The highly integrated, low-power keyboard controller incorporates a fully compatible 8042-style host interface with expanded memory, keyboard-scan and power management. The 80C51SL supports both serial and local keyboard interfaces and is available in pre-programmed versions to get to market quickly and ensure full code compatibility.

For ultimate user flexibility, the 80C51SL can be customized with additional ASIC modules or standard cells for specific application requirements.

15-2-1. Product Highlights

- Based on Intel's industry-standard 8051 architecture, incorporating AT Bus interface, keyboard scan and power management
- 2 MHz to 16 MHz clock frequency
- Fully compatible 8042-style host interface
- Supports Power-Down and Idle modes inherent to 8051
- Flexible Power Management options allow tailoring to specific application requirements
- Directly supports local 16 x 8 keyboard switch matrix
- Supports 6Kbytes on-chip masked ROM*
- External memory interface of up to 32Kbytes, including Flash, EPROM and SRAM
- Five high-drive LED outputs*
- Optional hardware acceleration of Gate A20
- Up to four high-drive outputs support two external serial interfaces*
- Plastic Quad Flat Pack (PQFP), 100-lead package*
- Easily customizable* for specific applications:
 - ✓ On-chip masked ROM, extendable to 16Kbytes
 - ✓ On-chip RAM, extendable to 256 bytes
 - ✓ Number of LED outputs may be increased
 - ✓ 8-bit Analog-to-Digital; supports up to eight channels
 - ✓ Additional serial I/O
 - ✓ Additional timers
 - ✓ General-purpose I/O ports
 - ✓ Proprietary application logic
 - ✓ Wide range of packaging options

15-2-2. Product Description

The 80C51SL is based on Intel's MCS-51 family of 8-bit microcontrollers. Through Intel's advanced CHMOS III semiconductor technology, the 80C51SL integrates AT bus interface, keyboard scan, expanded memory, and power management with a high-performance, low power 80C51 CPU core.

The enhanced integration, low power and increased performance of the 80C51SL make it ideal for PC laptop, notebook and palmtop applications. The 80C51SL is also suitable as a desktop solution for those applications requiring high performance or increased functionality.

(1) Customizable 80C51SL

through Intel's unique "Template" approach, the 80C51SL keyboard controller can be easily customized to meet specific customer or application requirements. Since the 80C51SL Template exists in silicon and in Intel's modular library, the additional effort required to achieve customization is minimal.

An 80C51SL keyboard controller variation can be executed by the customer, jointly developed or Intel-executed to suit the customer's unique requirements. Complex modules including various RAM/ROM configurations, timers, A/D, additional I/O ports or LED drivers are available in the modular library. Intel also handles customer-specific packaging requirements.

(2) Assured Compatibility

Intel's rigorous testing and validation procedures ensure full compatibility with existing 8042 interface, when implemented as a keyboard controller in a PC-based system, as well as a serial keyboard interface. Compatibility is fully validated hardware and software, for increased confidence in application-compatibility.

(3) Memory Configuration Flexibility

The 80C51SL offers customizable configurations of RAM and masked ROM, with interfaces to external memory configurations as high as 32 Kbytes. External memory options include Flash, EPROM and SRAM.

15-2-3. Block diagram

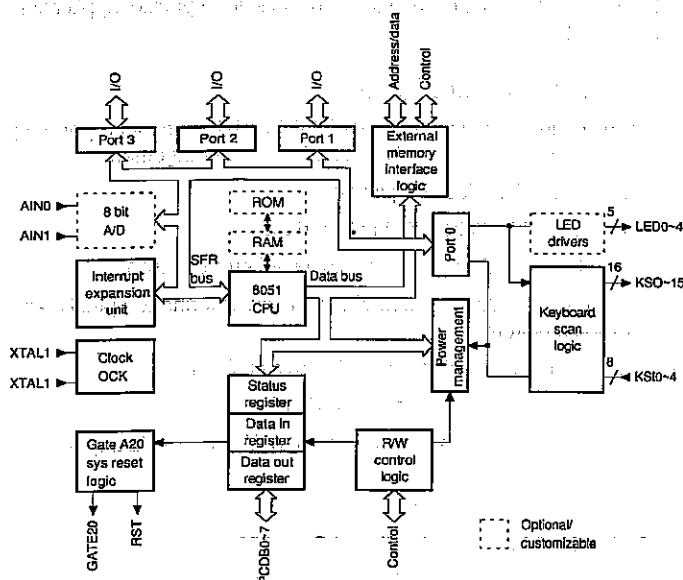


Fig. 15-2 80C51SL Internal Block Diagram

16. 3.5" FDD INTERFACE

An FDC TC8566AF is the heart of this circuit, and it interfaces between the floppy disk drive units and the CPU.

The computer was designed so that it can read data from the FDD at three different transfer rates, 250 Kbps, 300Kbps and 500 Kbps.

16-1. FDC

The FDC employs the TC8566AF device. Using a data bus, the FDC transfers status and data corresponding to the command sent from the CPU. To detect the selection by the CPU, the chip select signal and A0 signals are used.

The FDC has two important registers: a status register and a data register. The status register stores the status information of the FDC and floppy disk drives. The status register is assigned by the I/O address 3F4H and the data register is 3F5H.

(1) DOR (Digital Output Register)

This register selects drive A or B, controls the drive motors, reset FDC and defines whether to permit an interruption of the FDC or DMA request or not.

The DOR consists of 16-bit flip-flop circuits. Description for each bit are listed in Table 16-1.

I/O Address	Bit	Description
3F2	0	This bit selects the disk drive. LOW: drive A (drive1) HIGH: drive B (drive2)
	1	Low level of this bit enables the drive select signal.
	2	FDC is reset when this bit is LOW.
	3	HIGH level of this bit allows FDC interrupt and DMA request.
	4	HIGH level of this bit enables the drive motor and the drive A can be selected.
	5	HIGH level of this bit enables the drive motor and the drive B can be selected.

Table 16-1. DOR BIT DESCRIPTIONS

Data transfer between FDD and memory is executed by the DMAC and FDC. The FDC sends the DREQ signal to DMAC when data transfer to/from the FDD becomes enable. This signal delays four 2MHz clocks (2 ms) for adjustment of DREQ timing. After the delay the signal is sent to the DMAC DREQ2 line.

After passing through the tristate gate, control is done by the bit 3 of the FDD control register.

When the DMAC receives a DMA request from the FDC, it places the CPU in hold state, and then sends the DACK2 signal to the FDC after it is ANDed with bit 3 of the FDD control register to begin data transfers.

When the byte-by-byte base data transfer is completed, the FDC sends an interruption signal via the IRQ6 terminal of the PIC. In this case, if bit 3 of this register is LOW, the DMA request and interruption are disabled.

(2) DIR (Digital Input Register)

The DIR was used as an 8-bit read-only register assigned at the I/O address 3F7H; however, 7 of 8 bits are reserved for hard disk drives in actual use. The CHANGE signal selects this CNG signal. This bit is active unless a disk is present and a step pulse is received when the drive is selected.

(3) DCR (Digital Control Register)

This write-only register is assigned at the I/O address 3F7H, and it selects the VFO, and sets the condition of the FCLK and WCLK signals. Table 16-2 lists the bit assignment of this register.

Bit 1	Bit 0	Transfer Rate	FDC Clock	Write Clock	Applicable Drive	Applicable Medium
L	L	500 Kbps	8 MHz	1 MHz	2HD	2HD
L	H	300 Kbps	4.8MHz	0.6MHz	—	—
H	L	250 Kbps	4 MHz	0.5MHz	2D	2D
H	H	250 Kbps	4 MHz	0.5MHz	2D	2D

Table 16-2 DCR bit assignment

Because the data concerning the disk drive type is stored in the RAM of the RTC, the CPU reads the data before it accesses FDDs. Then the CPU writes the data to the DCR to select the VFO and to set the LOWDEN, WCLK, VFOCLK and FCLK signals.

16-2. 3.5" FDD UNIT

16-2-1. Features of product

The MD3651 (Ultra-thin type, DC +5V single power source, double side 3.5 inch microfloppy disk unit) is the 2MB/1MB microfloppy disk unit with high cost performance and high reliability of the conventional YD-700 series.

The recording media is a replaceable 3.5 inch microfloppy disk (with auto shutter).

(1) Ultra-thin

The MD3651 is ultra-thin (15.5 mm thick) and ultra-light weight (175g).

(2) Low power consumption

As low as 1.3W for standard operations, and 25mW for standby state to enable battery drive.

(3) High performance

For the disk drive system, the direct drive system of the high performance DC brushless motor is employed to provide high performance.

(4) Environment resistance

The semi-hermetically sealed construction protects the head and disk against several environment.

(5) Shock resistance

The lead screw feed mechanism where the lead teeth and the carriage are integrated into one has improved the resistance as high 80G.

16-2-2. Product specifications

Item	Mode	2M mode	1M mode	
Memory capacity	Unformatted	2 MBytes	1 MBytes	
	Formatted (Note 1)	1474.6 KBytes	737.3 KBytes	
	Track capacity	12.5 KBytes	6.25 KBytes	
Data transfer rate		500 Kbits/sec.	250 Kbits/sec.	
Memory capacity selection		Automatic medium recognition		
Access time	Traverse time	3 msec. (min)		
	Seek settling time	15 msec. (max)		
	Average seek time	94 msec.		
Disk rotation		300 rpm		
Average rotational delay		100 msec.		
Spindle motor start-up time (Note 2)		400 msec. (max)		
Track 0: Track density		17434 B.P.I.	8717 B.P.I.	
No. of tracks	One side	80		
	Double sides	160		
Track density		135 T.P.I.		
No. of heads		2		
Modulation		MFM (Note 3)		
Environmental condition	Item	Operational	Non-operational	Transportation
	Temperature	5 ~ 45°C	-22 ~ 55°C	-40 ~ 62°C
	Humidity	20 ~ 80%RH	10 ~ 90%RH	5 ~ 90%RH
	Max. wet bulb temperature (Note 4)	29°C	40°C	42°C
Vibration (5 ~ 500 Hz, excluding resonance point)		0.5 G	2 G	2 G
Impact		5 G	100 G or less (Impact time: 11 msec.)	
Power supply		+5 ±10% V, ripple: 100 mVp-p		
Power consumption		Stand-by: 25 mW (TYP)		
		Operation: 1.3 W (TYP)		
External dimension (excluding front panel)		15.5 mm (H) x 96 mm (W) x 130 mm (D)		
Weight		175g (TYP)		
Panel/Button color		Gray 165 (Color No.: 100Z-)		
Display LED		Green (lights with SELECT signal)		
Reliability	MTBF	30,000 POH		
	MTTR	30 minutes		
	Unit life	5 years		
	Soft read error	10-9 bits or less		
	Hard read error	10-12 bits or less		
	Seek error	10-6 seeks or less		
Safety standard compliance		UL, TUV, CSA (Note 5)		

Note 1: IBM compatible, 18 sectors/track (512 bytes/sector): 2 MB mode

15 sectors/track (512 bytes/sector): 1.6 MB mode

9 sectors/track (512 bytes/sector): 1 MB mode

Note 2: The spindle motor start-up time indicates the time required before the spindle motor rotation reaches 300 ±1.5% rpm when the disk is chucked.

Note 3: FM modulation is also available. The memory capacity and data transfer rate for the FM modulation, however, are half of those for the MFM modulation.

Note 4: Without condensation

Note 5: Approval requirement for CAS standards

"The whole weight of the system including the drive unit should not exceed 18 kg."

Fig. 16-3 List of performances

16-2-3. Interface signals

For interface connection, refer to Fig. 16-7.

The interface line is composed of CMOS. (However, the WRITE DATA line is TTL.)

(1) Input signals

This product has the following input lines which are valid in LOW level.

- (1) SELECT 0 ~ 1
- (2) MOTOR ON
- (3) DIRECTION IN
- (4) STEP
- (5) WRITE DATA
- (6) WRITE GATE
- (7) SIDE 1 SELECT

Fig. 16-1 Input signals

(※1) MODE SELECT is an option.

The signal voltage level is as shown below.

Invalid	HIGH level	2.0V ~ 5.25V
Valid	LOW level	0V ~ 0.8V
Input impedance		Pulled up to 5V with 5.6 KΩ

Table 16-4 Input signal voltage level

① SELECT 0 ~ 1

Max. two units of the products can be connected with daisy chain by setting the jumper chip on the print PWB. When, for example, the jumper chip of a drive is set to "SELECT0", the drive is selected by setting the SELECT 0 to LOW level.

For the drive whose jumper chip is set to "SELECT1", the drive is similarly selected by setting the SELECT 1 to LOW level.

In this manner, drive selection is made by setting the corresponding jumper chip for the drive.

② MOTOR ON

When this signal becomes LOW, the drive motor starts.

It takes max. 0.4 sec for the drive to reach read enable state after making this signal LOW.

③ DIRECTION SELECT

This signal is used to select the shift direction of the magnetic head when a step pulse is input.

HIGH level	Out direction (Outward direction of the disk)
LOW level	In direction (Inward direction of the disk)

Table 16-5 DIRECTION IN signal

Selection of direction must be completed 1 μs before the front edge of the step pulse, and must be held more than 1 μs after the rear edge of the step pulse.

④ STEP

This signal is used to move the magnetic head in the direction selected by the DIRECTION IN signal.

The operation is performed when LOW level is changed to HIGH level, that is, at the rear edge of the pulse.

When seeking, it takes 18 ms of shifting time between tracks and setting time from when the last step pulse is provided to when read/write becomes enable.

Also after completion of seeking (including after completion of track 00 signal detection when recalibration), when seeking is performed continuously, it takes 18 ms of wait time from the last step pulse.

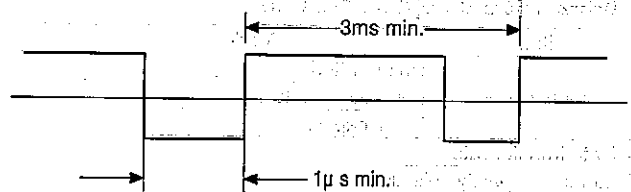


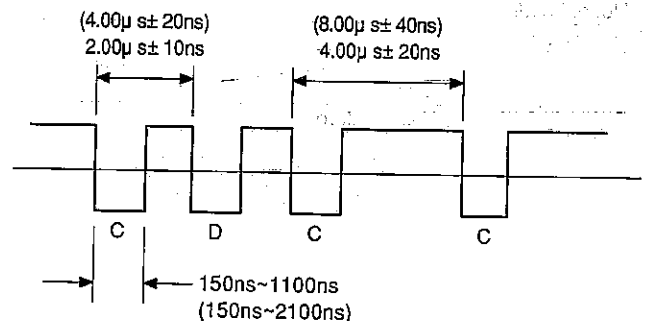
Fig. 3.5 STEP signal

⑤ WRITE DATA

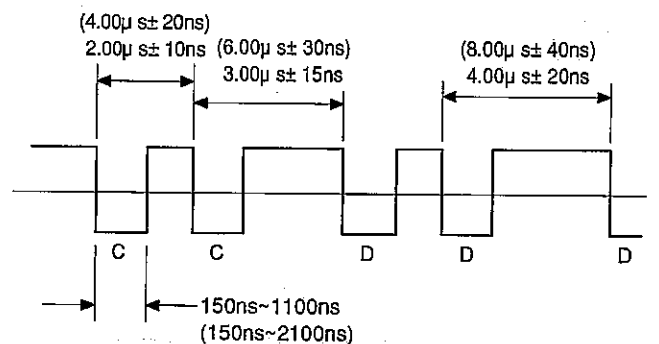
This signal is used to write data onto the disk.

The current flowing through the magnetic head is reversed every time when HIGH level is changed to LOW level and the data bits are written. Data write is performed when the WRITE GATE signal is LOW.

FM record



MFM record



Figures in () show the values in the 1MB mode.

Fig. 16-3 WRITE DATA signal

Note 1: Perform write precompensation of 125 ns for all the tracks in 2.0MB mode. For 1.0MB mode, write precompensation is not required as the conventional models.

⑥ WRITE GATE

When this signal is LOW, data write into the disk is allowed.

When this signal is HIGH, read or seek is allowed.

Since the erase head will operate for about 650 [1000]*1 μs after the WRITE GATE signal is turned off, the DRIVE SELECT signal and the MOTOR ON signal must be kept ON and SIDE 1 SELECT and STEP signals must be kept unchanged.

*1 The value in [] is that in the case of 1MB mode.

⑦ SIDE 1 SELECT

This signal is used to select the disk side for read/write.

When this signal is HIGH, the magnetic head of disk side 0 will be selected. When this signal is LOW, the magnetic head of disk side 1 will be selected.

It takes more than 100 μs from when side 0 is changed to side 1 or vice versa to when read/write operation is started.

⑧ IN USE

This signal is used to control ON/OFF of the lamps during operation.

⑨ MODE SELECT (Option)

This signal is used to select circuits in the drive according to the record density mode (2MB/1MB).

When this signal is HIGH, 2MB mode is selected. When LOW, 1MB mode.

Note: This MODE SELECT signal is optionally available. When it is LOW, the 2MB mode is selected. The reverse specification is also available.

If this signal is not optionally selected, the inserted media is identified in the FDD side and mode selection is automatically performed.

(2) Output signal

This product has the following output line.

Signals are outputted from these output lines when the DRIVE SELECT signal is LOW.

- | |
|-------------------|
| (1) TRACK 00 |
| (2) INDEX |
| (3) WRITE PROTECT |
| (4) READ DATA |
| (5) DISK CHANGE |

Fig. 16-4 Output signals

As the output line driver, a CMOS drive is used.

HIGH level	Invalid	High impedance $I_{OZ} = 20 \mu A$ (Max.)
LOW level	Valid	$0 - 0.4V$ $I_{OL} = 6 mA$

Table 16-6. Output signal level

① TRACK 00

When this signal is LOW, the magnetic head is at track 00 (the circumference track). When the magnetic head is at a track other than track 00, the signal is HIGH.

② INDEX

After starting the drive motor, one pulse of this signal is delivered for each rotation of the disk.

This signal is normally HIGH, and becomes LOW when its pulse is delivered.

When using this INDEX signal, judgment must not be made with its level but at its front edge.

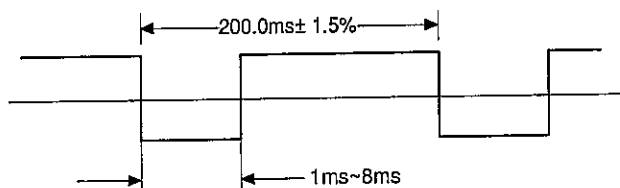


Fig. 16-5 INDEX signal

③ WRITE PROTECT

This signal shows that a disk with write protect is inserted.

When a disk with write protect is inserted, this signal becomes LOW. When a disk with write protect is used, write protect is performed in the drive.

④ READ DATA

This signal is "RAW DATA" (where the clock bits and the data bits are not separated) read by the internal circuit of the drive.

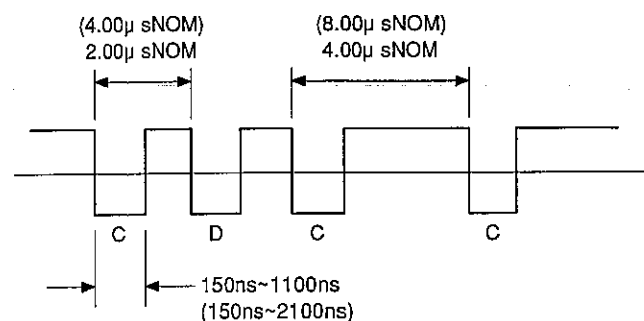
Normally HIGH, and becomes LOW when detected.

For separation of the clock bits and the data bits, use the edge when the signal changes from HIGH to LOW.

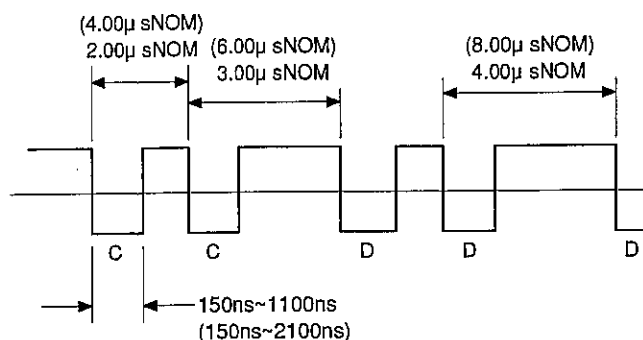
The front edge of each bit pulse is within $\pm 350 [700]^{\ast 1}$ ns from the reference position.

^{\ast 1} The figures in [] show the figures in the 1MB mode.

FM record



MFM record



Figures in () show the values in the 1MB mode.

Fig. 16-6 READ DATA

⑤ DISK CHANGE

This signal becomes LOW when the power is supplied or the disk is ejected, and becomes HIGH at the rear edge of the STEP signal when a disk is inserted.

⑥ HD (High Density) (Option)

This signal is used to identify that the disk inserted in the FDD is of 2HD (high density) or 2DD (normal density).

When a 2HD (high density) disk is inserted, this signal is LOW. When a 2DD (normal density) disk is inserted, this signal is HIGH.

* Note: This signal is optionally available and is used to select mode with the MODE SELECT signal in the host side.

16-2-4. Interface

(1) Signal interface

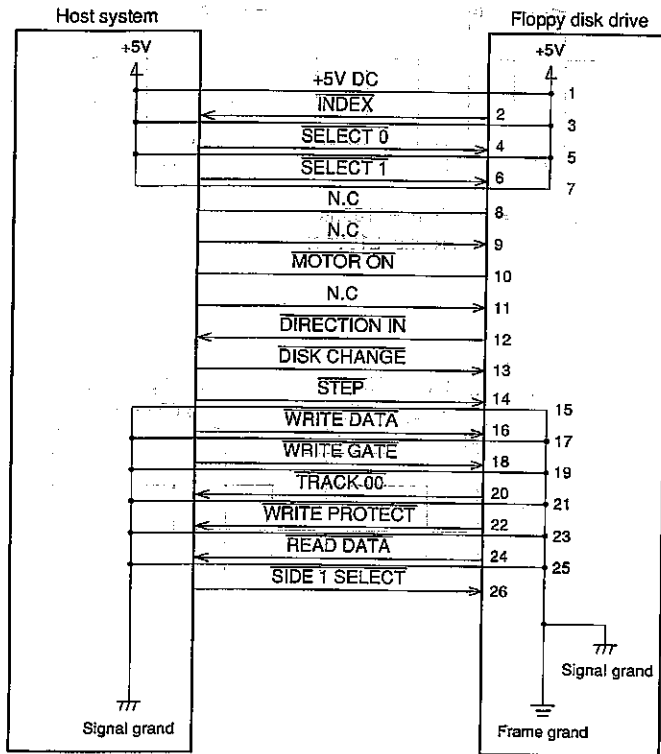


Fig. 16-7 Signal interface

(2) I/O interface circuit

① Input interface circuit

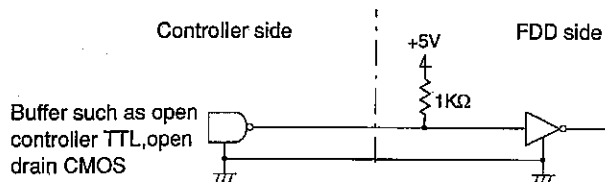


Fig. 16-8 Input interface circuit driver/receive
* Drive input condition: Terminal resistance 1 KΩ

② Output interface circuit

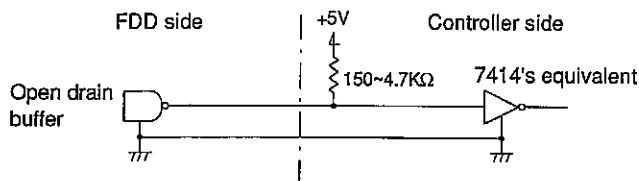
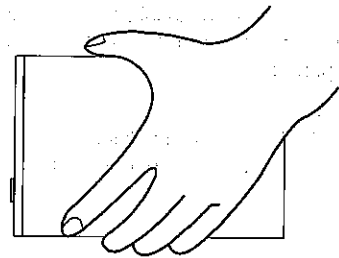


Fig. 16-9 Output interface circuit receiver/driver
* Drive output condition: $I_{OL} = 48 \text{ mA}$, $V_{OL} = 0.4 \text{ V}$

6-2-5. Precautions for handling drive

- When transporting drives, put them in their packing box.
- When handling drive, hold the area as shown in figure below.
- When insert FFC into drives, be careful not insertion a reverse side.



How to hold drive

16-2-6. Assembly and deassembly

(1) Front Bezel and Button

A. Tools used

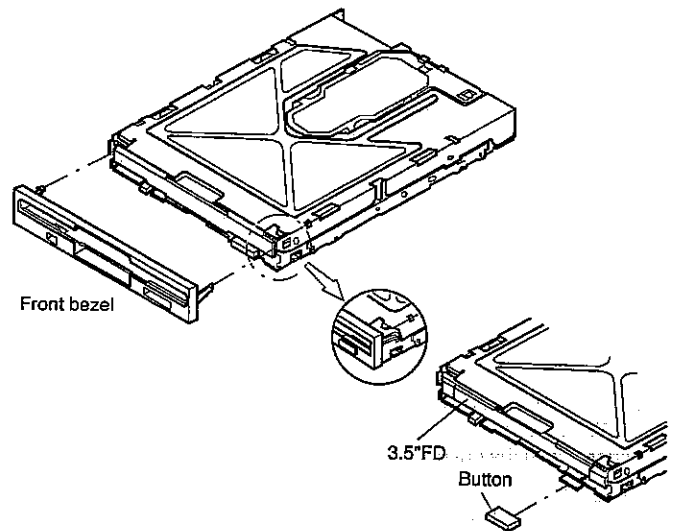
- Radio pliers

B. Removal procedures

- Remove two hooks inside the holes of both sides of base, and remove the front bezel.
- Insert the disk cassette, and you can see protruding button.
- Pull out the button using radio pliers.

C. Mounting procedures

- Insert the button.
- Hang two hooks of front bezel into the base.



(2) Shutter

A. Tools used: None

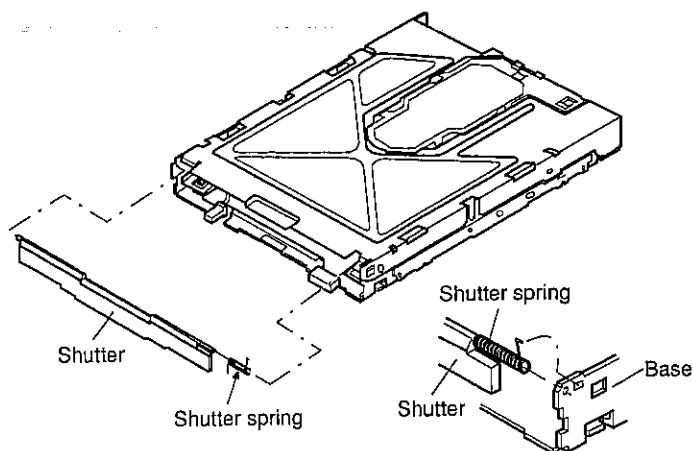
B. Removal procedures

- Remove front bezel.
- Move shutter to button side, and remove shutter and shutter spring.

Note: Be careful not lose a shutter spring.

C. Mounting procedures

1. Pass a shutter spring through the shaft of shutter, and install the shutter and shutter spring to the base.



(3) Track Position Adjustment

A. Equipment and tools used

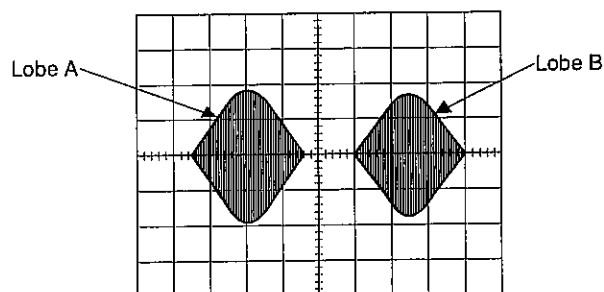
1. Exerciser
2. Oscilloscope
3. Alignment disk
4. Wave form checking fixture

B. Procedures

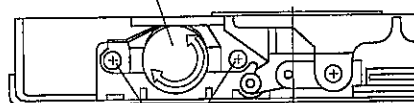
1. Connect drive to Exerciser.
2. Connect probes (1:1) of oscilloscope as shown in the following.

CH1: 500mV AC → CHK2
 CH2: 500mV AC, INVERT → CHK4
 VERT MODE: ADD
 TIME/DIV: 20 msec
 TRIGGER: EXT, NORM NEG → CHK3 (INDEX)

3. Insert an alignment disk.
4. Turn motor on and seek head to track 40.
5. Loosen the mounting screws of Step motor.
6. Turn step motor in the direction as shown by the arrow so that amplitude of two lobes (catseye pattern) are within 85% for both sides and tighten the mounting screws of step motor.



Stepping motor



Mounting screws

$$\text{Ratio of two lobes} = \frac{\text{Smaller lobe}}{\text{Larger lobe}} \times 100(\%)$$

7. Seek head in steps from track 39 to track 40, and seek head out steps from track 41 to track 40. Confirm that amplitude of two lobes are within 75% for both sides.

(4) Index Burst Position Adjustment

A. Equipment and tools used

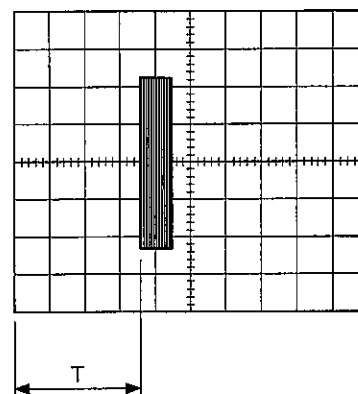
1. Exerciser
2. Oscilloscope
3. Alignment disk
4. Wave form checking fixture

B. Procedures

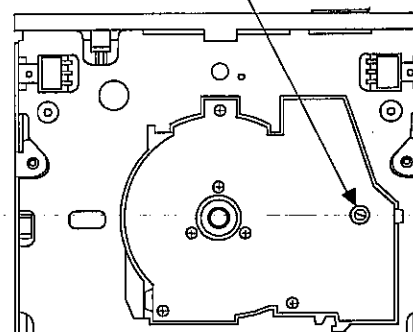
1. Connect drive to Exerciser.
2. Connect probes (1:1) of oscilloscope as shown in the following.

CH1: 0.1V AC → CHK2
 CH2: 0.1V AC, INVERT → CHK4
 VERT MODE: ADD
 TIME/DIV: 50 usec.
 TRIGGER: EXT, NORM NEG → CHK3 (INDEX)

3. Insert an alignment disk.
4. Turn motor on and seek head to track 40.
5. Confirm the time between sweep starting point and burst starting point (indicated by "T" in Fig. 1) is within check-range as shown in table below.
 If it is outside the range, adjust the index burst adjustment volume, so that "T" is within adjust-range as shown in table below.



Index burst adjustment volume



Index Burst Position

	Adjust-range	Check-range
2MB/1MB mode	400±150 usec	400±400 usec
1.6 MB mode	320±100 usec	320±200 usec

(5) Azimuth confirmation**A. Equipment and tools used**

1. Exerciser
2. Oscilloscope
3. Alignment disk
4. Wave-form checking fixture

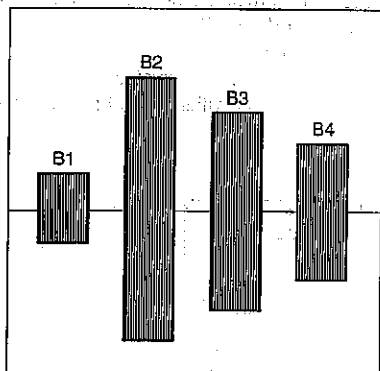
B. Procedures

1. Connect drive to Exerciser.
2. Connect probes (1:1) of oscilloscope as shown in the following.

CH1: 0.1V AC → CHK2
 CH2: 0.1V AC, INVERT → CHK4
 VERT MODE: ADD
 TIME/DIV: 0.4 msec
 TRIGGER: EXT, NORM NEG → CHEK3 (INDEX)

3. Insert an alignment disk.
4. Turn motor on and seek head to track 40.
5. Compare the burst of B1 and B4, and calculate burst ratio by using following formula (1) and (2).

Formula to calculate burst ratio



- (1) In case of $B1 > B4$; Burst ratio = $B1/B2$
- (2) In case of $B1 < B4$; Burst ratio = $B4/B3$

6. Confirm the burst ratio is as follows for both sides.

Side 0: Less than 1.177
 Side 1: Less than 1.199

17. Memory and I/O Card Interface

17-1. Introduction

The PC Host Interface controller (PHIC) provides the capability to connect PCMCIA compatible memory or I/O PC cards to an 8- or 16-bit system bus. The PC Host Interface Controller:

(1) Supports

- Memory or I/O Cards slot independent
- ISA bus compatible with hooks for 386SL
- 386SL power management
- ISA, EISA system bus
- 8-bit processors

(2) Provides

- Memory paging
- Address mapping for attribute memory
- Address mapping for common memory
- Address mapping for I/O space

- Independent data path size for I/O, common memory, attribute memory
- Interface status
 - Interface identity and revision code
 - Card insert detection
 - Memory write protect
 - Battery voltage detection
 - Ready/Bus detection
 - PC card power status
- Interface configuration
 - PC card type (Memory or I/O) selection
 - PC card power control
 - PC card software reset
 - Selection of VPP or VCC source for VPP1 and VPP2 voltages
 - Software common memory write protect
 - Software CIS memory write protect
 - Interrupt steering
- Card status change,
- Card status change interrupt configuration

17-2. PC Card Memory Addressing

Memory on the PCMCIA card is accessed using one or more memory address windows for the 16 Mbyte ISA bus. These memory windows map into the 64 Mbyte PC Card memory address space. The PC card memory address is generated either using an offset from the ISA address or high order address replacement from the pager or a block pointer. A total of 4 memory windows are provided by the PHIC. Two copies of 2 window types are supported each having independent control of window enable, common memory or attribute memory mapping, memory data bus width, ISA bus wait states, and software write protect.

Two TYPE A windows are MASK & MATCH windows which provide PC card access for windows of 4 Kbytes to 512 Kbytes within the first 1 megabyte of ISA address space. PC Card address mapping for the TYPE A window causes the upper address bits of the ISA address to be replaced with the value of the BLOCK registers. An alternative mapping is available by attaching the LIM pager to a window of 16 Kbytes, 32 Kbytes or 64 Kbytes.

The TYPE B window provides a FIRST & LAST address defining a range of addresses which can start and stop on any 64 Kbyte boundary across the full 16 Mbyte ISA address space. PCMCIA address mapping for the TYPE B window uses an OFFSET from the ISA address. This pager may also be attached to either of the TYPE B memory windows using a 64 Kbyte size window.

The PC Card pager provides for up to 4 contiguous 16 Kbyte ISA pages mapped to any set of 4 pages on the PCMCIA card. Only one pager is present in the PHIC and can only be attached to one of the four ISA windows at a given time.

Fig. 17-1 shows an example mapping for both one TYPE A & one TYPE B ISA window to PCMCIA memory address space. Figure 2 shows the pager attached to one of the TYPE B windows to access the PCMCIA memory.

The PHIC does not allow mapping of an ISA memory window in the first 64 Kbytes. Only I/O address windows are allowed to be mapped in the first 64 Kbytes of ISA address space. This resolves any conflict that might arise from using both I/O and memory addresses to access the same PCMCIA card. If an ISA memory window is set up within the first 64 Kbytes of ISA memory address space, any accesses to this window will not select the PC memory card (A23: A16 = 00h disables the ISA memory window).

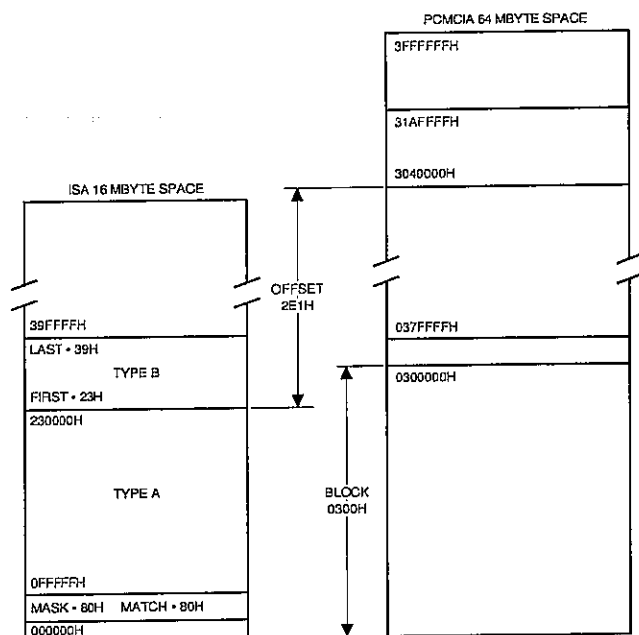


Fig. 17-1 Memory window mapping example for both TYPE A & TYPE B

Memory on the PCMCIA card is selected when the following conditions are satisfied:

1. The ISA memory address mapping window is enabled;
2. the ISA address window conditions are satisfied:
 - a. TYPE A - MASK selected address bits are found to be equal to the MASK selected MATCH bits.
 - b. TYPE B - when the ISA address is greater than or equal to the value in the FIRST register and the address is less than or equal to the value in the LAST register.

The ISA memory address mapping windows allow for the placement of multiple ROM executable images on a single PC card. These images would be aligned on the PCMCIA memory to match the boundary condition of the window used to select the memory, typically any 64 Kbyte boundary. Access to these ROM executable images is achieved by setting the size of an ISA memory address mapping window to the size of the executable image (minimum 64 Kbyte block), and setting the PC card memory offset from the ISA memory FIRST address to generate the address of the first byte of the executable image on the PC card.

The PC card memory OFFSET allows for either positive and negative (2's complement) values from the ISA (ISA) address. The PHIC does no checking for a window whose size and offset allow it to wrap from the last PC card address to the first PC card address. Software has the full responsibility for preventing the occurrence of address wrapping.

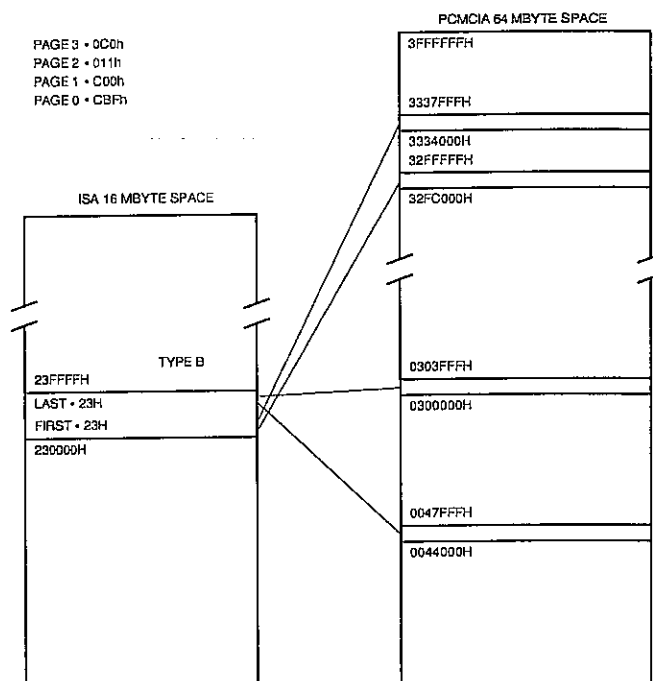


Fig. 17-2 Memory Paged

17-3. PC Card I/O Addressing

The system (ISA) bus is limited to 768 bytes of common I/O address space between the I/O address 100h and 3FFh. The PHIC supports system I/O address decode from 0 to 64 Kbytes. I/O addressing on PC cards is very similar to memory addressing. The PC card can request certain common I/O address locations or can request only the size of the I/O space required. In the latter implementation, the system is free to allocate to the PC card an I/O space anywhere in the 64 Kbyte system I/O address space. The PC card decodes the CE2#, CE1#, IORD#, and IOWR# signals to respond to an I/O access.

The PHIC has two 92) independently enabled and controlled I/O address windows which define a 16 address line decode to achieve a 1 byte resolution. This allows for two noncontiguous I/O address windows for each PCMCIA slot. Each window has independent control of I/O data bus width, zero wait state system bus access, and generation of IOCS16#.

The PC I/O card is selected when the following conditions are satisfied:

1. The I/O address window is enabled;
2. The system (ISA) address is greater than or equal to the I/O address start register A15:A0 (high and low byte); and
3. The system (ISA) address is less than or equal to the I/O address stop register A15:A0 (high and low byte).

It is ultimately up to the system software to account for each I/O address range assigned to a particular PC card and to resolve I/O address conflicts.

The reservation of a particular I/O address range to each PC card conserves system power since only one PC card is enabled during a single I/O access.

The PHIC provides for a 1 byte resolution in the I/O address space. The PC card can request a minimum I/O address space of 1 byte and it is recommended that the PC card not request more than 256 bytes of contiguous I/O address space.

17-4. System Interface Diagram

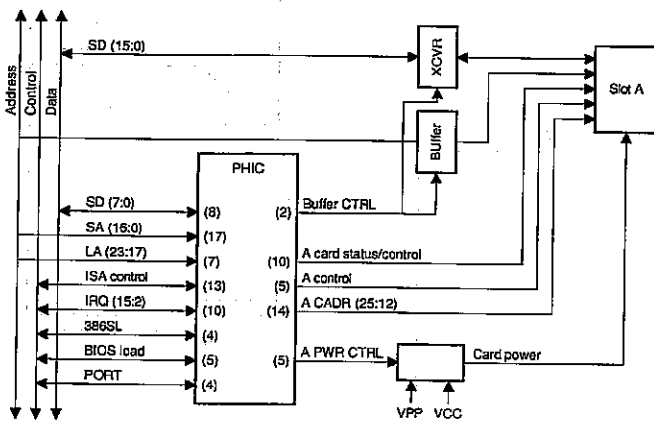
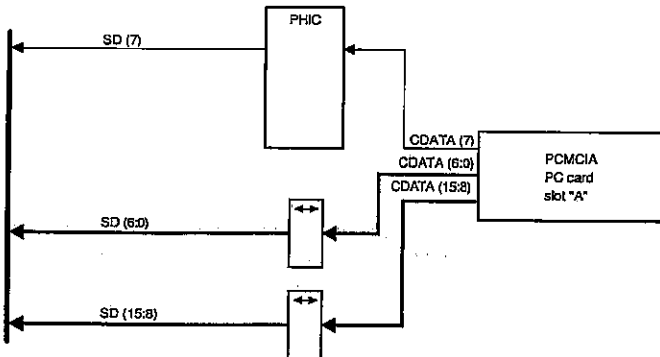


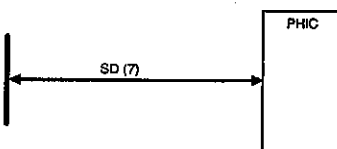
Fig. 17-3 PC HOST Interface Controller Block Diagram

17-5. CARD SLOT A

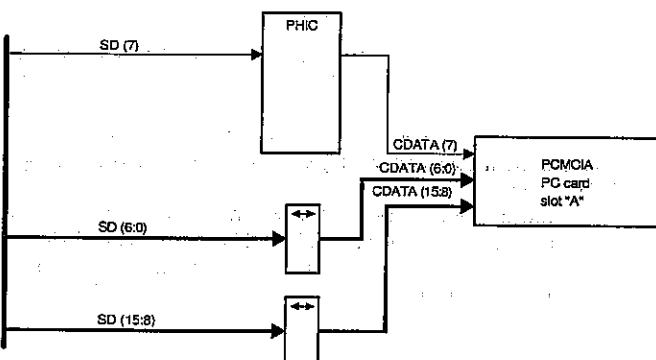
(1) Normal PCMCIA card read datapath



(2) PHIC ASIC internal I/O registers datapath



(3) All PCMCIA card write datapath



18. MICRO TRACK BALL INTERFACE

The track ball is connected to COMB (serial interface). For data transmission, TXD signal is used. For control signal, RTS signal is used. The other signals are not used.

Data transmission format and RTS control are shown below:

1. Data transmission format

Count data are outputted in the following format according to the count number which is processed by resolution switch process. UP/DOWN detection of the encoder is performed even during data output.

Baud rate: 1200 Bps $\pm 2\%$

Data format: Start 1 bit
Data 7 bit
Stop 2 bit or more
Parity No

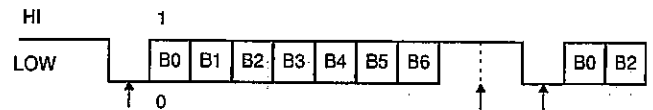


Fig. 18-1 OUTPUT CYCLE

Data composition: 3 Byte

Block data of 3 byte is delivered when the status is changed. In this case, values of X and Y are the formerly delivered data displacement value. Though X and Y are not changed, 3 bite data are delivered by the change in SW-L and R. (Only SW MAKE, SE BREAK.)

	B6	B5	B4	B3	B2	B1	B0
DATA1	1	SW-L	SW-R	Y7	Y6	X7	X6
DATA2	0	X5	X4	X3	X2	X1	X0
DATA3	0	Y5	Y4	Y3	Y2	Y1	Y0

SW-L: Left SWON=1, OFF=0

SW-R: Right SWON=1, OFF=0

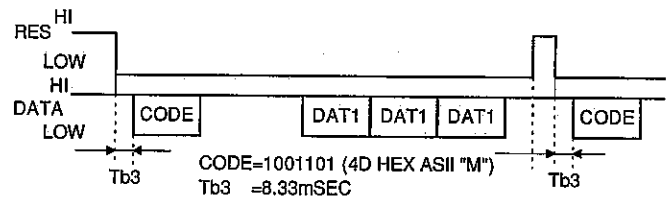
X7 - X0: X shift data (Resolution switch processed)

Y7 - Y0: Y shift data (Resolution switch processed)

2. RTS signal wire treatment

2-2. Serial 1 output

The following special code is outputted only once depending on HI/LOW of the RTS signal wire.



19. DISPLAY CONTROL BOARD

19-1. Display circuit

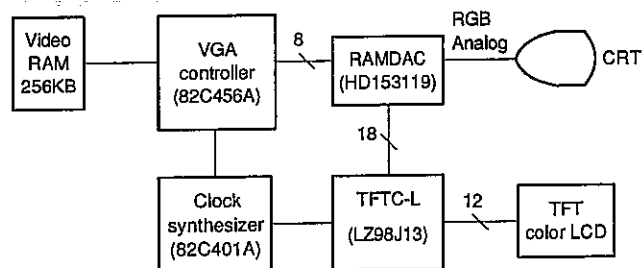


Fig. 19-1 Display circuit block diagram

The display system is configured as shown above. With using the TFT color LCD and the newly designed TFTC-L (TFT panel controller), the PC-6881 can represent 256 out of 256K colors which is fully compatible with the VGA spec.

19-2. VGA controller (82C456A)

19-2-1. GENERAL

The 82C456A is an IBM compatible VGA controller. For the video RAM, eight 256K bit DRAMs are used.

- CPU interface (to 82C456A)

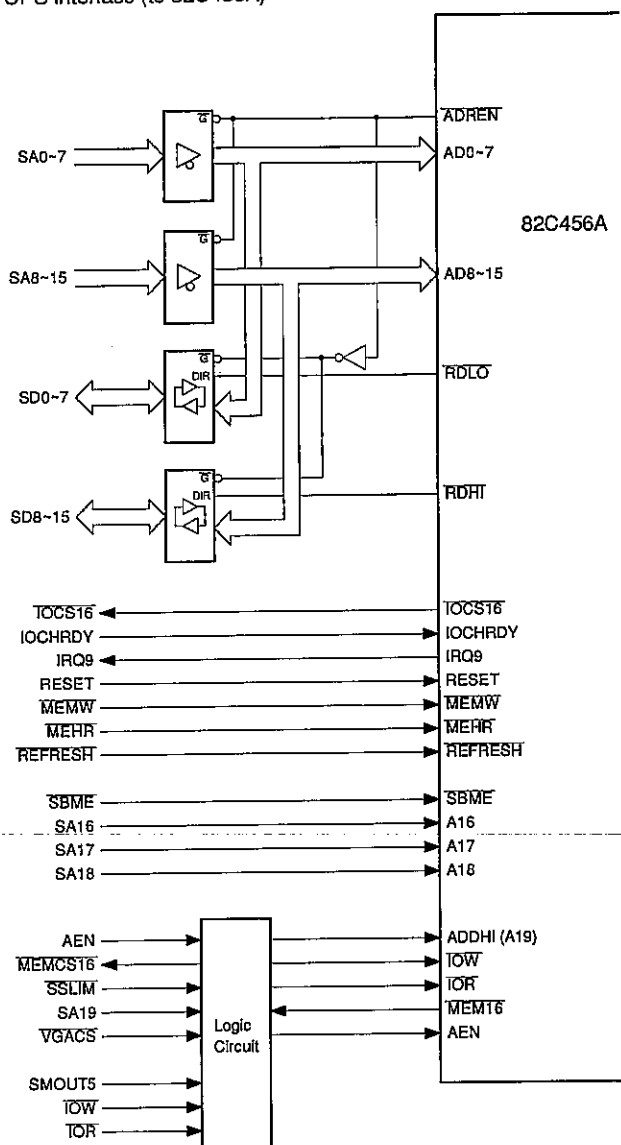


Fig. 19-2 Display control signal

SA0 - 15 and SD0 - 15 are multiplexed and added to the 82C456A as AD0 ~ 15.

$\overline{RDLO}$ signal controls the direction of the HCT245 data transceivers on the lower order byte (Bit 0 - 7) of the data bus.

It becomes active when data is read from the 82C456A.

Similarly, $\overline{RDHI}$ signal controls the direction of the HCT245 on the higher order byte (Bit 8 - 15).

These two signals are 3-stated during RESET.

$\overline{ADREN}$ signal controls the external multiplexing of the address/data bus. $\overline{ADREN}$ low selects the address and HIGH selects the data. When any one of $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, or $\overline{IOW}$ is low, $\overline{ADREN}$ becomes high.

19-2-2. 82C456A PINOUT TOP VIEW

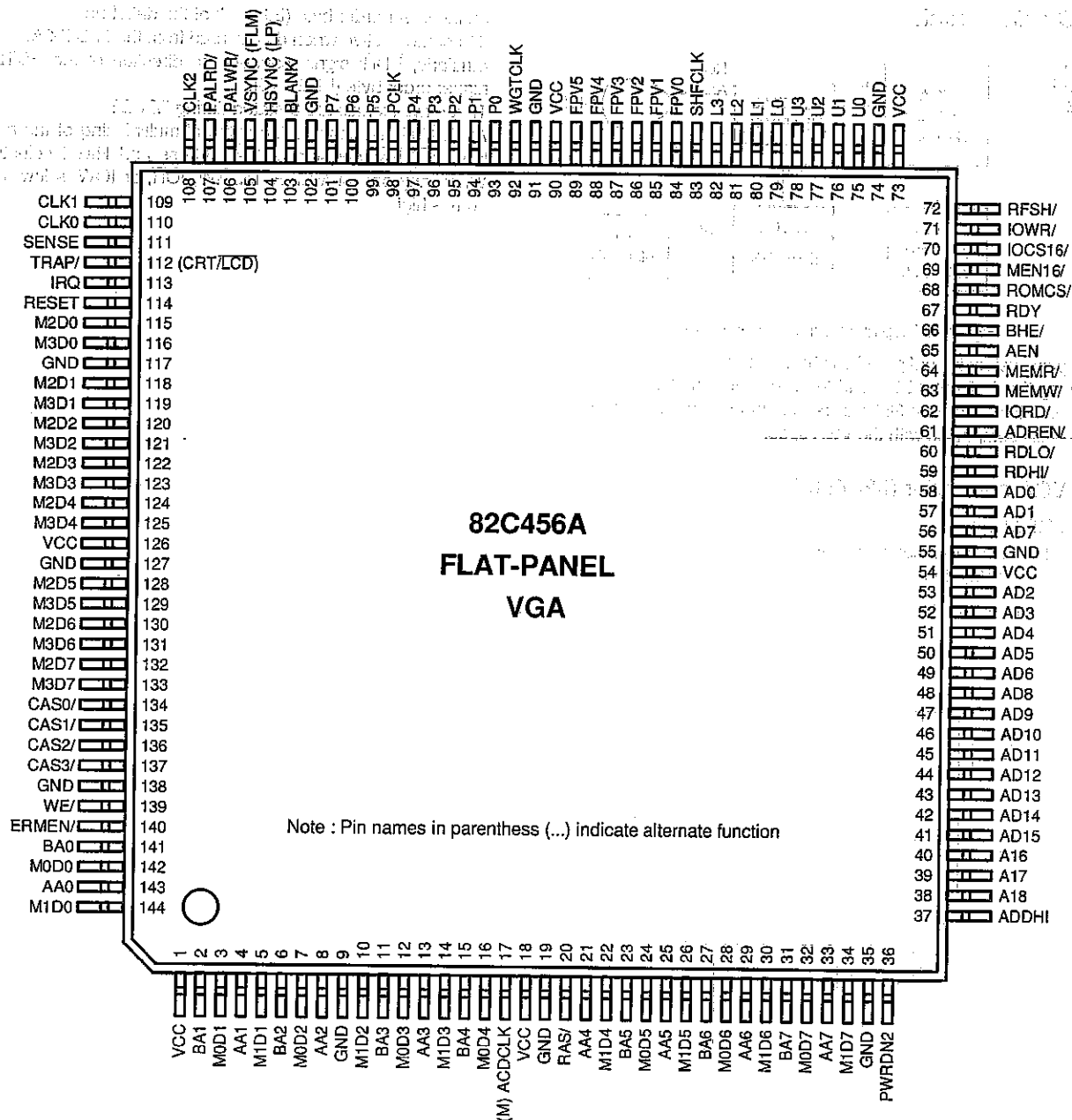


Fig. 19-3 82C456A PINOUT TOP VIEW

Flatpack Pin #	Name	Type	Active	Description
84 85 86 87 88 89	FPV0 FPV1 FPV2 FPV3 FPV4 FPV5	In In In In In In	Both Both Both Both Both Both	No use. These pins are clamped low.
75 76 77 78	U0 U1 U2 U3	Out Out Out Out	Both Both Both Both	No use. These pins are not connected.
79 80 81 82	L0 L1 L2 L3	Out Out Out Out	Both Both Both Both	No use. These pins are not connected.
1 18 54 73 90 126	VCC VCC VCC VCC VCC VCC			POWER
9 19 35 55 74 91 102 117 127 138	GND GND GND GND GND GND GND GND GND GND			GROUND
93 94 95 96 97 99 100 101	P0 P1 P2 P3 P4 P5 P6 P7	Out Out Out Out Out Out Out Out	Both Both Both Both Both Both Both Both	VIDEO PIXEL DATA 7-0. Eight outputs to drive color or monochrome CRTs. These pins are connected to the inputs to the external color palettes. (82C460 and Inmos ISMG176 compatibles.) Color values for digital CRT interface are assigned as follows: P0 B Blue P1 G Green P2 R Red P3 BS/V Secondary Blue/Monochrome P4 GS/I Secondary Green/Intensity P5 RS Secondary Red P6 User Defined P7 User Defined
83	SHFCLK	Out	Both	SHIFT CLOCK. Output pixel clock to which panel output data is synchronized.
98	PCLK	Out	Both	PIXEL CLOCK. Output pixel clock to which CRT Video output data and Flat Panel Video input data is synchronized. This pin is 3-stated during RESET.
92	WGTCLK	Out	High	WEIGHT CONTROL CLOCK. On this board, this signal is used to control external logics.
17	ACDCLK	Out	Both	LCD CLOCK. 50% duty cycle square-wave signal. Phase of this signal inverts every frame.
140	ERMEN/	Out	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C456 to refresh the display. High indicates display access and low indicates CPU access. This pin is not used on this board.
20	RAS/	Out	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	CAS0/	Out	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	CAS1/	Out	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	CAS2/	Out	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	CAS3/	Out	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.

19-2-3. PIN DESCRIPTIONS

Flatpack Pin #	Name	Type	Active	Description
37	ADDHI	In	High	ADDRESS HI. This high order memory address enable input is generated external to the 82C456 by decoding system addresses A19-A23. As an address, it must be valid when ADREN/ is low. It is latched internally and specifies that the current memory address is valid for the 82C456. This input pin is ignored during I/O cycles.
61	ADREN/	Out	Low	ADDRESS ENABLE. The ADREN/ output controls external multiplexing of the system address/data bus. ADREN/ low selects address and ADREN/ high selects data. When MEMR/, MEMW/, IORD/, and IOWR/ are all high. ADREN/ is high when any one of MEMR/, MEMW/, IORD/ or IOWR/ is low.
60	RDLO/	Out	Low	READ LOW. This output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address/data bus. It is low when data is read from the 82C456. DATEN/ can be used to enable the external transceiver. This pin is 3-stated during RESET.
59	RDHI/	Out	Low	READ HIGH. This output operates identically to the RDLO/ output except that it controls the direction for the high order byte (Bits 8-15) of the address/data bus. RDHI/ is low when data is read from the 82C456 and high when data is written to the 82C456. This pin is 3-stated during RESET.
65	AEN	In	Low	ADDRESS ENABLE. When this input and the ADREN/ input is low, it indicates a valid I/O address. The AEN signal is latched internally.
63	MEMW/	In	Low	MEMORY WRITE. This input must be low for CPU writes to display memory.
64	MEMR/	In	Low	MEMORY READ. This input must be low to permit the CPU to read display memory.
71	IOWR/	In	Low	I/O WRITE. This input must be low to permit the CPU to write to an 82C456 I/O register.
62	IORD/	In	Low	I/O READ. This input must be low to permit the CPU to read an I/O register.
72	RFSH/	In	Low	REFRESH. RFSH/ high indicates a valid memory cycle.
70	IOCS16/	Out	Low	I/O SELECT 16. This active low signal indicates a valid 16 bit I/O cycle. IOCS16/ is driven when the VGA is accessed and 3-stated when the VGA is inactive.
67	RDY	Out	Low	VGA READY. When low, this output indicates that the current CPU read/write cycle must be extended with wait states. RDY is driven when the VGA is accessed; it is 3-stated when the VGA is inactive.
69	MEN16/	Out	Low	MEMORY ENABLE 16. This active low signal indicates 16-bit memory cycle transfers are enabled. This signal should be used by external logic to enable decode of high order addresses and generation of MEMCS16/ for the PC-AT bus.
68	ROMCS/	Out	Low	ROM CHIP Select. This active low signal indicates a valid memory read in the range C0000h-C7FFFh. It is not used on this board.
113	IRQ	Out	High	VGA INTERRUPT. An interrupt can be generated whenever the vertical sync signal goes active.
114	RESET	In	High	RESET. An active high input which resets the 82C456.
36	PWRDN2	In	High	POWER DOWN 2. The Power Down input pin selects the Normal or Retire modes of operation. 0: Normal Operation 1: Retire Mode
108 110 109	CLK2 CLK1 CLK0	In In In	Both Both Both	CLOCK 2-0. Video Clock inputs. One of these dot clock inputs is selected by the Miscellaneous Output Register.
111	SENSE	In	Both	SENSE. The state of this input pin can be read at Input Status Register 0, Bit 4.
107	PALRD/	Out	Low	PALETTE READ. This output is active low during I/O reads from addresses in the range 3C6h or 3C8-3C9h (I/O reads from 3C7h are handled directly by the 82C456). This output is normally connected to the Read input of an external Palette/DAC (Inmos IMSG176 or equivalent).
106	PALWR/	Out	Low	PALETTE WRITE. This output is active low during I/O writes to addresses in the range 3C6-3C9h and is normally connected to the Write input of an external Palette/DAC (Inmos IMSG176 or equivalent).
112	CRT/LCD	Out	Low	The Chips BIOS redefines this as a CRT/LCD output. If this pin is high, the BIOS has programmed the part for CRT displays; if low, the BIOS has programmed the part for LCD displays.

Flatpack Pin #	Name	Type	Active	Description
84 85 86 87 88 89	FPV0 FPV1 FPV2 FPV3 FPV4 FPV5	In In In In In In	Both Both Both Both Both Both	No use. These pins are claimed low.
75 76 77 78	U0 U1 U2 U3	Out Out Out Out	Both Both Both Both	No use. These pins are not connected.
79 80 81 82	L0 L1 L2 L3	Out Out Out Out	Both Both Both Both	No use. These pins are not connected.
1 18 54 73 90 126	VCC VCC VCC VCC VCC VCC			POWER
9 19 35 55 74 91 102 117 127 138	GND GND GND GND GND GND GND GND GND GND			GROUND
93 94 95 96 97 99 100 101	P0 P1 P2 P3 P4 P5 P6 P7	Out Out Out Out Out Out Out Out	Both Both Both Both Both Both Both Both	VIDEO PIXEL DATA 7-0. Eight outputs to drive color or monochrome CRTs. These pins are connected to the inputs to the external color palettes. (82C460 and Inmos ISMG176 compatibles.) Color values for digital CRT interface are assigned as follows: P0 B Blue P1 G Green P2 R Red P3 BS/V Secondary Blue/Monochrome P4 GS/I Secondary Green/Intensity P5 RS Secondary Red P6 User Defined P7 User Defined
83	SHFCLK	Out	Both	SHIFT CLOCK. Output pixel clock to which panel output data is synchronized.
98	PCLK	Out	Both	PIXEL CLOCK. Output pixel clock to which CRT Video output data and Flat Panel Video input data is synchronized. This pin is 3-stated during RESET.
92	WGTCLK	Out	High	WEIGHT CONTROL CLOCK. On this board, this signal is used to control external logics.
17	ACDCLK	Out	Both	LCD CLOCK. 50% duty cycle square-wave signal. Phase of this signal inverts every frame.
140	ERMEN/	Out	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C456 to refresh the display. High indicates display access and low indicates CPU access. This pin is not used on this board.
20	RAS/	Out	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	CAS0/	Out	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	CAS1/	Out	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	CAS2/	Out	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	CAS3/	Out	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.

Flatpack Pin #	Name	Type	Active	Description
139	WE/	Out	Low	WRITE ENABLE. Active low write enable signal for all display memory banks/planes.
104	HSYNC (LP)	Out	Either	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (in the MSR @ 3C2, D6) is low. It is active low if the horizontal polarity bit is high. In flat panel mode this polarity is active high.
105	VSNC (FLM)	Out	Either	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (in the MSR @ 3C2, D7) is low. It is active low if the vertical polarity bit is high. In flat panel mode this polarity is active high.
103	BLAND/(DE)	Out	Either	BLANK or DISPLAY ENABLE. BLANK/ is a programmable output for blanking the display which is normally connected to the RAMDAC. For CRTs, it can be redefined as a Display Enable signal in systems where a RAMDAC is not required. For Flat Panels, the Display Enable signal is output on this pin.
144 5 10 14 22 26 30 34	M1D0 M1D1 M1D2 M1D3 M1D4 M1D5 M1D6 M1D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 1 DATA. Display memory data bus for Plane 1 (Map 1).
115 118 120 122 124 128 130 132	M2D0 M2D1 M2D2 M2D3 M2D4 M2D5 M2D6 M2D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 2 DATA. Display memory data bus for Plane 2 (Map 2).
116 119 121 123 125 129 131 133	M3D0 M3D1 M3D2 M3D3 M3D4 M3D5 M3D6 M3D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 3 DATA. Display memory data bus for Plane 3 (Map 3).
143 4 8 13 21 25 29 33	AA0 AA1 AA2 AA3 AA4 AA5 AA6 AA7	Out Out Out Out Out Out Out Out	Both Both Both Both Both Both Both Both	ADDRESS PLANES 1, 0. Display memory address bus for DRAM planes 0 and 1.
141 2 6 11 15 23 27 31	BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7	Out Out Out Out Out Out Out Out	Both Both Both Both Both Both Both Both	ADDRESS PLANES 3, 2. Display memory address bus for DRAM Planes 2 and 3.

Flatpack Pin #	Name	Type	Active	Description
58	AD0	I/O	Both	SYSTEM ADDRESS and DATA BITS 0-15. These bits are used to address display memory and the I/O mapped 82C456 internal registers. They also transfer data between the CPU bus and the 82C456 registers and display memory. Addresses must be valid when output signal ADREN/ is low and data must be held while ADREN/ is high. Addresses are latched internally.
57	AD1	I/O	Both	
53	AD2	I/O	Both	
52	AD3	I/O	Both	
51	AD4	I/O	Both	
50	AD5	I/O	Both	
49	AD6	I/O	Both	
48	AD7	I/O	Both	
47	AD8	I/O	Both	
46	AD9	I/O	Both	
45	AD10	I/O	Both	
44	AD11	I/O	Both	
44	AD12	I/O	Both	
43	AD13	I/O	Both	
42	AD14	I/O	Both	
41	AD15	I/O	Both	
40	A16	In	Both	SYSTEM ADDRESS BITS 18-16. These bits transfer a high-order address when ADREN/ is low. The address bits are latched internally and are ignored for I/O cycles.
39	A17	In	Both	
38	A18	In	Both	
66	BHE/	In	Low	BYTE HIGH ENABLE BHE/ low indicates that the high order byte at the current word address is being accessed. If active, BHE/ must be valid when ADREN/ is low. This data bit is latched internally on the falling edge of IORD/.
142	M0D0	I/O	Both	MEMORY 0 DATA. Display memory data bus for Plane 0 (Map 0).
3	M0D1	I/O	Both	
7	M0D2	I/O	Both	
12	M0D3	I/O	Both	
16	M0D4	I/O	Both	
24	M0D5	I/O	Both	
28	M0D6	I/O	Both	
32	M0D7	I/O	Both	

19-3. HD153119 PINOUT TOP VIEW (RAMDAC)

19-3-1. PINOUT TOP VIEW

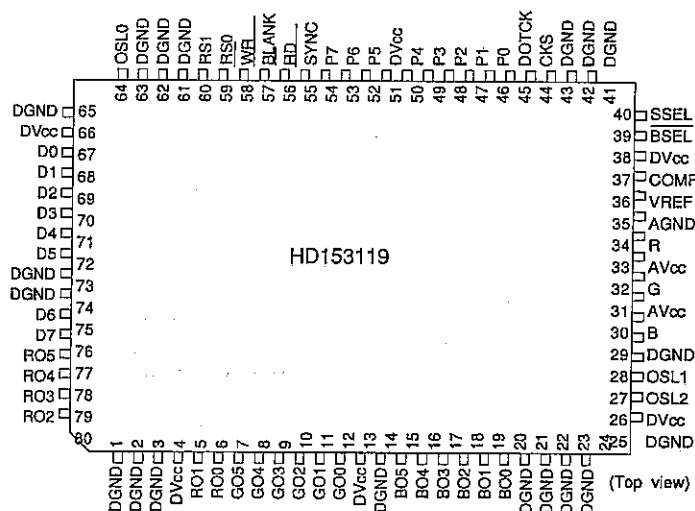


Fig. 19-4 HD153119 PINOUT TOP VIEW

19-6. VIDEO Board Power Management

19-6-1. Features

The video board has been assigned 'SL' power management bits "SMOUT (5)", "SMOUT (1)" and "SMOUT (0)". SMOUT (5) when driven to its active low state places the 82C456A into the power saving "retire" mode.

Additionally, the LCD port data and control lines are driven to their inactive low states. Exactly how the 82C456A behaves in the "power down" state is determined by the BIOS as it has several program-mable option for this mode. SMOUT (0) and SMOUT (1) place LCD panel into the power saving mode by each their combination.

19-6-2. Description

• SMOUT (5)

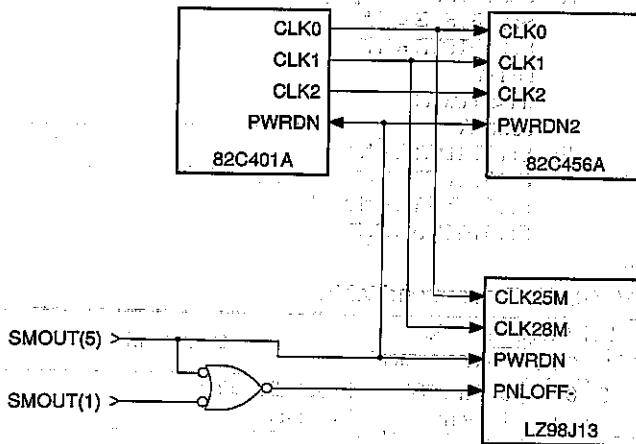


Fig. 19-9 General Power Down Block Diagram

	Normal Operation (SMOUT (5) = H)	Power Down Mode (SMOUT (5) = L)
CLK0	25.175MHz	L
CLK1	28.322MHz	L
CLK2	14.318/40.0MHz	0.795MHz

Clock Power Down

When in powerdown mode, the power consumption of both the 82C401A and the 82C456A are reduced. The power consumption of 82C401A is reduced because it disables all three of its internal VCO's. The 82C401A does keep the reference frequency running, dividing it by an integral value to generate an output frequency which will guarantee DRAM refresh by the 82C456A. The resulting frequency fed to the 82C456A is much lower than the active input hence this feature reduces power consumption in the 82C456A as well.

Furthermore in powerdown mode, both LCD and CRT are off by LZ98J13.

• SMOUT (0), SMOUT (1)

SMOUT (0) and SMOUT (1) signal are used in order to control power supply for the LCD panel and back-light system with the following logic combinations:

SMOUT (1) (CN100-35pin)	SMOUT (0) (CN100-34pin)	Backlight	LCD Drive
0	0	Off	Off
0	1	Off	Off
1	0	Medium Intensity	On
1	1	High Intensity	On

SMOUT (0), SMOUT (1) SELECTION

CHAPTER 6. KEYBOARD

* Note: This keyboard must be replaced in a whole unit when servicing. Therefore only the outline is described below:

1. Full keyboard

1-1. External view

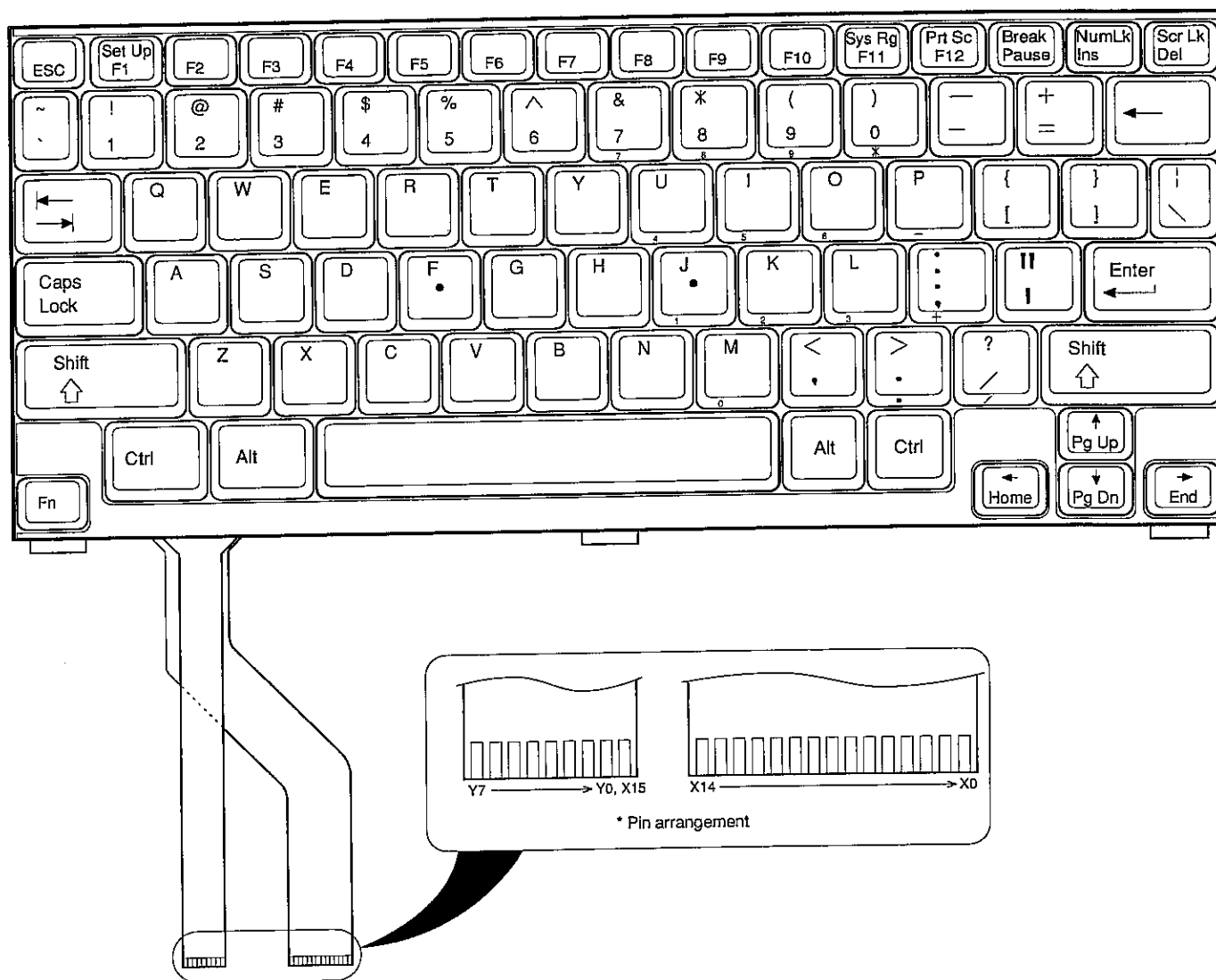


Fig. 6-1

1-2. Keyboard layout and matrix

(1) US Version [79 key] DUNT-2679ACZZ

- Layout for US version

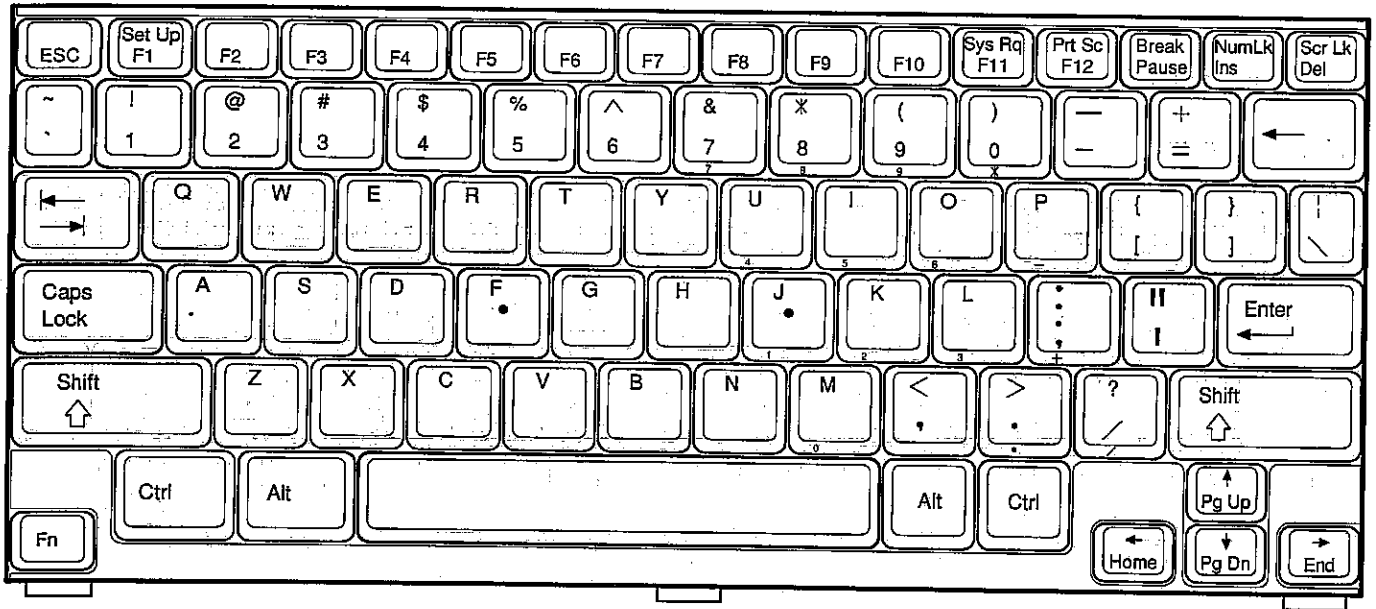
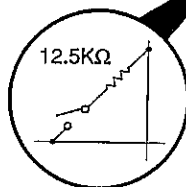


Fig. 6-2

- Matrix for US version

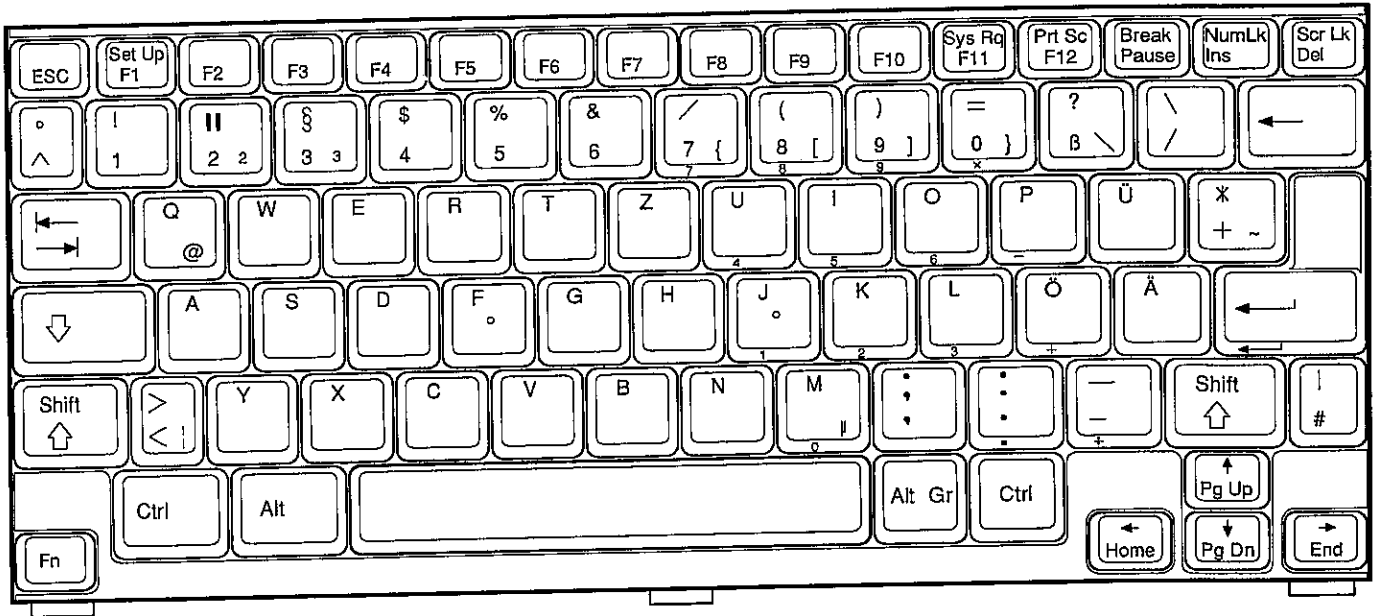
	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	X12	X13	X14
Y0	← Home	R-Alt	R-Ctrl	↖	Enter	↖	+ =	↖	↖	↖					
Y1	↖	SPACE	R-Shift	↑ PgUp	←	}	- _	(9	F8	↖					
Y2	↖	↖	↖	↖	* 8	) 0	% 5	^ 6	L	F6					
Y3	↖	↖	↖	{ [		:	M	L-Alt	B	C					
Y4	? /	< ,	> .	P	O	& 7	K	X	V	J	Y	R	# 3	F5	F4
Y5	↖	↖	↖	N	4	F	D	T	Q	E	\$ 4	↖	@ 2	! 1	F3
Y6	↖	↖	↖	↖	H	G	S	W	A	Z	Caps Lock	↖	Pal F2	L-Ctrl	Esc
Y7	↓ PgDn	→ End	↖	ScrLk Del	NumLK Ins	Break Pause	PrtSc F12	SysRq F11	F10	F9	F7	L-Shift	SetUp F1	~ /	Fn

12.5KΩ



(2) German Version [80 key] DUNT-2681ACZZ

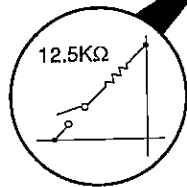
- Layout for German version



- Matrix for German version

	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	X12	X13	X14
Y0	← Home	AltGr	R- Ctrl	~ #	←	↖	↗	↖	↗						
Y1	↖	SPACE	R- Shift	↑ PgUp	←	* + ~	? \ β	(9]	F8	↖					
Y2	↖	↖	Ä	↖	(8 [	) 0 }	% 5	& 6	L	F6					
Y3	↖	↖	↖	U	I	Ö	M	Alt	B	C					
Y4	-	;	:	P	O	/ 7 {	K	X	V	J	Z	R	S 3 3	F5	F4
Y5	↖	↖	↖	N	U	F	D	T	Q @	E	\$ 4	↔	" 2 2	! 1	F3
Y6	↖	↖	↖	↖	H	G	S	W	A	Y	↓	> <	Pal F2	L- Ctrl	Esc
Y7	↓ PgDn	→ End	↖	ScrLK Del	NumLK Ins	Break Pause	PrtSc F12	SysRq F11	F10	F9	F7	L- Shift	SetUp F1	° ^	Fn

X15
12.5KΩ

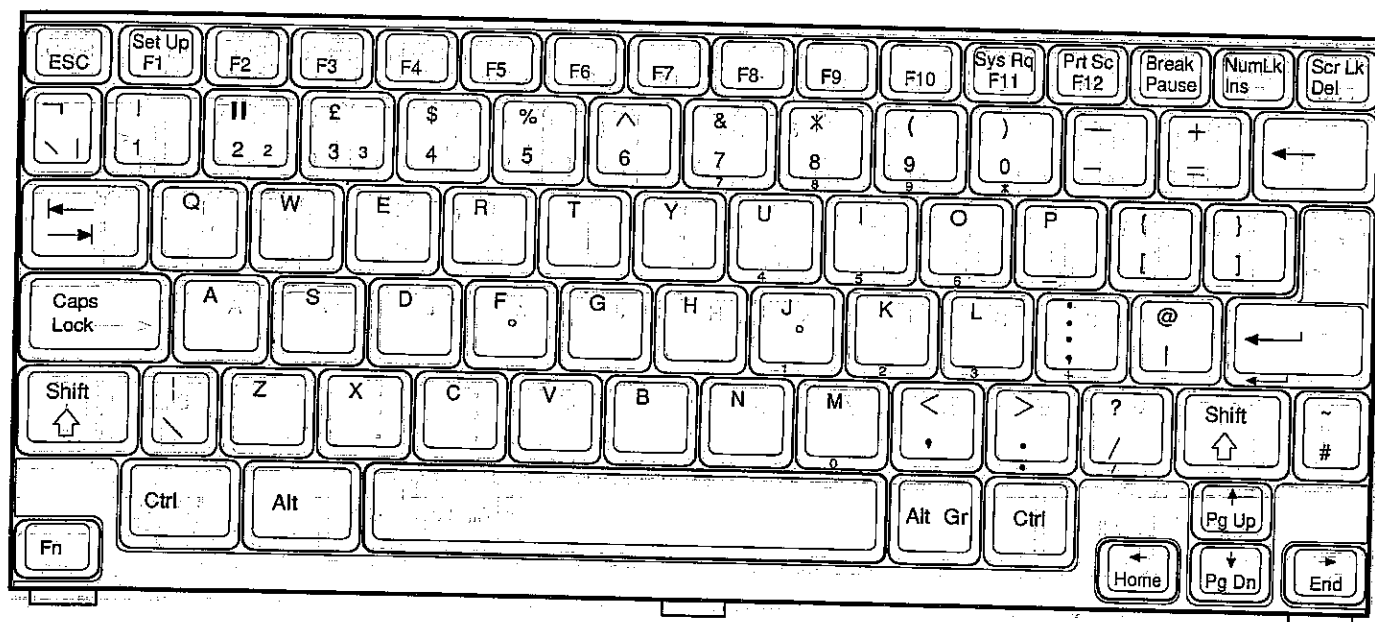


(3) UK Version [80 key] DUNT-2680ACZZ

- Layout for UK version

SYNOPSIS: DUNT-2680ACZZ is a 80-key keyboard.

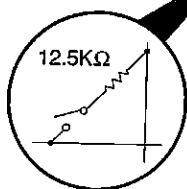
DUNT-2680ACZZ is a 80-key keyboard.



- Matrix for UK version

	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	X12	X13	X14
Y0	← Home	AltGr	R-Ctrl	~ #	Enter	/ =									
Y1		SPACE	R-Shift	↑ PgUp	←	}	-	(9	F8						
Y2			@		* 8	) 0	% 5	^ 6	L	F6					
Y3			{	[	I	:	;	M	Alt	B	C				
Y4	? /	< ,	> .	P	O	& 7	K	X	V	J	Y	R	£ 3	F5	F4
Y5				N	4	F	D	T	Q	E	\$ 4	← →	" 2	1	F3
Y6					H	G	S	W	A	Z	Caps Lock	\	Pal F2	L-Ctrl	Esc
Y7	↓ PgDn	→ End		ScrLK Del	NumLK Ins	Break Pause	PrtSc F12	SysRq F11	F10	F9	F7	L-Shift	SetUp F1	⏏	Fn

X15 12.5KΩ



1-3. 100/102 Key Emulation

(1) U.S. English (101 Key Emulation) Num Lock Off

110	112	113	114	115	116	117	118	119	120	121	122	123	126	75	76
	127													124A	124

1	2	3	4	5	6	7	8	9	10	11	12	13	15
							91	96	101	105			
16	17	18	19	20	21	22	23	24	25	26	27	28	29
							92	97	102	106			
30	31	32	33	34	35	36	37	38	39	40	41	43	
							93	98	103	100		108	
44	46	47	48	49	50	51	52	53	54	55	57		
							99		104	95			
58		60	61						62	64			

128				83	
				85	
			79	84	89
			80	86	81

(2) U.S. English (101 Key Emulation) Num Lock On

110	112	113	114	115	116	117	118	119	120	121	122	123	126	75	76
	127										124A	124		90	125

1	2	3	4	5	6	7	91	96	101	105	12	13	15
							8	9	10	11			
16	17	18	19	20	21	22	92	97	102	106	27	28	29
							23	24	25	26			
30	31	32	33	34	35	36	93	98	103	100	41	108	
							37	38	39	40		43	
44	46	47	48	49	50	51	99	53	104	95	57		
							52		54	55			
58		60	61						62	64			

128				83	
				85	
			79	84	89
			80	86	81

(5) Others (102 Key Emulation) Num Lock On

110	112	113	114	115	116	117	118	119	120	121	122	123	126	75	76
	127										124A	124		90	125

1	2	3	4	5	6	7	91	96	101	105	12	13	15
							8	9	10	11			

16	17	18	19	20	21	22	92	97	102	106	27	28	43
							23	24	25	26			

30	31	32	33	34	35	36	93	98	103	100	41	108
							37	38	39	40		

44	45	46	47	48	49	50	51	99	53	104	95	57	42
								52		54	55		

58	60	61	62	64	83
					85

128	79	84	89
	80	86	81

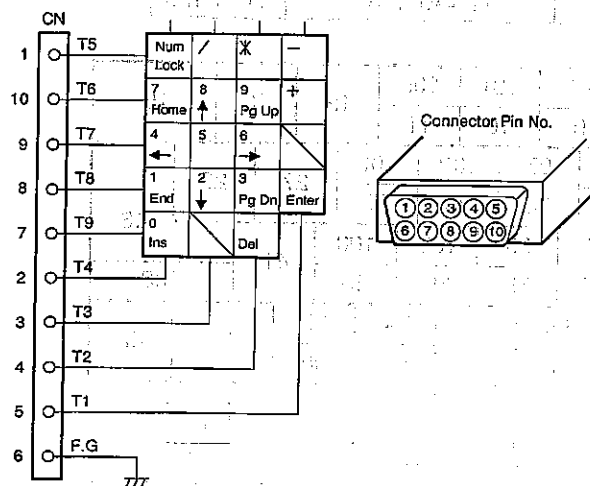
(6) Others (102 Key Emulation) 10 Key Connected

110	112 127	113	114	115	116	117	118	119	120	121	122 124A	123 124	126	75	76
-----	------------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-------------	------------	-----	----	----

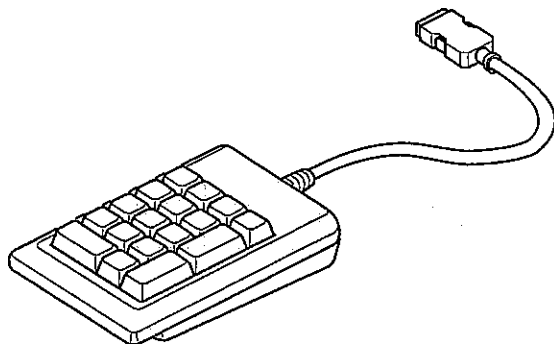
1	2	3	4	5	6	7	8	9	10	11	12	13	15									
16	17	18	19	20	21	22	23	24	25	26	27	28	43									
30	31	32	33	34	35	36	37	38	39	40	41											
44	45	46	47	48	49	50	51	52	53	54	55	57	42									
58		60	61						62	64	<table><tr><td>83</td></tr><tr><td>85</td></tr><tr><td>79</td><td>84</td><td>89</td></tr><tr><td>80</td><td>86</td><td>81</td></tr></table>				83	85	79	84	89	80	86	81
83																						
85																						
79	84	89																				
80	86	81																				
128																						

2.10 Keypad [CE-671NK: Option]

2-1. Matrix



2-2. External view



The keyboard has number keys, arithmetic symbol keys, and cursor shift keys for convenience of inputting table calculation and adding up of data.

2-3. Numeric Key Code

90	95	100	105
91	96	101	106
92	97	102	
93	98	103	108
99	104		

3. System Scan Code Table

KEY No.	Make-Code	Break-Code
1	29	A9
2	02	82
3	03	83
4	04	84
5	05	85
6	06	86
7	07	87
8	08	88
9	09	89
10	0A	8A
11	0B	8B
12	0C	8C
13	0D	8D
15	0E	8E
16	0F	8F
17	10	90
18	11	91
19	12	92
20	13	93
21	14	94
22	15	95
23	16	96
24	17	97
25	18	98
26	19	99
27	1A	9A
28	1B	9B
29 (101 key)	2B	AB
30	3A	BA
31	1E	9E
32	1F	9F
33	20	A0
34	21	A1
35	22	A2
36	23	A3
37	24	A4
38	25	A5
39	26	A6
40	27	A7
41	28	A8
42 (102 key)	2B	AB
43	1C	9C
44	2A	9A
45 (102 key)	56	D6
46	2C	AC
47	2D	AD
48	2E	AE
49	2F	AF
50	30	B0

KEY No.	Make-Code	Break-Code
51	31	B1
52	32	B2
53	33	B3
54	34	B4
55	35	B5
57	36	B6
58	1D	9D
60	38	B8
61	39	B9
62	E0 38	E0 B8
64	E0 1D	E0 9D
75 (Case 1)	E0 52	E0 D2
75 (Case 2)	E0 AA E0 52	E0 D2 E0 2A
75 (Case 3)	E0 2A E0 52	E0 D2 E0 AA
76 (Case 1)	E0 53	E0 D3
76 (Case 2)	E0 AA E0 53	E0 D3 E0 2A
76 (Case 3)	E0 2A E0 53	E0 D3 E0 AA
79 (Case 1)	E0 4B	E0 CB
79 (Case 2)	E0 AA E0 4B	E0 CB E0 2A
79 (Case 3)	E0 2A E0 4B	E0 CB E0 AA
80 (Case 1)	E0 47	E0 C7
80 (Case 2)	E0 AA E0 47	E0 C7 E0 2A
80 (Case 3)	E0 2A E0 47	E0 C7 E0 AA
81 (Case 1)	E0 4F	E0 CF
81 (Case 2)	E0 AA E0 4F	E0 CF E0 2A
81 (Case 3)	E0 2A E0 4F	E0 CF E0 AA
83 (Case 1)	E0 48	E0 C8
83 (Case 2)	E0 AA E0 48	E0 C8 E0 2A
83 (Case 3)	E0 2A E0 48	E0 C8 E0 AA
84 (Case 1)	E0 50	E0 D0
84 (Case 2)	E0 AA E0 50	E0 D0 E0 2A
84 (Case 3)	E0 2A E0 50	E0 D0 E0 AA
85 (Case 1)	E0 49	E0 C9
85 (Case 2)	E0 AA E0 49	E0 C9 E0 2A
85 (Case 3)	E0 2A E0 49	E0 C9 E0 AA
86 (Case 1)	E0 51	E0 D1
86 (Case 2)	E0 AA E0 51	E0 D1 E0 2A
86 (Case 3)	E0 2A E0 51	E0 D1 E0 AA
89 (Case 1)	E0 4D	E0 CD
89 (Case 2)	E0 AA E0 4D	E0 CD E0 2A
89 (Case 3)	E0 2A E0 4D	E0 CD E0 AA
90	45	C5
91	47	C7
92	4B	CB
93	4F	CF
95 (Case 4)	E0 35	E0 B5
95 (Case 5)	E0 AA E0 35	E0 B5 E0 2A
96	48	C8
97	4C	CC
98	50	D0
100	37	B7
101	49	C9
102	4D	CD
103	51	D1
104	53	D3
105	4A	CA
106	4E	CE
108	E0 1C	E0 9C
110	01	81
112	3B	BB
113	3C	BC
114	3D	BD
115	3E	BE
116	3F	BF

KEY No.	Make-Code	Break-Code
117	40	C0
118	41	C1
119	42	C2
120	43	C3
121	44	C4
122	57	D7
123	58	D8
124 (Case 4)	E0 2A E0 37	E0 B7 E0 AA
124 (Case 6)	E0 37	E0 B7
124A	54	D4
125	46	C6
126 *1 (Case 4)	E1 1D 45 E1 9D C5	-
126 *1 (Case 7)	E0 46 E0 C6	-
127	1D 38 1F	9D B8 9F
128	-	-

Case 1: Base Case, or Shift + Num Lock ON

Case 2: Shift + Num Lock Off

If the left shift key is held down, the AA/2A is sent.

If the right shift key is held down, the B6/36 is sent.

If both shift keys are held down, both sets of codes are sent.

Case 3: Num Lock ON + Base Case

Case 4: Base Case

Case 5: Shift Case (Same as Case 2)

Case 6: Ctrl Case + Shift Case

Case 7: Ctrl Case

*1: This key is not typematic. All associated scan codes occur on the make of the key.

CHAPTER 7. 2.5 inch HDD (80MB)

1. Feature

The WDA280 is a high performance 2.5 inch low-profile (17mm) 80 megabyte (formatted) disk drive with 16.5 ms average seek time (typ) which is designed to operate on an IBM PC/XT & PC/AT or equivalent computer. The drive features a low 5V power requirement and high shock resistance, enabling battery operation in portable environments.

Key Features include:

- 2.5" Form factor
- Single 5 Volt supply
- Low power requirements
- Unit weight 180g
- High performance rotary voice coil actuator with embedded servo system.
- Single connector for power & interface
- One of seven run length limited code.
- High shock resistance.

Key Features continued

- Sealed HDA with internal air filtration system
- Automatic actuator latch against inner stop upon power down.
- Microprocessor-controlled diagnostic routines that are automatically executed at start-up.
- Block size 512 bytes.
- PC/AT interface
- 1:1 Interleave
- 8K Buffer with Look-Ahead Read Capability
- Master/Slave option.
- Used to ATA interface (Rev 2.2 Aug 15 1990)

2. Specification Summary

2-1. Capacity

Formatted Mbytes	80 Mbytes
------------------	-----------

2-2. Physical Configuration

Actuator Type	Rotary Voice-Coil
Number of Disks	2
Data Surfaces	4
Data Heads (Logical)	10
Servo	Embedded
Tracks per Surface (Logical)	965
Formatted Track Capacity (Bytes) (Logical)	8704
Bytes per Block	512
Blocks per Drive	164,050
Sectors per Track:	
Logical	17

2-3. Performance

Seek Times	Track to Track: 5.0 ms Average: 16.5 ms (typ)
Average Latency	8.33 ms
Rotation Speed (+0.1%)	3600 RPM
Controller Overhead (typ)	1.0 ms
Data Transfer Rate (To/From Media)	1.167 MByte/second
(0 RPM - Ready)	Typical: 6 seconds Maximum: 18 seconds
Stop time (Power Down)	Maximum: 5 seconds
Start/Stop Cycles	52,000 min.
Interleave	1:1
Buffer Size	8K

3. Functional Description

The WDA240/280 contains all necessary mechanical and electronic parts to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

3-1. Read/Write and Control Electronics

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is head selection, read preamplification, and write data circuitry.

The single microprocessor controlled circuit card provides the remaining electronic functions which include:

- Read/Write Circuitry
- Rotary Actuator Control
- Interface Control
- Spin Speed Control
- Dynamic Bracking
- Power Management

At power down or the start of STANDBY MODE the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is inside the data tracks.

3-2. Drive Mechanism

A brushless DC direct drive motor rotates the spindle at 3600 RPM. The motor/spindle assembly is balanced to provide minimal mechanical runout to the disks and to reduce vibration of the HDA. A dynamic brake is used to provide a fast stop to the spindle motor when power is removed, or upon initiation of STANDBY MODE.

3-3. Air Filtration System

The head-disk assembly is a sealed enclosure with filter which maintains a clean environment for the heads and disks.

3-4. Head Positioning Mechanism

The two read/write heads are supported by a mechanism coupled to the voice coil actuator.

3-5. Read/Write Heads and Disks

Data is recorded on one 65mm diameter disk through two miniature thin film heads.

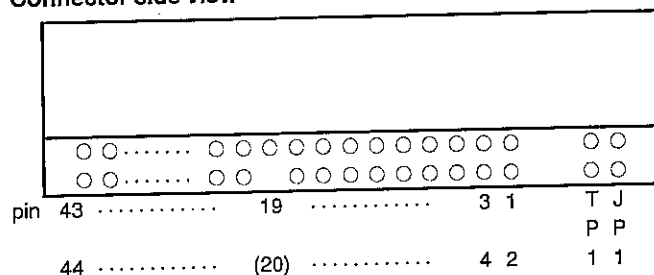
3-6. PC AT Interface

The WDA280 are designed to operate in AT interface single drive mode. An LED drive signal is provided via the interface.

3-7. Master/Slave

The WDA280 is designed to operate either as a master (C drive) or a slave (D drive) depending on the state of Jumper JP1. The drive will be configured as a master or single drive when its shipped. On power up, the state of jumper JP1 is sampled and the appropriate role (master/slave) is selected. When jumper JP1 is closed, the drive will assume the role of master. When jumper JP1 is open, the drive will act on the slave. In single drive configurations, jumper JP1 must be closed. For location of jumper JP1, see outline drawing (Fig. 7-1).

Connector side view



Note 1: Pin 20 position is left blank for secure connector insertion.

Note 2: TP1 is used for manufacturer's test purpose. These pins shall be left unconnected.

Note 3: JP1 is used to characterize a drive to DRIVE-0 or DRIVE-1. A jumper plug in the JP1 position forces DRIVE-0 mode.

Fig 7-1. 44 pin AT Connector

4. Interface Connector

The WDA240/280 has a 44 pin right angle interface/power connector mounted on the PCB. The recommended mating connector is DuPont Part Number: 69764-044 or equivalent. The maximum cable length is 18 inches. For location of the interface connector, see Fig. 7-2.

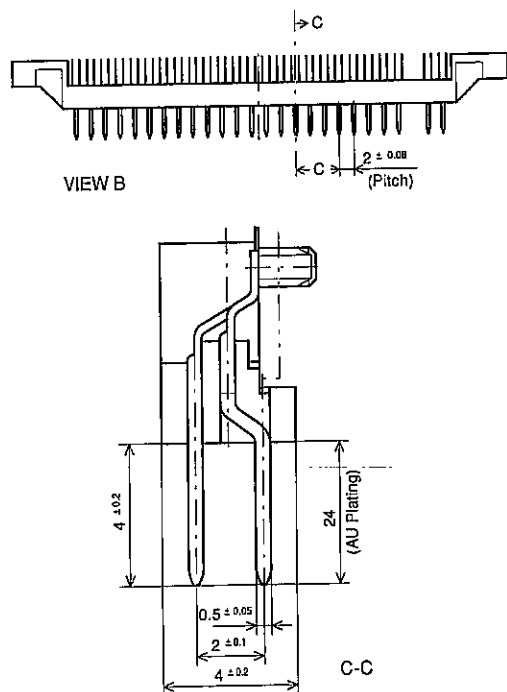


Fig 7-2. AT I/F Connector Pin

5. Mechanical Characteristics

5-1. Mechanical Dimensions (not including mounting hardware)

DIMENSIONS		WDA-280
Height	(mm)	17.0 +0.35 -0.30
Width	(mm)	70.0 ±0.25
Depth	(mm)	100.0 ±0.25
Weight	(g)	180 Max.

Table 7-1. mechanical Dimensions

See IBM Drawings, P/N 95F7161 for WDA-280 for the exact dimensions and tolerances and other requirements.

5-2. Mounting Orientation

The disk drive shall operate within specified error rates in all axis with no limitation. The test was done within ±5 degrees from these positions.

Performance and error rate must stay within specification limits if the disk drive is operated in the other permissible orientations from which it was formatted. Thus a disk drive formatted in a horizontal orientation must be able to run vertically and vice versa.

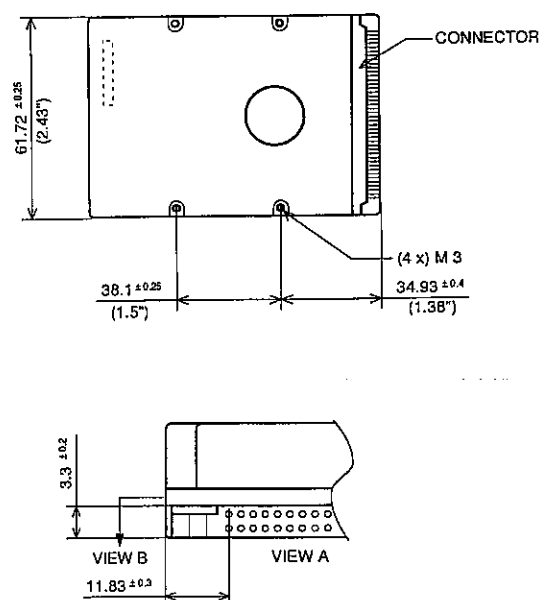
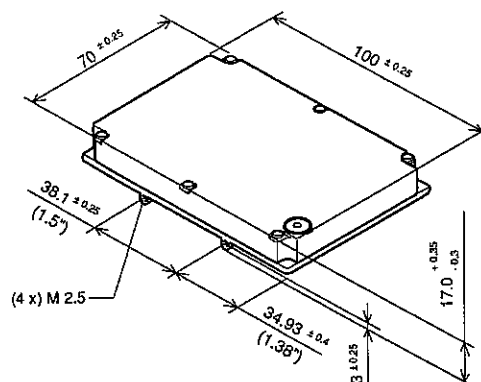


Fig 7-3. WD-280 Outline

6. Electrical interface specification

6-1. Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	-HRESET	I	TTL	02	GND		
03	HD07	I/O	3-state	04	HD08	I/O	3-state
05	HD06	I/O	3-state	06	HD09	I/O	3-state
07	HD05	I/O	3-state	08	HD10	I/O	3-state
09	HD04	I/O	3-state	10	HD11	I/O	3-state
11	HD03	I/O	3-state	12	HD12	I/O	3-state
13	HD02	I/O	3-state	14	HD13	I/O	3-state
15	HD01	I/O	3-state	16	HD14	I/O	3-state
17	HD00	I/O	3-state	18	HD15	I/O	3-state
19	GND			(20)	Key		
21	(Resv)			22	GND		
23	-HIOW	I	TTL	24	GND		
25	-HIOR	I	TTL	26	GND		
27	IORDY	O	OC	28	(Resv)		
29	(Resv)			30	GND		
31	HIRQ	O	3-state	32	-HIOCS16	O	3-state
33	HA01	I	TTL	34	-PDIAG	I/O	OC
35	HA00	I	TTL	36	HA02	I	TTL
37	-HCS0	I	TTL	38	-HCS1	I	TTL
39	-DASP	I/O	OC	40	GND		
41	+5V LOGIC	PWR		42	+5V MOTOR	PWR	
43	GND	I/O	OC	44	-XT/AT	I	TTL

Note: "O" designates an output from the Drive.

"I" designates an input to the Drive.

"I/O" designates an input/output common.

"PWR" designates a power supply to the Drive.

"OC" designates Open-Collector output.

"(Resv)" designates reserved pins and all of these have to be left unconnected.

Table 7-2. Table of signals

The pin description are listed as follows:

Signal Name	Description
HD00-HD15	16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, HD00-07, are used for Register and ECC access. All 16 lines, HD00-15, are used for data transfer. These are Three-State lines with 24 mA drive capability.
HA00-HA02	Address used to select the individual register in the HDD.
-HCS0	Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error {Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status {Command when written} register) can be selected. (See Table 7-5)
-HCS1	Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status {Devices Control when written} and Drive Address register) can be selected. (See Table 7-5)
-HRESET	This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.
-HIOW	Its rising edge holds data from the host data bus to a register or data register of the HDD.
-HIOR	When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latches on the rising edge of -HIOR.
HIRQ	Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 10 mA drive capability.
IORDY	Indication to host that the drive is ready to complete current I/O cycle. This line is driven low at the falling edge of -HIOR or -HIOW, when HDD needs some additional WAIT cycle(s) to extend PIO cycle. This line can be connected to host IORDY signal in order to insert WAIT state(s) in the host PIO cycle. This is an open-collector output with 10 mA drive capability.
-HIOCS16	Indication to the host that 16-bit data register has been addressed and that the drive is prepared to send or receive a 16-bit data word. This signal is a 3-State line with 24 mA drive capability.
-DASP	This is a time-multiplexed signal which indicates that a drive is active, or that drive 1 is present. This signal is driven by Open Collector driver and internally pulled-up to 5 Volt through 10Kohm resistor. During Power-On initialization or after -RESET is negated, -DASP shall be asserted by Drive 1 within 400 msec to indicate that drive 1 is present. Drive 0 shall allow up to 450msec for drive 1 to assert -DASP. If drive 1 is not present, drive 0 may assert -DASP to drive a LED indicator. -DASP shall be negated following acceptance of the first valid command by drive 1 or after 31 seconds, whichever comes first. Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.

Signal Name	Description
-PDIAG	This signal shall be asserted by drive 1 to indicate to drive 0 that it has completed diagnostics. This line is pulled-up to 5 Volt internally through a 10Kohm resistor. Following a Power On Reset, software reset or -HRESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to drive 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status. After the assertion of -PDIAG, drive 1 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY = 1). Following the receipt of a valid Execute Drive Diagnostics command, drive 1 shall negate -PDIAG within 1 msec to indicate to drive 0 that it is busy and has not yet passed its drive diagnostics. If drive 1 is present then drive 0 shall wait for up to 5 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Drive 1 should clear BSY before asserting -PDIAG, as -PDIAG is use to indicate that drive 1 has passed its diagnostics and is ready to post status. If -DASP was not asserted by drive 1 during reset initialization, drive 0 shall post its own status immediately after it completes diagnostics, and clear the drive 1 Status register to 00h. Drive 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY = 1).
KEY	Pin 20 position was left blank. It is recommended to close this position of the cable connector in order to avoid reverse insertion by mistake.
XT/AT	This line is pulled-up to +5V through 4.7Kohm in HDD (high = AT mode).
5V Power	There are two input pins for +5V power supply, "+5V LOGIC" and "+5V MOTOR". "+5V LOGIC" is connected to the internal logic circuits and "+5V MOTOR" is connected to the spindle motor and motor driver. It is possible to turn on and off "+5V LOGIC" by external switch circuit to reduce power consumption as less as possible. At this mode, the voltage drop out by means of motor spin up rush current can be relieved by connecting "+5V MOTOR" line into system power source directory. If above power management is applied, all signal line that will be electrically active in the host system while the HDD is disconnected from power line shall be isolated by Three-State line drivers. Internal leak through ESD protection circuit may pull down LPUL (Least Positive Up Level) of logic signal below the spec. Use both lines parallely, for regular HDD applications.

Table 7-3. Signal description

6-2. Interface Logic Signal Levels

The interface logic signal have the following electrical specifications:

Inputs:

Input High Voltage
2.0 V min.

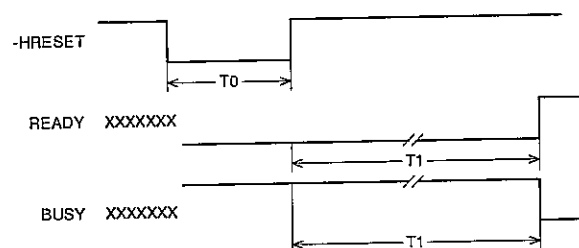
Input Low Voltage
0.8 V max.

Outputs:

Output High Voltage
2.4 V min.

Output Low Voltage
0.5 V max.

HDD reset timing



Current:

Driver Sink Current
24 mA min.

Driver Source Current
=400 μ A min.

6-3. Reset timings

HDD reset timing.

	PARAMETER DESCRIPTION	Min (μ sec)	Typ (sec)	Max (sec)
T0	-HRESET low width	25	—	—
T1	-HRESET high to READY/Not BUSY	—	6	18

Fig 7-4. System Reset timing

6-4. PIO timings

Timings of Pio cycle meets the CAM description for mode 1 PIO timing, except IORDY timing.

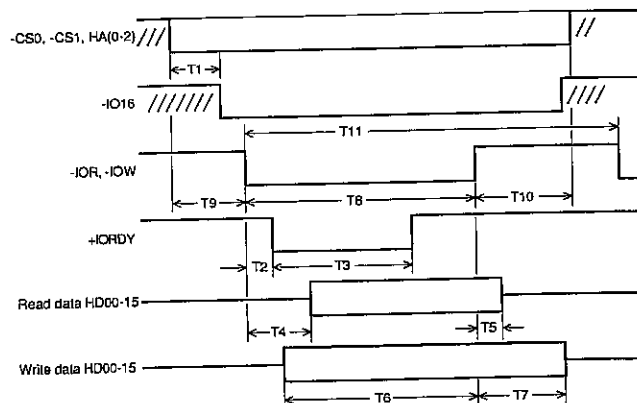


Fig 7-5. PIO cycle timings

In Fig. 7-5, drive shall meet timings below.

	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T1	-CS0, -CS1, HA00-02 low to -IO16 low	—	50	
T2	-IOR/W low to +IORDY low	—	35	
T3	+IORDY pulse width	0	2500	*1
T8	-IOR/W pulse width	100	—	
T11	-IOR to -IOR or -IOW to -IOW	350	—	*2

Note:

1. This value does not meet CAM (1250nsec). But only in Read/Write multiple command execution, this violation occurs.
2. When the I/O cycle is shorter than 300nsec, +IORDY is negated (up to 300nsec).

And, in Fig. 7-5, typical host system shall meet timings as below.

Table 7-3 Drive Signal timing

	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T4	-IOR low to HD00-15 valid	—	90	
T5	-IOR high to HD00-15 high-impedance	5	—	
T6	HD00-15 setup to -IOW high	40	—	
T7	HD00-15 hold from -IOW high	20	—	
T9	-CS0, -CS1, HA00-02 setup to -IOR/W low	25	—	
T10	-CS0, -CS1, HA00-02 hold from -IOR/W high	10	—	

Table 7-4. Host Bus timing

6-5. Drive Address and Mode

A jumper plug is available to determine drive mode.

DRIVE-0/DRIVE-1 Jumper (JP1) Address of DRIVE-0 and 1 are selectable. With a jumper plugged on JP1, the drive responds as DRIVE-0.

6-6. Addressing of HDD Registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the host's I/O space. Two chip select lines (-CS0 and -CS1) and three address lines (ADDR 0-2) are used to select one of these registers, while a -IOR or -IOW is provided at the specified time.

The -CS0 is used to address Command Block registers. While the -CS1 is used to address Control Block registers.

The following table shows the I/O address map.

Addr.	-CS0	-CS1	HA2	HA1	HA0	-IOR = 0 (Read)	-IOW = 0 (Write)
Command Block Registers							
1F0	0	1	0	0	0	Data Reg.	Data Reg.
1F1	0	1	0	0	1	Error Reg.	Features Reg.
1F2	0	1	0	1	0	Sector count Reg.	Sector count Reg.
1F3	0	1	0	1	1	Sector number Reg.	Sector number Reg.
1F4	0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
1F5	0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
1F6	0	1	1	1	0	Drive/head Reg.	Drive/head Reg.
1F7	0	1	1	1	1	Status Reg.	Command Reg.
Control Block Registers							
3F6	1	0	1	1	0	Alt. status Reg.	Device control Reg.
3F7	1	0	1	1	1	Drive address Reg.	—

Note: "Addr." field is shown just as an example.

Table 7-5 Task File

6-7 Cabling

The maximum cable length from the host system to the HDD and wire pattern length in the host system shall not exceed 18 inches.

CHAPTER 8. MICRO TRACK BALL

Note: This Micro Track Ball unit must be replaced in a whole unit except for the ball. Therefore only the outline is described below:

1. Outline

When the Micro Track Ball (MTB hereinafter) is shifted from right to left by your fingers, the cursor on the display also moves from right to left accordingly. The cursor moving speed is same as the ball shifting speed to easily locate the cursor at your desired position. The use of optical system sensor assures high life and high reliability in the compact design, being suitable for lap-top or note PC or other devices.

Features

- Long life/High reliability
- Low power consumption
- Small and light weight
- 5V single power
- Easy installation

2. Structure

The MTB has a ball at the center and two shafts crossing vertical to each other in connection with the ball. The encoder is directly connected to these shafts. When the ball is rotated, the two shafts are rotated and the rotations in X and Y directions are detected by the encoder.

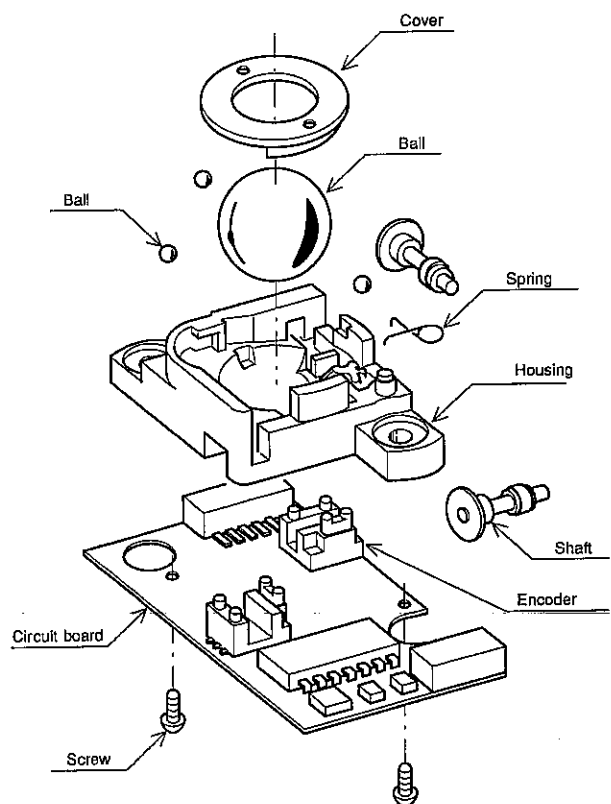


Fig. 8-1 MTB structure

3. Composition

MTB composition is shown in Fig. 8-2.

- (1) Composition
- [1] Cover
 - [2] Ball ($\phi 11$)
 - [3] MTB body
 - [4] Circuit board

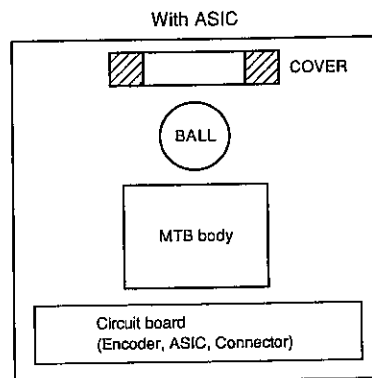


Fig. 8-2 MTB composition

4. Mechanical description

4-1. External dimensions

Fig. 8-3 shows external dimensions of the MTB.

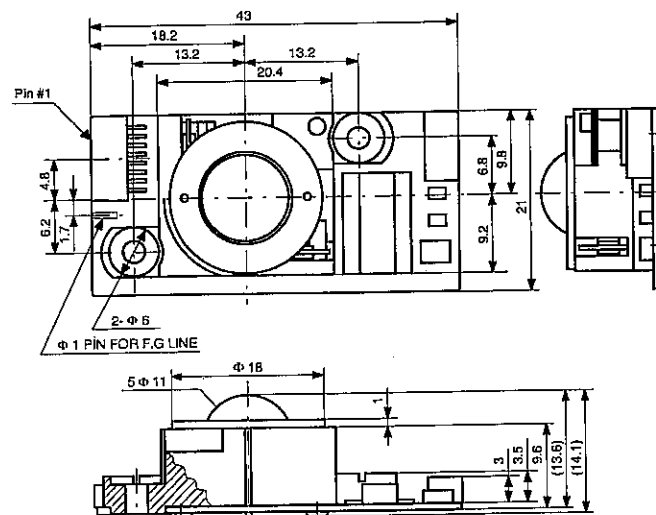
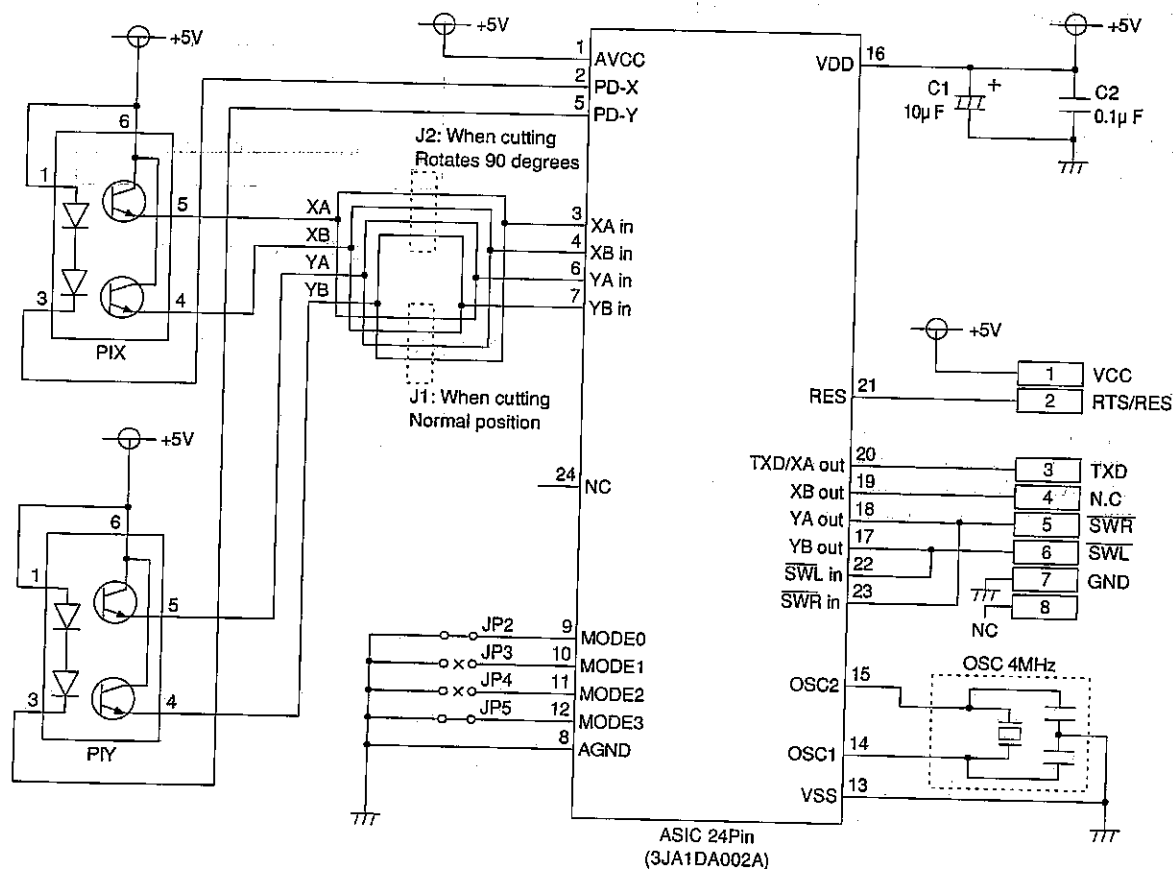


Fig. 8-3 External dimensions

5. Electrical description

The MTB has built-in ASIC, which has all functions: (pre-amplifier, waveform rectifying circuit, low current consumption control function; automatic resolution switching, interface <serial/bus>) to allow direct connection with system. The bus/serial function and the automatic resolution switching are set to serial 1, turbo medium-speed mode by pattern cut when shipping. For details, refer to Fig. 8-4. The MTB circuit diagram, connection, pin assignment, and cable shapes are shown in the following.

5-1. Circuit diagram



● MODE selection table:

MODE0	MODE1	Operation mode
1	1	Bus
0	1	Serial 1
1	0	Serial 2

* 2 →

MODE2	MODE3	Operation mode
1	1	Turbo low speed
1	0	Turbo medium speed
0	1	Turbo high speed
0	0	Turbo stop

* 2 →

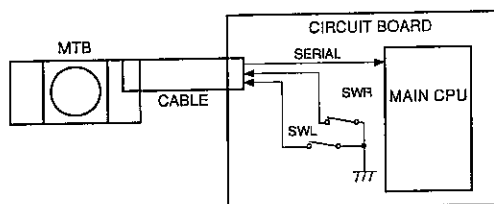
*1: 1 = Cut
0 = Short

*2: Setting mode (default) in this unit is shown with arrow ➡

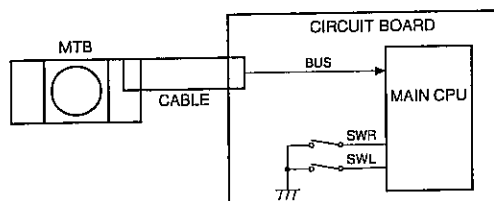
Fig. 8-4. Circuit diagram

5-2. MTB connection

(1) Serial



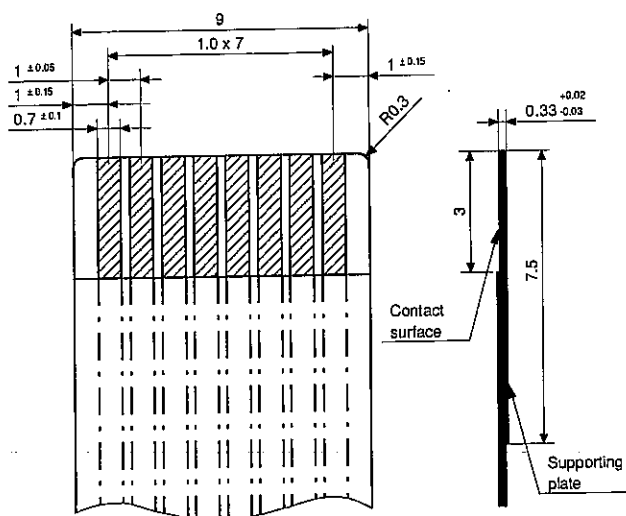
(2) Parallel (Not used)



5-3. Pin assignment

Pin No.	Signal name
	Serial
1	+5
2	RTS
3	TD-
4	-
5	SWR
6	SWL
7	GND
8	-

5-4. Cable shape



CHAPTER 9. COLOR DISPLAY UNIT

1. COLOR TFT LCD UNIT (LQ9D010)

1-1. Operating theory

Liquid crystal display is usually called LCD in short which applies to mean a mesomorphism substance whose state is between liquid and solid like soap water. In 1963, Williams of RCA discovered that an electrical stimulation to liquid crystal causes it to change its optical path. Five year later, a group headed by Heilmeyer of RCA created the display unit which utilized this property. This is the beginning of the liquid crystal display.

Now, an explanation will be provided to discuss the theory of a display that uses the property of liquid crystal molecules, taking the TN type liquid crystal as an example.

(1) Liquid crystal with regular alignment twisted

- **Liquid crystal is a substance whose phase is in-between liquid and solid.**

It is a translucent liquid which is slight viscose. Liquid crystal was discovered by Austrian botanist whose name is Lienitzer.

- **Property molecules regularly distributed**

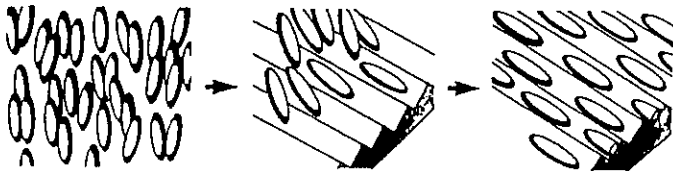
Almost any liquid crystal material is an organic compound that has a monocular structure of a bar form.

In nature, molecules are aligned with regularity.

- **Molecules resting along grooves on a plate**

When liquid crystal molecules are placed on the plate that has grooves in one direction, they align along the grooves.

Natural state



In the natural state, liquid crystals rest modestly along the axial direction of molecules in regular phase.

Liquid crystal's placed on the plate (orientation film) that has fine grooves arranged in one direction.

Liquid crystal molecules aligned along grooves.

Fig. 9-1

- When liquid crystal is sandwiched by two plates whose grooves are displaced 90 degrees, the liquid crystal molecules are twisted 90 degrees.

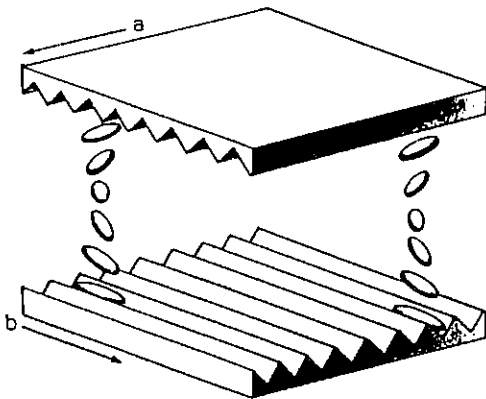


Fig. 9-2

Molecules "a" aligned to the top plate and "b" to the bottom plate, so that liquid crystal molecules are twisted 90 degrees within a layer. (TN type liquid crystal)

- (2) Voltage applied to liquid crystal changes optical course

- **Light advances along the slits molecules rest**
Light passing through twisted liquid crystal is also twisted.

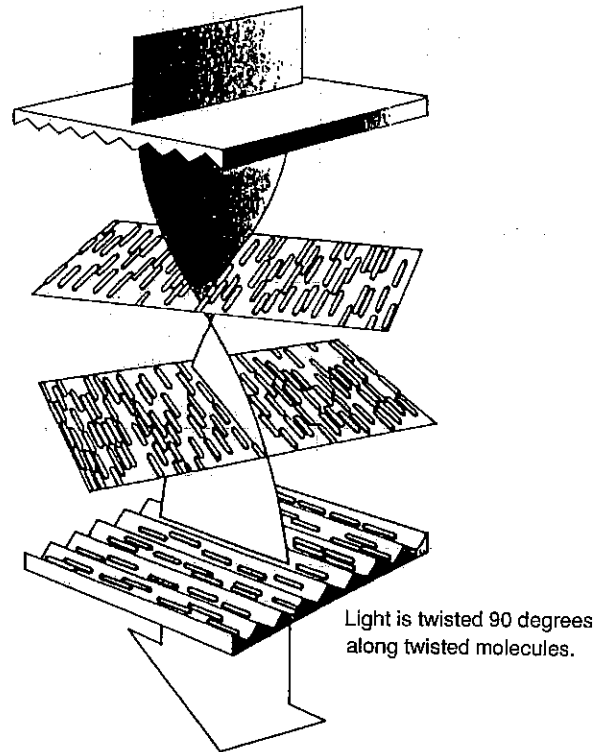


Fig. 9-3

When light is applied to liquid crystal, it moves along slits molecules are arranged. As shown in the above illustration, if molecules are arranged 90 degrees twisted, light also advances 90 degrees twisted.

- **Applying voltage changes molecule arrangements**

When voltage is applied to the twisted liquid crystal, light is released from twisting.

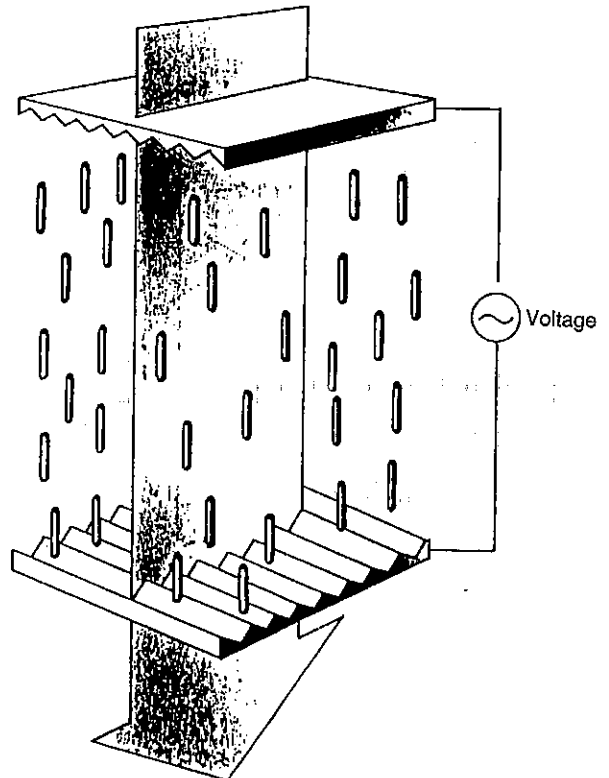


Fig. 9-4

Alignment of molecules is disturbed by applying voltage from an external source. When the voltage is applied, molecules change their direction towards the vertical direction or along an electric field. Light advances forward along the alignment of molecules.

(3) Theory of liquid crystal display

• Light obstructed using a combination of polarizing filters

When the combined two polarizing filters are placed between the twisted liquid crystal and voltage is applied, it becomes the liquid crystal display.

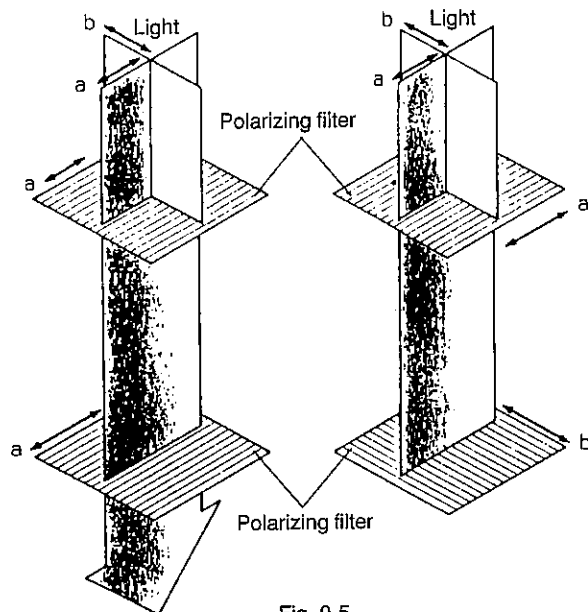
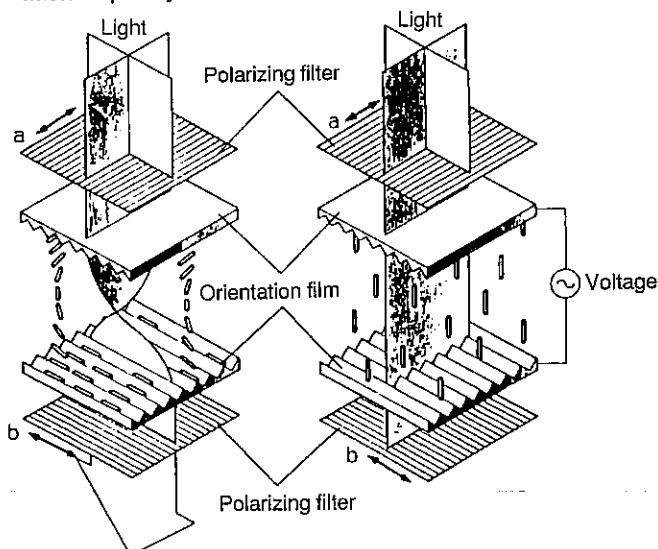


Fig. 9-5

- When two filters are set in the same polarizing direction as shown in the above figure, light passes through.
- When two filters are set in the direction light intersects as shown in the figure right, light is blocked.
- **Theory of NT type liquid crystal display**
A liquid crystal display can be made using polarizing filters and twisted liquid crystal.



Twisted liquid crystal is placed between two polarizing filters whose polarizing directions intersect to block light, the light from above is twisted 90 degrees along the slits of the liquid crystal so that light can pass through the filter placed below.

When voltage is applied, liquid crystal is released from twisting and set straight. The light from above advances down so that it cannot pass through the bottom filter. (Light is blocked)

Fig. 9-6

The illustration above shows an example of typical NT type liquid crystal. For the TN type, liquid crystal whose molecules are 90 degrees twisted are placed between two polarizing filters. When the voltage is not applied, the light passes through, but it appears black as the light is shut off when the voltage is applied. In other words, the voltage triggers the optical shutter.

1-2. Theory of color display

When a color filter is placed over a display phase, it becomes possible to display color. In the case of dot matrix device, three basic colors (red, green, blue) are filtered with the filter of respective color to form dots of red, green, or blue. Combination in this way allows to represent a variety of colors.

Display types

Incoming light or other light source coming from a lamp is used as the light source for the liquid crystal.

Depending on the relationship with the light source, the display type can be determined in one of the following three types.

1. Transparent type (liquid crystal display)
2. Reflect type (liquid display electronic calculator, liquid crystal clock)
3. Project type (liquid crystal projector)

■ Types

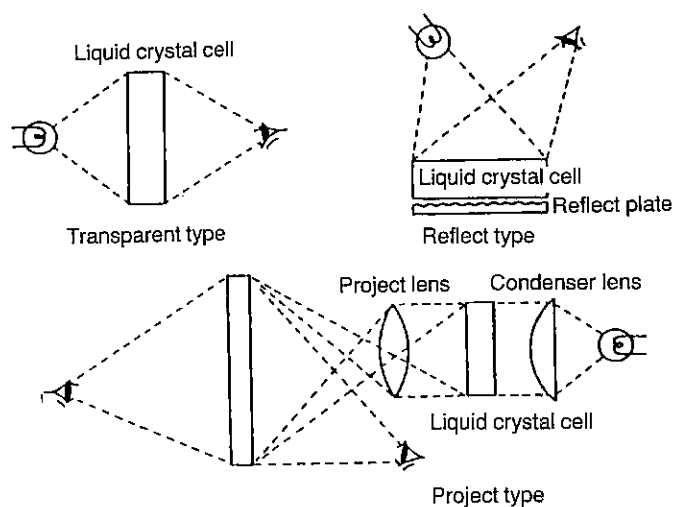


Fig. 9-7

1-3. Structure of liquid crystal display and how it is constructed

In this section, the structure of the liquid crystal display is discussed having a single matrix type as an example. Also discussed are material and creation method.

Structure of liquid crystal

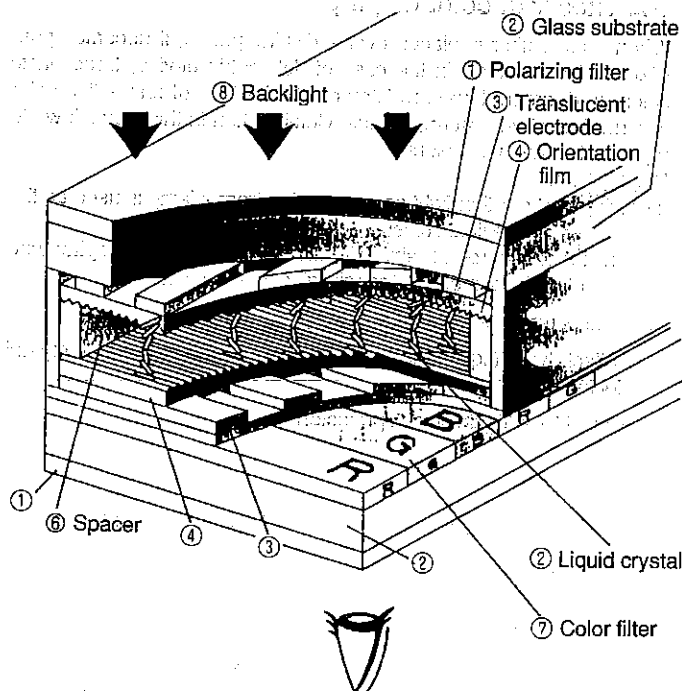


Fig. 9-8

• Sandwich like structure

The structure of the color liquid crystal display consists of elements form a sandwich.

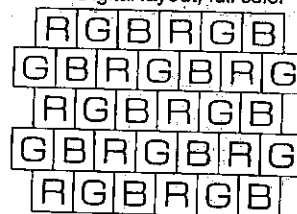
- ① Polarizing filter
Used to control incoming and outgoing light.
- ② Glass substrate
Used to prevent electricity at the electrode from leaking to other area.
- ③ Transparent electrode
This is the electrode used to drive the liquid crystal display. A highly transparent material is used to avoid display performance.
- ④ Orientation film
This film is used to arrange the liquid crystal molecules in one direction.
- ⑤ Liquid crystal
- ⑥ Spacer
Used to provide an even space to two glass substrates employed to hold the liquid crystal material.
- ⑦ Color filters
Color filters of red, green, blue are used to select colors.
- ⑧ Backlight
Light is projected from the back of the display to illuminate the display screen. For some of monochrome liquid crystal displays, the reflect plate is used in place of the backlight in order to be visible under natural light.

• Multi-color display because of the stripe layout

For the AV application display, full color representation is achieved using delta form of RGB colors. For the OA application, a stripe layout multi-color method is used in order to clearly display graphics and characters.

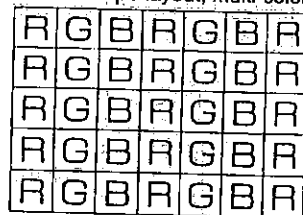
■ For AV application:

Digital layout, full color



■ For OA application:

Stripe layout, multi-color



1-4. TFT color liquid crystal display

An active matrix type color display unit is composed of amorphous silicon thin film transistors. It consists of a TFT color liquid crystal display panel, driver IC, control circuit, and power supply circuit. Using 9-bit data signal lines, three timing signal lines, +5V DC supply lines, and backlight power supply line, it will display 512 colors graphics on a 640 x 480 dots panel, though only 256 colors are supported by this machine because of display device. The panel housing is detachable as separately provided from the backlight for ease of machine servicing which allows to replace the lamp from the back of the unit.

1-5. Structure of TFT

The TFT color LCD is an active matrix driven LCD which means that a transistor or diode is used to each pixel so that a target pixel may be turned on and off as desired. The display which uses the transistor is a TFT (Thin Film Transistor) liquid crystal and the one which uses the diode is a MIM (Metal Insulator Metal) liquid crystal.

When the active element (transistor) provided to the X electrode is turned on and off, the active element in the on state keeps its voltage. When voltage is applied to the Y electrode, the target pixel is turned on.

Since the terminal connected to the switched X electrode is separated by the insulation layer, a high speed on and off action is possible

• Structure of the active matrix drive method (TFT)

■ View

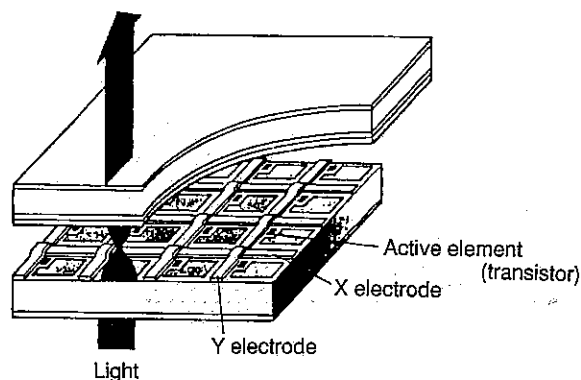


Fig. 9-9

2. Backlight inverter PWB

2-1. Outline

This backlight inverter PWB serves as the power source for lighting the backlight(CCFT backlight unit) and color TFT LCD with the AC adaptor and Nicd battery.

2-2. Specifications

(1) Input

AC adaptor input	
Rated voltage	DC 12.9V
Voltage fluctuation range	DC 12.2V-DC 14.2V
Battery input	
Rated voltage	DC 7.2V
Voltage fluctuation range	DC 6.0V-DC 9.6V

(2) Output

DC output	+5V	For color TFT LCD For CCFT Backlight
Output open voltage	1200 Vrms	
Tube voltage	400 Vrms	
Output current	5mA rms	

(3) Connector pin layout

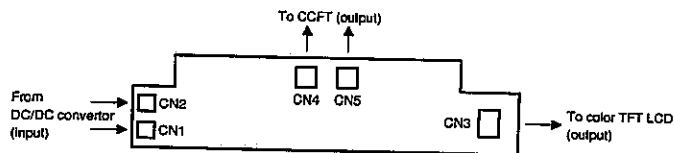


Fig. 9-14 Pin layout

• CN1

Pin No.	Name	Function	Input/Output
1	MDL	Backlight Brightness control	Input
2	BLOFF	Backlight On/Off control	Input
3	GND	—	—

• CN2

Pin No.	Name	Function	Input/Output
1	VBL	Backlight input voltage	Input
2	GND	—	—

• CN3

Pin No.	Name	Function	Input/Output
1	VBB	5V output	Output
2	VBB	5V output	Output
3	GND	—	—
4	GND	—	—
5	N.C	No connection	—

• CN4

Pin No.	Name	Function	Input/Output
1	GND	—	—
2	N.C	No connection	—
3	BLOUT	CCFT output	Output

2-3. Block diagram

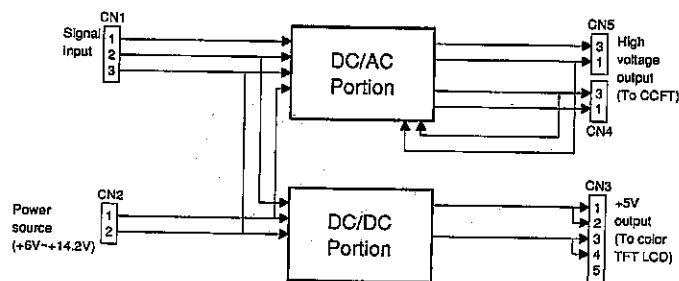


Fig 9-15. Block diagram

2-4. Operational description

(1) DC/DC conversion portion

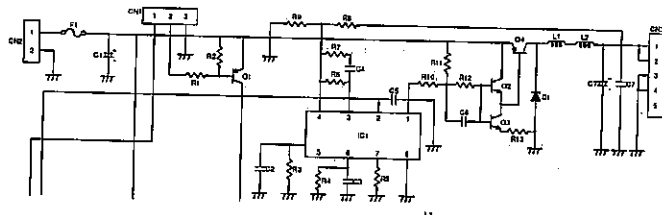


Fig. 9-16

Power supplied from connector CN2 Pin1 is transformed into high frequency power by Q4.(Q4 is turned on/off by the drive signal of IC1 to oscillated in 100KHz rectangular waveform.) Then high frequency power is stepped down by Q4,D1,L1 and L2 and smoothed by L1,L2 and C7 to make 5V DC output.

(2) DC/AC conversion portion

① High frequency swtting section and self excitement resonance section

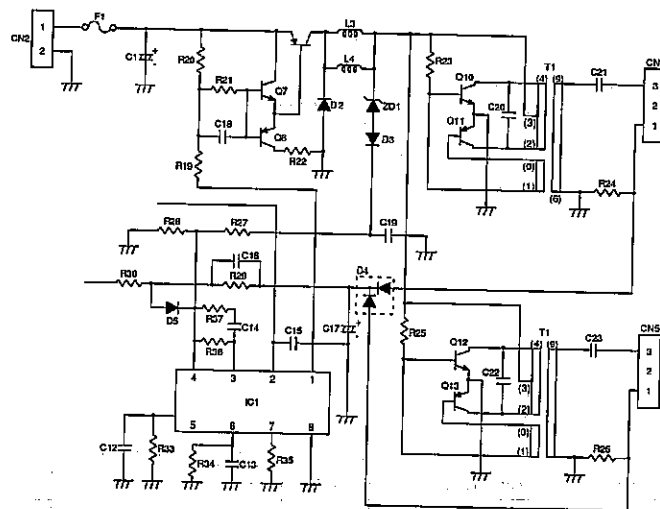


Fig. 9-17

Power supplied from connector CN2 Pin1 is transformed into high frequency power by Q9 and supplied to the self excitement resonance section.

Q9 is turned on/off by drive signal of IC2 to oscilate in 50KHz rectangular waveform.

IC2 detects the output current of the self excitement resonance section with resistors and controls ON width of Q9 to keep the current at a constant level.

The high frequency power transformed by the high frequency switching section is supplied to the self excitement resonance section. Q10 and Q11 (Q12 and Q13) oscillate in the frequency determined by T1(T2) inductance and the capacity of C20 and C21 (C22 and C23).

When Q10 and Q11 (Q12 and Q13) oscillate, a voltage of sine wave is induced in the primary winding of T1(T2), generating a voltage in the second winding.

C21(C23) is a ballast capacitor to limit a current flowing to the output, R24(R26) is a resistor to detect a current flowing to the output.

The current detected by R24(R26) is feed back through D4 to the control section.

② Control signal section

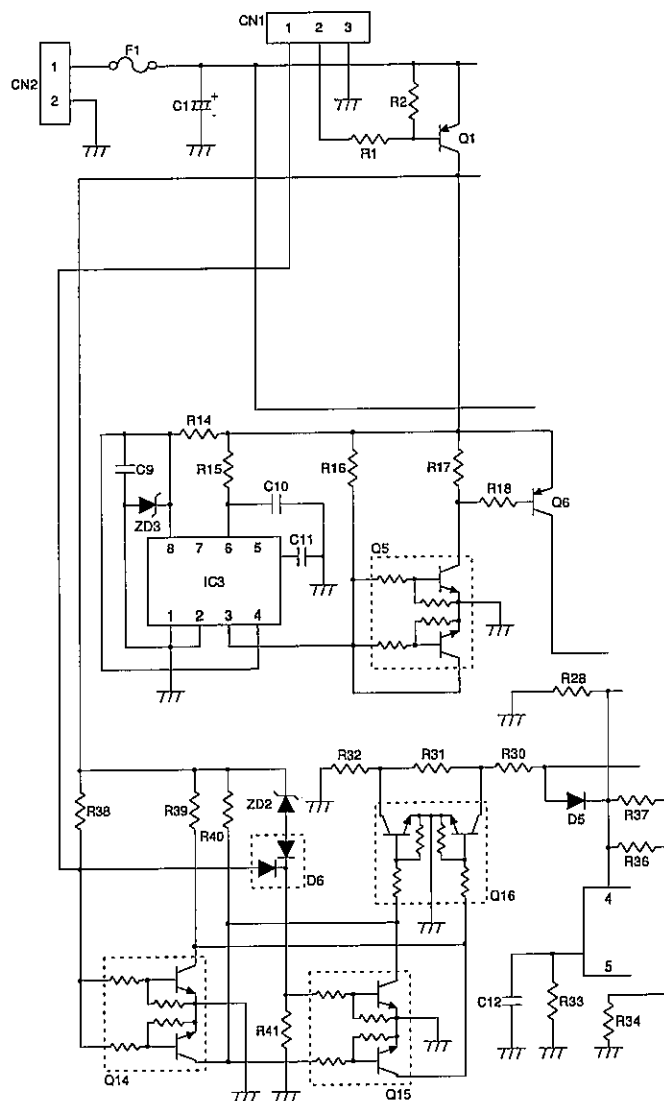


Fig. 9-18

- BLOFF signal coming from CN1 Pin2 turns on/off the backlight. When backlight is turned off, 5V output is also turned off.

H: Backlight On, 5V On

L: Backlight Off, 5V Off

When BLOFF is "H", Q1 and Q6 are turned off, then backlight and 5V output become off.

- MDL signal coming from CN1 Pin1 controls the brightness of the backlight.

Also the brightness of the backlight is related whether operated with the battery or AC adaptor. (Refer to the table below.)

MDL	Power source	CCFT tube current	Brightness
H	—	3mA	Low
L	Battery	5mA	Medium
	AC adaptor	6mA	High

Backlight brightness is determined with three resistors (R30, R31 and R32).

When MDL is "H", both transistor in Q14 are on both in Q16 are turned off.

So R30, R31 and R32 are connected to IC2 Pin4 through D5 makes brightness LOW.

When MDL is "L" and operated by battery, both transistor in Q14 are off and upper transistor in Q15 is off, lower is on.

Then, left side of transistor in Q16 is on and right side is off.

So R30 and R31 are connected makes brightness Medium.

When MDL is "L" and operated by AC adaptor, both transistor in Q14 are off lower transistor in Q15 is turned off.

So right side of transistor in Q16 is turned on and only R30 is connected to IC2 makes brightness High.

- Time delay circuit for backlight

To avoid the garbage display during the power on sequence, backlight circuit has certain time delay (about 150mS) between BLOFF is "H" and Backlight is turned on.

IC3 (Timer IC) is used for this purpose and when BLOFF becomes "H", output signal (IC3 Pin3) keeps "H" state for about 150mS (backlight stays off) then becomes "L" (backlight is turned on).

- Caution

Use the same type and ratings of fuse when replace.

Ratings: F1 ... 125V 2.5A

3. Backlight unit

3-1. Optical characteristics

The optical characteristics of the backlight unit are shown below:

Item	Code	Min.	Typ.	Max.	Unit	Remark
Brightness on the diffusion plate surface	Y _L		1.450		cd/m ²	(Reference value) * Note
Chroma on the diffusion plate surface	x	0.269	0.299	0.329		
	y	0.261	0.291	0.321		

* Note: The values are obtained by using inverter CXAM10L (12.0V input/output floating) made by TDK and the TOPCON brightness meter BM-7, and by measuring the brightness at the center of the backlight diffusion plate at an angle of 1 degree after 15 ~ 20 minutes from it's lighting.

3-2. Environmental conditions

Operating temperature: 0 ~ +50°C

Storage temperature: -25 ~ +60°C

3-3. Backlight unit replacement

Fig. 3-1 shows the replacement procedure of the backlight unit.

For replacement, follow the procedure below:

- (1) Extend five pawls ② of frame 1 ①, and remove frame 1.
- (2) Extend two pawls ④ of frame 2 ③, loosen four PWB fixing screws ⑤, and remove LCD panel ass'y ⑥.
Cushion ⑧ attached to backlight unit ⑦ may adhere tightly to the panel, insert tweezers between the panel right side and the cushion and remove it slowly.
Use finger sucks or gloves to avoid contaminating the LCD panel.
- (3) Remove the backlight unit (which is locked with four pawls) from frame 2, and replace it with a new one.
- (4) Attach the LCD panel in the reversed procedures of removal, and attach frame 1.
Be careful not to allow dust to enter between the LCD panel and the backlight.

No.	Product name	Quantity
1	Frame 1	1
2	Pawl	5
3	Frame 2	1
4	Pawl	2
5	M2 screw	4
6	Panel	1
7	Backlight unit	1
8	Cushion	4

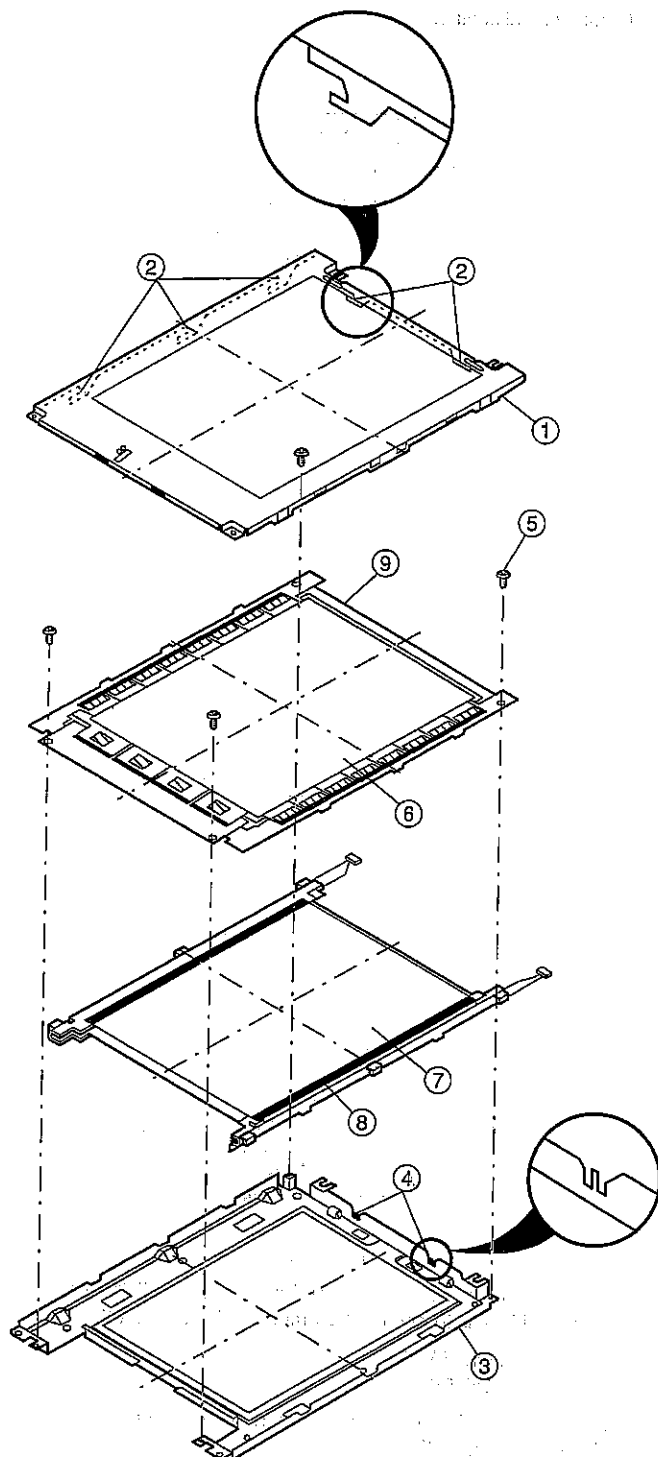
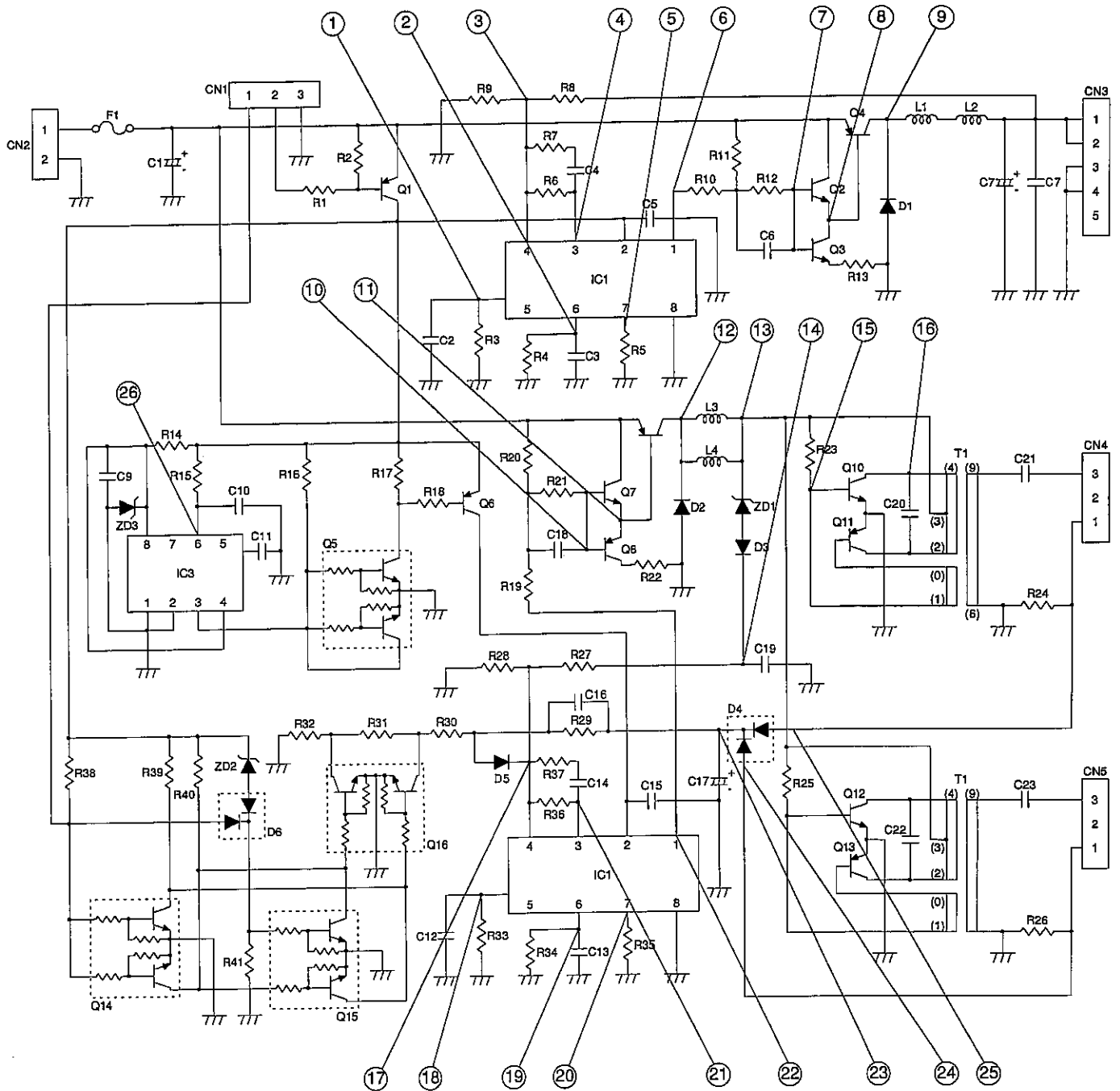
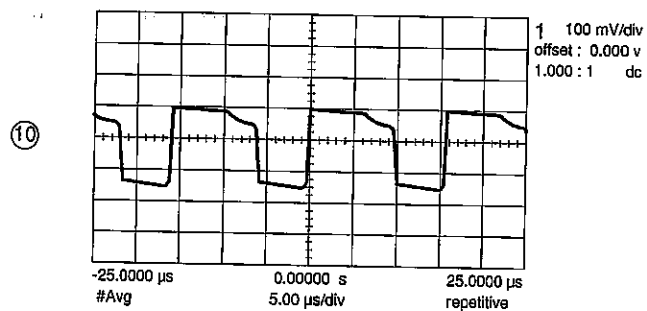
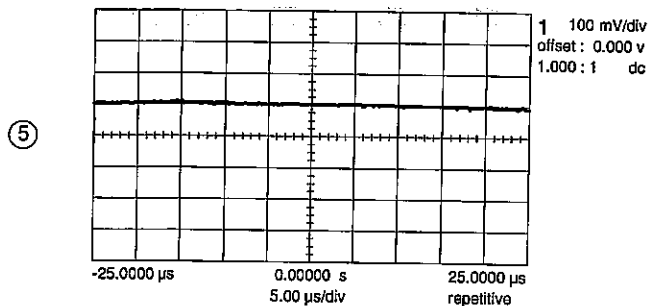
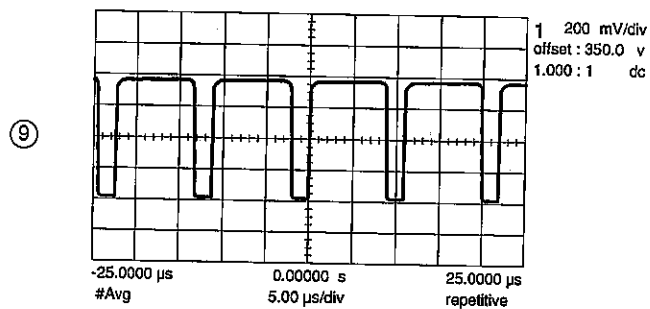
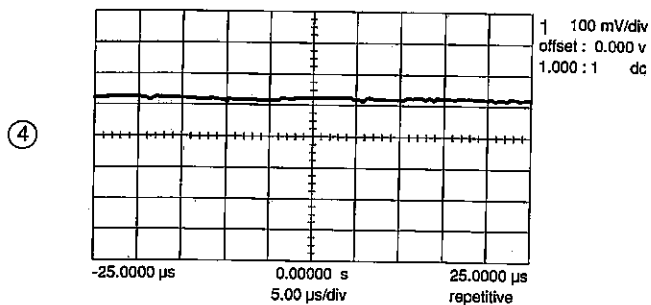
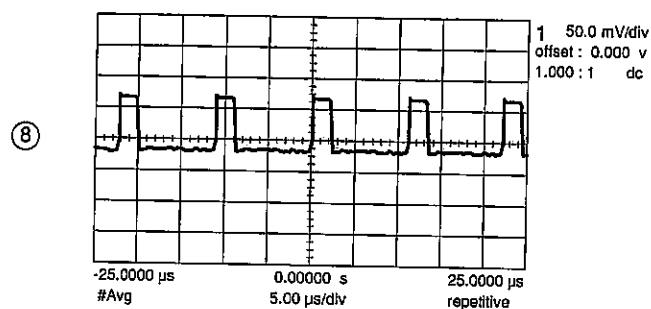
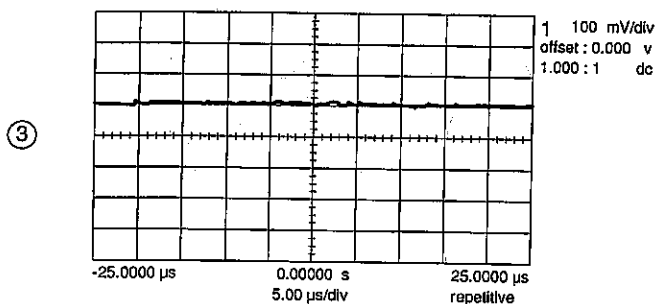
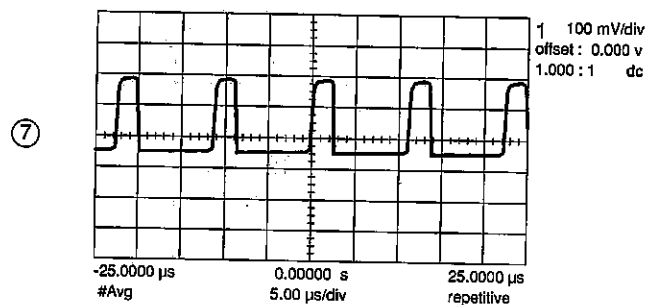
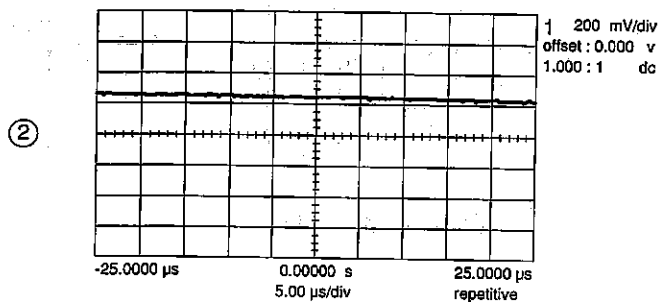
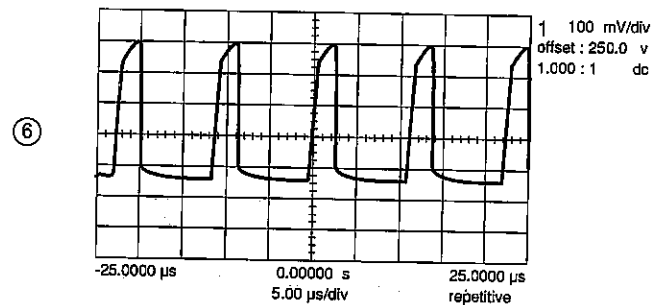
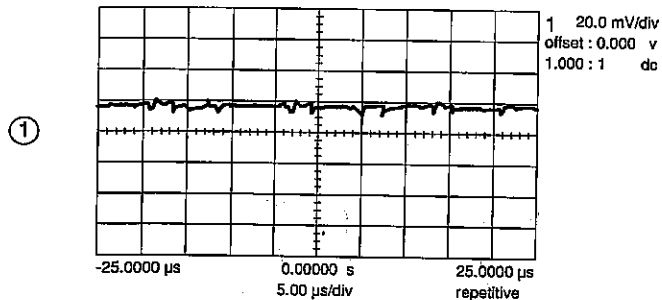
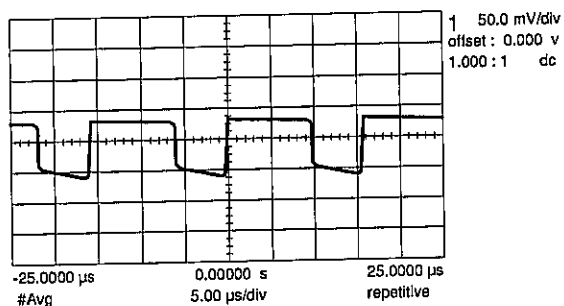


Fig. 3-1. Backlight unit replacement

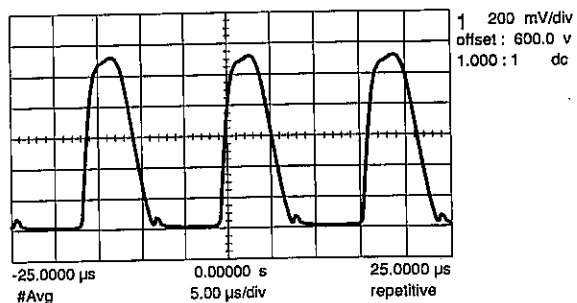




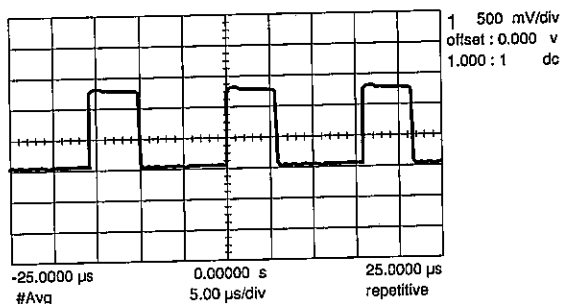
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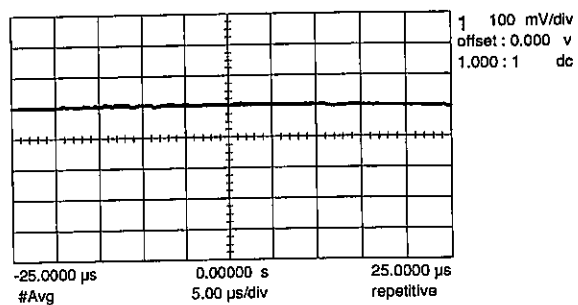
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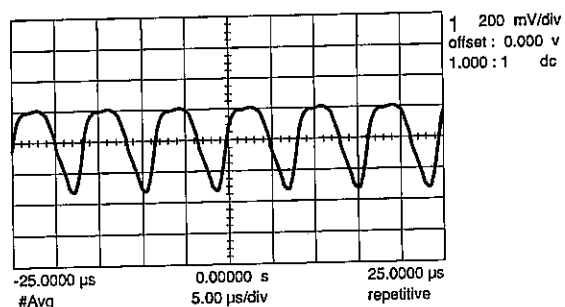
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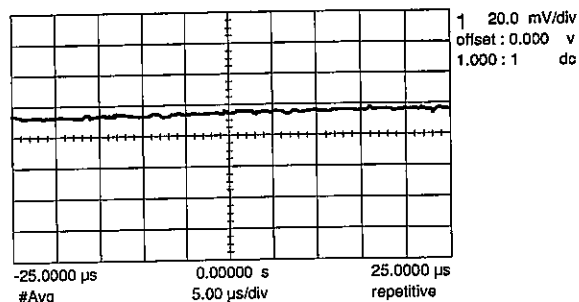
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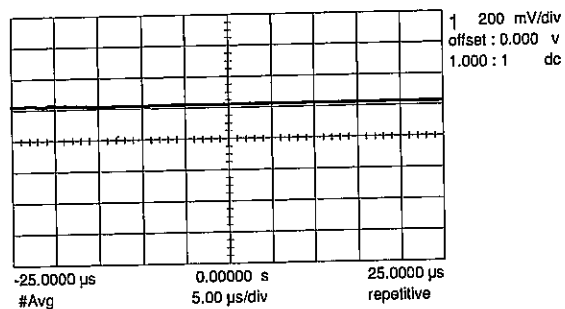
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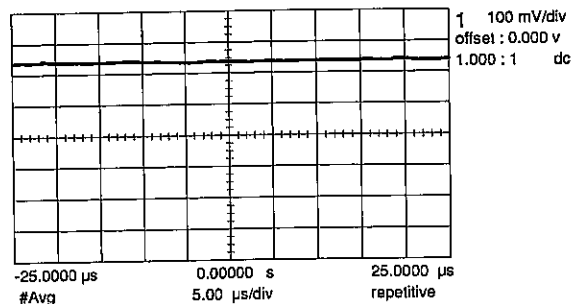
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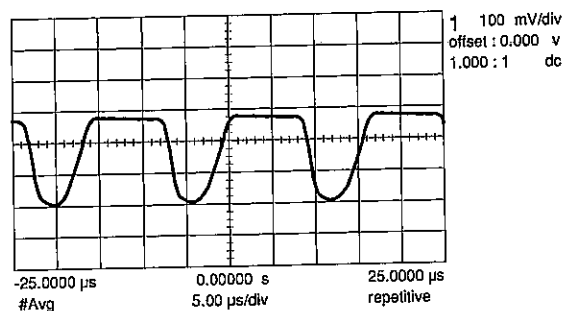
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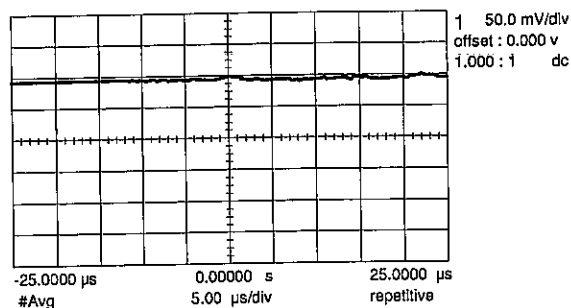
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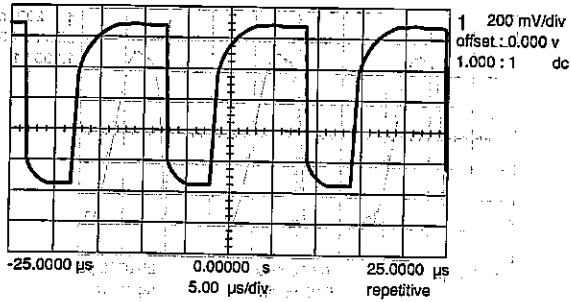
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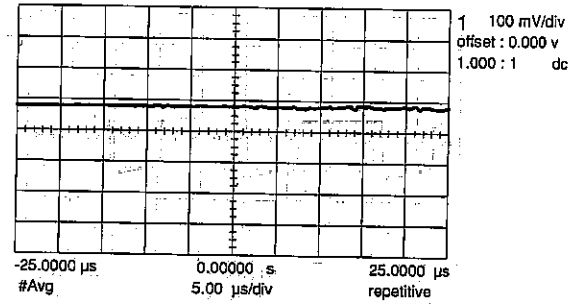
⑳



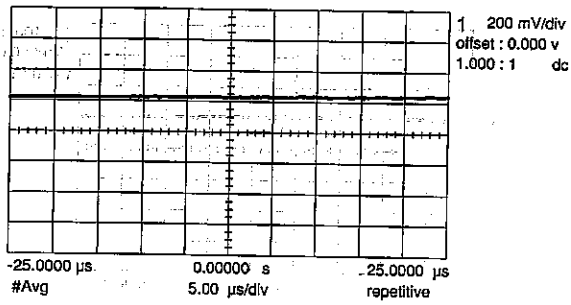
22



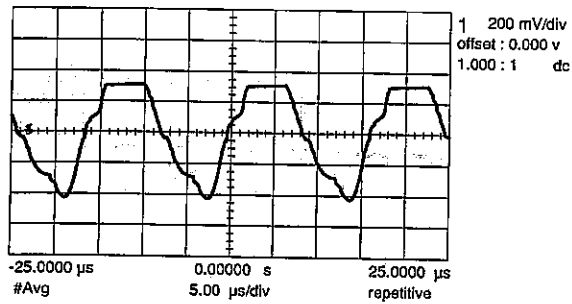
21



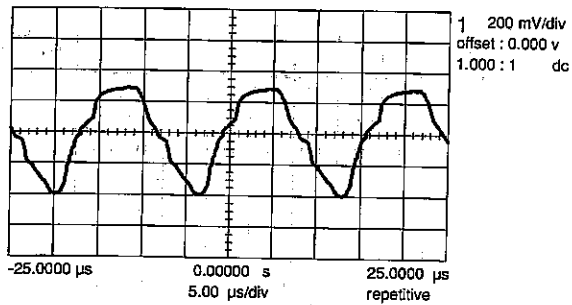
23



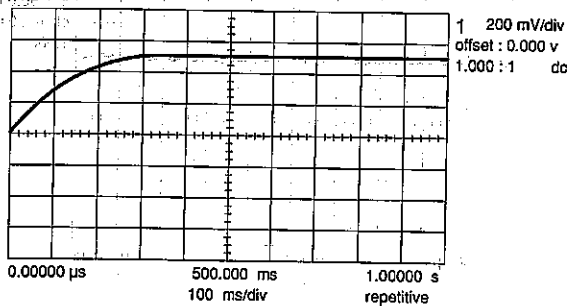
24



25



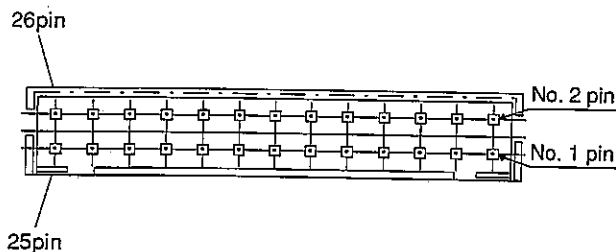
26



3-1. Signal descriptions

Signal name	Signal description
EGOD/EFB	•Informs that the Vcc voltage of expansion unit is normal. •Informs that the external battery is fully charged.
PONETB	Informs the external battery that the main power of the body is on.
PONEXP	Informs the expansion unit that the main power of the body is on.
CNEXP	Informs that the expansion unit is connected or not.
SPST	Informs that the set is in the suspend mode.
PLMP	Lights up the power LED.
CEB	Informs of connection of external batteries.
CB	Informs of connection of internal batteries.
PWRGD	Informs that Vcc voltage is normal.
PWRSW	Controls on/off of DC output.
CHGMD	Charges the internal batteries at medium speed.
FB	Informs of full charge of the batteries.
LB	Informs of discharge state of internal and external batteries.
BEEP	Drives the buzzer to show discharge of internal and external batteries.
PWROFF	turns off DC output.
CNETB	Informs that the external battery is connected or not.
VACO	Informs of connection of AC adapter.

Table. 10-1. Signal description table



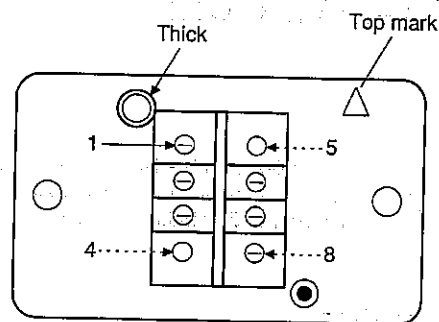
3-2. Connector pin arrangement

(1) CN1

Pin No.	Signal name
1	SPST
2	PLMP
3	PWRSW
4	PWROFF
5	BEEP
6	PWRGD
7	FB
8	LB
9	GND
10	CHGMD
11	CEB
12	CB
13	GND
14	GND
15	VBAT

Pin No.	Signal name
16	VBAT
17	N.C.
18	VACO
19	GND
20	Vbu
21	VDD
22	N.C.
23	GND
24	GND
25	VCC
26	VCC

(2) CN2



Pin No.	Circuit name
1	VACI
2	CNETB
3	VETB
4	GND
5	PONETB
6	EGOD/FEB
7	PONEXP
8	CNEXP

Pin No. corresponds to No. in Fig. 1, and is displayed in the rear of the connector.

4. Operational description

The DC/DC convertor is composed of PWB and aluminum shield plate fixed externally to it.

4-1. Input filter section

Fig. 4-1 shows the filter input section.

This is filter composed of C1, L1, and C2. The circuit is used to damp the input noise, unnecessary radiation inside the convertor, and conduction noise.

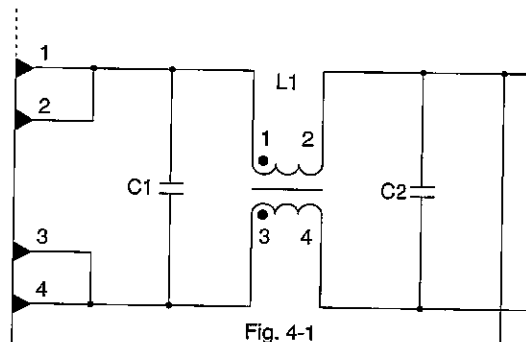


Fig. 4-1

4-2. 5V Vcc circuit

Fig. 2 shows the 5V Vcc circuit.

DC6V – 14.2V supplied from the AC adapter or the battery is dropped to 5V by switching to supply stable output of 5V. TR1 is switched at 90KHz by IC1 control signal to convert the DC input into a high frequency rectangular waveform then to rectify and smooth by DS2, L2 and C4.

To stabilize the output voltage, voltage is detected and divided by R20, R2, and VR1 and the divided voltage is inputted to IC1 comparison section. TR1 ON width is controlled by the drive signal whose error is amplified by the error amplifier in IC1 to stabilize the voltage. ON/OFF of Vcc is controlled by detecting input signal of CN1 by IC5.

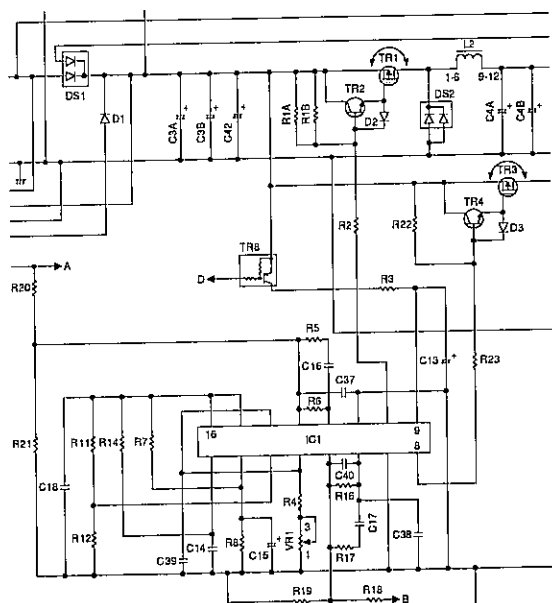


Fig. 4-2

4-3. 5V Vbu circuit

The output of three-terminal regulator IC3 is supplied to control IC (IC5) to obtain Vbu output.

Vbu output is used for CMOS and RTC backed up by battery.

4-4. 12V VDD₁ circuit

Fig. 4-3 shows the 12V VDD₁ circuit.

A DC input is boosted by TR3 switching and transformer T1, and reversed to supply stable outputs of +12V.

Similarly to the VCC circuit, TR3 is switched at about 90KHz with IC1 control signal to transform into high frequency rectangular waveform and to input to transformer T1. It is then smoothed and rectified by D4 and C7 in the 12V circuit in the output side of the transformer T1.

To stabilize the output voltage of the +12V circuit, the voltage detected by R18 and R19 is inputted to the comparison section of IC1 and ON width of TR3 is controlled by the drive signal whose error is amplified by error amplifier in IC1.

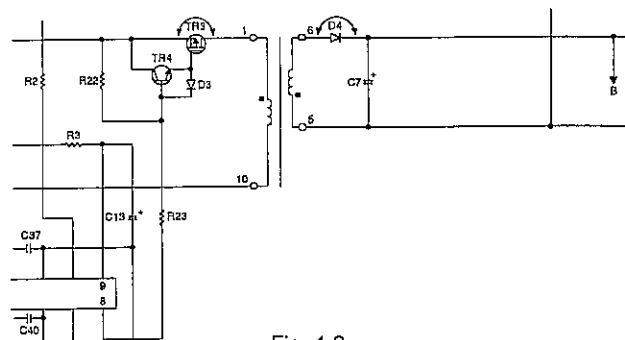


Fig. 4-3

4-5. VBL circuit

Fig. 4-4 shows the VBL circuit.

The VBL output is made in the input through circuit. (Diode or ed AC adaptor, Internal Battery and External Battery input.) F1, F2 and F3 are the fuse for protection against short.

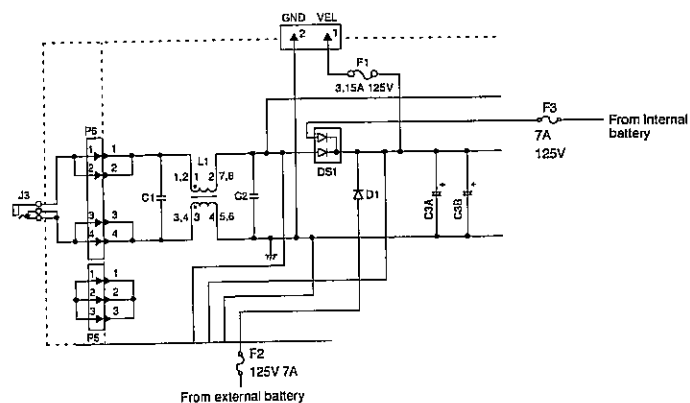


Fig. 4-4

4-6. Charge circuit

Fig. 4-5 shows the charge circuit.

Signal sent from the main PWB is received by IC5 to select among quick charge, standard charge, and trickle charge. Fig. 4-6 shows the charge circuit.

The quick charge circuit and the standard charge circuit switches TR5 at about 70KHz with IC2 control signal, DC current rectified and smoothed by D7, L4, and C23 charges the batteries. Battery conditions and signals from the body are detected by IC5 to control battery charging.

The trickle charge circuit supplies a current to the batteries through R24.

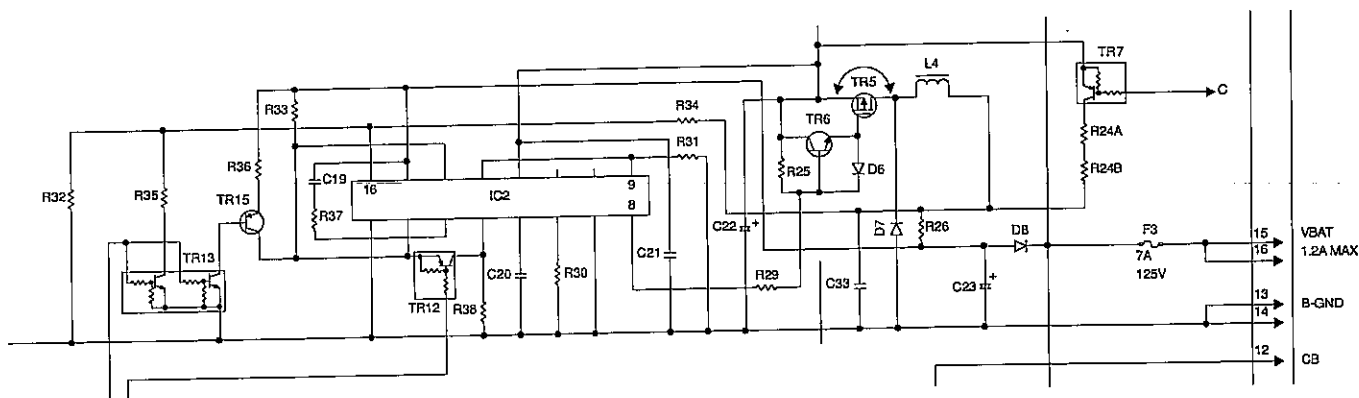
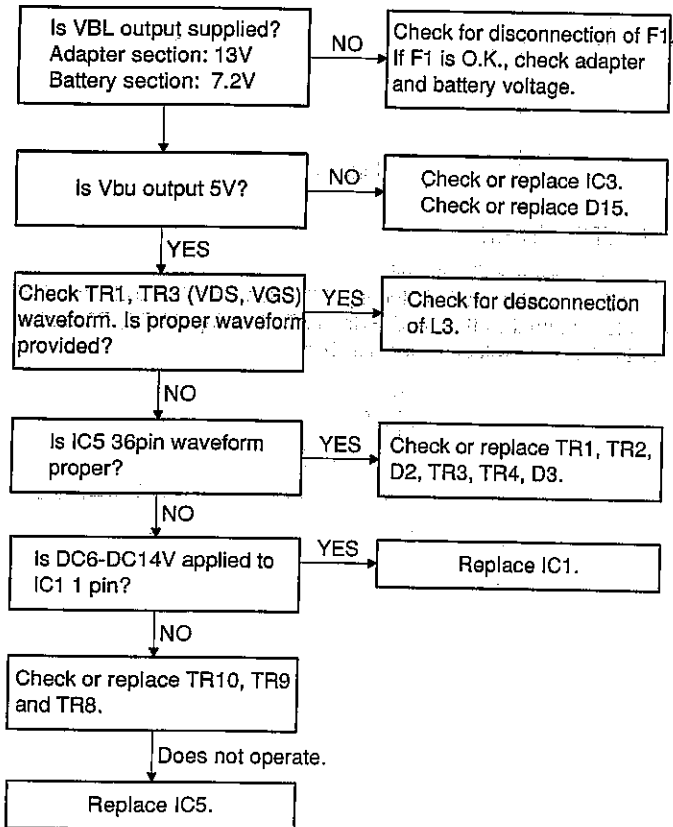


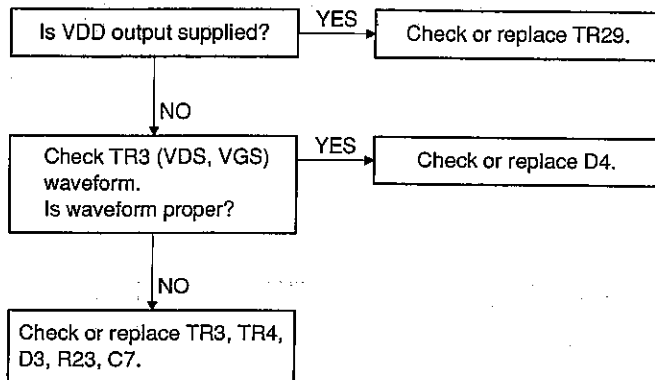
Fig. 4-5

5. Troubleshooting

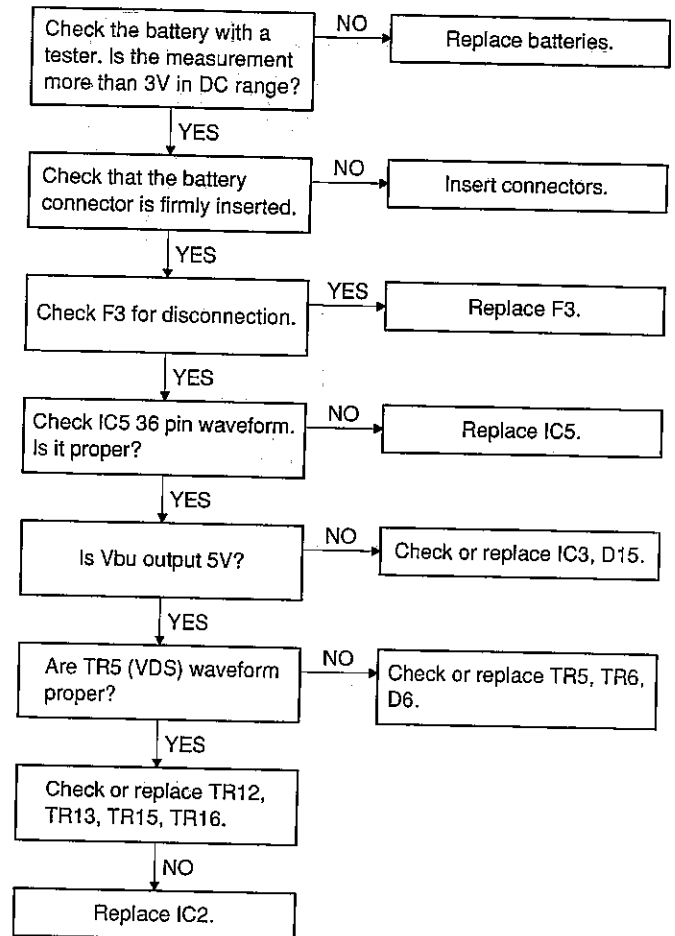
5-1. Vcc output is not supplied when SW is turned on.



5-2. Vcc is supplied but terminated soon.



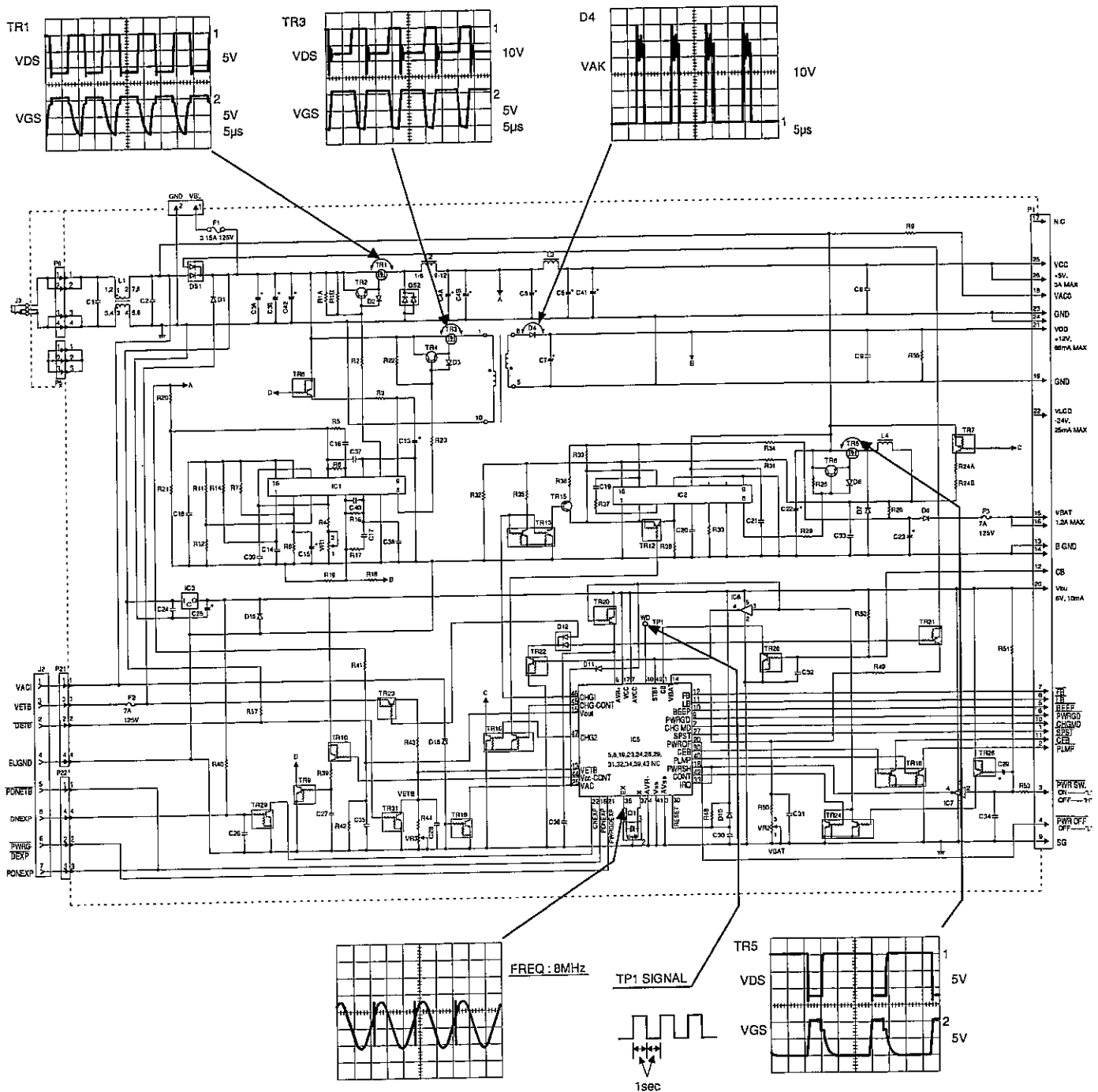
5-3. Battery charge is not performed.



● Caution

Use the same type and ratings of fuse when replace.

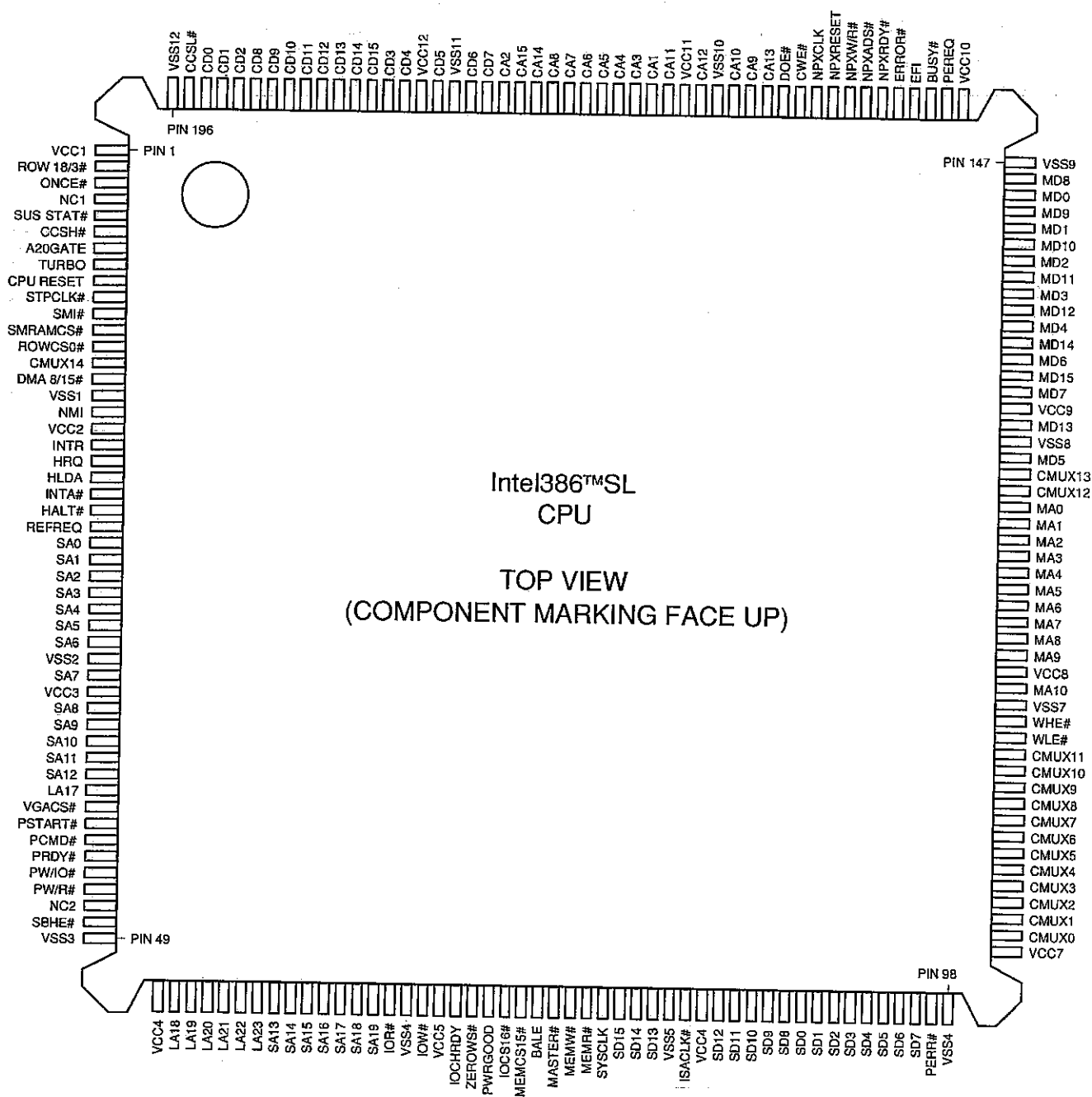
Ratings: F1 ... 125V 3.15A
F2 ... 125V 7A
F3 ... 125V 7A



CHAPTER 11. DESCRIPTION OF LSI

1. 80386SL MICROPROCESSOR

1-1. Pin configuration



1-2. Pin table

Signal Name	PQFP Pin #	Type	Term	Drive IoL, IoH	Load Min, Max	Susp	Stpck	ONCE
A20GATE	A007	I	20K			Tri	Pd	Tri
BALE	A073	O	Hold	24, 4	50, 240	Hold	Drv	Hold
BUSY #	A150	I	60K			Tri	Pu	Tri
CA1	A167	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA2	A176	O	Hold	4, 2	15, 60	Hold	Drv	Hold
CA3	A168	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA4	A169	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA5	A170	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA6	A171	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA7	A172	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA8	A173	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA9	A161	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA10	A162	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA11	A166	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA12	A164	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA13	A160	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA14	A174	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CA15	A175	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CCSH#	A006	O	Hold	4, 2	20, 35	Hold	Drv	Hold
CCSL#	A195	O	Hold	4, 2	20, 35	Hold	Drv	Hold
CD0	A194	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD1	A193	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD2	A192	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD3	A183	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD4	A182	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD5	A180	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD6	A178	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD7	A177	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD8	A191	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD9	A190	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD10	A189	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD11	A188	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD12	A187	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD13	A186	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD14	A185	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CD15	A184	IO	Hold	4, 2	20, 50	Hold	Drv	Hold
CMUX0	A100	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX1	A101	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX2	A102	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX3	A103	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX4	A104	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX5	A105	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX6	A106	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX7	A107	O	Hold	4, 2	15, 72	Hold(1)	Drv	Hold
CMUX8	A108	O	Hold	4, 2	32, 144	Hold(1)	Drv	Hold
CMUX9	A109	O	Hold	4, 2	32, 144	Hold(1)	Drv	Hold
CMUX10	A110	O	Hold	4, 2	32, 144	Hold(1)	Drv	Hold
CMUX11	A111	O	Hold	4, 2	32, 144	Hold(1)	Drv	Hold
CMUX12	A127	O	Hold	4, 2	8, 32	Hold	Drv	Hold
CMUX13	A128	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
CMUX14	A014	O	Hold	4, 2	20, 65	Hold	Drv	Hold
COE#	A159	O	Hold	4, 2	15, 45	Hold	Drv	Hold
CPURESET	A009	I	20K			Actv	Pd	Tri
CWE#	A158	O	Hold	4, 2	15, 45	Hold	Drv	Hold
DMA8/16#	A015	I	60K			Tri	Pu	Tri
EFI	A151	I				Actv		
ERROR#	A152	I	60K			Tri	Pu	Tri
HALT#	A023	O	Hold	4, 2	20, 65	Hold	Drv	Hold
HLDA	A021	O	Hold	4, 2	20, 65	Hold	Drv	Hold

Signal Name	PQFP Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	Stpck	ONCE
HRQ	A020	I	20K			Tri	Pd	Tri
INTA#	A022	O	Hold	4, 2	20, 65	Hold	Drv	Hold
INTR	A019	I	20K			Tri	Pd	Tri
IOCHRDY	A068	IO	1K	24, 4	50, 240	Tri	Pu	Tri
IOCS16#	A071	IO	1K	24, 4	50, 240	Tri	Pu	Tri
IOR#	A064	IO	60K	24, 4	50, 240	Tri	Pu	Tri
IOW#	A065	IO	60K	24, 4	50, 240	Tri	Pu	Tri
ISACLK2	A082	I						
LA17	A040	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA18	A051	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA19	A052	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA20	A053	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA21	A054	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA22	A055	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
LA23	A056	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
MA0	A126	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA1	A125	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA2	A124	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA3	A123	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA4	A122	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA5	A121	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA6	A120	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA7	A119	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA8	A118	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA9	A117	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MA10	A115	O	Hold	4, 2	32, 288	Hold(1)	Drv	Hold
MASTER#	A074	I	1K			Tri	Pu	Tri
MD0	A145	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD1	A143	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD2	A141	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD3	A139	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD4	A137	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD5	A129	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD6	A135	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD7	A133	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD8	A146	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD9	A144	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD10	A142	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD11	A140	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD12	A138	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD13	A131	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD14	A136	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MD15	A134	IO	Hold	4, 2	8, 32	Hold	Drv	Hold
MEMCS16#	A072	IO	1K	24, 4	50, 240	Tri	Pu	Tri
MEMR#	A076	IO	60K	24, 4	20, 240	Tri	Pu	Tri
MEMW#	A075	IO	60K	24, 4	20, 240	Tri	Pu	Tri
NMI	A017	I	20K			Tri	Pd	Tri
NPXADS#	A154	O	Hold	4, 2	20, 32	Hold	Drv	Hold
NPXCLK	A157	O	Hold	4, 2	20, 40	Hold	Drv	Tri
NPXRDY#	A153	I	20K			Tri	Pd	Tri
NPXRESET	A156	O	Hold	4, 2	20, 32	Hold	Drv	Hold
NPXW/R#	A155	O	Hold	4, 2	20, 32	Hold	Drv	Tri
ONCE#	A003	I	60K			Tri	Pu	Actv
PCMD#	A043	O	Hold	4, 2	20, 65	Hold	Drv	Hold
PEREQ	A149	I	20K			Tri	Pd	Tri
PERR#	A097	O	Hold	4, 2	8, 32	Hold	Drv	Hold
PM/IO#	A045	O	Hold	4, 2	20, 65	Hold	Drv	Hold
PRDY#	A044	I	60K			Tri	Pu	Tri
PSTART#	A042	O	Hold	4, 2	20, 65	Hold	Drv	Tri
PW/R#	A046	O	Hold	4, 2	20, 65	Hold	Drv	Hold
PWRGOOD	A070	I				Actv	Actv	Tri

Signal Name	PQFP Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	Stpck	ONCE
REFREQ	A024	I	Hold			Actv	Actv	Tri
ROM16/8#	A002	I	60K			Tri	Pu	Tri
ROMCS0#	A013	O	Hold	4, 2	20, 65	Hold	Drv	old
SA0	A025	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA1	A026	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA2	A027	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA3	A028	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA4	A029	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA5	A030	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA6	A031	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA7	A033	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA8	A035	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA9	A036	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA10	A037	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA11	A038	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA12	A039	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA13	A057	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA14	A058	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA15	A059	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA16	A060	IO	Hold	24, 4	50, 240	Hold	Drv	Hold
SA17	A061	O	Hold	24, 4	50, 240	Hold	Drv	Hold
SA18	A062	O	Hold	24, 4	50, 240	Hold	Drv	Hold
SA19	A063	O	Hold	24, 4	50, 240	Hold	Drv	Hold
SBHE#	A048	IO	Hold	24, 4	20, 240	Hold	Drv	Hold
SD0	A089	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD1	A090	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD2	A091	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD3	A092	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD4	A093	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD5	A094	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD6	A095	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD7	A096	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD8	A088	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD9	A087	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD10	A086	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD11	A085	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD12	A084	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD13	A080	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD14	A079	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SD15	A078	IO	60K	24, 4	50, 240	Tri	Pu	Tri
SIM#	A011	I	60K			Tri	Pu	Tri
SMRAMCS#	A012	O	Hold	4, 2	20, 65	Drv	Drv	Hold
STPCLK#	A010	I	60K			Tri	Pu	Tri
SUS_STAT#	A005	I	60K			Actv	Actv	Tri
SYSCLK	A077	O	Hold	4, 2	20, 120	Hold	Drv	Hold
TURBO	A008	I	60K			Tri	Pu	Tri
VGACS#	A041	O	Hold	4, 2	20, 65	Hold	Drv	Hold
WHE#	A113	O	Hold	4, 2	15, 144	Hold(2)	Drv	Hold
WLE#	A112	O	Hold	4, 2	15, 144	Hold(2)	Drv	Hold
ZEROWS#	A069	I	1K			Tri	Pu	Tri

Power Pins

Vcc POFF: A001, A018, A034, A050, A067, A063, A099, A116, A132, A148, A165, A181

Vss POFF: A016, A032, A049, A065, A061, A096, A114, A130, A147, A163, A179, A196

No Connects

PQFP: A004, A047

NOTE 1: These pins are driven in suspend state if suspend refresh is enabled.

NOTE 2: These pins are driven inactive in the suspend state if suspend refresh is enabled.

Table 1-1 Pin characters

1-3. SIGNAL DESCRIPTIONS

Intel386™ SL Microprocessor

The following table provides a brief description of the signals of the Intel386 SL CPU. Signal names which end with the character "#" indicate that the corresponding signal is low when active.

Symbol	Name and Function																								
A20GATE	A20 Gate: This active HIGH input signal controls the Intel386 SL CPU A20 address line. When LOW this signal forces the Intel386 SL CPU to mask off (force LOW) the internal physical address signal A20. When this signal is HIGH, A20 is available on the System Address (SA) bus. When A20 gate is LOW this allows emulation of the 8086 1 Mbyte address "wrap-around".																								
BALE	Bus Address Latch Enable (ISA bus signal): This active HIGH output signal is used for two purposes. BALE is used to latch the address lines on the LA bus (LA17 ~ LA23) on the falling edge of BALE. BALE is also used to qualify ISA bus cycles for signals on the Peripheral Interface (PI) bus (PM/IO# and PW/R#). On the falling edge of BALE, PM/IO# and PW/R# can be sampled to determine the type of ISA bus cycle that is going to occur. BALE may be used to qualify and generate buffered control and status signals to the ISA expansion bus. The PI bus signal decoding is as follows: <table><tr><th>Type of Bus Cycle</th><th>PM/IO#</th><th>PW/R#</th></tr><tr><td>Memory Read</td><td>1</td><td>0</td></tr><tr><td>Memory Write</td><td>1</td><td>1</td></tr><tr><td>I/O Read</td><td>0</td><td>0</td></tr><tr><td>I/O Write</td><td>0</td><td>1</td></tr><tr><td>Interrupt Acknowledge</td><td>0</td><td>1</td></tr><tr><td>HALT (address = 2)*</td><td>1</td><td>1</td></tr><tr><td>Shutdown (address = 0)*</td><td>1</td><td>1</td></tr></table> *Note that BALE is not generated for these cycles, however the PM/IO# and PW/R# will reflect these states during HALT and Shutdown bus cycles where BALE is driven in typical ISA bus systems. Memory read/write, IO read/write and interrupt/interrupt acknowledge cycles correspond to the standard ISA bus cycle.	Type of Bus Cycle	PM/IO#	PW/R#	Memory Read	1	0	Memory Write	1	1	I/O Read	0	0	I/O Write	0	1	Interrupt Acknowledge	0	1	HALT (address = 2)*	1	1	Shutdown (address = 0)*	1	1
Type of Bus Cycle	PM/IO#	PW/R#																							
Memory Read	1	0																							
Memory Write	1	1																							
I/O Read	0	0																							
I/O Write	0	1																							
Interrupt Acknowledge	0	1																							
HALT (address = 2)*	1	1																							
Shutdown (address = 0)*	1	1																							
BUSY#	BUSY: This active LOW input signal indicates a busy condition a math co-processor (MCP).																								
CA [15:1]	Cache Address Bus: This is the address bus output used to select the memory cell in the cache memory. The CA2 signal is also connected to the CMD0# input of the MCP indicating Opcode (when high) or Data (when low) during a write cycle and control/status register (high) or data register (low) during a read. CA2 is used to address the upper or lower DWORD port of the MCP.																								
CCSH#	Cache Chip Select High Byte: This active LOW output is used to enable the upper byte of the cache SRAMs. This signal should be connected to the upper byte cache SRAM chip-select input.																								
CCSL#	Cache Chip Select Low Byte: This active LOW output is used to enable the lower byte of the cache SRAMs. This signal should be connected to the lower byte cache SRAM chip-select input.																								
CD[15:0]	Cache Data Bus: This is the bi-directional data bus used to transfer data between the cache SRAMs and the Intel386 SL CPU. The Cache Data bus is also used to transfer data between the MCP and the Intel386 SL CPU.																								
CMUX0 (CASL3#/ DIR)	CPU Multiplexed Pin Zero: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASL3#" and should be connected to the lower byte of DRAM bank 3 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as an SRAM controller this signal becomes the direction control (DIR) and should be connected to the direction control input of the SRAM data transceiver.																								
CMUX1 (CASH3#/ LE)	CPU Multiplexed Pin One: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASH3#" and should be connected to the upper byte of DRAM bank 3 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this signal becomes "LE" and should be connected to the latch enable input of the SRAM address latch. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".																								
CMUX2 (CASL2#/ DEN3#)	CPU Multiplexed Pin Two: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL2#" and should be connected to the lower byte of DRAM bank 2 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN3#" and should be connected to the data transceiver enable input for bank 3 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".																								
CMUX3 (CASH2#/ DEN2#)	CPU Multiplexed Pin Three: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH2#" and should be connected to the upper byte of DRAM bank 2 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN2#" and should be connected to the data transceiver enable input for bank 2 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".																								
CMUX4 (CASL1#/ DEN1#)	CPU Multiplexed Pin Four: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL1#" and should be connected to the lower byte of DRAM bank 1 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1#" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".																								

Symbol	Name and Function
CMUX5 (CASH1#/ DEN1#)	CPU Multiplexed Pin Five: This output signal has two functions. When the Intel386SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH1#" and should be connected to the upper byte of DRAM bank 1 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1#" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX6 (CASL0#/ DEN0#)	CPU Multiplexed Pin Six: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL0#" and should be connected to the lower byte of DRAM bank 0 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN0#" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX7 (CASH0#/ DEN0#)	CPU Multiplexed Pin Seven: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH0#" and should be connected to the upper byte of DRAM bank 0 CAS# input. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN0#" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX8 (RAS3#/ CE3#)	CPU Multiplexed Pin Eight: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS3#" and should be connected to the upper and lower byte of DRAM bank 3 RAS# inputs. When the Intel386 SL CPU Memory controller Unit is configured as a SRAM controller then this pin becomes "CE3#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 3 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX9 (RAS2#/ CE2#)	CPU Multiplexed Pin Nine: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS2#" and should be connected to the upper and lower byte of DRAM bank 2 RAS# inputs. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE2#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 2 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX10 (RAS1#/ CE1#)	CPU Multiplexed Pin Ten: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS1#" and should be connected to the upper and lower byte of DRAM bank 1 RAS# inputs. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE1#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX11 (RAS0#/ CE0#)	CMU Multiplexed Pin Eleven: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS0#" and should be connected to the upper and lower byte of DRAM bank 0 RAS# inputs. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE0#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX12 (PARL/ OLE#)	CPU Multiplexed Pin Twelve: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARL" and should be connected to the lower byte of DRAM bank 0 data parity bit. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OLE#" and should be connected to the lower byte of the SRAM output enable input of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX13 (PARH/ OHE#)	CPU Multiplexed Pin Thirteen: This output signal has two functions. When the Intel386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARH" and should be connected to the upper byte of DRAM bank 0 data parity bit. When the Intel386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OHE#" and should be connected to the upper byte of the SRAM output enable input of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX14 (ROMCS1#/ FLSHDCS#)	CPU Multiplexed Pin 14: This output signal has two functions. The Intel386 SL CPU can be configured to use this pin as either a BIOS ROM chip-select (ROMCS1#), or a FLASH disk chip-select signal (FLSHDCS#). In either case, the signal is driven LOW when an access to the selected interface occurs.

Symbol	Name and Function
COE#	Cache Output Enable: This active LOW output signal is used to indicate a read access to the CACHE SRAMs, and is used to enable the cache SRAMs' output buffers. This signal should be connected to the output enable signals of the upper and lower byte cache SRAMs.
CPURESET	CPU Reset: This active HIGH input forces the Intel386 SL CPU to execute a reset to the internal CPU core and state machines. The configuration registers are not reset.
CWE#	Cache Write Enable: This active LOW output is used to indicate write (LOW) access to the cache SRAMs. This signal should be connected to the write enable signal of the upper and lower cache SRAMs.
DMA8/16#	DMA 8-bit or 16-bit Cycle: This input, in conjunction with HRQ, indicates to 386 SL CPU if an 8-bit or 16-bit DMA access is occurring. If an 8-bit DMA access is occurring, the Intel386 SL CPU will swap the upper byte of data to the lower data byte for upper byte accesses.
EFI	External Frequency Input: This is an oscillator input. This clock controls all CPU core and memory controller timings and is equal to twice the desired processor frequency.
ERROR#	Numerics ERROR: This active LOW input to the Intel386 SL CPU is generated from a math co-processor (MCP). It also indicates to the 82360SL that an unmasked exception has occurred in the MCP. ERROR# is provided to allow numerics error handling compatible with the ISA bus compatible Personal Computer.
HALT#	HALT: This active LOW output indicates to external devices that the Intel386 SL CPU has executed a HALT instruction (address = 2) or a shutdown condition (address = 0). This can be used as an indicator for devices to assert the STPCLK# signal.
HLDA	HoLD Acknowledge: This active HIGH output indicates to external devices that the Intel386 SL CPU has relinquished control of the ISA bus. At this time the Intel386 SL CPU has floated the address and control signals of the ISA bus.
HRQ	Hold ReQuest: This active HIGH input indicates to the Intel386 SL CPU that an external device wishes to take control of the ISA bus.
INTA#	INTerrupt Acknowledge: This active LOW output indicates that the Intel386 SL CPU is executing an interrupt acknowledge bus cycle. During this process an external interrupt device will pass an interrupt vector to the Intel386 SL CPU.
INTR	Interrupt Request: This active HIGH input indicates to the Intel386 SL CPU that an external device is requesting the execution of an interrupt service routine.
IOCHRDY	I/O Channel ReaDY: This active HIGH input indicates that the I/O Channel, (ISA expansion bus), is ready to terminate the bus cycle. The ISA expansion bus is a normally ready bus and IOCHRDY is active HIGH. When an ISA bus peripheral needs to extend the standard 3 SYSClk, 16-bit ISA bus cycle the peripheral device asserts IOCHRDY LOW.
IOCS16#	I/O Chip Select 16: This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit I/O cycle. This signal has an active pull-up, when not driven the default I/O bus cycle is 8 bits.
IOR#	I/O Read: This active LOW signal indicates that the ISA bus is executing an I/O read cycle.
IOW#	I/O Write: This active LOW signal indicates that the ISA bus is executing an I/O write cycle.
ISACK2	ISA Clock Two: This is an oscillator input. This clock controls all of the ISA bus timings and is equal to twice the SYSClk frequency. Normally the ISA bus SYSClk is 8 MHz, and the ISACK2 oscillator is 16 MHz.
LA[23:17]	Latchable local Address bus: This is the unlatched local address of the ISA bus for access to memory above 1 megabyte. The LA bus is also used by the Peripheral Interface (PI) Bus.
MA[10:0]	Memory controller Multiplexed Address bus: This is the address bus output for the Memory Controller Unit. The 22-bit address is output in a row/column fashion for both DRAM and SRAM memory subsystems. The Memory Controller Unit places the ROW address out first and qualifies it by the RAS# signal going active in DRAM mode or the LE signal going active in the SRAM mode. The column address is then placed on the Memory Address bus and is qualified by the CASX# signals going active for the DRAM mode. This pin is disabled when SUS_STAT# is active (LOW). when the pin is disabled the output is sustained at the previous state by internal "keepers".
MASTER#	Master: This active LOW input indicates that an ISA bus peripheral is controlling the bus. The peripheral device asserts this signal in conjunction with a DMA request (DRQ) line or the HRQ (hold request) to gain control of the bus. When the MASTER# signal is asserted LOW along with HRQ being asserted HIGH or a DRQ line being asserted HIGH, the Intel386 SL CPU will float all address, data and control signals on the ISA bus.
MD[15:0]	Memory controller local Memory Data bus: This is the bi-directional data bus of the Memory Controller Unit. All accesses by the Memory Controller Unit that transfer data between the Intel386 SL CPU and SRAM or DRAM use the Memory Data Bus. This pin is disabled when SUS_STAT# is active (low) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MEMCS16#	MEMory Chip Select 16: This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit memory cycle. This signal has an active pull-up, when not driven the default memory bus cycle is 8 bits.
MEMR#	MEMory Read: This bi-directional active LOW signal indicates when a memory read access is taking place on the ISA bus. When the Intel386 SL CPU is performing a memory read to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMR#.
MEMW#	MEMory Write: This bi-directional active LOW signal indicates when a memory write access is taking place on the ISA bus. When the Intel386 SL CPU is performing a memory write to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA controller or Bus Master drives MEMW#.
N/C	No connection: These pins must not be connected to any voltage, but must be left floating in order to guarantee proper operation of the Intel386 SL CPU and to maintain compatibility with future Intel Processors.
NMI	Non-Maskable Interrupt: This rising edge sensitive input will latch a request to the Intel386 SL CPU for a non-maskable interrupt on a LOW-to-HIGH transition.
NPXADS#	Numerics Address Strobe: This active LOW output signal indicates the start of a math co-process (MCP) data transfer cycle.

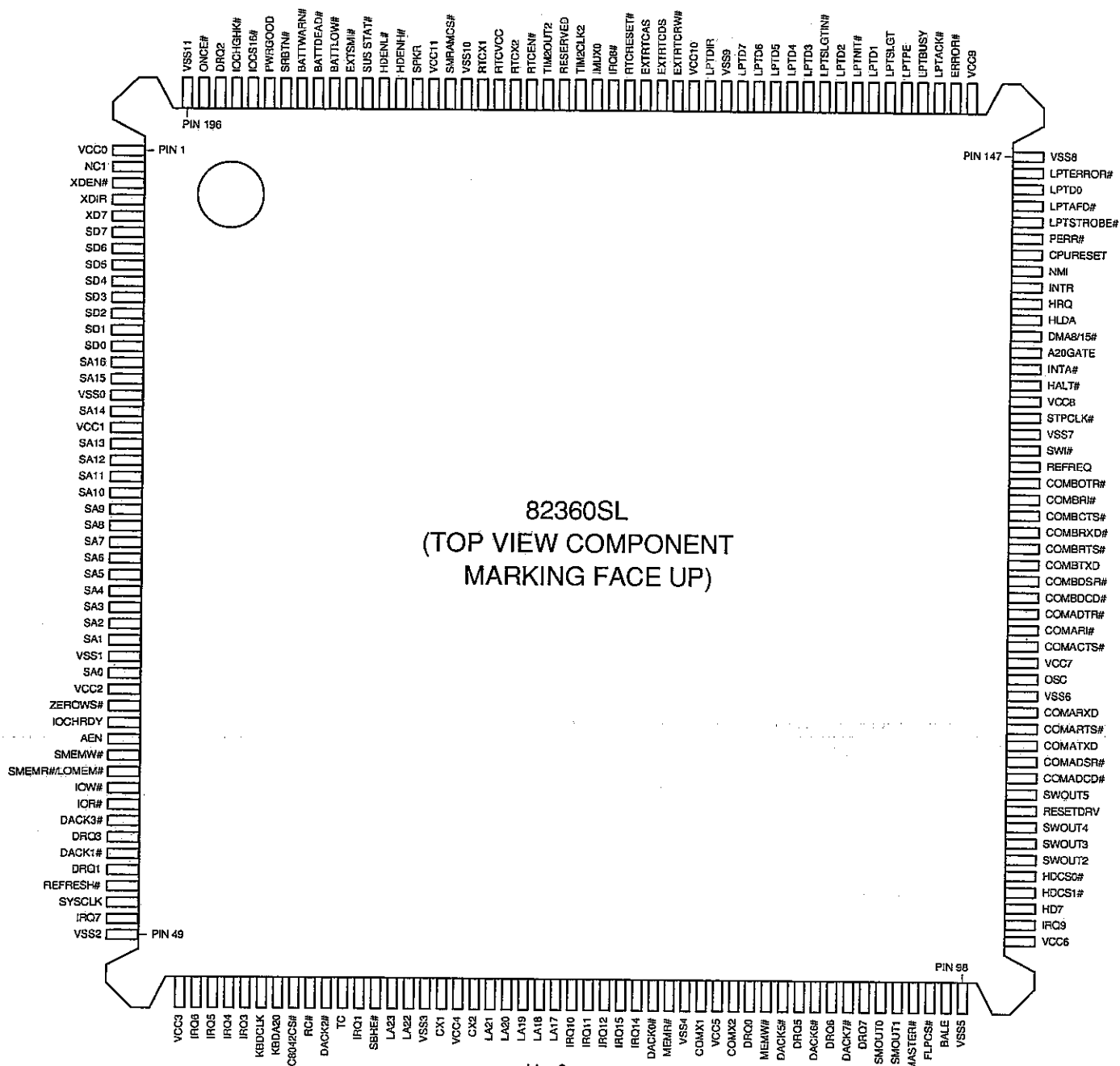
Symbol	Name and Function
NPXCLK	Numerics Clock: This output signal is used to drive the MCP clock input.
NPXRDY#	Numerics Ready: this active LOW input is used to terminate a MCP bus cycle. This signal is low for I/O and data operand MCP cycles.
NPXRESET	Numerics Reset: This active HIGH output signal is used to reset the MCP.
NPXW/R#	Numerics Write or Read: This output signal indicates the type of data transfer that is being performed between the Intel386 SL CPU and the MCP. When high this signal indicates a MCP write, when low this signal indicates a MCP read.
ONCE#	ON-board Circuit Emulation: This active LOW input signal floats the necessary outputs from the Intel386 SL CPU allowing an in-circuit emulation (ICE™-Intel386™ SL) module to drive the Intel386 SL CPU signals. this allows an emulator to be used for system testing and development while the Intel386 SL CPU and the 82360SL are still physically populated on the system motherboard. The state of all Intel386 SL CPU and 82360SL signal when ONCE# is asserted low is summarized in section 2, (Intel386 SL CPU and 82360SL signal characteristics). Note that the ONCE# pin of the Intel386 SL CPU should not be connected to the ONCE# pin of the 82360 SL I/O.
PCMD#	PI-BUS command: This active LOW output indicates that valid write data is on the System data bus (SD[15:0]) signals, or that the Intel386 SL CPU is ready to sample valid read data from the PI bus for Peripheral Interface bus cycles.
PEREQ	Processor Extension Request: This active HIGH input signal indicates that the MCP has data to transfer to or from the Intel386 SL CPU.
PERR#	Parity ERROR: This active LOW output indicates to an external device that the Intel386 SL CPU Memory Controller Unit has detected a memory parity error. The PERROR# signal is used by the 82360SL to generate NMI back to the Intel386 SL CPU.
PM/IO#	PI-BUS Memory or I/O: This output indicates the type of bus cycle the Intel386 SL CPU is executing on the Peripheral Interface Bus (PI-bus): Either a Memory (HIGH) or I/O (LOW) cycle.
PRDY#	PI-BUS Ready: This active LOW input is used to terminate Peripheral Interface bus cycles. the Peripheral Interface Bus is a normally not-ready bus, and will continue the bus cycle until the PRDY# is activated or a Peripheral Interface Time-out occurs.
PSTART#	PI-BUS START: This active LOW output indicates that the address (SA[19:0], LA[23:17] and SBHE#), command signals (PM/IO# and PW/R#) and chip-selects (VGACS# or FLSHDCS#) are valid for a Peripheral Interface Bus cycle.
PW/R#	PI-BUS Write or Read: This output indicates the type of bus cycle the Intel386 SL CPU is executing on the Peripheral Interface Bus: Either a Write (HIGH) or Read (LOW) cycle.
PWRGOOD	Power Good: This active HIGH input indicates that power to the system is good. This signal is generated by the power supply circuitry, and a LOW level on this signal causes the Intel386 SL to totally reset: The CPU core is reset, internal state machines are reset, all configuration registers are reset. Power Good should be low for a specified minimum number of CPU clocks for valid recognition in order to perform a global Intel386 SL CPU reset.
REFREQ	REFresh REQUEST: This active HIGH input indicates that the Intel386 SL CPU should execute an internal DRAM refresh cycle to the on-board local memory.
ROM16/8#	ROM 16-bits or 8-bits: This input configuration signal pin selects if the BIOS interface is a 16-bit (when high) or 8-bit interface (when low). this pin has an internal pull-up resistor defaulting to a 16-bit wide BIOS EPROM.
ROMCS0#	ROM Chip Select 0: This LOW true output provides the chip select for the System BIOS EPROM.
SA[19:0]	System Address Bus: This is the bi-directional system address of the ISA bus, as well as the Peripheral Interface Bus. SA[16:0] are inputs during DMA and Master operation. SA[19:17] are outputs only since a 8237 compatible DMA controller accesses up to 64 kBytes at a time. The 74LS612 module in the 82360SL is used to furnish the DMA upper addresses for DMA access to 16 Megabyte.
SBHE#	System Byte High Enable: When this output signal is LOW, it indicates that data is being transferred on the upper byte of the 16-bit data bus (SD[15:8]).
SD[15:0]	System Data Bus: This 16-bit bi-directional data bus is used to transfer data between the Intel386 SL CPU and the ISA bus. The system data bus is also used to transfer data between the Intel386 SL CPU and the Peripheral Interface (PI-BUS).
SMI#	System power Management Interrupt: This falling edge sensitive input latches a Power Management interrupt request with a High-to-Low edge. The SMI# is the highest priority interrupt in the Intel386 SL processor.
SMRAMCS#	System power Management RAM Chip Select: This active LOW output is used to select an external system power management SM-RAM, and to indicate to the 82360SL device when accesses to the system power management SM-RAM are occurring.
STPCLK#	Stop Clock: This active LOW input stops the clock to the internal Intel386 CPU core. (This signal is functionally tested by the execution of HALT or I/O read instructions.)
SYSCLK	System Clock: This is a clock output equal to one half of the ISACK2 input frequency.
SUS_STAT#	SUSpend STATUS: This active LOW input indicates to the Intel386 SL CPU that system power is being turned off. The Intel386 SL CPU will respond by electrically isolating selected pins as indicated in Section 2, (Intel386 SL CPU signal characteristics).
TURBO	Turbo: This active HIGH input signal indicates to Intel386 SL CPU when to enter "Turbo Mode". Turbo Mode is defined as the CPU executing at full speed, the default speed for the system. When this signal is forced inactive LOW, the Intel386 SL CPU executes from a divide by two or a divide by four clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is HIGH, the CPU executes from a clock as defined by the Fast CPU clock field in the CPUPWRMODE register.
Vcc	System Power: Provides the +5V nominal D.C. supply inputs.
VGACS#	VGA Chip-select: This active LOW output is asserted anytime an access occurs to the user defined VGA address space.
Vss	System Ground: Provides the 0V connection from which all inputs and outputs are referenced.

Symbol	Name and Function
WHE#	Write High Enable: This active LOW output indicates that a write access to the upper byte of the Intel386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the upper byte for either DRAM or SRAM memory subsystems. This pin is driven inactive during a suspend operation.
WLE#	Write Low Enable: This active LOW output indicates that a write access to the lower byte of the Intel386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the lower byte for either DRAM or SRAM memory subsystems. This pin is driven inactive during a suspend operation.
ZEROWS#	ZERO Wait State (ISA bus signal): This active LOW input indicates that an ISA bus peripheral wishes to execute a zero wait state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 SYSCLKs or one PC/AT equivalent wait state). When ZEROWS# is driven low, a 16-bit bus cycle will occur in two SYSCLKs. When ZEROWS# is driven low for an 8-bit memory cycle the default 6 SYSCLK bus cycle is shortened to 3 SYSCLKs.

Note: 1. Pins CMUX4 and CMUX5 both carry the signal DEN1# in the SRAM mode. This is done to provide increased drive capacity align please on the DEN1# signal.
 2. Pins CMUX6 and CMUX7 both carry the signal DEN0# in the SRAM mode. This is done to provide increased drive capacity on align, please the DEN0# signal.

2. 82360SL I/O SUBSET

2-1. Pin configuration



2-2. Pin table

Table 2-3. 82360SL Pin Characteristics

Signal Name	PQFP Pin #	Type	Term	Drive I _{OL} , I _{OH}	Load Min, Max	Susp	ONCE
A20GATE	B135	O		12, 2	20, 50	Tri	Tri
AEN	B37	O		24, 4	50, 240	Tri	Tri
BALE	B97	I				Tri	Tri
BATTDEAD#	B188	I				Actv	Tri
BATTLOW#	B187	I				Actv	Tri
BATTWARN#	B189	I	60K PU			Tri	Tri
C8042CS#	B57	O		12, 2	20, 50	Tri	Tri
COMACTS#	B117	I	60K PU			Tri	Tri
COMADCD#	B109	I	60K PU			Tri	Tri
COMADSR#	B110	I	60K PU			Tri	Tri
COMADTR#	B119	O		12, 2	20, 50	Tri	Tri
COMARI#	B118	I	60K PU			Actv	Tri
COMARTS#	B112	O		12, 2	20, 50	Tri	Tri
COMARXD	B113	I	20K PD			Tri	Tri
COMATXD	B111	O		12, 2	20, 50	Tri	Tri
COMBCTS#	B125	I	60K PU			Tri	Tri
COMBDCD#	B120	I	60K PU			Tri	Tri
COMBDSR#	B121	I	60K PU			Tri	Tri
COMBDTR#	B127	O		12, 2	20, 50	Tri	Tri
COMBRI#	B126	I	60K PU			Actv	Tri
COMBRTS#	B123	O		12, 2	20, 50	Tri	Tri
COMBRXD	B124	I	20K PD			Tri	Tri
COMBTXD	B122	O		12, 2	20, 50	Tri	Tri
COMX1	B82	I				Tri	Tri
COMX2	B84	O				1	1
CPURESET	B141	O		12, 2	20, 50	Actv	Tri
CX1	B66	I				Tri	Tri
CX2	B68	O				1	1
DACK0#	B79	O		12, 2	20, 50	Tri	Tri
DACK1#	B44	O		12, 2	20, 50	Tri	Tri
DACK2#	B59	O		12, 2	20, 50	Tri	Tri
DACK3#	B42	O		12, 2	20, 50	Tri	Tri
DACK5#	B87	O		12, 2	20, 50	Tri	Tri
DACK8#	B89	O		12, 2	20, 50	Tri	Tri
DACK7#	B91	O		12, 2	20, 50	Tri	Tri
DMA8/16#	B136	O		12, 2	20, 50	Tri	Tri
DRQ0	B85	I	20K PD			Tri	Tri
DRQ1	B45	I	20K PD			Tri	Tri
DRQ2	B194	I	20K PD			Tri	Tri
DRQ3	B43	I	20K PD			Tri	Tri
DRQ5	B88	I	20K PD			Tri	Tri
DRQ6	B90	I	20K PD			Tri	Tri
DRQ7	B92	I	20K PD			Tri	Tri
ERROR#	B149	I	60K PU			Tri	Tri
EXTRTCRW#	B166	O	60K PU	12, 2	20, 50	1	Tri
EXTRTCAS	B168	O	20K PD	12, 2	20, 50	0	Tri
EXTRTCDS	B167	O	60K PU	12, 2	20, 50	1	Tri
EXTSMI#	B186	I	60K PU			Tri	Tri
FLPCS#	B96	O		12, 2	20, 50	Tri	Tri
HALT#	B133	I	60K PU			Tri	Tri
HD7	B101	IO	60K PU	24, 4	20, 100	Tri	Tri
HDCS0#	B103	O		12, 2	20, 50	Tri	Tri
HDCS1#	B102	O		12, 2	20, 50	Tri	Tri

Signal Name	PQFP Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	ONCE
HDENH#	B183	O		12, 2	20, 50	Tri	Tri
HDENL#	B184	O		12, 2	20, 50	Tri	Tri
HLDA	B137	I	20K PD			Tri	Tri
HRQ	B138	O		12, 2	20, 50	Tri	Tri
IMUX0	B171	I	20K PD			Tri	Tri
INTA#	B134	I	60K PU			Tri	Tri
INTR	B139	O		12, 2	20, 50	Tri	Tri
IOCHCK#	B193	I	4.7K PU			Tri	Tri
IOCHRDY	B36	IO OD		24, 4	20, 240	Tri	Tri
IOCS16#	B192	I				Tri	
IOR#	B41	IO		24, 4	50, 240	Tri	Tri
IOW#	B40	IO		24, 4	50, 240	Tri	Tri
IRQ1	B61	I	10K PU			Tri	Tri
IRQ3	B54	I	10K PU			Tri	Tri
IRQ4	B53	I	10K PU			Tri	Tri
IRQ5	B52	I	10K PU			Tri	Tri
IRQ6	B51	I	10K PU			Tri	Tri
IRQ7	B48	I	10K PU			Tri	Tri
IRQ8#	B170	I	20K PD			Activ	Tri
IRQ9	B100	I	10K PU			Tri	Tri
IRQ10	B74	I	10K PU			Tri	Tri
IRQ11	B75	I	10K PU			Tri	Tri
IRQ12	B76	I	10K PU			Tri	Tri
IRQ14	B78	I	10K PU			Tri	Tri
IRQ15	B77	I	10K PU			Tri	Tri
KBDA20	B56	I	60K PU			Tri	Tri
KBDCLK	B55	O		12, 2	20, 50	Tri	Tri
LA17	B73	IO		24, 4	50, 240	Tri	Tri
LA18	B72	IO		24, 4	50, 240	Tri	Tri
LA19	B71	IO		24, 4	50, 240	Tri	Tri
LA20	B70	IO		24, 4	50, 240	Tri	Tri
LA21	B69	IO		24, 4	50, 240	Tri	Tri
LA22	B64	IO		24, 4	50, 240	Tri	Tri
LA23	B63	IO		24, 4	50, 240	Tri	Tri
LPTACK#	B150	I	60K PU			Tri	Tri
LPTAFD#	B144	O OD ⁽¹⁾	4.7K PU	12	20, 100	Tri	Tri
LPTBUSY	B151	I	20K PD			Tri	Tri
LPTD0	B145	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD1	B154	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD2	B156	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD3	B158	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD4	B159	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD5	B160	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD6	B161	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTD7	B162	IO	20K PD	8, 2	20, 100	Tri	Tri
LPTDIR	B164	O OD ⁽¹⁾	4.7K PU	12	20, 100	Tri	Tri
LPTERROR#	B146	I	60K PU			Tri	Tri
LPTINIT#	B155	O OD ⁽¹⁾	4.7K PU	12	20, 100	Tri	Tri
LPTPE	B152	I	20K PD			Tri	Tri
LPTSLCT	B153	I	20K PD			Tri	Tri
LPTSLCTIN#	B157	O OD ⁽¹⁾	4.7K PU	12	20, 100	Tri	Tri
LPTSTROBE#	B143	O OD ⁽¹⁾	4.7K PU	12	20, 100	Tri	Tri
MASTER#	B95	I				Tri	Tri
MEMR#	B80	IO		24, 4	20, 240	Tri	Tri
MEMW#	B86	IO		24, 4	20, 240	Tri	Tri
NC	B2						

Signal Name	PQFP Pin #	Type	Term	Drive IoL, IoH	Load Min, Max	Susp	ONCE
NMI	B140	O		12, 2	20, 50	Tri	Tri
ONCE#	B195	I	60K PU			Tri	Actv
OSC	B115	O		24	50, 240	Tri	Tri
PERR#	B142	I	60K PU			Tri	Tri
PWRGOOD	B191	I				Actv	Tri
RC#	B58	I	60K PU			Tri	Tri
REFREQ	B128	O		12, 2	20, 50	Actv	Tri
REFRESH#	B46	IO OD	300 PU	8	50, 240	Tri	Tri
RESETDRV	B107	O		24	50, 240	Tri	Tri
RTCEN#	B175	I				Actv	Tri
RTCRESET#	B169	I				Actv	Tri
RTCVCC	B177						
RTCX1	B178	I				Actv	Tri
RTCX2	B176	O				Actv	1
Reserved	B173						
SA0	B33	IO		24, 4	50, 240	Tri	Tri
SA1	B31	IO		24, 4	50, 240	Tri	Tri
SA2	B30	IO		24, 4	50, 240	Tri	Tri
SA3	B29	IO		24, 4	50, 240	Tri	Tri
SA4	B28	IO		24, 4	50, 240	Tri	Tri
SA5	B27	IO		24, 4	50, 240	Tri	Tri
SA6	B26	IO		24, 4	50, 240	Tri	Tri
SA7	B25	IO		24, 4	50, 240	Tri	Tri
SA8	B24	IO		24, 4	50, 240	Tri	Tri
SA9	B23	IO		24, 4	50, 240	Tri	Tri
SA10	B22	IO		24, 4	50, 240	Tri	Tri
SA11	B21	IO		24, 4	50, 240	Tri	Tri
SA12	B20	IO		24, 4	50, 240	Tri	Tri
SA13	B19	IO		24, 4	50, 240	Tri	Tri
SA14	B17	IO		24, 4	50, 240	Tri	Tri
SA15	B15	IO		24, 4	50, 240	Tri	Tri
SA16	B14	IO		24, 4	50, 240	Tri	Tri
SBHE#	B62	O		24, 4	50, 240	Tri	Tri
SD0	B13	IO		24, 4	50, 240	Tri	Tri
SD1	B12	IO		24, 4	50, 240	Tri	Tri
SD2	B11	IO		24, 4	50, 240	Tri	Tri
SD3	B10	IO		24, 4	50, 240	Tri	Tri
SD4	B9	IO		24, 4	50, 240	Tri	Tri
SD5	B8	IO		24, 4	50, 240	Tri	Tri
SD6	B7	IO		24, 4	50, 240	Tri	Tri
SD7	B6	IO		24, 4	50, 240	Tri	Tri
SMEMR#/LOMEM#	B39	O	60K PU	24, 4	50, 240	Tri	Tri
SMEMW#	B38	O	60K PU	24, 4	50, 240	Tri	Tri
SMI#	B129	O		12, 2	20, 50	Tri	Tri
SMOUT0	B93	O		12, 2	20, 50	Tri	Tri
SMOUT1	B94	O		12, 2	20, 50	Tri	Tri
SMOUT2	B104	O		12, 2	20, 50	Tri	Tri
SMOUT3	B105	O		12, 2	20, 50	Tri	Tri
SMOUT4	B106	O		12, 2	20, 50	Tri	Tri
SMOUT5	B108	O		12, 2	20, 50	Tri	Tri
SMRAMCS#	B180	I	60K PU			Tri	Tri
SPKR	B182	O		12, 2	20, 50	Tri	Tri
SRBTN#	B190	I				Actv	Tri
STPCLK#	B131	O		12, 2	20, 50	Tri	Tri
SUS_STAT#	B185	O		12, 2	20, 50	Act	Tri
SYSCLK	B47	I				Tri	Tri

Signal Name	PQFP Pin #	Type	Term	Drive IOL, IOH	Load Min, Max	Susp	ONCE
TC	B60	O		24, 4	50, 240	Tri	Tri
TIM2CLK2	B172	I	20K PD			Tri	Tri
TIM2OUT2	B174	O		12, 2	20, 50	Tri	Tri
XD7	B5	IO	60K PU	24, 4	20, 100	Tri	Tri
XDEN#	B3	O		12, 2	20, 50	Tri	Tri
XDIR	B4	O		12, 2	20, 50	Tri	Tri
OWS#	B35	O OD		24, 4	50, 240	Tri	Tri

NOTE: 1. These outputs become CMOS drivers when bit 7 of the FPP_CNTL register is set.

Power Pins

V_{CC}: B001, B018, B084, B060, B067, B083, B099, B116, B132, B148, B165, B181

V_{SS}: B016, B082, B049, B085, B081, B098, B114, B130, B147, B163, B179, B196

2-3. SIGNAL DESCRIPTIONS

82360SL ISA Peripheral I/O

The following table provides a brief description of the signals of the 82360SL I/O. Signal names which end with the character "#" indicate that the corresponding signal is low true when active.

Symbol	Name and Function
A20GATE	A20 Gate (direct to CPU): This active HIGH output signal allows the Intel386 SL CPU to pass A20 on the system address bus. When this signal is LOW, A20 is masked to allow emulation of an 8086.
AEN	Address ENabled (ISA-bus signal): This active HIGH output indicates a DMA access or refresh. The 82360SL drive this signal high to signify a valid DMA address. It is used by bus slaves to decode I/O ports. All ports must be decoded for AEN low. There are no DMA cycles to addressed I/O ports.
BALE	Buffered Address Latch Enable (ISA-bus signal): This active HIGH input to the 82360SL is driven by the Intel386 SL CPU during standard ISA bus cycles. During ISA bus memory and I/O cycles BALE is used to indicate valid addresses at the start of a bus cycle. SA[19:0] are valid on the falling edge and LA[23:17] are valid while BALE is high. BALE is also driven high by the Intel386 SL CPU and remains high during DMA, REFRESH and Master cycles.
BATTDEAD#	BATTERY DEAD: This signal acts as a reset to the state machines connected to RTCVCC.
BATTLOW#	BATTERY LOW: This active LOW input indicates that the battery power is low. BATTLOW# is typically driven by a D.C. power converter associated with the battery power supply. A thermal power monitor indicates that the main battery power is dropping below the adequate charge level to sustain operation. If this signal is asserted LOW a SMI request will be generated. The feature is enabled via S/W control. The signal will also prevent a resume operation if asserted LOW.
BATTWARN#	BATTERY WARNING: This active LOW input indicates the battery has minimal charge left (eg. one half an hour of full power use remaining). It is used to generate a battery low warning tone.
C8042CS#	Keyboard controller Chip Select: This active LOW output is driven when there is an I/O read or write to the Keyboard Controller Ports 60 or 64 hex.
COM(A, B)CTS#	Clear To Send: This active LOW input indicates to the Serial Port Controller for COMA or COMB that a serial device is clear to accept data. This signal is typically used for a modem control function. a change in the state of this signal generates a modem status interrupt. The modem or data set asserts this signal when it is ready to accept data for transmission.
COM(A, B)DCD#	Data Carrier Detect: This active LOW input indicates that the Serial Port Controller COMA or COMB has detected a data carrier from the data set of a serial device. Typically this signal is from a modem.
COM(A, B)DSR#	Data Set Ready: This active LOW input signal is used by the modem or data set to indicate that the modem or data set is ready to establish the communication link and transfer data with the Serial Port Controller.
COM(A, B)DTR#	Data Terminal Ready: This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to communicate.
COM(A, B)RXD	Serial data Receive: This input signal is used to receive serial data. Each character can consist of from five to eight bits of data with one start bit and one, one and a half or two stop bits. The least significant bit is received first.
COM(A, B)RI#	Ring Indicator: This active LOW input signal is used for a modem control function. A change in the state (either from high to low or from low to high) of this signal generates a modem status interrupt. The modem or data set asserts this signal to indicate that it has detected a telephone ring. This will cause the 82360SL to wake the Intel386 SL CPU from a suspended state if modem ring is enabled as a wake-up event.
COM(A, B)RTS#	Request To Send: This output signal is used to transmit data serially between the Serial Port Controller and serial device. Each character can consist of five to eight bits of data with one start bit and either one, one and a half, or two stop bits. The least significant bit is transmitted first. The control of the format of a character is defined under S/W control via the Line Control Register. Please consult the Intel386 SL Microprocessor SuperSet Programmer's Reference Manual for additional information. Information regarding the functional timing specifications of transmitted and received serial data may be found in sections 6 and 7 (A. C. timing specifications and timing diagrams).

Symbol	Name and Function
COM (A, B) TXD	Serial data transmission: This output signal is used to transmit data serially between the Serial Port Controller and serial device. Each character can consist of five to eight bits of data with one start bit and either one, one and a half, or two stop bits. The least significant bit is transmitted first. The control of the format of a character is defined under S/W control via the Line Control Register. Please consult the Intel386 SL Microprocessor SuperSet Programmer's Reference Manual for additional information. Information regarding the functional timing specifications of transmitted and received serial data may be found in sections 6 and 7 (A. C. timing specifications and timing diagrams).
COMX1, COMX2	Crystal oscillator input and output pins: The crystal attached to these signals should be tuned to 1.8432 Mhz. The on-chip oscillator uses an external crystal and tank circuit to generate an internal clock. This clock is used to generate the various baud rates for the serial ports. Optionally an external oscillator may be connected to the COMX1 input.
CPURESET	CPU RESET: This active HIGH output is connected directly to the Intel386 SL CPU to provide a reset of the Intel386 CPU core. CPURESET always occurs during a PWRGOOD reset. CPURESET may also be generated by RC# from a keyboard controller, Fast Reset from I/O Port 92 or other programmable Reset, or a resume from suspend.
CX1, CX2	Crystal oscillator input and output pins: The crystal should be tuned to 14.31818 MHz. It is used for the ISA bus signal OSC signal and is internally divided by 12 to clock the timer counters. The oscillator input may be directly driven from an external source.
DACK[7:5], [3:0]#	DMA ACKnowledge channel n (ISA bus signal): The 82360SL DMA controller drives the respective DMA acknowledge signal low after a device has requested DMA service. The corresponding output signal indicates that the DMA channel transfer may begin.
DMA8/16#	DMA 8-bit or 16-bit cycle: This output signal is directly connected to the Intel386 SL CPU. When the signal is HIGH it indicates that the current DMA cycle is 8-bit. When this signal is low it indicates that the DMA cycle is using a 16-bit channel.
DRQ[7:5], [3:0]	DMA ReQuest channel n (ISA bus signal): These input signals are used to request DMA service from devices residing on the ISA bus. An ISA bus device drives this signal to request service from the appropriate DMA channel by asserting this signal high.
ERROR#	MCP ERROR: This signal is an active LOW input to the 82360SL. The math coprocessor error signal generates a IRQ13 through the 82360SL.
EXTSMI#	EXternal System Management Interrupt request: This active low input will generate a SMI request if the function is enabled.
EXTRTCAS	EXternal RTC Address Strobe: this output signal is active HIGH when there is a write access to the RTC I/O address port and when an external RTC is selected.
EXTRTCDS	EXternal RTC read Data Strobe: This output signal is active LOW when there is a read access to an external RTC I/O data port and when an external RTC is selected.
EXTRTCRW#	External RTC (Real Time Clock) Read/Write: This output signal is active LOW when there is a write access to an external RTC I/O data port and when an external RTC is selected.
FLPCS#	FLoPpy Chip Select: This LOW true output signal is the chip select for the floppy disk controller I/O ports (03F0-03F5 and 3F7 hex).
HALT#	HALT: This LOW true input signal is driven by the Intel386 SL CPU and indicates when the CPU has executed a HLT instruction (address=2) or is in a shutdown condition (address=0).
HD7	HD-bus Data bit HD7: The bi-directional System Data Bit 7 is controlled separately for the Integrated Drive electronics (I.D.E.) hard disk drive and floppy disk drive. This is provided to accommodate the I/O address 3F7 hex which is split between the floppy disk drive controller and I.D.E. hard disk. Data transfer between storage peripherals connected to the I.D.E. Hard Disk and Floppy Disk and the 82360SL are on separate busses. Data bit 7 has to be separated from data bits [6:0]. The 82360SL controls and buffers data bit 7 separately.
HDCS[1:0]#	Hard Disk Chip Select: These LOW true output signals are the I.D.E. hard disk drive chip selects decoded from the I/O address ports 01F0-01F7h (HDCS0#) and 03F0-03F7h (HDCS1#).
HDEN(H, L)#	Hard Disk buffer ENable: These LOW true output signals control the I.D.E. hard disk data buffers, high and low bytes.
HLDA	HoLD Acknowledge (direct to CPU): This HIGH true input signal indicates that the Intel386 SL CPU has released the ISA bus for refresh, DMA or master cycles.
HRQ	Hold ReQuest (direct to CPU): This active HIGH output signal indicates a request to the Intel386 SL CPU to release the ISA bus when the 82360SL requests the bus for ISA bus style refresh, DMA or master mode cycles.
IMUX0	This pin is multiplexed. It can be used as Timer 2 gate 2 input or an external audio input.
INTA#	INTerrupt Acknowledge (direct to CPU): This active LOW input to the 82360SL indicates that the Intel386 SL CPU has recognized an interrupt and will initiate an interrupt acknowledge bus cycle. The INTA bus cycle is comprised of two eight-bit I/O cycles in which the interrupt vector transferred on the second eight-bit I/O write of the INTA cycle.
INTR	INTerrupt Request (direct to CPU): This active HIGH output requests a standard maskable interrupt to the Intel386 SL CPU.
IOCHCK#	IO CHannel Check (ISA bus signal): This maskable active LOW input is driven by a device on the ISA bus typically used to indicate a parity error on the ISA bus. This signal is one of the possible sources which may generate an NMI. NMI generation via IO Channel Check may be enabled or disabled using PORT 61 (IOCKEN). NMI may be masked using the ISA bus compatible NMI control port at I/O 70 hex bit 7.

Symbol	Name and Function
IOCHRDY	I/O Channel Ready (ISA bus signal): This active HIGH I/O signal is used by the 82360SL DMA controller to extend ISA bus cycles. IOCHRDY is also used to extend bus cycles for I/O device trapping. Additional wait states extend the bus cycle, allowing for start up during Resume mode. The ISA bus is a normally ready bus, an external device can extend a DMA cycle or ISA bus cycle by deasserting this signal (driven low). This signal is normally high on the ISA bus.
IOCS16#	16-bit I/O Chip Select (ISA bus signal): This active LOW input signal to the 82360SL is used to indicate a 16-bit I/O bus cycle. The I.D.E. hard disk high byte buffer enable is generated when IOCS16# is driven low during an I.D.E. 16-bit I/O access. IOCS16# is also an input to the Intel386 SL CPU driven by devices residing on the ISA bus to indicate a 16-bit I/O bus cycle.
IOR#	I/O Read (ISA bus signal): This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O read. This signal is an output from the 82360SL during DMA bus cycles for I/O to memory transfers.
IOW#	I/O Write (ISA bus signal): This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O write. This signal is an output from the 82360SL during DMA bus cycles for memory to I/O transfers.
IRQ[15, 14, 12-9, 7-3, 1]	Interrupt ReQuest n (ISA bus signal): These active HIGH input signals are used to request interrupt service. The interrupt request lines are driven by devices on the ISA bus which have a corresponding interrupt service routine associated with the interrupt vector and interrupt request.
IRQ8#	Interrupt ReQuest 8: This active LOW signal is used by the external Real Time Clock to request interrupt service.
KBDA20	KeyBoard A20 gate: This active HIGH input is "ORed" with internal bits to produce A20GATE which goes to the Intel386 SL CPU. The bit is connected to prot 2, bit 1 of an 8042 in a standard ISA bus compatible system.
KBDCLK	KeyBoard CLock: This output signal is used to drive the clock input to the keyboard controller. It is derived from the 8 MHz SYSClk and can be divided by 1, 2, 4 or stopped.
LA[23:17]	Local Address bus (ISA bus signal): These are input signals to the 82360SL during memory transfers (decoding for X-bus buffer controls) and output signals during DMA accesses and refresh. The latched address lines allow access to physical memory on the ISA bus to 16 megabytes.
LPTACK#	Line PrinTer ACKnowledge: Active LOW input signal which is part of the parallel port data handshake. The line printer asserts this signal to show that data transfer was complete and that it is ready for the next transfer. If the enable set in control this signal can be used to generate an interrupt.
LPTAFD#	Line PrinTer Auto line Feed: This signal is an active LOW output from 82360SL to a printer. When asserted, it instructs the printing device to insert a line feed at the end of every line. In the Fast parallel port mode, this signal is used as a data strobe. It can be used to latch data during write cycles and to enable buffers during read cycles.
LPTBUSY	Line PrinTer BUSY: This signal is an active HIGH input to 82360SL. The printer asserts this signal when it is not ready to accept further data from 82360SL. In the Fast parallel port mode this signal is active LOW.
LPTD[7:0]	Line PrinTer Data bus: These signals are the 8-bit bi-directional data bus for the parallel port. In PC/AT mode these signals are output only. The 82360SL also supports a bi-directional mode for the PS/2 style parallel port.
LPTDIR	Line PrinTer DIRection: This active HIGH output signal is only valid in bi-directional mode for data transfer using the parallel port. This signal is LOW in ISA compatible and Fast parallel port modes. In the PS-2 expanded mode, this signal is LOW for writes and HIGH for reads.
LPTERROR#	Line PrinTer ERROR: This active LOW input signal is driven by a peripheral device to flag an error condition.
LPTINIT#	Line PrinTer INITialize: This active LOW output from 82360SL instructs the peripheral to initialize itself.
LPTPE	Line PrinTer Paper End: This active HIGH input to 82360SL signals that the printer has run out of paper when asserted.
LPTSLCT	Line PrinTer SeLeCTed: This active HIGH input signal is asserted by the printer to confirm that it has been selected.
LPTSLCTINE#	Line PrinTer SeLeCT IN: This active LOW output signal is asserted to select the printer interfaced to the parallel port. In the Fast parallel port mode, this signal is used as an address strobe. It indicates that an access is being made to the port X7Bh.
LPTSTROBE#	Line PrinTer STROBE: This active LOW output signal is used to strobe data into the peripheral device. The parallel port controls are read and written through I/O registers. In the Fast parallel port mode, this signal is used to indicate a write cycle.
MASTER#	ISA bus MASTER (ISA bus signal): This active LOW input signal is used by the 82360 SL to determine when to go into an external master refresh arbitration mod. In this mode, the master controls the REFRESH signal but the 82360SL generates the address, the REFREQ# signal, the AEN and command signals.
MEMR#	MEMory cycle Read (ISA bus signal): This bi-directional active LOW signal indicates a read cycle anywhere in the 16 Mbyte memory address space. During memory read cycles to memory on the ISA bus, this signal is an input into the 82360SL. MEMR# is driven by the 82360SL during DMA cycles.
MEMW#	MEMory cycle Write (ISA bus signal): This bi-directional active LOW signal indicates a write cycle anywhere in the 16 Mbyte memory address space. During memory write cycles to memory on the ISA bus, this signal is an input. MEMW# is an output from the 82360SL during DMA cycles.
N/C	No Connection: These signals must not be connected to any voltage. The No Connection signals must be left floating in order to guarantee proper operation of the 82360SL and compatibility with future Intel processors.
NMI	Non Maskable Interrupt (direct to CPU): This active HIGH output is directly connected to the Intel386 SL CPU. The 82360 SL asserts NMI to request the Intel386 SL CPU to service a high priority non-maskable interrupt. The low to high transition of this signal is recognized by the Intel386 SL CPU.

Symbol	Name and Function
ONCE#	ON-board Circuit Emulation: This active LOW input pin floats the appropriate outputs of the 82360SL as indicated in Section 2 pin assignments. This allows the system to be tested with external logic while the 82360SL is still physically populated on the motherboard. Note that the ONCE# pin on the 82360SL I/O should not be connected to the ONCE# pin on the Intel386 SL CPU.
OSC	OSCillator (ISA bus signal): This is the 14.31818 MHz output signal with a 50% duty cycle and is asynchronous to SYSCLK.
PERR#	Parity ERROR (direct from CPU): This active LOW input signal is connected to the output of the Intel386 SL CPU. When the Intel386 SL CPU detects a parity error from the local DRAM subsystem it drives this signal to the 82360SL. The system memory parity error will generate a NMI via the 82360SL when NMI is enabled via I/O port 70h bit 7 and PERR# is enabled via port 61h.
PWRGOOD	Power GOOD: This active HIGH input is typically supplied by the power supply. When Power good is activated high this indicates that the supply voltage is stable. Power Good low is also used to generate System Reset, RESETDRV, and CPURESET.
RC#	Reset CPU: This active low input is typically driven by the keyboard controller. RC# is "ORed" with internal bits to produce a programmable pulse width CPURESET signal. It is connected to port 2, bit 0 of an 8042 in a standard ISA bus compatible system.
REFREQ	REFresh REQuest (direct to CPU): This active HIGH output signal is directly connected to the Intel386 SL CPU. When Refresh Request is asserted it indicates that the Intel386 SL CPU should refresh the local DRAM subsystem.
REFRESH#	System REFRESH (ISA bus signal): This active LOW input signal indicates a refresh cycle. It is driven for the duration of the cycle. It is an input during master generated refresh bus cycles.
RESETDRV	RESET DRIVe (ISA bus signal): This active HIGH output is the main system cold reset, generated from the power supply "power good" signal and by system resume.
RTCEN#	RTC ENable: This active LOW input signal should be strapped to GND or RTCVCC depending on whether an internal or external RTC is used in the system. The 82360SL on-chip real time clock and CMOS RAM are enabled by this signal when LOW.
RTCRESET#	Internal RTC RESET input: This active LOW input signal is used to reset the internal RTC status and flag registers, (typically when the RTC battery has been changed).
RTCVCC	This is a separate power supply input for the internal RTC. It should be connected to a 3V battery when the system is fully off and 5V during active operation.
RTCX1, RTCX2	RTC Crystal oscillator input and output pins: The crystal should be tuned to 32.768 Khz. It is used for the RTC and system power management state machines. The oscillator may be driven directly from the input signal.
SA[16:0]	System Address bus (ISA bus signal): The bi-directional system address bus is an input for decoding internal I/O registers and an output during DMA and refresh cycles.
SBHE#	System Byte High Enable (ISA bus signal): The active LOW output signal indicates when there is valid data on the upper data byte of the system data bus.
SD[7:0]	System Data bus (ISA bus signal): This is the bidirectional system data bus. The 82360SL directly drives the ISA bus system data bits [7:0] without external transceivers or buffers. 8-bit data is transferred to and from the 82360SL with these signals.
SMEMR#/LOMEM#	System MEMory Read (ISA bus signal): This multiplexed signal has two functions. When configured as SMEMR#, this signal is driven by the 82360SL to signify a memory read cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles. When configured as LOMEM#, this signal indicates that the lower 1 Mbyte is being addressed.
SMEMW#	System MEMory Write (ISA bus signal): This signal is driven by the 82360SL to signify memory write cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles.
SMI#	System Management Interrupt (direct to CPU): This active LOW output is directly connected to the Intel386 SL CPU. When the falling edge of SMI# is detected by the Intel386 SL CPU it generates the highest priority interrupt when enabled. The typical use of SMI# is for power management.
SMOUT[5:0]	System Management OUTput control: These six outputs can be connected to control the power circuits for various devices in the system. These output pins are directly controlled by the SMOUT_CNTRL register.
SMRAMCS#	System Management RAM Chip Select: This active LOW input is driven by the Intel386SL CPU whenever the Intel386 SL CPU is accessing System Management SM-RAM. It is active even when SM-RAM is part of the Intel386 SL CPU system memory RAM. The 82360SL uses the SMRAMCS# to determine when the SMI code is being executed on the ISA bus, and enables the X-bus control signals.
SPKR	SPeaKeR output: This is the output of the 8254 megacell, timer/counter #1, channel 2, or directly driven through IMUX0, or from the 8254 megacell, timer/counter #2, channel 1 depending on the programming. This output signal is typically connected to an external speaker. There is additional circuitry to ensure that the signal is low when not being used.
SRBTN#	Suspend/Resume BuTtoN: This active LOW input generates a SMI requesting a system suspend or resume. Activation of this input can be used as a wake up event for the STPCLK# signal.
STPCLK#	SToP CLoCK: This active LOW output signal stops the clock to the Intel386 CPU core of the Intel386 SL Microprocessor. Stop clock is directly connected to the Intel386 SL CPU from the 82360SL. The 82360SL activates this signal upon detection of a halt bus cycle or when an I/O read to the stop clock register in the 82360SL occurs.

Symbol	Name and Function
SYSCLK	SYSTEM Clock (ISA bus signal): This signal is an output from the Intel386 SL CPU and an input to the 82360SL. The SYSCLK signal is used to clock the ISA bus state machines and is also used to derive the internal DMA clock signal and to generate the KBDCLK output in the 82360SL. The SYSCLK is the 8 MHz typical clock which is one half of the frequency of ISACKL2.
SUS_STAT#	SUSpend STATus: The 82360SL power management controls this active low output signal to switch the power off to all non-critical devices during a suspend.
TC	Terminal Count (ISA bus signal): This active HIGH output signal is used to indicate the termination of a DMA transfer.
TIM2CLK2	TIMER 2 CLK: This is the input clock for timer/counter #2, channel 2 when it is programmed to be used in the General Purpose (GP) mode.
TIM2OUT2	TIMER 2 OUTput: This signal is the frequency output from timer/counter#2 and can be used as a general purpose timer/counter output when programmed for GP mode.
Vcc	System Power: Provides the +5V nominal D.C. supply inputs for the 82360SL.
Vss	System Ground: Provides the 0V connection from which all inputs and outputs are referenced.
XD7	X-bus Data bit XD7: I/O port 3F7h is split between the floppy and hard disk and the storage peripherals which transfer data reside on separate busses. Data bit XD7 is separated from bits XD[6:0]. The 82360SL separately controls and buffers bit XD7 to isolate data bit 7 from the floppy disk and I.D.E. hard disk.
XDEN#	X-bus Data ENable: This active LOW output signal is used to control the X-bus data transceiver. It is only activated by the 82360SL on valid accesses to X-bus peripherals.
XDIR	X-bus data DIRection: This active HIGH output signal controls the direction of the X-bus and HD-bus data transceivers. XDIR is high for read cycles.
ZEROWS#	ZERO Wait State (ISA-bus signal): This active LOW output signal is driven by the 82360SL when it can accept a zero wait state write cycle.

3. CLOCK GENERATOR AV9127-09

3-1. Block diagram

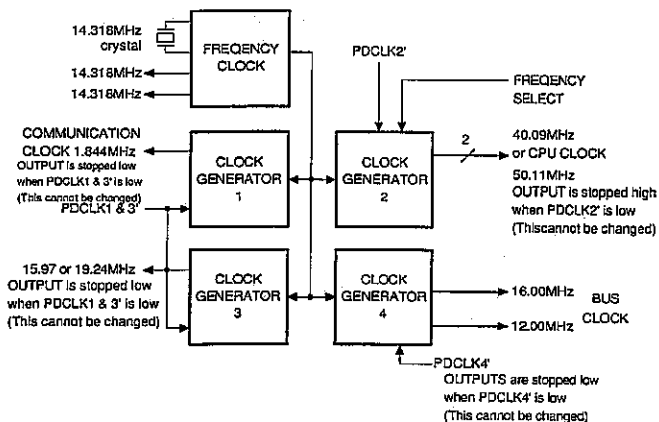


Fig. 3-1. Block diagram

3-2. Top view

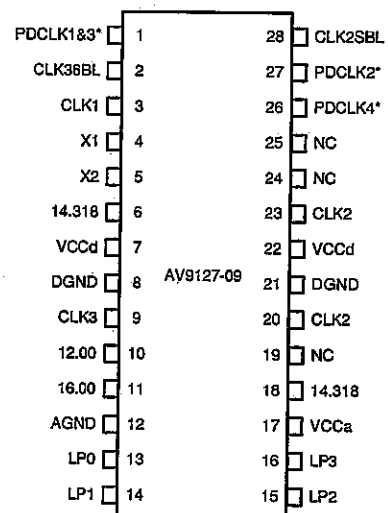


Fig. 3-2. Top view (28 pin DIP, SOIC)

3-3. PIN DESCRIPTION

Pin Name	Pin#	Pin type	Description
PDCLK1&3*	1	Input	POWER DOWN CLOCKS 1 & 3. shuts down clocks 1 and 3 when low.
CLK3SEL	2	Input	CLOCK 3 SELECT, selects 15.97MHz when low, 19.24MHz when high.
CLK1	3	Output	CLOCK 1. 1.844MHz clock output
X1	4	Input	CRYSTAL connection for 14.318 MHz crystal
X2	5	Output	CRYSTAL CONNECTION FOR 14.318 MHz crystal
14.318	6	Output	14.318MHz clock output
VCCd	7	—	DIGITAL POWER SUPPLY (+5V)
DGND	8	—	DIGITAL GROUND
CLK3	9	Output	CLOCK 3. 15.97MHz or 19.24MHz
12.00	10	Output	12.00 MHz clock output
16.00	11	Output	16.00 MHz clock output
AGND	12	—	ANALOG GROUND
LF0	13	I/O	LOOP FILTER
LF1	14	I/O	LOOP FILTER
LF2	15	I/O	LOOP FILTER
LF3	16	I/O	LOOP FILTER
VCCa	17	—	ANALOG POWER SUPPLY (+5V DC)
14.318	18	Output	14.318MHz clock output
NC	19	—	NO CONNECT
CLK2	20	Output	CLOCK 2. 2XCPU clock output
DGND	21	—	DIGITAL GROUND
VCCd	22	—	DIGITAL POWER SUPPLY (+5V)
CLK2	23	Output	CLOCK 2. 2XCPU clock output
NC	24	—	NO CONNECT
NC	25	—	NO CONNECT
PDCLK4*	26	Input	POWER DOWN CLOCK 4. Shuts off CLK4 when low.
PDCLK2*	27	Input	POWER DOWN CLOCK 2. shuts off CLK2 when low.
CLK2SEL	28	Input	CLOCK 2 SELECT. Selects 50.11MHz when high, 40.09MHz when low.

Table 3-1. Pin description

3-4. LOOP FILTER CONNECTIONS

The external loop filters must be connected to pins 13, 14, 15, and 16 for proper operation of the AV9127. Each of the pins should have an RC network connected as shown in Fig. 3-2.

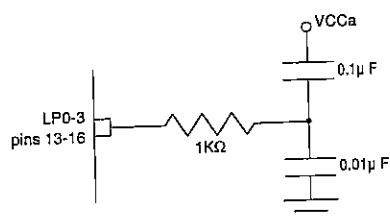


Fig. 3-3. RC network connected

4. KEY CONTROLLER 80C51SL-BG

4-1. PIN configuration

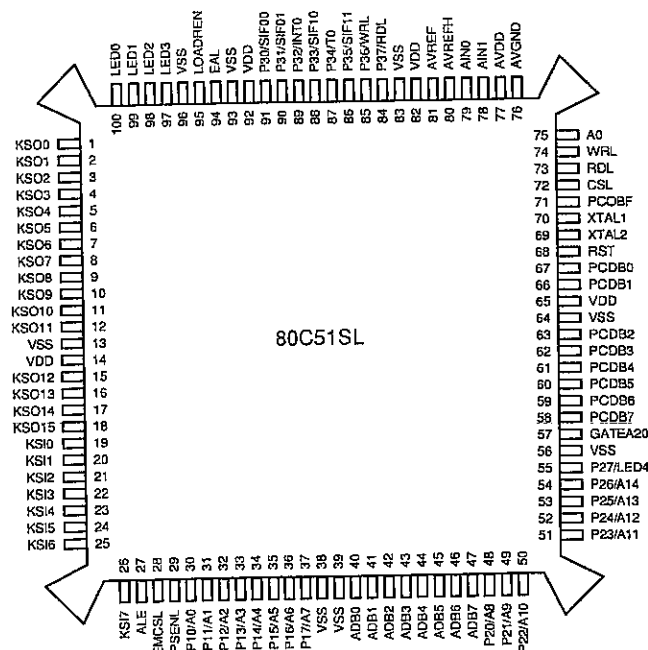


Fig. 4-1. Pin configurations

4-2. PIN DESCRIPTIONS

Name	I/O	Description
VSS		Circuit ground potential.
AVGND		Analog ground potential.
VDD		Supply voltage during normal, Idle, and Power-Down operation; nominally +5V±10%.
AVDD		Analog supply voltage; nominally +5V±10%.
AVREFH		A/D reference voltage; nominally +5V±10%.
AVREFL		A/D reference ground.
XTAL1	I	Input to the on-chip oscillator.
XTAL2	O	Output from the on-chip oscillator.
AIN0-1	I	A/D Analog input channels.
PORT 1	I/O	Port 1 is a general-purpose, 8-bit bidirectional port with internal pull-ups. It also supports the following user-selectable functions: P10-P16 are available for connection to dedicated keyboard inputs. A0-A7 output the low-order address byte.
P10/A0-P17/A7		
PORT 2	I/O	Port 2 is a general-purpose, 8-bit bidirectional port with internal pull-ups. It also supports the following user-selectable functions: P20-6/A8-14 output the high-order address byte. P27/LED4 is available as a fifth LED output driver.
P20-6/A8-14		
P27/LED4		
PORT 3	I/O	Port 3 is a general-purpose, 8-bit bidirectional port. P32/INT0, P34/T0, P36/WRL, and P37/RDL have internal pull-ups. P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11, which are high-drive open-drain outputs. It also supports the following user-selectable functions: A high-drive, open-drain output to support an EXT serial keyboard interface; RXD (8051 UART serial input port); SIF0INTL (serial interface interrupt 0). A high-drive, open-drain output to support an EXT serial keyboard interface; TXD (8051 UART serial output port). INT0L (external interrupt 0). A high-drive serial interface for extended keyboard or mouse; SIF1NTL (external interrupt 1). AUXOBF1 (output buffer full – mouse support); T0 (Timer/Counter 0 external input). A high-drive serial interface for extended keyboard or mouse; T1 (Timer/Counter 1 external input). WRL (external data memory write strobe). AUXOBF2 (output buffer full interrupt); INT2L (external interrupt); RDL (external data memory read strobe).
P30/SIF00		
P31/SIF01		
P32/INT0		
P33/SIF10		
P34/T0		
P35/SIF11		
P36/WRL		
P37/RDL		
ADB0-7	I/O	External address/data bus. Multiplexes the low-address byte and data during external memory accesses.
RST	I	Resets the keyboard controller. Hold RST high for two machine cycles.
EAL	I	External address input. When held high, the 80C51SL CPU executes out of internal Program Memory unless the program counter exceeds 1FFFH. When held low, the 80C51SL CPU always executes out of external memory. EAL is latched on the falling edge of RST.
MEMCSL	O	External Memory Chip Select for code space address 8000H and above, when EAL is inactive (i.e., high). For EAL low, MEMCSL is active. Goes inactive during Power-Down mode.
ALE	O	Address Latch Enable output pulse latches the low address byte during external memory access. ALE is output at a constant rate of 1/6 the oscillator frequency, whether or not there are accesses to external memory. One ALE pulse is skipped during the execution of a MOVX instruction.
PSENL	O	Program Store Enable is the read strobe to external program memory. PSENL is qualified with RDL and A15 for use with an external Flash memory. PSENL is not active when the device executes out of internal program memory.
LED0-3	O	LED output drivers.
KSO0-15	O	Keyboard output scan lines.
KSI0-7	I	Keyboard input scan lines (into Port 0). Schmitt inputs with 5-20K pull-up resistors.
PCDB0-7	I/O	Host interface data bus. An 8-bit, bidirectional port for data transfers between the host processor and the keyboard controller.
WRL	I	The active-low, host-interface write signal.
RDL	I	The active-low, host-interface read signal.
A0	I	Host interface Address select input. When high, it selects the command/status registers; when low it selects the data registers.
CSL	I	The active-low, host-interface chip select.
PCDBF	O	The active-high, host-interface Output Buffer Full interrupt.
LOADREN	O	Low address enable. When set high, address bits A0-A7 are output on P10-P17.
GATEA20	O	Gate A20 control signal output.

Table 4-1. Pin descriptions

5. FD/PRT CONTROLLER SC14L010AF-1233 (ASIC)

5-1. Top view

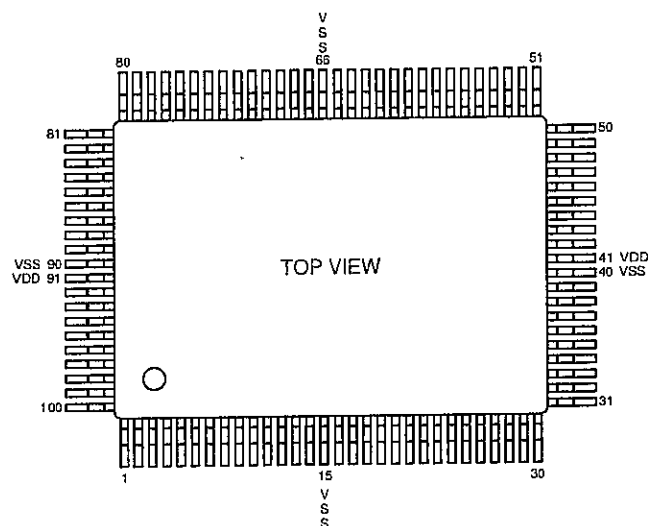


Fig. 5-1. Pin configurations (QFP100)

5-2. Pin descriptions

PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O
1	IORN	IN	26	LSTBN	I/O	51	PD7	I/O	76	DSKCHGN	IN
2	IOWN	IN	27	LD0	I/O	52	PD6	I/O	77	MS16N	OUT
3	SA0	IN	28	SMOUT3	IN	53	BDIR1	OUT	78	SEL19M	OUT
4	SA1	IN	29	LD1	I/O	54	PD5	I/O	79	MOTERONN	OUT
5	SA2	IN	30	LD2	I/O	55	PD4	I/O	80	DS0	OUT
6	SA3	IN	31	LD3	I/O	56	PD3	I/O	81	RDTN	OUT
7	SA4	IN	32	LD4	I/O	57	PD2	I/O	82	WDTN	IN
8	SA5	IN	33	LD5	I/O	58	PD1	I/O	83	WEN	IN
9	SA6	IN	34	LD6	I/O	59	PD0	I/O	84	HSN	IN
10	SA7	IN	35	LD7	I/O	60	LOWDEN	OUT	85	STPN	IN
11	SA8	IN	36	LAFDN	I/O	61	INIT	OUT	86	DRN	IN
12	SA9	IN	37	LERRORN	OUT	62	AUFDX	OUT	87	IDXN	OUT
13	AEN	IN	38	LACKN	OUT	63	SLECTN	OUT	88	WPN	OUT
14	RESET	IN	39	LBUSY	OUT	64	STROBE	OUT	89	TKON	OUT
15	VSS	—	40	VSS	—	65	STRBIN	IN	90	VSS	—
16	SD0	I/O	41	VDD	—	66	VSS	—	91	VDD	—
17	SD1	I/O	42	LPE	OUT	67	PSLCTIN	I/O	92	FDCSTB	IN
18	SD2	I/O	43	LSLCT	OUT	68	PINIT	I/O	93	LIDOPEN	IN
19	SD3	I/O	44	LINITN	I/O	69	PAFDX	I/O	94	LIDOPEN	IN
20	SD4	I/O	45	LSLCTN	I/O	70	ERRN	I/O	95	SRSW	IN
21	SD5	I/O	46	LDIR	IN	71	SLCT	I/O	96	SRBTN	OUT
22	SD6	I/O	47	PDCLKN	OUT	72	BUSY	I/O	97	PRTFD	IN
23	SD7	I/O	48	VGACSN	IN	73	ACKN	I/O	98	BLOAD	IN
24	FDCSN	OUT	49	SMEMRN	IN	74	PE	I/O	99	ROMCS0	IN
25	SMOUT4	IN	50	SMEMWN	IN	75	BDIR2	OUT	100	CSBIOSN	OUT

6. IC CARD I/F SC14L080AF-1031 (ASIC)

6-1. Top view

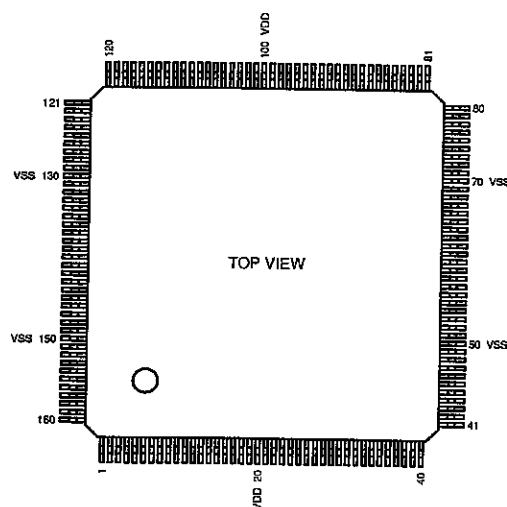


Fig. 6-1. Pin configuration (QFP160)

6-2. Pin description

Number(s)	Name	Description	Connection
1:9, 12:19, 21:27, 29:35, 37, 158:160	B_*	Pins reserved for socket B	NC
10, 28, 36, 50, 70, 71, 80, 91, 114, 120, 130, 150	VSS	Ground Pins	GND
20, 38, 43, 60, 81, 100, 121	VDD	Power Pins	VCC
11	NC	No Connect	NC
39	A_ENABL#	External Data Buffer Enable	External Buffers OE pin
40	EXT_DIR	External Data Buffer Direction	External Buffers DIR pin
41	A_CADR12	PCMCIA Card Address 12	PCMCIA Socket pin
42	A_CADR13	PCMCIA Card Address 13	PCMCIA Socket pin
44	A_CADR14	PCMCIA Card Address 14	PCMCIA Socket pin
45	A_CADR15	PCMCIA Card Address 15	PCMCIA Socket pin
46	A_CADR16	PCMCIA Card Address 16	PCMCIA Socket pin
47	A_CADR17	PCMCIA Card Address 17	PCMCIA Socket pin
48	A_CADR18	PCMCIA Card Address 18	PCMCIA Socket pin
49	A_CADR19	PCMCIA Card Address 19	PCMCIA Socket pin
51	A_CADR20	PCMCIA Card Address 20	PCMCIA Socket pin
52	A_CADR21	PCMCIA Card Address 21	PCMCIA Socket pin
53	A_CADR22	PCMCIA Card Address 22	PCMCIA Socket pin
54	A_CADR23	PCMCIA Card Address 23	PCMCIA Socket pin
55	A_CADR24	PCMCIA Card Address 24	PCMCIA Socket pin
56	A_CADR25	PCMCIA Card Address 25	PCMCIA Socket pin
57	A_WAIT#	PCMCIA Card Wait	PCMCIA Socket pin
58	A_GD1#	PCMCIA Card Detect 1	PCMCIA Socket pin
59	A_CD2#	PCMCIA Card Detect 2	PCMCIA Socket pin
61	A_BVD1	PCMCIA Card Battery Voltage Detect 1	PCMCIA Socket pin
62	A_BVD2	PCMCIA Card Battery Voltage Detect 2	
63	A_WP	PCMCIA Card Write Protect	
64	A_READY	PCMCIA Card READY & BUSY	

Number(s)	Name	Description	Connection
65	A_IOW#	PCMCIA Card I/O Write Command	
66	A_IOR#	PCMCIA Card I/O Read Command	
67	A_OE#	PCMCIA Card Memory Read Command	
68	A_WE#	PCMCIA Card Memory Write or Program Command	
69	A_REG#	PCMCIA Card Attribute Memory Line	
72	A_CE1#	PCMCIA Card Enable Lower Byte	
73	A_CE2#	PCMCIA Card Enable Upper Byte	
74	A_RESET	PCMCIA Card RESET	
75	A_V1_VCC	Enable VCC to PCMCIA Card VPP1	
76	A_V1_VPP	Enable VCC to PCMCIA Card VPP1	
77	A_V2_VCC	Enable VCC to PCMCIA Card VPP1	
78	A_V2_VPP	Enable VCC to PCMCIA Card VPP1	
79	A_VC_EN#	Enable VCC to PCMCIA Card VCC	
82	PWRGOOD	Power on reset line	
83	RI_OUT#	Ring Indicator output	
84	INTR#	Interrupt output from card status change	
85	SPKROUT#	Digital Speaker output	
86	IRQ3	ISA Interrupt Request 3	
87	IRQ4	ISA Interrupt Request 4	
88	IRQ5	ISA Interrupt Request 5	
89	IRQ7	ISA Interrupt Request 7	
90	IRQ9	ISA Interrupt Request 9	
92	IRQ10	ISA Interrupt Request 10	
93	IRQ11	ISA Interrupt Request 11	
94	IRQ12	ISA Interrupt Request 12	
95	IRQ14	ISA Interrupt Request 14	
96	IRQ15	ISA Interrupt Request 15	
97	BRESET#	BIOS load RESET output	
98	BLOAD	BIOS LOAD active output	
99	XD7	Data bit 7 to XBUS	
101	CDATA7	Data bit 7 from card socket	
102	S_BLOAD#	SET Bios LOAD input - from switch	
103	SYSCLK	ISA bus SYStem CLock	
104	AEN	ISA AEN signal	
105	BALE	ISA Address Latch Enable	
106	SBHE#	ISA Byte High Enable	
107	MEMR#	ISA Memory Read Command	
108	MEMW#	ISA Memory Read Command	
109	IORC#	ISA I/O Read Command	
110	IORC#	ISA I/O Write Command	
111	ZEROWS#	ISA ZERO Wait State	
112	IOCHRDY	ISA I/O CHannel ReaDY	
113	IOCS16#	ISA I/O Card Selected 16 bits wide	
115	MEMCS16#	ISA I/O Card Selected 16 bits wide	
116	SD0	ISA Data bit 0	
117	SD1	ISA Data bit 1	
118	SD2	ISA Data bit 2	
119	SD3	ISA Data bit 3	
122	SD4	ISA Data bit 4	
123	SD5	ISA Data bit 5	
124	SD6	ISA Data bit 6	
125	SD7_OUT	ISA Data bit 7 output	
126	SD7_IN	ISA Data bit 7 input	
127	SA0	ISA Latched Address bit 0	
128	SA1	ISA Latched Address bit 1	
129	SA2	ISA Latched Address bit 2	

Number(s)	Name	Description	Connection
131	SA3	ISA Latched Address bit 3	Pin 3 A
132	SA4	ISA Latched Address bit 4	Pin 4 A
133	SA5	ISA Latched Address bit 5	Pin 5 A
134	SA6	ISA Latched Address bit 6	Pin 6 A
135	SA7	ISA Latched Address bit 7	Pin 7 A
136	SA8	ISA Latched Address bit 8	Pin 8 A
137	SA9	ISA Latched Address bit 9	Pin 9 A
138	SA10	ISA Latched Address bit 10	Pin 10 A
139	SA11	ISA Latched Address bit 11	Pin 11 A
140	SA12	ISA Latched Address bit 12	Pin 12 A
141	SA13	ISA Latched Address bit 13	Pin 13 A
142	SA14	ISA Latched Address bit 14	Pin 14 A
143	SA15	ISA Latched Address bit 15	Pin 15 A
144	SA16	ISA Latched Address bit 16	Pin 16 A
145	LA17	ISA Unlatched Address bit 17	Pin 17 A
146	LA18	ISA Unlatched Address bit 18	Pin 18 A
147	LA19	ISA Unlatched Address bit 19	Pin 19 A
148	LA20	ISA Unlatched Address bit 20	Pin 20 A
149	LA21	ISA Unlatched Address bit 21	Pin 21 A
151	LA22	ISA Unlatched Address bit 22	Pin 22 A
152	LA23	ISA Unlatched Address bit 23	Pin 23 A
153	CS#	Chip Select	Pin 24 A
154	MODE	Internal decode versus External decode MODE	Pin 25 A
155	SEL0	SEL socket least significant bit	Pin 26 A
156	SEL1	SEL socket most significant bit	Pin 27 A
157	RESETDRV	ISA RESETDRV	Pin 28 A

7. FDC TC8566AF

7-1. General

The TC8566AF is the floppy disk control LSI for interface between the CPU and four FDD's (Floppy Disk Drives). The LSI is integrated with the FDC body, high performance VFO circuit, and peripheral logic into one chip.

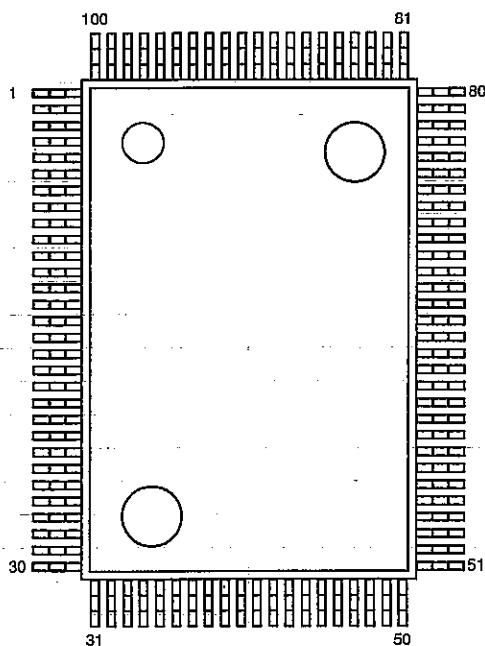


Fig. 7-1. Top view

7-2. Feature

- Si-gate CMOS structure
- 5V signal power source
- 100 pin flat package
- Built-in oscillating circuit
- Built-in VFO circuit
- Built-in standby function
- Standard floppy/mini-floppy select function
- FM/FMM recording system
- Built-in write compensation circuit
- Motor enable output control
- Built-in I/O address decoder
- Multi-sector function, multi-track function
- Simultaneous seek function (up to 4 units)
- Drive interface, Schmidt trigger input
- Step rate programmable
- IBM track format compatible
- CRC generation, built-in check circuit ($X16 + X12 + X5 + 1$)
- Head load time, head unload time programmable
- Data scan function
- DMA/NonDMA data transmission

7-3. Floppy disk control system

(1) TC8566AF block diagram

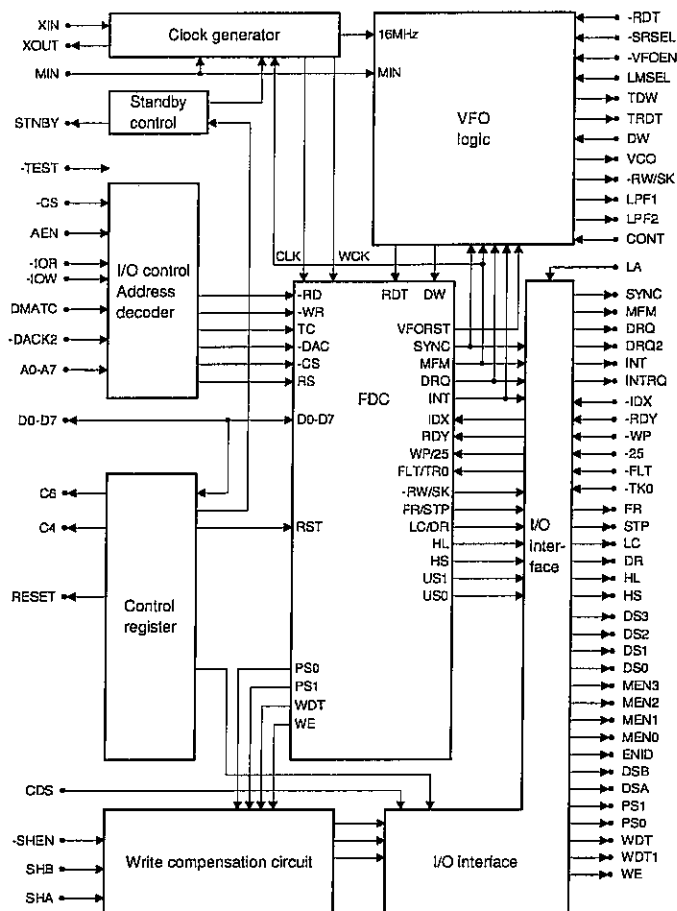


Fig. 7-2 Block diagram/

7-4. Pin table

Pin No.	I/O	Pin name	Pin No.	I/O	Pin name
1	O	C6	51		NC
2	I	IOR	52		NC
3		NC	53	I	SRSEL
4	I	LOW	54	G	VSS
5	I	A0	55	O	SYNC
6	I	A1	56	O	WDT1
7	I	A2	57	O	WE
8	I	A3	58	O	HS
9	I	A4	59	O	HL
10	I	A5	60	O	MEN3
11	I	A6	61	O	MEN2
12	I	A7	62	O	MEN1
13	I	CS	63	O	MEN0
14	I	AEN	64	G	VSS
15	IO	D0	65	V	VDD
16	IO	D1	66	O	DS3
17	IO	D2	67	O	DS2
18	IO	D3	68	O	DS1
19	IO	D4	69	O	DS0
20	IO	D5	70	O	STP
21	IO	D6	71	O	FR
22	IO	D7	72	O	LC
23	O	DRQ2	73	O	DR
24	O	INTRQ	74	G	VSS
25	O	INT	75	V	VDD
26	O	DRQ	76	I	IDX
27	G	VSS	77	I	RDY
28	G	AG	78		NC
29		NC	79		NC
30		NC	80	I	WP
31		NC	81	I	2S
32	I	DACK2	82	I	FLT
33	I	DMATC	83	I	TK0
34	I	CONT	84	O	PS1
35	I	TEST	85	O	PS0
36	IO	VCO	86	O	DSB
37	O	LPF2	87	O	DSA
38	O	LPF1	88	I	LA
39	O	TRDT	89		NC
40	I	DW	90	V	VDD
41	O	RD/SK	91		NC
42	O	TDW	92	I	CDS
43	I	LMSEL	93	I	RESET
44	I	RDT	94	I	SHB
45	O	XOUT	95	I	SHA
46	I	XIN	96	I	SHEN
47	I	VFOEN	97	O	STNBY
48	I	MIN	98	O	WDT
49	O	MFM	99	O	END
50		NC	100	O	C4

Table 7-1. Pin table

7-5. Pin description

Pin No.	Pin name	I/O	Pin description
1	C6	O	Control register C6 output
2	IOR	I	Used for data transmission from FDC to data bus
4	LOW	I	Control signal used for data transmission from FDC to data bus.
5	A0	I	Address signal
6	A1	I	
7	A2	I	
8	A3	I	
9	A4	I	
10	A5	I	
11	A6	I	
12	A7	I	
13	CS	I	FDC chip select signal
14	AEN	I	Address enable signal from CPU
15	D0	IO	Bi-directional 8-bit data bus
16	D1	IO	
17	D2	IO	
18	D3	IO	
19	D4	IO	
20	D5	IO	
21	D6	IO	
22	D7	IO	
23	DRQ2	O	DMA transmission request signal. Output signal which delayed DRQ signal. Signal stays LOW when control register ENID bit is "0."
24	INTRQ	O	Interrupt request signal outputted by FDC. Remains LOW when the control register ENID bit is "0."
25	INT	O	Interrupt request signal outputted by FDC.
26	DRQ	O	DMA transmission request signal
27	[VSS]	G	FDC digital ground
28	AG	G	VCO section analog ground
32	DACK2	I	If LOW is inputted in DMA transmission, DMA cycle becomes valid.
33	DMATC	I	Shows the completion of data transmission in DMA transmission.
34	CONT	I	VCO section control voltage input pin
35	TEST	I	Test input pin with pull-up resistor. Used in non-connect or fixed to HIGH.
36	VCO	IO	Input/output pin for test. Input in test mode, and output in normal mode. Used in non-connection.
37	LPF2	O	Output pin connected to LPF of PLL circuit. Selected after taking in frequency to connect filter in low gain side.
38	LPF1	O	Output pin connected to LPF of PLL circuit. Selected after taking in frequency to connect filter in, high gain side.
39	TRDT	O	Test output pin used in non-connect.
40	DW	I	Data window input signal when external VFO circuit is sued. Normally fixed to LOW or HIGH.
41	RW/SK	O	Shows that FDC is in read/write mode when LOW. Shows FDC is in seek mode when HIGH.
42	TDW	O	Test output pin used in non-connect.
43	LMSEL	I	VFO circuit operation mode select signal with pull-up resistor. When LOW, VFO is in operation mode without filter selection. When HIGH or non-connect, VFO is in operation mode with filter selection between high gain and low gain.
44	RDT(RDT)	I	Read data signal from floppy disk drive. When external VFO circuit is used, read data signal (RDT) is inputted from external VFO circuit.
45	XOUT	O	Output pin of reverse amplifier of crystal oscillation circuit.
46	XIN	I	Input pin of reverse amplifier of crystal oscillation circuit.
47	VFOEN	I	Internal VFO circuit select signal. When LOW, internal VFO is selected. When HIGH, external VFO is selected.
48	MIN	I	Selection input between standard floppy disk and mini-floppy disk. STandard floppy disk: LOW Mini-floppy disk: HIGH
49	MFM	O	When HIGH, MFM mode. When LOW, FM mode.

Pin No.	Pin name	I/O	Pin description																				
53	$\overline{\text{SRSEL}}$	I	This signal becomes valid when in mini-floppy mode to allow FDC operation clock selection by FDC operation mode. Pull-up resistor is provided. <table border="1"> <thead> <tr> <th>MIN</th><th>$\overline{\text{SRSEL}}$</th><th>RW/SK</th><th>FDC operation clock</th></tr> </thead> <tbody> <tr> <td>LOW</td><td>x</td><td>x</td><td>Standard mode</td></tr> <tr> <td>HIGH</td><td>HIGH or non-contact</td><td>x</td><td>Mini mode</td></tr> <tr> <td>HIGH</td><td>LOW</td><td>LOW</td><td>Mini mode</td></tr> <tr> <td>HIGH</td><td>LOW</td><td>HIGH</td><td>Standard mode</td></tr> </tbody> </table>	MIN	$\overline{\text{SRSEL}}$	RW/SK	FDC operation clock	LOW	x	x	Standard mode	HIGH	HIGH or non-contact	x	Mini mode	HIGH	LOW	LOW	Mini mode	HIGH	LOW	HIGH	Standard mode
MIN	$\overline{\text{SRSEL}}$	RW/SK	FDC operation clock																				
LOW	x	x	Standard mode																				
HIGH	HIGH or non-contact	x	Mini mode																				
HIGH	LOW	LOW	Mini mode																				
HIGH	LOW	HIGH	Standard mode																				
54	[VSS]	G	FDC digital ground																				
55	SYNC	O	Shows that FDC is reading.																				
56	WDT1	O	Write data to FDC. Output signal of writing compensation circuit. When LA signal is HIGH, active LOW. 57																				
58	HS	O	If LA signal is LOW; selects head 0 when LOW, and selects head 1 when HIGH. If LA signal is HIGH; selects head 0 when HIGH, and selects head 1 when LOW.																				
59	HL	O	Signal to instruct FDD to make contact between read/write head and disk. When LA signal is HIGH, active LOW.																				
60	MEN3	O	Third drive motor enable signal. When LA signal is HIGH, active LOW.																				
61	MEN2	O	Second drive motor enable signal. When LA signal is HIGH, active LOW.																				
62	MEN1	O	First drive motor enable signal. When LA signal is HIGH, active LOW.																				
63	MEN0	O	No. 0 drive motor enable signal. When LA signal is HIGH, active LOW.																				
64	[VSS]	G	FDC digital ground																				
65	[VDD]	V	+5V single power source. Connects all VDD pins to +5V.																				
66	DS3	O	Shows that the third drive is selected. When LA signal is HIGH, active LOW.																				
67	DS2	O	Shows that the second drive is selected. When LA signal is HIGH, active LOW.																				
68	DS1	O	Shows that the first drive is selected. When LA signal is HIGH, active LOW.																				
69	DS0	O	Shows that the No. 0 drive is selected. When LA signal is HIGH, active LOW.																				
70	STP	O	Outputs step pulse to shift the FDD head to another cylinder. When LA signal is HIGH, active LOW.																				
71	FR	O	Signal to reset FDD fault state. When LA signal is HIGH, active LOW.																				
72	LC	O	Signal to show that read/write head is in 43th cylinder or later. When LA signal is HIGH, active LOW.																				
73	DR	O	Shows step direction of head in seek mode. When LA signal is LOW; shows centrifugal direction in LOW, and inner direction in HIGH. When LA signal is HIGH; shows centrifugal direction in HIGH, and inner direction in LOW.																				
74	[VSS]	G	FDC digital ground																				
75	[VDD]	V	+5V single power. Connects all VDD pins to +5V.																				
76	$\overline{\text{IDX}}$	I	Signal to show start point in track on disk.																				
77	$\overline{\text{RDY}}$	I	Signal to show that FDD is in ready state.																				
80	$\overline{\text{WP}}$	I	Signal to show that the disk is in write-protected state.																				
81	$\overline{\text{2S}}$	I	Signal to show both-surface media is used.																				
82	$\overline{\text{FLT}}$	I	Signal to show FDD is in fault state.																				
83	$\overline{\text{TK0}}$	I	Signal to show read/write head in track 0.																				
84	PS1	O	In MFM mode, shows write compensation information. Late when PS0 is LOW and PS1 is HIGH. Early when PS0 is HIGH and PS1 is LOW. Normal when PS0 is LOW and PS1 is LOW.																				
85	PS0	O																					
86	DSB	O	FDD select signal No. 0 drive when DSB is LOW and DSA is LOW. No. 1 drive when DSB is LOW and DSA is HIGH. No. 2 drive when DSB is HIGH and DSA is LOW. No. 3 drive when DSB is HIGH and DSA is HIGH.																				
87	DSA	O																					
88	LA	I	Signal to determine logic in drive side output. When LA signal is HIGH; WDT1, WE, HS, HL, MEN0 – MEN3, DS0 ~ DS3, STP, FR, LS, DR are active LOW.																				
90	[VDD]	V	+5V single power. Connects all VDD pins to +5V.																				
92	CDS	I	When HIGH, DSB and DSA of control register are selected as drive select signals. When LOW, US1 and US0 of internal FDC block are selected as drive select signals.																				
93	RESET	I	Resets control register contents.																				

Pin No.	Pin name	I/O	Pin description
94	SHB	I	Signal to show shift quantity of write compensation circuit. In mini-floppy mode: 125ns when SHB is LOW and SHA is LOW. 250ns when SHB is LOW and SHA is HIGH. 375ns when SHB is HIGH and SHA is LOW. 500ns when SHB is HIGH and SHA is HIGH. In standard floppy mode, each value becomes 1/2.
95	SHA	I	
96	SHEN	I	Signal to make SHB and SHA valid. When SHEN is HIGH, shift quantity of write compensation circuit is 0.
97	STNBY	O	Shows that FDC is standby state. When in standby state, WDT1, WE, HS, HL, MEN0 ~ MEN3, DS0 ~ DS3, STP, FR, LC, DR signals are inactive.
98	WDT	O	Write data signal to FDD. Composed of clock bit and data bit.
99	ENID	O	Control register ENID bit output.
100	C4	O	Control register C4 output.

Table 7-1. Pin description

CHAPTER 12. EXTENSION MEMORY CARD (CE-671B/672B)

- CE-671B (2MB memory card)
- CE-672B (4MB memory card)

1. Specifications

The CE-671B/672B is the memory card inserted into internal extension memory connector. The combination is as follows:

(1) CE-671B only

One CE-671B is installed to expand by 2MB. Insertion position may be either ① or ② in Fig. 1.

$$\begin{aligned} \text{Total capacity} &= 2\text{MB (PC-6800)} \\ &+ 2\text{MB (CE-671B)} \\ &= 4\text{MB} \end{aligned}$$

(2) CE-671B x 2

Two CE-671B's are installed to expand by 4MB. Insertion position may be either ① and ② in Fig. 1.

$$\begin{aligned} \text{Total capacity} &= 2\text{MB (PC-6800)} \\ &+ 2\text{MB (CE-671B)} \\ &+ 2\text{MB (CE-671B)} \\ &= 6\text{MB} \end{aligned}$$

(3) CE-672B only

One CE-672B is inserted to expand by 4MB. Insertion position may be either ① or ② in Fig. 1.

$$\begin{aligned} \text{Total capacity} &= 2\text{MB (PC-6800)} \\ &+ 4\text{MB (CE-672B)} \\ &= 6\text{MB} \end{aligned}$$

(4) CE-671B and CE-672B

One CE-671B and one CE-672B are inserted to expand by 6MB. Insertion position may be either ① or ② in Fig. 1.

$$\begin{aligned} \text{Total capacity} &= 2\text{MB (PC-6800)} \\ &+ 2\text{MB (CE-671B)} \\ &+ 4\text{MB (CE-672B)} \\ &= 8\text{MB} \end{aligned}$$

(5) Note for memory expansion

Expansion can be made in the above four combination only. Two CE-672B's cannot be inserted. (Physically impossible.)

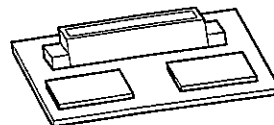
<External view>

CE-671B

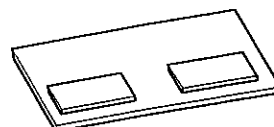
Two standard type 4M-DRAMs (TSOP) are installed on the surface, and two units of reverse type are installed on the rear surface. Total 4 units.

CE-672B

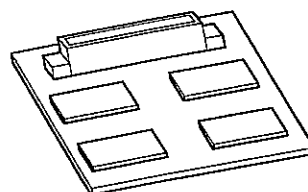
Four standard type 4M-DRAMs (TSOP) are installed on the surface, and four reverse type are installed on the rear surface.



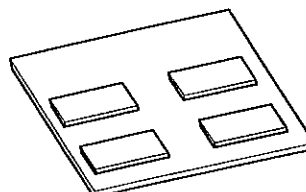
Surface



Rear
CE-671B



Surface



Rear
CE-672B

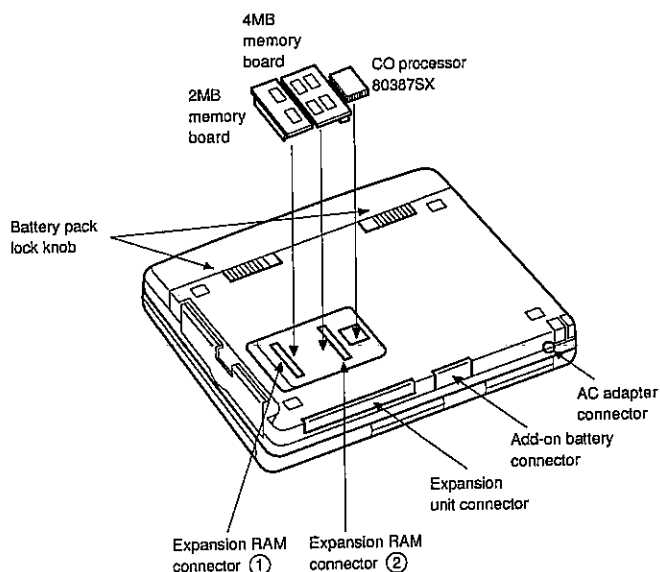


Fig. 13-1 Rear of the body

(1) CPU, COPROCESSOR, CACHE

SPST#

CHAPTER 13. CIRCUIT

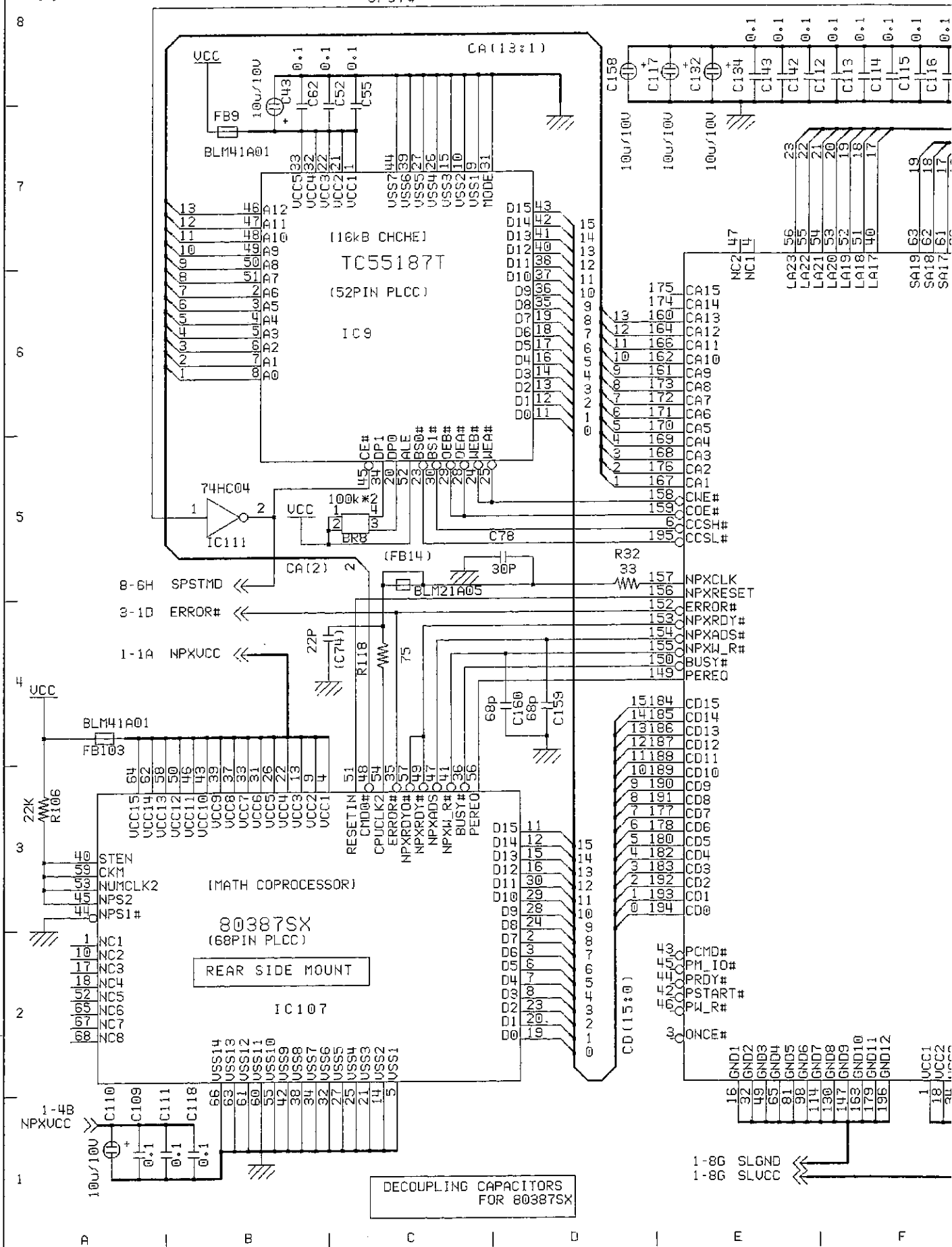
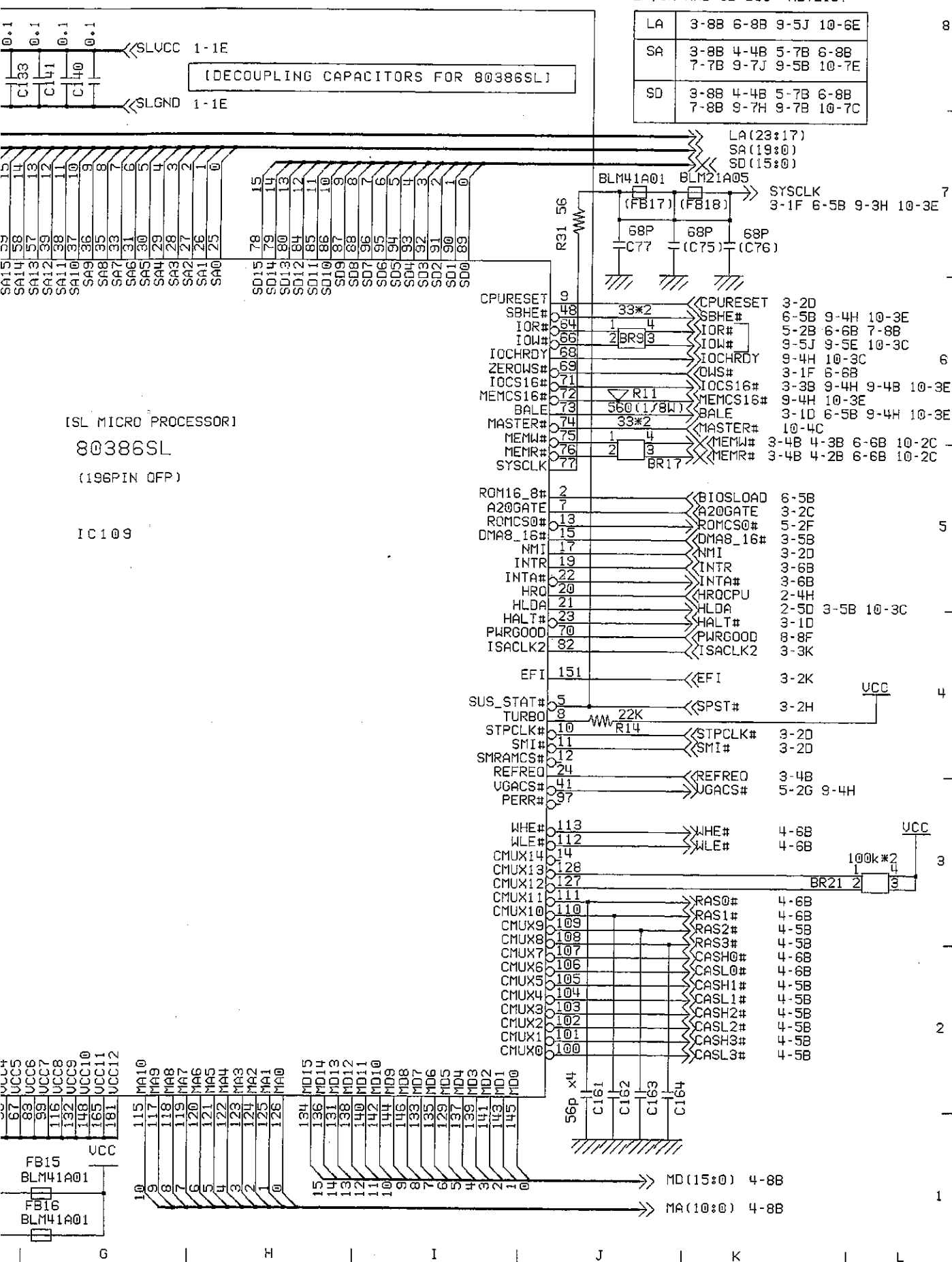
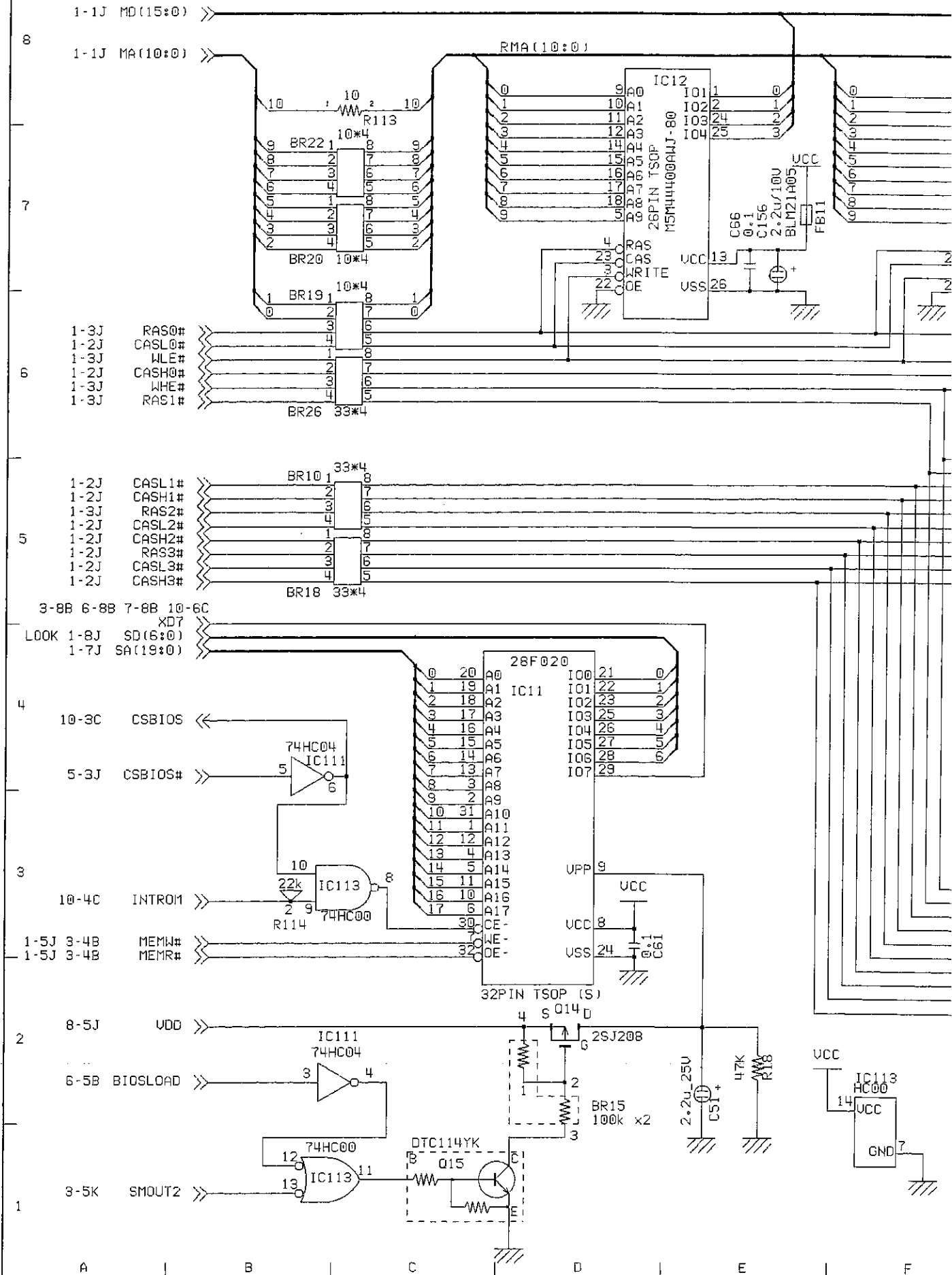
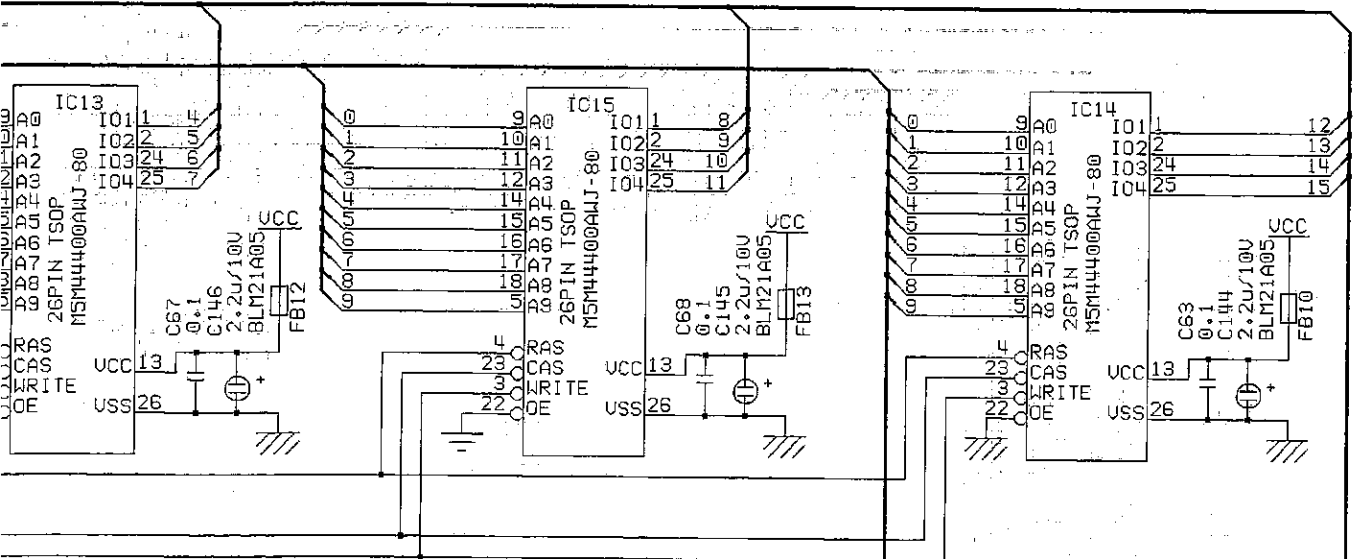


DIAGRAM AND PWB LAYOUT

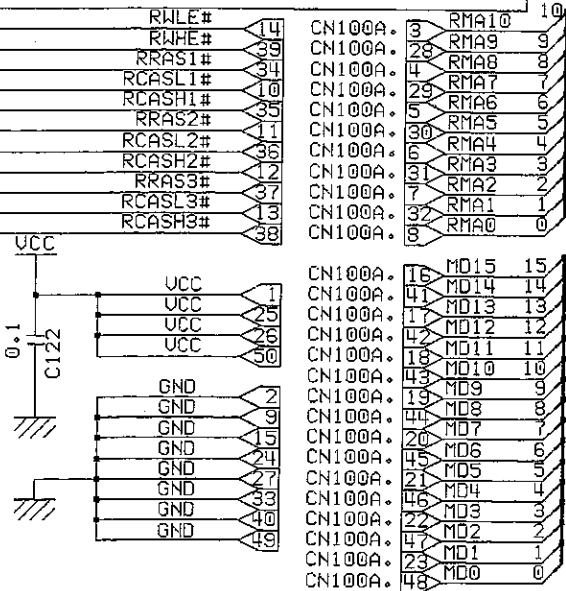
OUT NETWORK 1/10



(4) MAIN MEMORY, BIOS ROM

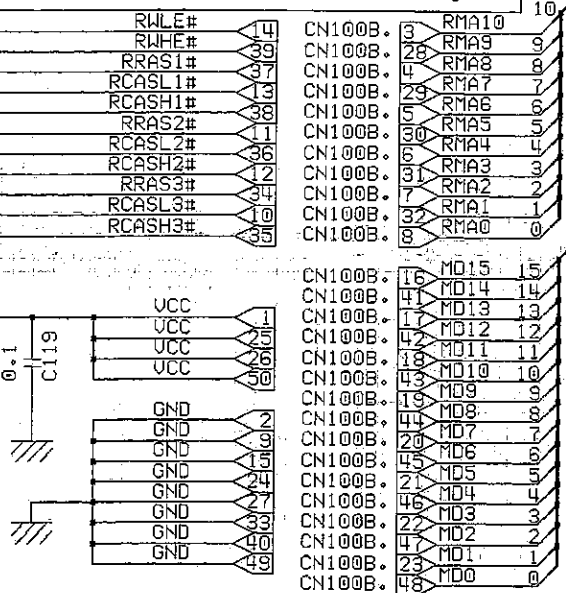


EXPANSION MEMORY BOARD (2Mbyte)



CN100A.-REAR MOUNT

EXPANSION MEMORY BOARD (4Mbyte)



CN100B.-REAR MOUNT

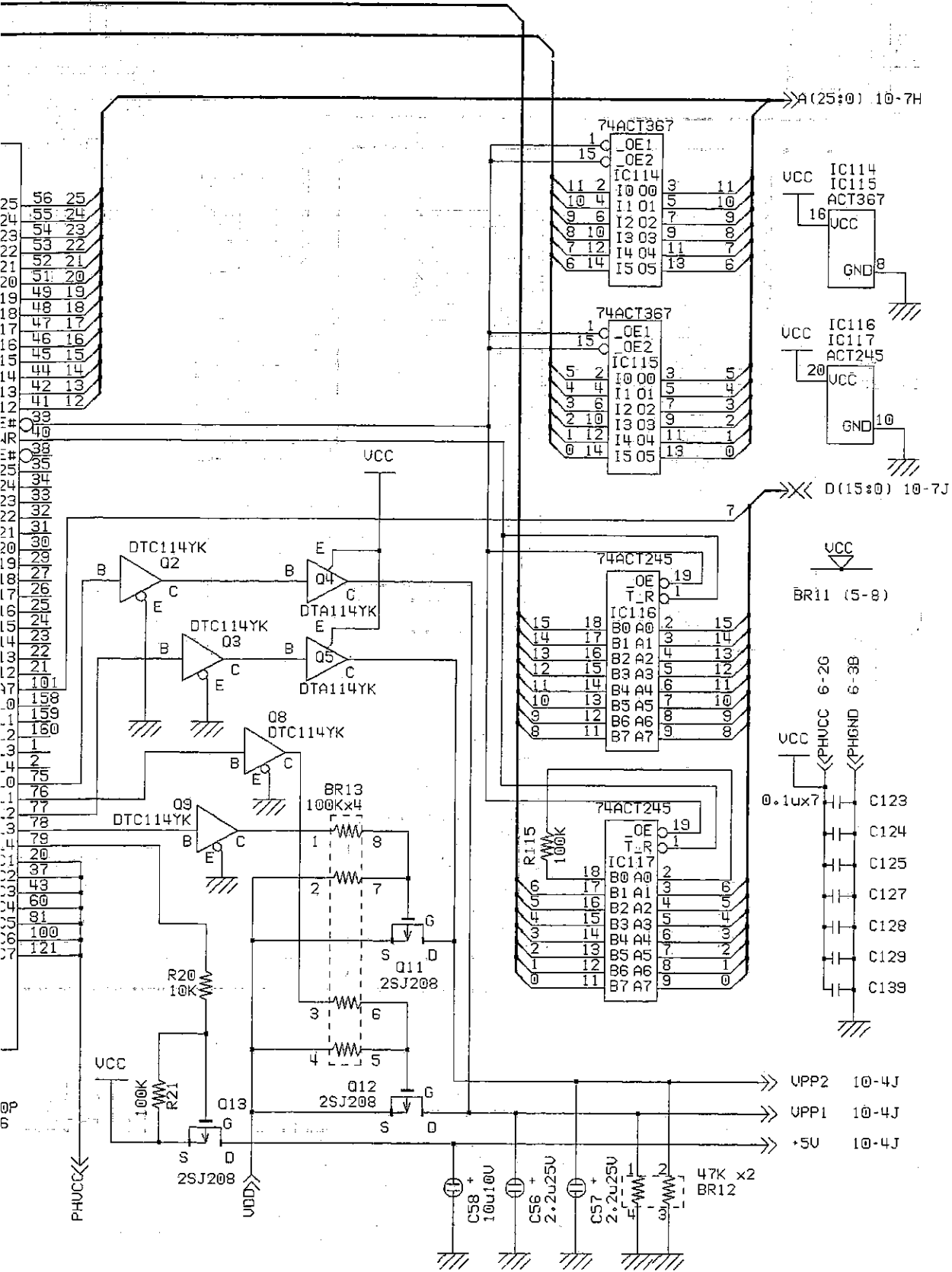
XD7>X4

```

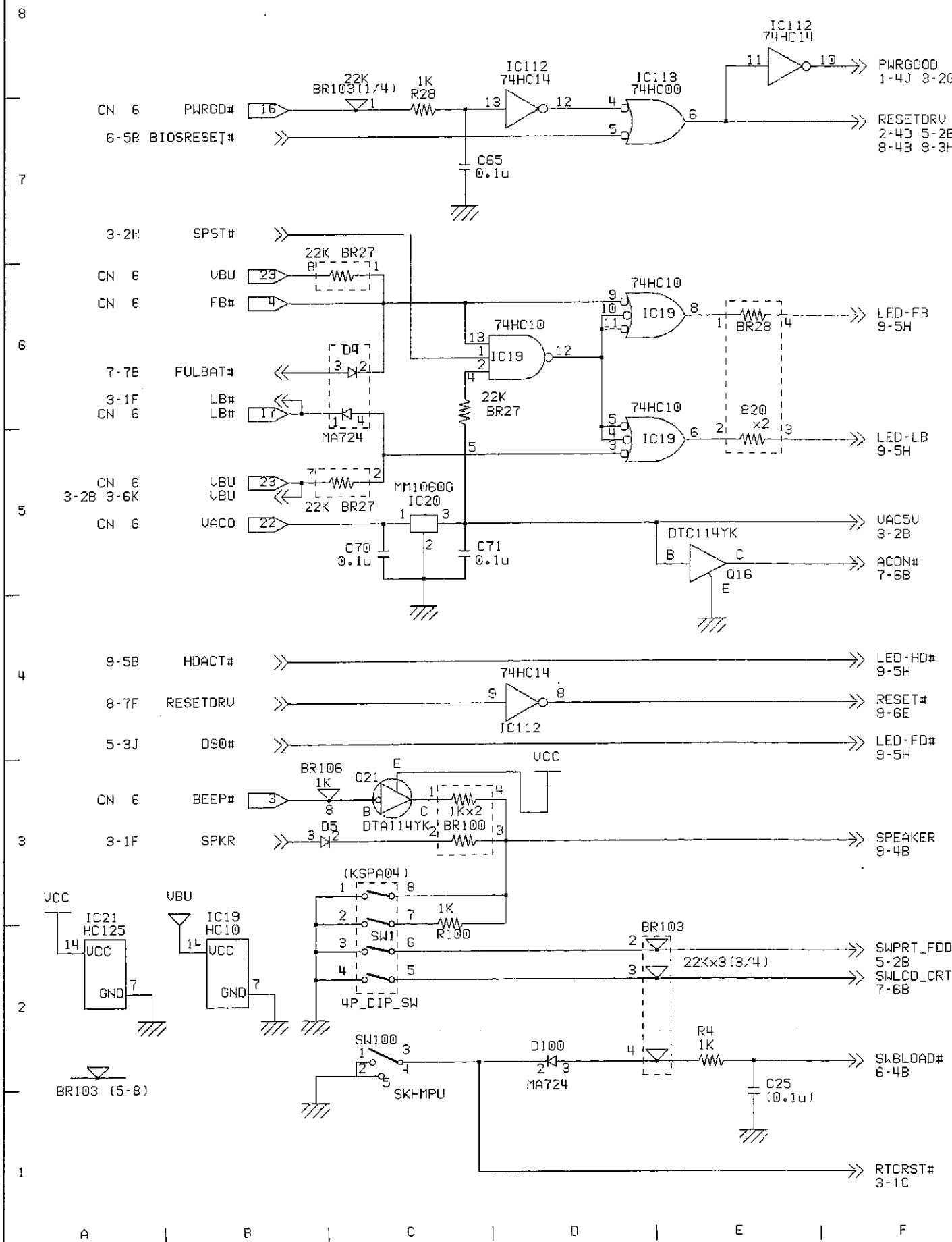
8 LOOK 1-8J SD(15:0)>><<
      1-7J SA(16:0) >>
      1-7J LA(23:17) >>

```



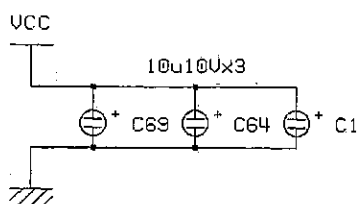
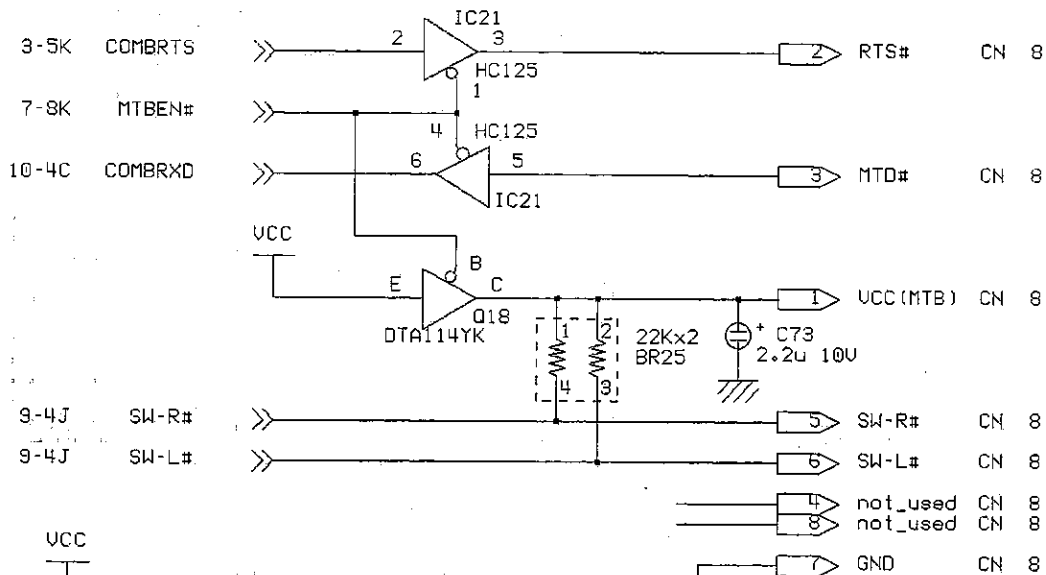
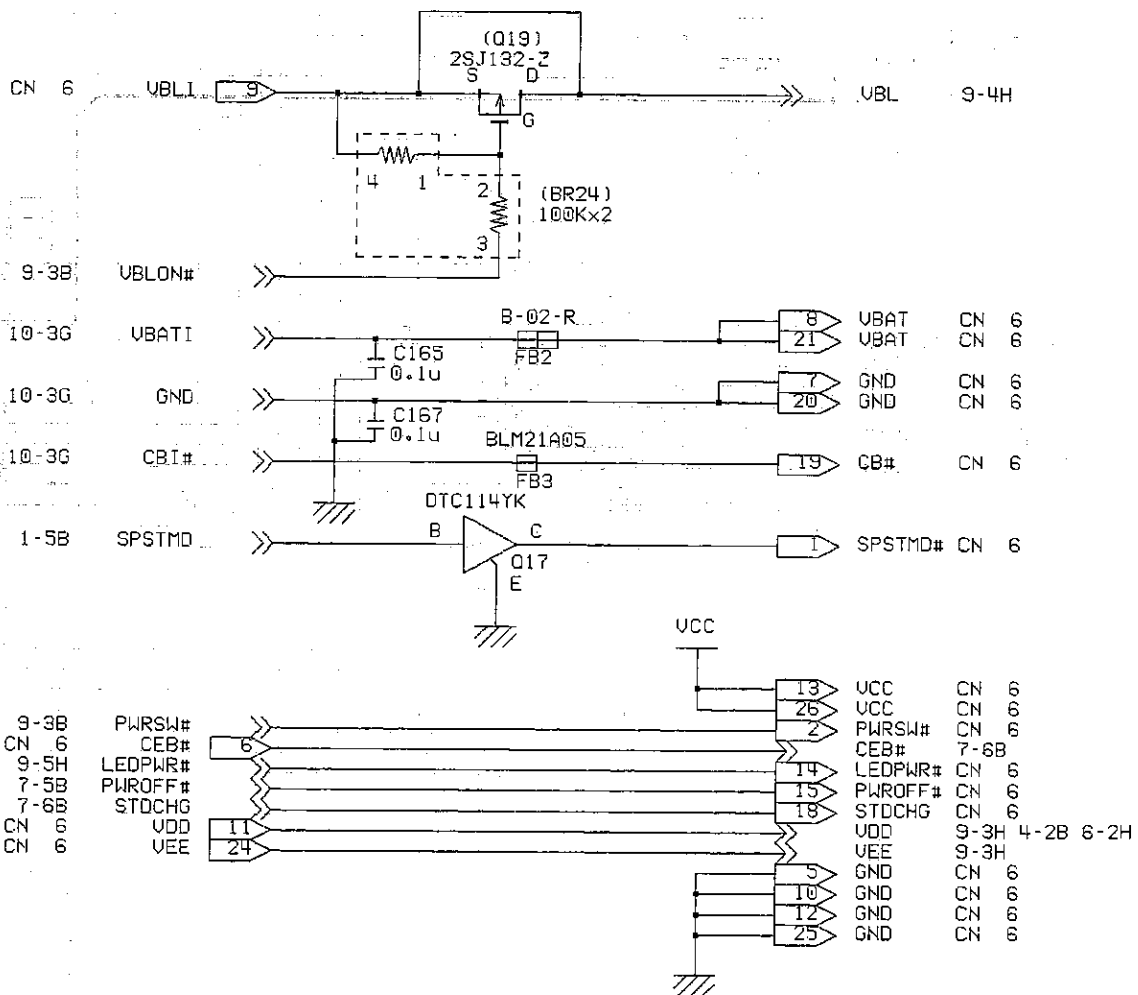


(8) INDICATOR & SWITCH

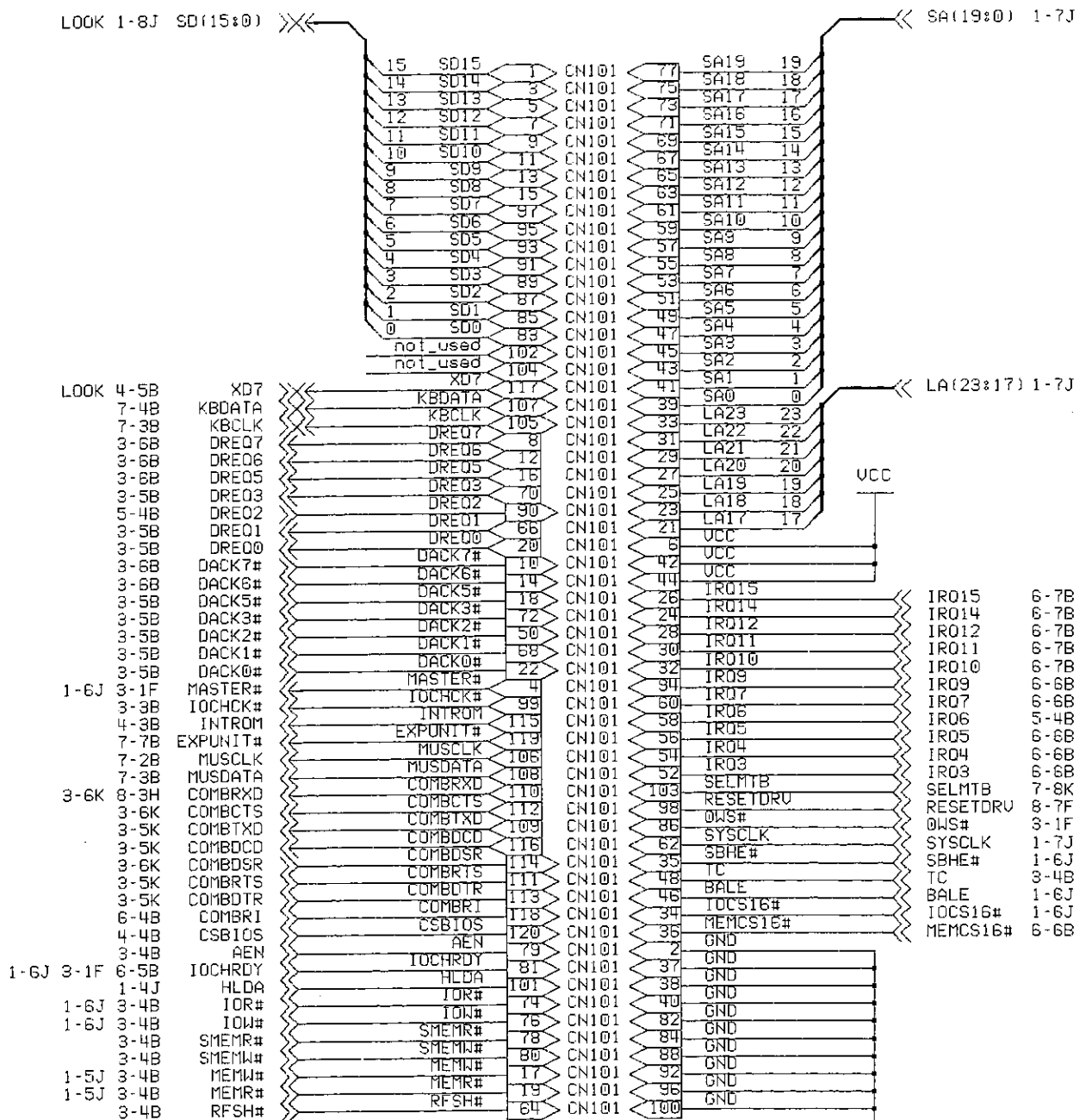


3-5B

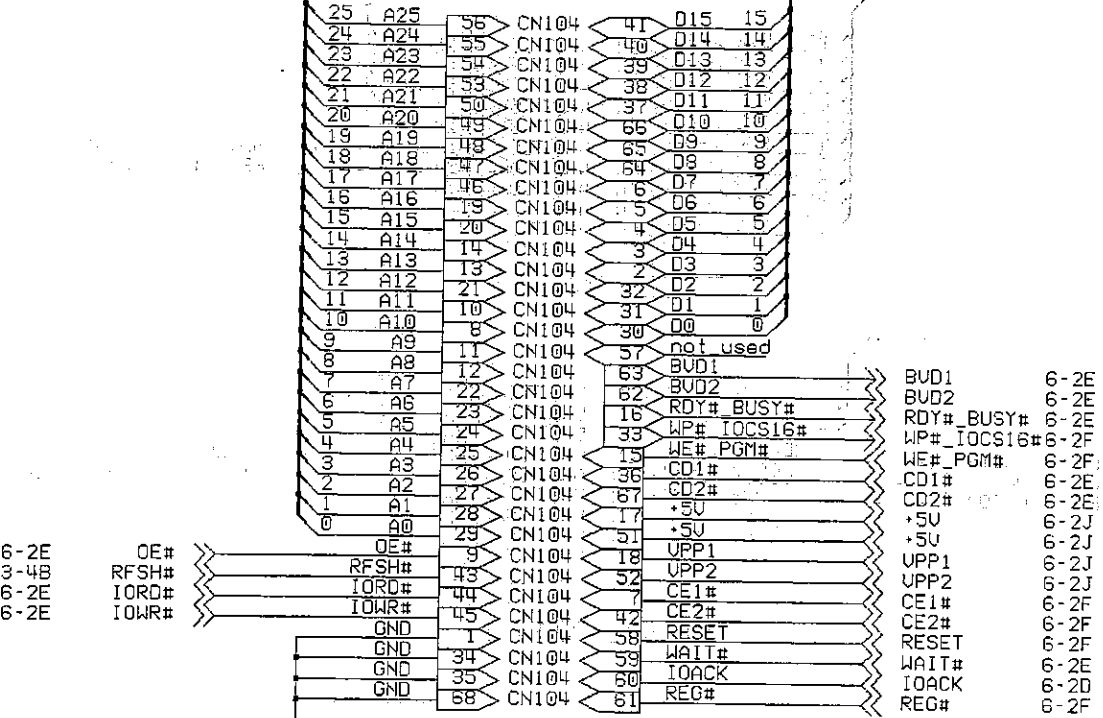
3-5B 7-8B
10-4E



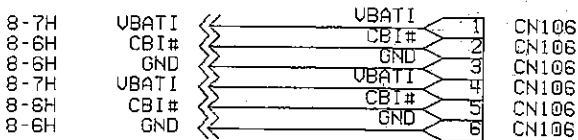
(10) MAIN BOARD CONNECTOR (REAR SIDE MOUNT)



6-7J A(25:0) >>> >>> D(0:15) 6-5J



CN104 PCMCIA CORD CN(68PIN)



CN106 BATTERY CN(6PIN)

(12) MAIN BOARD CONNECTOR TABLE (REAR SIDE MOUNT)

CN 100A. EXPANSION RAM CARD

No.	SIGNAL	No.	SIGNAL
1	VCC	26	VCC
2	GND	27	GND
3	RMA10	28	RMA9
4	RMA8	29	RMA7
5	RMA6	30	RMA5
6	RMA4	31	RMA3
7	RMA2	32	RMA1
8	RMA0	33	GND
9	GND	34	RRAS1#
10	RCASL1#	35	RCASH1#
11	RRAS2#	36	RCASL2#
12	RCASH2#	37	RRAS3#
13	RCASL3#	38	RCASH3#
14	RWLE#	39	RWHE#
15	GND	40	GND
16	MD15	41	MD14
17	MD13	42	MD12
18	MD11	43	MD10
19	MD9	44	MD8
20	MD7	45	MD6
21	MD5	46	MD4
22	MD3	47	MD2
23	MD1	48	MD0
24	GND	49	GND
25	VCC	50	VCC

CN 100B. EXPANSION RAM CARD

No.	SIGNAL	No.	SIGNAL
1	VCC	26	VCC
2	GND	27	GND
3	RMA(10)	28	RMA9
4	RMA8	29	RMA7
5	RMA6	30	RMA5
6	RMA4	31	RMA3
7	RMA2	32	RMA1
8	RMA0	33	GND
9	GND	34	RRAS3#
10	RCASL3#	35	RCASH3#
11	RRAS2#	36	RCASL2#
12	RCASH2#	37	RRAS1#
13	RCASL1#	38	RCASH1#
14	RWLE#	39	RWHE#
15	GND	40	GND
16	MD15	41	MD14
17	MD13	42	MD12
18	MD11	43	MD10
19	MD9	44	MD8
20	MD7	45	MD6
21	MD5	46	MD4
22	MD3	47	MD2
23	MD1	48	MD0
24	GND	49	GND
25	VCC	50	VCC

CN 101 EXPANSION B

No.	SIGNAL	No.	SIGNAL
2	GND	1	
4	MASTER#	3	
6	VCC	5	
8	DRE07		
10	DACK7#	9	
12	DRE06	11	
14	DACK6#	13	
16	DRE05	15	
18	DACK5#	17	
20	DRE00	19	
22	DACK0#	21	
24	IRO14	23	
26	IRO15	25	
28	IRO12	27	
30	IRO11	29	
32	IRO10	31	
34	IOCS16#	33	
36	MEMCS16#	35	
38	GND	37	
40	GND	39	
42	VCC	41	
44	VCC	43	
46	BALE	45	
48	TC	47	
50	DACK2#	49	
52	IRO3	51	
54	IRO4	53	
56	IRO5	55	
58	IRO6	57	
60	IRO7	59	

CN 105 FD

No.	SIGNAL	No.	SIGNAL
1	SIDE1SEL#	13	STEP#
2	GND	14	DSKCHG#
3	RDDT#	15	DIRIN#
4	GND	16	MTON#
5	WTPRT#	17	MS16#
6	GND	18	VCC
7	TRK00#	19	VCC
8	GND	20	DS0#
9	WTG#	21	VCC
10	GND	22	INDEX#
11	WTDI#	23	VCC
12	GND		

CN 102 KEY CN(9PIN)

No.	SIGNAL
1	X15
2	Y0
3	Y1
4	Y2
5	Y3
6	Y4
7	Y5
8	Y6
9	Y7

CN 103 KEY CN(15PI

No.	SIGNAL	No.	SIGNAL
1	X0	9	
2	X1	10	
3	X2	11	
4	X3	12	
5	X4	13	
6	X5	14	
7	X6	15	
8	X7		

CN 104 PCMCIA CORD CONNECTOR

SIGNAL
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
MEMW#
MEMR#
LA17
LA18
LA19
LA20
LA21
LA22
LA23
SBHE#
GND
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10

No.	SIGNAL	No.	SIGNAL
62	SYSCLK	61	SA11
64	RFSH#	63	SA12
66	DREQ1	65	SA13
68	DACK1#	67	SA14
70	DREQ3	69	SA15
72	DACK3#	71	SA16
74	IOR#	73	SA17
76	IOW#	75	SA18
78	SMEMR#	77	SA19
80	SMEMW#	79	AEN
82	GND	81	IOCHRDY
84	GND	83	SD0
86	OWS#	85	SD1
88	GND	87	SD2
90	DREQ2	89	SD3
92	GND	91	SD4
94	IRQ9	93	SD5
96	GND	95	SD6
98	RESETDRV	97	SD7
100	GND	99	IOCHCK#
102		101	HLDA
104		103	SELMTB
106	MUSCLK	105	KBCLK
108	MUSDATA	107	KBDATA
110	COMBRXD	109	COMBTXD
112	COMBCTS	111	COMBRTS
114	COMBDSR	113	COMBDTR
116	COMBDCD	115	INTROM
118	COMBRI	117	XO7
120	CSBIOS	119	EXPUNIT#

No.	SIGNAL	No.	SIGNAL
1	GND	35	GND
2	D3	36	CD1#
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	CE1#	41	D15
8	A10	42	CE2#
9	OE#	43	RFSH#
10	A11	44	IORD#
11	A9	45	IOWR#
12	A8	46	A17
13	A13	47	A18
14	A14	48	A19
15	WE#_PGM#	49	A20
16	RDY_BSY#	50	A21
17	+5V	51	+5V
18	UPP1	52	UPP2
19	A16	53	A22
20	A15	54	A23
21	A12	55	A24
22	A7	56	A25
23	A6	57	(N.C)
24	A5	58	RESET
25	A4	59	WAIT#
26	A3	60	IOACK
27	A2	61	REG#
28	A1	62	BUD2
29	A0	63	BUD1
30	D0	64	D8
31	D1	65	D9
32	D2	66	D10
33	WP_IOCS16#	67	CD2#
34	GND	68	GND

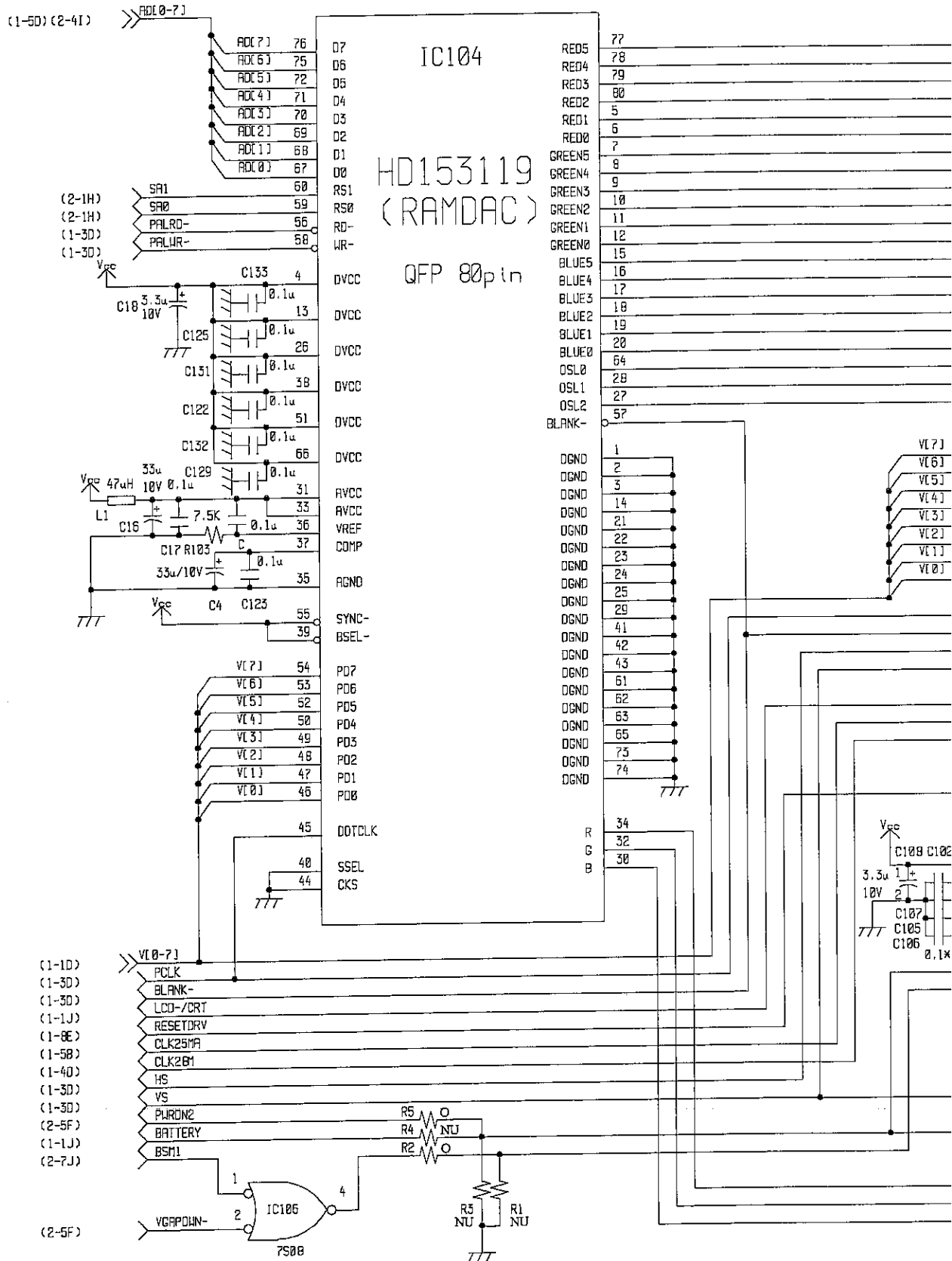
CN 106 BATTERY

GNAL
0
1
2
3
4

No.	SIGNAL	No.	SIGNAL
1	VBATI	4	VBATI
2	CBI#	5	CBI#
3	GND	6	GND



(3) RAMDAC AND TFTC



(5) DISPLAY BOARDS CONNECTOR

CN1, LCD CONNECTOR

No.	SIGNAL
1	CK
2	GND
3	HSYNC
4	VSYNC
5	R0
6	R1
7	R2
8	GND
9	G0
10	G1
11	G2
12	GND
13	B0
14	B1
15	B2
16	GND
17	(NC)
18	(NC)
19	GND
20	BLOFF
21	MDL

CN100, VIDEO BOARD

No.	SIGNAL	No.	SIGNAL
1	VCC	51	SD15
2	TFTSTB	52	SD14
3	TFTDATA	53	SD13
4	LED_PLR-	54	SD12
5	VCC	55	SD11
6	LED_LB	56	SD10
7	LED_FB	57	SD9
8	LED_FD-	58	SD8
9	LED_HD-	59	VCC
10	LED_CAPS-	60	VCC
11	LED_NUM-	61	LA17
12	LED_SCROLL-	62	LA18
13	LED_KANA	63	LA19
14	GND	64	(NC)
15	VGACS-	65	(NC)
16	VCC	66	(NC)
17	IOCS16-	67	(NC)
18	MEMCS16-	68	SBHE-
19	GND	69	GND
20	GND	70	SA0
21	OSC2	71	SA1
22	GND	72	SA2
23	BALE	73	SA3
24	VCC	74	SA4
25	SW_L-	75	SA5
26	SW_R-	76	SA6
27	SHUT-	77	SA7
28	RESUME-	78	SA8
29	(NC)	79	SA9
30	GND	80	SA10
31	SYSCLK	81	SA11
32	GND	82	SA12
33	REFRESH-	83	SA13
34	SMOUT(0)	84	SA14
35	SMOUT(1)	85	SA15
36	VGAPDOWN-	86	SA16
37	IOR-	87	SA17
38	IOW-	88	SA18
39	GND	89	SA19
40	SHEMR-	90	AEN
41	SHEML-	91	IOCHRDY
42	GND	92	SD0
43	RESETDRV	93	SD1
44	GND	94	SD2
45	VDD	95	SD3
46	GND	96	SD4
47	VEE	97	SD5
48	GND	98	SD6
49	VBL	99	SD7
50	VBL	100	IRQ9

(NO USED PIN:23,31,45,47,49,50,61,62,63)

CN101. CRT CONNECTOR

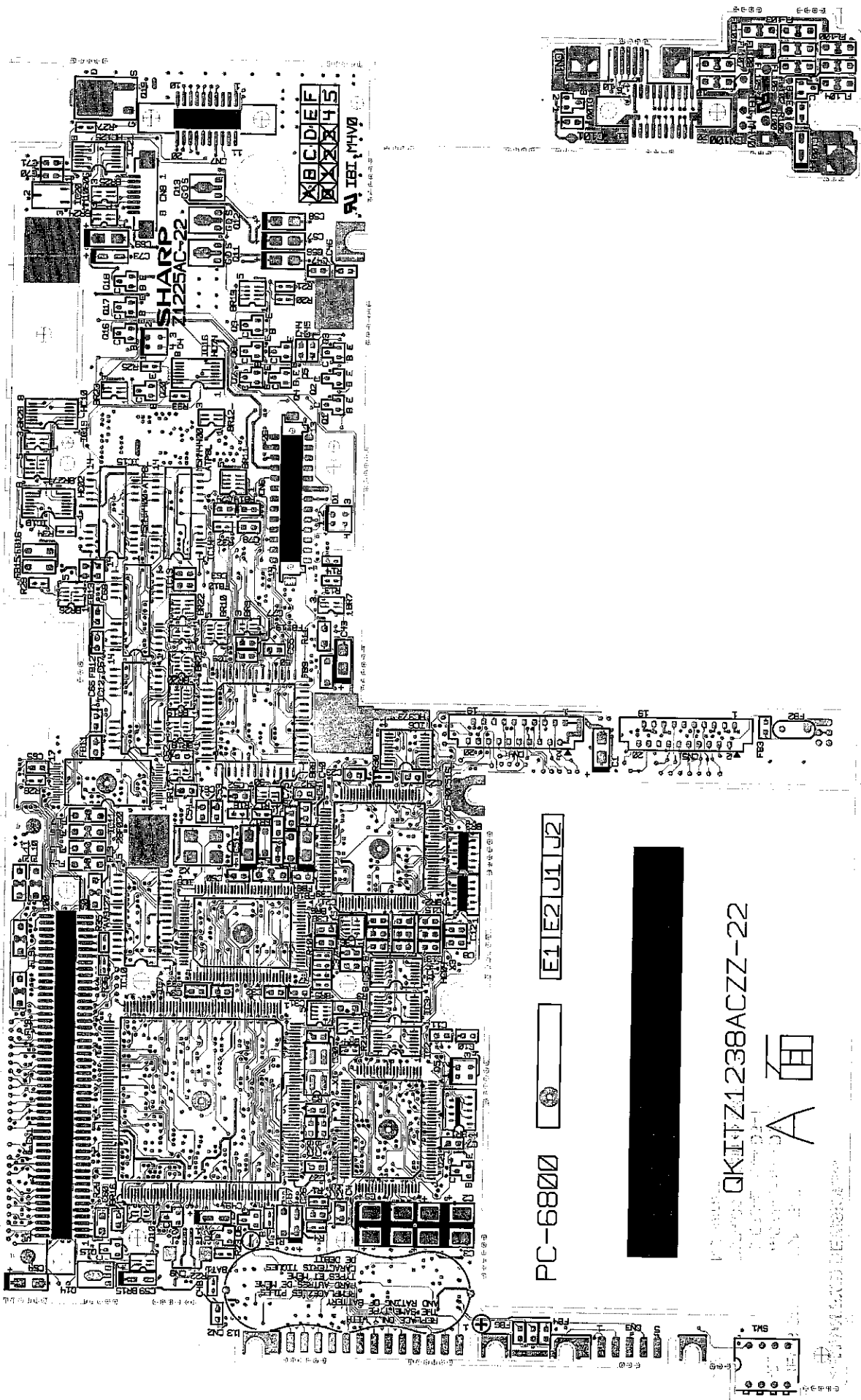
No.	SIGNAL
1	RED
2	GREEN
3	BLUE
4	(NC)
5	DGND
6	GND2
7	GND3
8	GND4
9	(NC)
10	DGND
11	REV1
12	REV2
13	HSCRT
14	VSCRT
15	(NC)

4. PWB LAYOUT

<<MAIN PWB REVISION>>

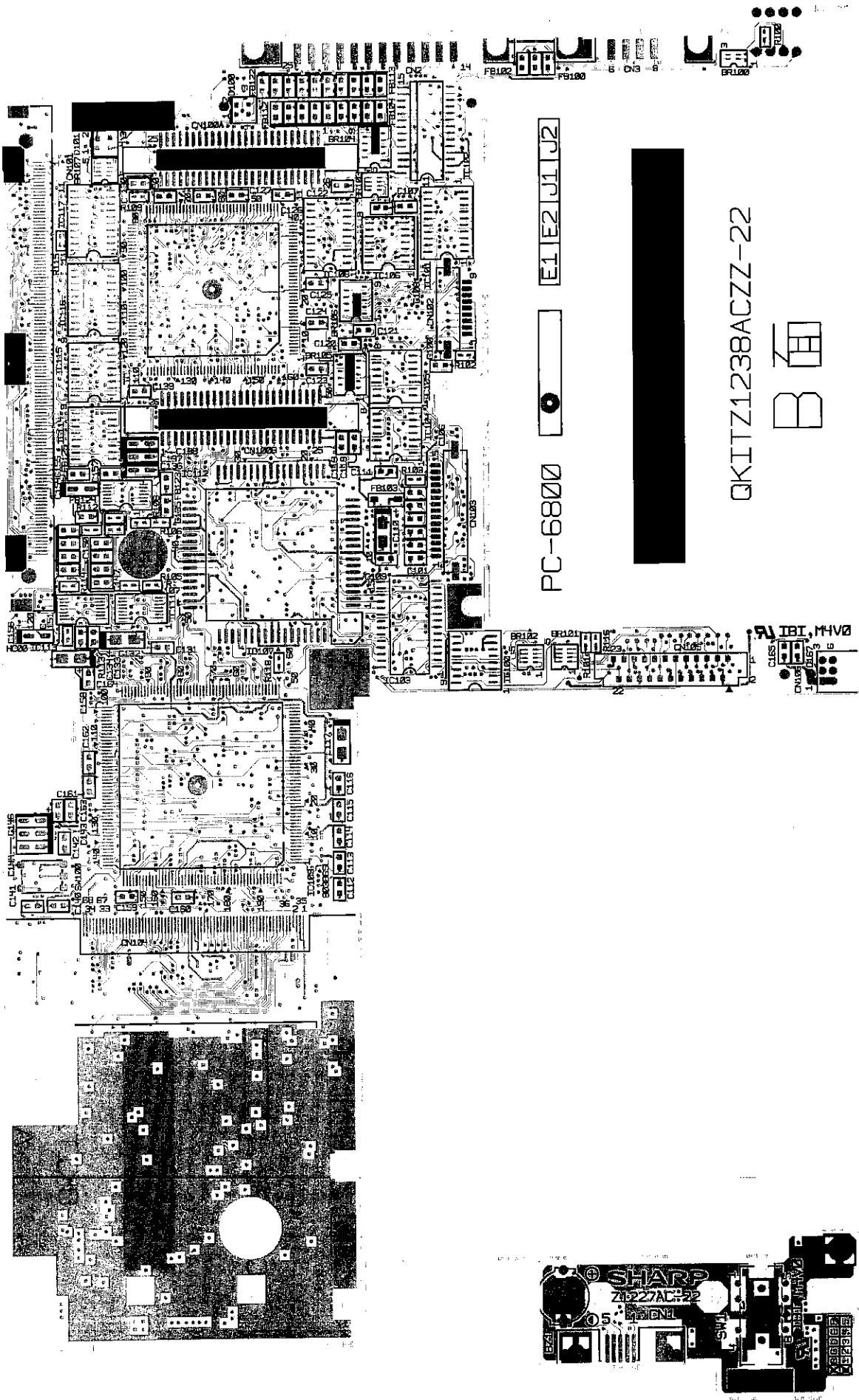
REVISION	CONTENT
-22	J1=C34-2pin ↔ D5-4pin J2=C39-2pin ↔ D5-1pin R37=IC8-100pin ↔ C37-2pin
-23	NO Jumper

(1) MAIN BOARD PWB LAYOUT [TOP VIEW] Z1238AC-22
 <<INCLUDE THE DISPLAY PWB AND THE SUB PWB>>

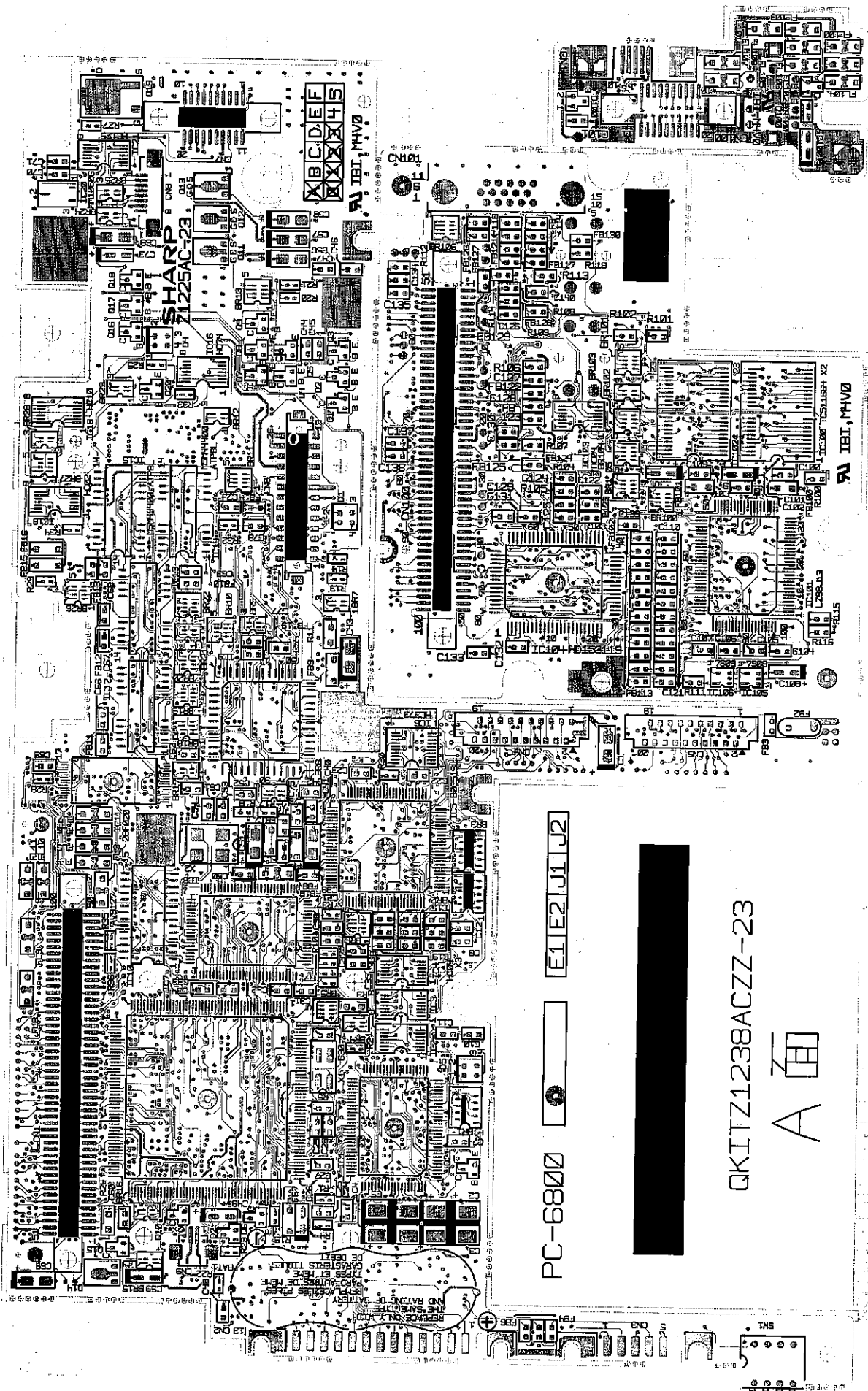


(2) MAIN BOARD PWB LAYOUT [BOTTOM VIEW] Z1238AC-22

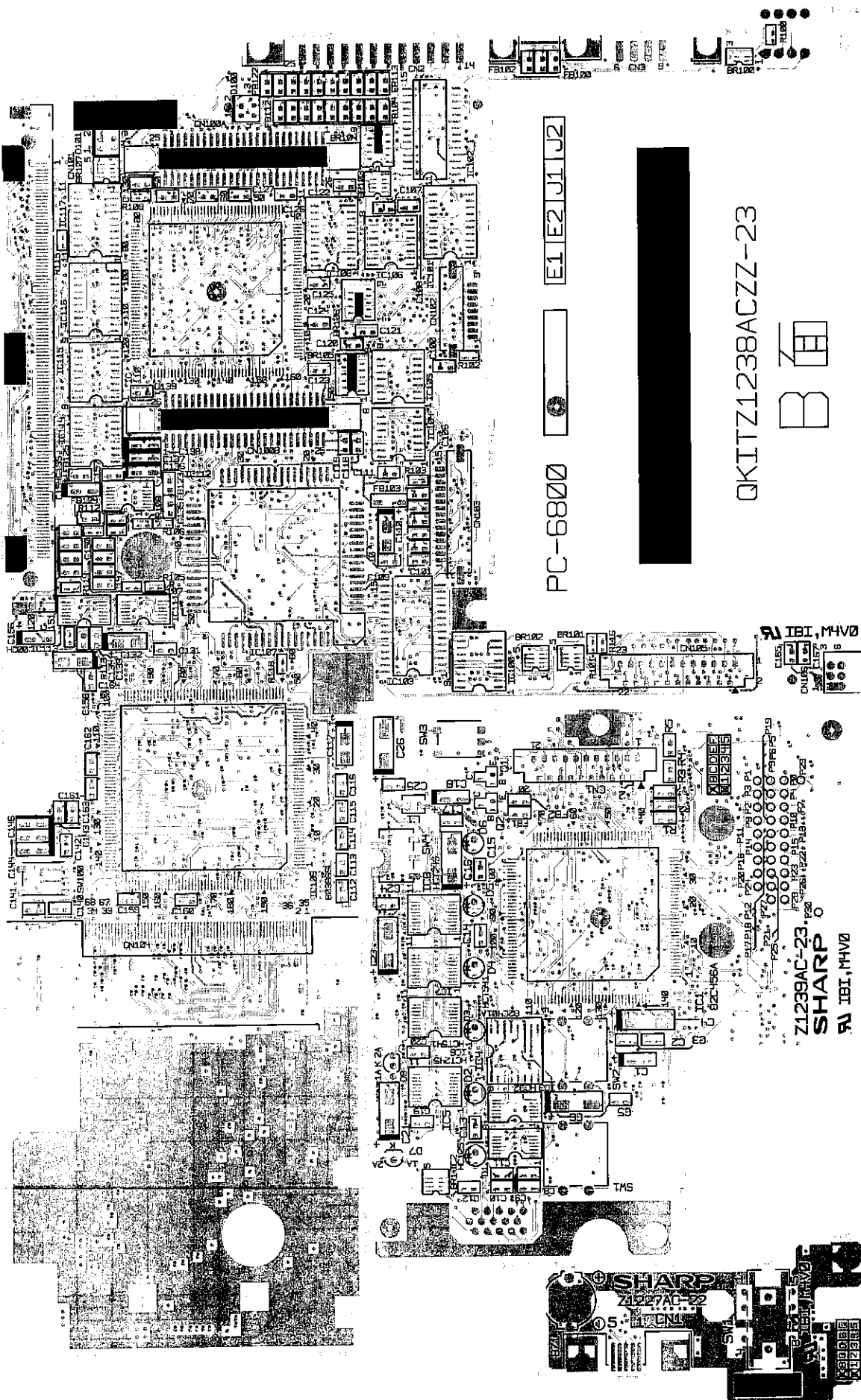
<<INCLUDE THE DISPLAY PWB AND THE SUB PWB>>



(3) MAIN BOARD PWB LAYOUT [TOP VIEW] Z1238AC-23

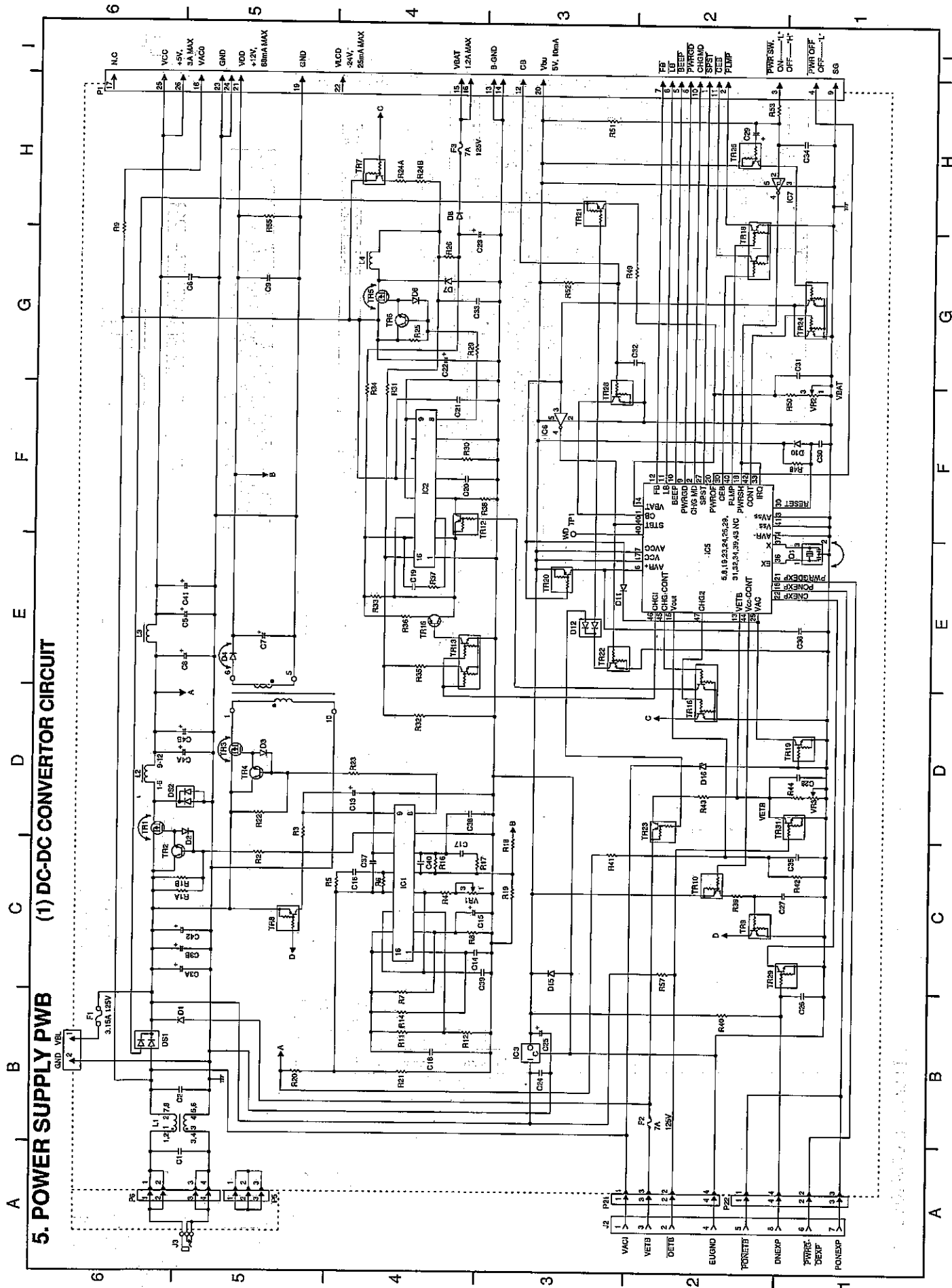


(4) MAIN BOARD PWB LAYOUT [BOTTOM VIEW] Z1238AC-23



5. POWER SUPPLY PWB (1) DC-DC CONVERTOR CIRCUIT

5. POWER SUPPLY PWB



SHARP PARTS GUIDE

MODEL PC-6881

CONTENTS

- | | |
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| 1 Exteriors | 7 Battery PWB unit |
| 2 Display unit | 8 Power supply unit |
| 3 Packing material & Accessories | 9 Inverter unit |
| 4 Main PWB unit | 10 FDD unit |
| 5 Display PWB unit | 11 Track ball unit |
| 6 Sub PWB unit | ■ Index |

Because parts marked with "▲" is indispensable for the machine safety maintenance and operation, it must be replaced with the parts specific to the product specification.

DESTINATION TABLE

U	USA
Y	Canada
G	Germany, Austria
H	U.Kingdom
Q	Australia
E	Agent

DEFINITION

The definition of each Rank is as follows and also noted in the list

A : Parts necessary to be stocked as High usage parts.

B : Parts necessary to be stocked as Standard usage parts.

C : Low usage parts.

D : Parts necessary for refurbish.

E : Unit parts recommended to be stocked for efficient after sales service.

Please note that the lead time for the said parts may be longer than normal parts.

S : Consumable parts.

Please note that the following parts used in Copier under the same description are classified into A or B Rank depending upon the place used.

Example : Gear made of Metal, Sprocket, Bearing, Belt made of Rubber, Spring clutch mechanism.

A Rank : The parts which may be with the revolution or loading.

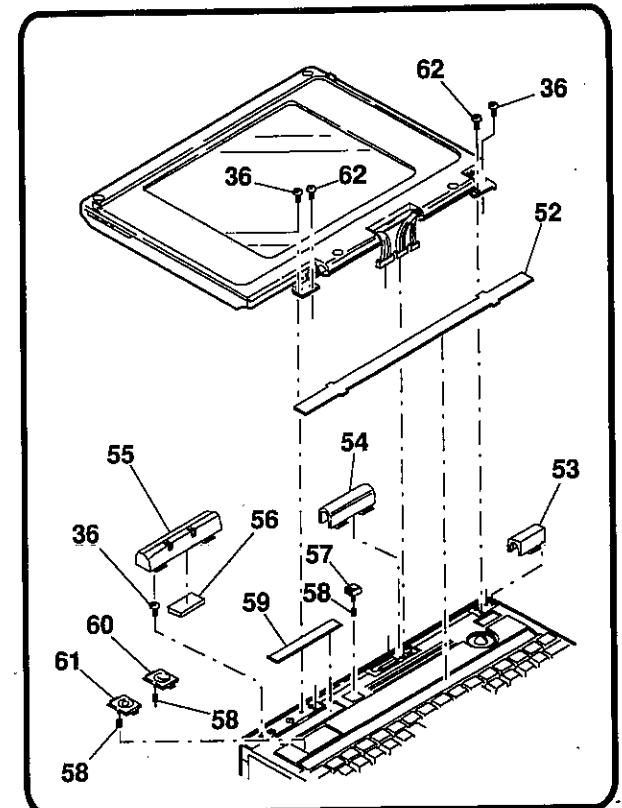
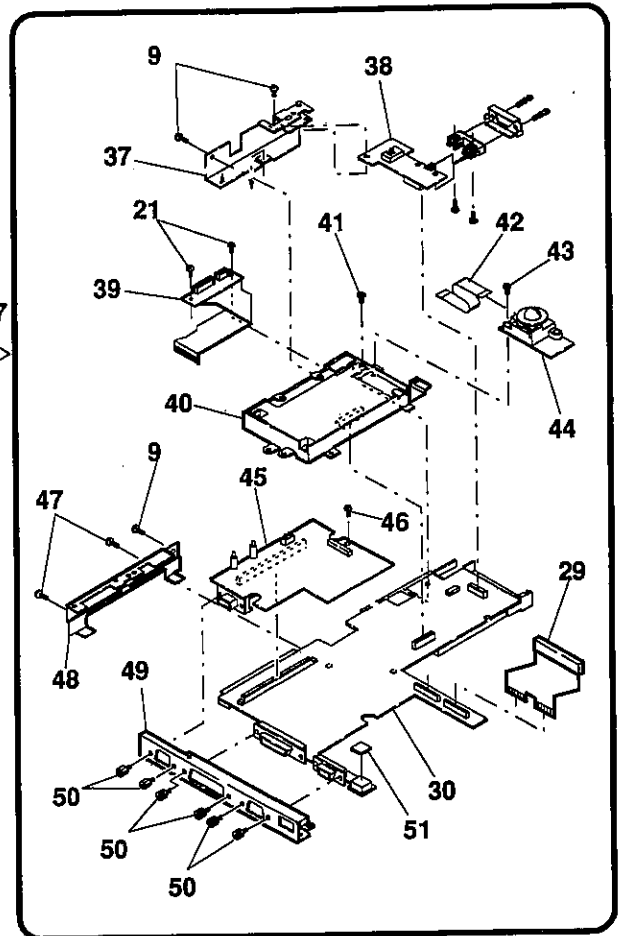
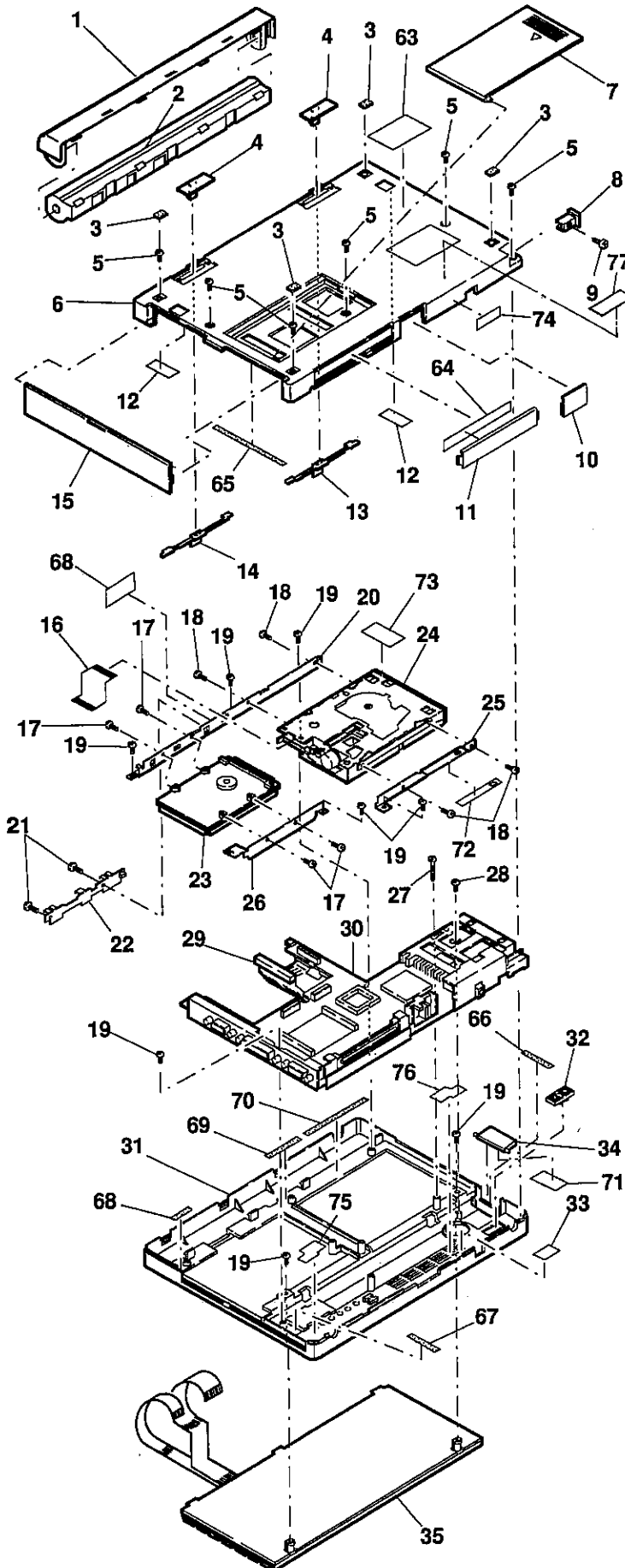
B Rank : Parts similar to A Rank parts, but are not included in Rank A.

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GC0VH1067ACZZ	AU		D	Battery cover
2	UBATN1010ACZZ	BN		B	Battery
3	GLEGG1007DCZZ	AA		C	Rubber foot
4	JKNBP1019ACZA	AC		C	Battery lock knob
5	XBBSF20P06000	AA		C	Screw (2X6)
6	GCABA1092ACZZ	BH		D	Bottom cabinet
7	GC0VA1065ACZZ	AK		D	Option cover
8	JBTN-1013ACZZ	AD		C	IC card eject button
9	XBBSF26P06000	AA		C	Screw (2.6X6)
10	GC0VH1062ACZZ	AE		D	Battery connector cover
11	GC0VH1061ACZZ	AF		D	EX-bus cover
12	PSHEZ1069ACZZ	AD		C	PVC blind sheet
13	LPLTF1038ACZZ	AG		C	Battery lock plate(Right)
14	LPLTF1037ACZZ	AG		C	Battery lock plate(Left)
15	GC0VH1064ACZZ	AH		D	D-Sub connector cover
16	QPWBM1234ACZZ	AG		C	FD FPC
17	LX-BZ1047ACZZ	AA		C	Screw
18	LX-BZ0406FCZZ	AA		C	Screw (3X4)
19	LX-BZ1051ACZZ	AA		C	Screw (2.6X8)
20	LANGT1245ACZA	AK		C	FD/HD angle
21	LX-BZ1187CCZZ	AA		C	Screw (2X2.8)
22	DUNTK2704ACZZ	AX		E	Battery PWB unit
23	DUNTK2736ACZZ	**		E	HDD unit (80MB)
24	DUNTK2688ACZZ	BW		E	FDD unit
25	LANGT1246ACZZ	AE		C	FD angle
26	LANGT1247ACZA	AF		C	HD angle
27	LX-BZ1052ACZZ	AA		C	Screw (2.6X10)
28	XJBSD20P10000	AA		C	Screw (2X10)
29	QPWBM1240ACZZ	AZ		C	HD FPC
30	CPWBZ1225ACN4	**	N	E	Main PWB unit
31	GCABB1091ACZZ	BH		D	Top cabinet
32	JKNBP1018ACZZ	AD		C	Power switch knob
33	PZETZ1052ACZZ	AB		D	PS jack insulation sheet
34	GC0VH1063ACZZ	AE		D	10 key connector cover
35	DUNT-2679ACZZ	BQ		E	Keyboard
	DUNT-2680ACZZ	BQ		E	Keyboard
	DUNT-2681ACZZ	BQ		E	Keyboard
36	XBBSD26P06000	AA		C	Screw (2.6X6)
37	LCHSM1031ACZZ	AK		C	Main chassis D
38	CPWBZ1227ACN1	CD		E	Sub PWB unit
39	QPWBM1242ACZZ	AY	N	C	LCD I/F FPC
40	RDENC1027ACZZ	CA	N	E	Power supply unit
41	XBBSD26P12000	AA		C	Screw (2.6X12)
42	QCNW-1347ACZZ	AC		C	MTB I/F cable
43	LX-BZ1050ACZZ	AC		C	Screw (2X6.6)
44	DUNT-2703ACZZ	BM		E	Track ball unit
45	CPWBZ1239ACN1	CN	N	E	Display PWB unit
46	XBBSD26P04000	AA		C	Screw (2.6X4)
47	XBPSN20P04000	AA		C	Screw (2X4)
48	LCHSM1030ACZZ	AK		C	Main chassis C
49	LCHSM1029ACZZ	AL		C	Main chassis B
50	LX-BZ1048ACZZ	AC		C	Screw (M3)
53	GC0VA1069ACZZ	AL	N	D	Dumper cover R
54	LHLDZ1029ACZB	AH	N	C	Cable holder
55	GC0VA1068ACZZ	AP	N	D	Dumper cover L
56	PFI1W1018ACZZ	AD	N	D	LED filter
57	JBTN-1010ACZZ	AD		C	Resume button
58	MSPRC1022ACZZ	AA		C	Coil spring 1
59	PFI1W1017ACZZ	AE		D	LED filter
60	JBTN-1009ACZZ	AC		C	MTB switch button R
61	JBTN-1008ACZZ	AC		C	MTB switch button L
62	XBBSD20P06000	AA		C	Screw (2X6)
63	TC AUS1028ACZZ	AB		D	Caution label
64	TLABP1697ACZZ	AD		D	Connector label
65	PCUSS1059ACZZ	AK		C	EMI cushion D
66	PCUSS1056ACZZ	AD		C	EMI cushion A
67	PCUSS1057ACZZ	AE		C	EMI cushion B
68	PCUSS1061ACZZ	AC		C	EMI cushion F
69	PCUSS1060ACZZ	AE		C	EMI cushion E
70	PCUSS1058ACZZ	AH		C	EMI cushion C
71	TLABZ1640ACZZ	AC		D	Key label
72	PSPAZ1065ACZZ	AC		C	FDD spacer
73	PSPAZ1063ACZZ	AB		C	Spacer (0.3T)
74	TC AUA1030ACZZ	AB	N	D	Caution label
75	PTPEZ1031ACZZ	AE		D	Tape L
76	PTPEZ1030ACZZ	AE		D	Tape R
77	TLABT1701ACZZ	AC	N	D	Hyatt label

(U)

1 Exteriors



2 Display unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	PCAPH1021ACZZ	AA		D	Rubber cap
2	LX-BZ1053ACZZ	AA		C	Screw (M2×6)
3	GCABD1096ACZZ	BL	N	D	Display cabinet(Front)
4	TLABP1677ACZZ	AG	N	D	Color symbol label
5	JBTN-1012ACZZ	AC		C	Stopper button R
6	MSPRC1026ACZZ	AB		C	Coil spring
7	JBTN-1011ACZZ	AC		C	Stopper button L
9	QCNW-1351ACZZ	AM	N	C	INV-LCD wire
10	QCNW-1350ACZZ	AZ	N	C	LCD cable
11	XBBSD26P06000	AA		C	Screw (2.6×6)
12	LANGF1250ACZZ	AE	N	C	Dumper angle
13	PDMP-1011ACZZ	AW	N	D	Dumper R
14	PDMP-1010ACZZ	AW	N	D	Dumper L
15	LX-BZ1147CCZZ	AA		C	Screw (2×4.5)
16	DUNTK2798ACZZ	BR	N	E	CCFT inverter unit
17	QCNW-1349ACZZ	AV	N	C	INV control cable
18	TLABH1065DCZZ	AA		D	Caution label
19	PZETZ1054ACZZ	AC	N	C	INV insulation sheet
20	LX-BZ1054ACZZ	AA		C	Screw
21	HBDGS1007ACZZ	AP	N	D	SHARP badge
22	GCABC1095ACZZ	BN	N	D	Display cabinet(Rear)
23	PGUMS1009ACZZ	AE	N	D	LCD cushion
24	LHLDN2101SCZZ	AB		C	Holder
101	DUNTK2849ACZZ	BX	N	E	Back light unit with CCFT
(Unit)					
901	DUNTG2800ACZZ	**	N	E	Display unit (Active)

3 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKC2299ACZZ	AR	N	D	Packing case
2	SPAKC2298ACZZ	AS	N	D	Packing case
3	SPAKA5416SCZZ	AB		D	Protector,handle (61400675)
4	JHNDP2008SCZZ	AB		C	Handle
5	SPAKA2295ACZZ	AK	N	D	Packing cushion(Left)
6	SPAKA2296ACZZ	AK	N	D	Packing cushion(Right)
7	SSAKA3001CCZZ	AA		D	Vinyl bag (140×360mm)
8	UBNDA1008CCZZ	AA		C	AC cord band (120mm)
9	SPAKA2250ACZZ	AE		D	Packing cushion for accessories B
10	QACCB7621QCZZ	AN		B	AC cord (250V 3A)
11	QACCV6621QCZZ	AT		B	AC cord (φ4.8 2pin) (250V 10A)
12	QACCL7620QCZZ	AW		B	AC cord (6A 250V)
13	QACCD7611QCZZ	AT		B	AC cord (U/C7A125V)
14	QACCF7622QCZZ	AX		B	AC cord (250V 3A)
15	UBATN1010ACZZ	BN		B	Battery
16	SPAKA2251ACZZ	AD		D	Packing cushion for accessories C
17	SPAKA2303ACZZ	AK	N	D	Packing case for accessories
18	RADPA1024ACZZ	BX	N	B	AC adaptor
19	RADPA1024ACZQ	BX	N	B	AC adaptor
20	RADPA1025ACZZ	BY	N	D	AC adaptor(with AC cord)
21	SPAKA2279ACZZ	AG		D	Media case
22	TLABE1635ACZZ	AF		D	Media label(Install)
23	TLABE1636ACZZ	AF		D	Media label(Operation)
24	TLABE1637ACZZ	AF		D	Media label(Shell)
25	UFLPC1001ABUB	BH	N	E	Master media(MS-DOS) (English)(V1.0B)
26	UFLPC1001ABVB	BH	N	E	Master media(MS-DOS) (English)(V1.0B)
27	UFLPC1001ABWB	BH		E	Master media(MS-DOS) (English)(V1.0B)
28	SSAKA1130QCZZ	AA		D	Vinyl bag (100×120mm)
29	SPAKP2288ACZZ	AG		D	Vinyl bag
30	SPAKA2252ACZZ	AB		D	Packing cushion D
31	TCAUS1054CCZZ	AB		C	Caution TAG
32	TLABP1675ACZZ	AB	N	D	Barcode label
33	TLABP1676ACZZ	AB	N	D	Barcode label
34	TLABP1720ACZZ	AA	N	D	Barcode label
35	UFLPC1001ACTA	BH		E	Master media(Utility) (V1.0A)
36	TLABE1668ACZZ	AH	N	D	Media label(Diag)
37	LPLTP1040ACZZ	AD		C	Template
38	SPAKA2294ACZZ	AH	N	D	Manual case
39	TGANE0056FCZZ	AF		D	Guaranty
40	TCADZ1006DCZZ	AW		D	Registration card
41	TINSE1670ACZZ	AY	N	D	Instruction book(Operation)
42	TINSE1671ACZZ	AY	N	D	Instruction book (Operation)
43	TINSE1669ACZZ	AY	N	D	Instruction book(Operation)
44	TCADZ1075ACZZ	AF		D	Registration card
45	TINSE1662ACZZ	AX		D	Instruction book(Soft)
46	SSAKA2010KCZZ	AA		D	Vinyl bag (240×300)
47	CCADZ1110AC01	AN	N	D	Service information
48	TLABB1381ACZZ	AC		D	Address label

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	UBATN1011ACZZ	AT		B	Battery (3-31FT-B)	[BAT1]
2	RR-TZ1011ACZZ	AE		B	Block resistor (22K Ω ×8)	[BR1]
3	RR-TZ1012ACZZ	AE		B	Block resistor (47K Ω ×8)	[BR2]
4	RR-TZ1012ACZZ	AE		B	Block resistor (47K Ω ×8)	[BR3]
5	RR-TZ1020ACZZ	AB		B	Block resistor (1K Ω ×2)	[BR4]
6	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR5]
7	RR-TZ1018ACZZ	AC		B	Block resistor (100K Ω ×4)	[BR6]
8	RR-TZ1019ACZZ	AB		B	Block resistor (22K Ω ×2)	[BR7]
9	RR-TZ1006ACZZ	AB		B	Block resistor (100K Ω ×2)	[BR8]
10	RR-TZ1014ACZZ	AB		B	Block resistor (33 Ω ×2)	[BR9]
11	RR-TZ1005ACZZ	AC		B	Block resistor (33 Ω ×4)	[BR10]
12	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR11]
13	RR-TZ1017ACZZ	AB		B	Block resistor (47K Ω ×2)	[BR12]
14	RR-TZ1018ACZZ	AC		B	Block resistor (100K Ω ×4)	[BR13]
15	RR-TZ1006ACZZ	AB		B	Block resistor (100K Ω ×2)	[BR15]
16	RR-TZ1006ACZZ	AB		B	Block resistor (100K Ω ×2)	[BR16]
17	RR-TZ1014ACZZ	AB		B	Block resistor (33 Ω ×2)	[BR17]
18	RR-TZ1005ACZZ	AC		B	Block resistor (33 Ω ×4)	[BR18]
19	RR-TZ1015ACZZ	AC		B	Block resistor (10 Ω ×4)	[BR19]
20	RR-TZ1015ACZZ	AC		B	Block resistor (10 Ω ×4)	[BR20]
21	RR-TZ1006ACZZ	AB		B	Block resistor (100K Ω ×2)	[BR21]
22	RR-TZ1015ACZZ	AC		B	Block resistor (10 Ω ×4)	[BR22]
23	RR-TZ1016ACZZ	AB		B	Block resistor (820 Ω ×2)	[BR23]
24	RR-TZ1019ACZZ	AB		B	Block resistor (22K Ω ×2)	[BR25]
25	RR-TZ1005ACZZ	AC		B	Block resistor (33 Ω ×4)	[BR26]
26	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR27]
27	RR-TZ1016ACZZ	AB		B	Block resistor (820 Ω ×2)	[BR28]
28	RR-TZ1020ACZZ	AB		B	Block resistor (1K Ω ×2)	[BR100]
29	RR-TZ1021ACZZ	AC		B	Block resistor (1K Ω ×4)	[BR101]
30	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR102]
31	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR103]
32	RR-TZ1008ACZZ	AE		B	Block resistor (1K Ω ×8)	[BR104]
33	RR-TZ1010ACZZ	AE		B	Block resistor (10K Ω ×8)	[BR105]
34	RR-TZ1008ACZZ	AE		B	Block resistor (1K Ω ×8)	[BR106]
35	RR-TZ1007ACZZ	AC		B	Block resistor (22K Ω ×4)	[BR107]
36	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C1]
37	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33 μ F)	[C2]
38	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33 μ F)	[C3]
39	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33 μ F)	[C4]
40	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33 μ F)	[C5]
41	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C7]
42	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C8]
43	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C10]
44	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C11]
45	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C12]
46	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C13]
47	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C14]
48	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C15]
49	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C16]
50	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C17]
51	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C18]
52	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C19]
53	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C20]
54	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C21]
55	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C22]
56	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C23]
57	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C24]
58	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C26]
59	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C27]
60	VCCSTV1HL680J	AA		C	Capacitor (50WV 68PF)	[C28]
61	VCCSTV1HL470J	AA		C	Capacitor (50WV 47PF)	[C29]
62	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C30]
63	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C31]
64	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C32]
65	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C33]
66	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C34]
67	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C35]
68	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C36]
69	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C37]
70	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C38]
71	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C39]
72	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C40]
73	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C41]
74	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C42]
75	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C43]
76	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C44]
77	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C45]
78	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C46]
79	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C47]
80	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C48]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
81	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C49]
82	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C50]
83	VCSAPJ1EE225M	AD		C	Capacitor (25WV 2.2 μ F)	[C51]
84	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C52]
85	VCCSTV1HL150J	AA		C	Capacitor (50WV 15PF)	[C53]
86	VCCSTV1HL150J	AA		C	Capacitor (50WV 15PF)	[C54]
87	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C55]
88	VCSAPJ1EE225M	AD		C	Capacitor (25WV 2.2 μ F)	[C56]
89	VCSAPJ1EE225M	AD		C	Capacitor (25WV 2.2 μ F)	[C57]
90	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C58]
91	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C59]
92	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C60]
93	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C61]
94	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C62]
95	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C63]
96	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C64]
97	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C65]
98	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C66]
99	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C67]
100	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C68]
101	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C69]
102	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C70]
103	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C71]
104	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C73]
105	VCCSTV1HL680J	AA		C	Capacitor (50WV 68PF)	[C77]
106	VCCSTV1HL300J	AA		C	Capacitor (50WV 30PF)	[C78]
107	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C100]
108	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C101]
109	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C102]
110	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C103]
111	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C104]
112	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C105]
113	VCCSTV1HL221J	AA		C	Capacitor (50WV 220PF)	[C106]
114	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C107]
115	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C108]
116	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C109]
117	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C110]
118	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C111]
119	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C112]
120	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C113]
121	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C114]
122	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C115]
123	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C116]
124	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C117]
125	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C118]
126	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C119]
127	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C120]
128	VCCSTV1HL101J	AA		C	Capacitor (50WV 100PF)	[C121]
129	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C122]
130	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C123]
131	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C124]
132	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C125]
133	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C126]
134	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C127]
135	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C128]
136	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C129]
137	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C130]
138	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C131]
139	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10 μ F)	[C132]
140	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C133]
141	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C134]
142	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C135]
143	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C136]
144	VCSAPJ1CE105M	AC		C	Capacitor (16WV 1.0 μ F)	[C137]
145	VCSAPJ1CE105M	AC		C	Capacitor (16WV 1.0 μ F)	[C138]
146	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C139]
147	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C140]
148	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C141]
149	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C142]
150	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C143]
151	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C144]
152	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C145]
153	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2 μ F)	[C146]
154	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C147]
155	VCKYTV1EB104K	AA		C	Capacitor (25WV 0.10 μ F)	[C148]
156	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C149]
157	VCKYTV1EB104K	AA		C	Capacitor (25WV 0.10 μ F)	[C150]
158	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C151]
159	VCKYTV1EB104K	AA		C	Capacitor (25WV 0.10 μ F)	[C152]
160	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.010 μ F)	[C153]

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
161	VCKYTV1EB104K	AA		C	Capacitor (25WV 0.10μF)	
162	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2μF)	[C154]
163	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2μF)	[C155]
164	VCCSTV1HL220J	AA		C	Capacitor (50WV 22PF)	[C156]
165	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10μF)	[C157]
166	VCCSTV1HL680J	AA		C	Capacitor (50WV 68PF)	[C158]
167	VCCSTV1HL680J	AA		C	Capacitor (50WV 68PF)	[C159]
168	VCCSTV1HL560J	AA		C	Capacitor (50WV 56pF)	[C160]
169	VCCSTV1HL560J	AA		C	Capacitor (50WV 56pF)	[C161]
170	VCCSTV1HL560J	AA		C	Capacitor (50WV 56pF)	[C162]
171	VCCSTV1HL560J	AA		C	Capacitor (50WV 56pF)	[C163]
172	QCNCM1191ACAJ	AR		C	Connector (100pin)	[C164]
173	QCNCW1195AC2E	AQ		C	Connector (25pin)	[CN1]
174	QCNCM1194AC0I	AQ		C	Connector (9pin)	[CN2]
175	QCNCW1185AC2J	AE		C	Connector (20pin)	[CN3]
176	QCNCW1185AC2J	AE		C	Connector (20pin)	[CN4]
177	QCNCW1190AC2F	AH		C	Connector (26pin)	[CN5]
178	QCNCM1191AC2J	AL		C	Connector (20pin)	[CN6]
179	QCNCW1189AC0H	AD		C	Connector (8pin)	[CN7]
180	QCNCM1191AC5J	AM		C	Connector (50pin)	[CN8]
181	QCNCM1191AC5J	AM		C	Connector (50pin)	[CN100A]
182	PZETZ1053ACZZ	AA		C	Insulation sheet B	[CN100B]
183	QCNCW1192ACCJ	AX		C	Connector (120pin)	[CN101]
184	QCNCW1196AC0I	AE		C	Connector (9pin)	[CN101]
185	QCNCW1197AC1E	AE		C	Connector (15pin)	[CN102]
186	LHLDZ1030ACZZ	AS		C	IC card holder	[CN103]
187	QCNCM1193AC6H	AT		C	Connector (68pin)	[CN104]
188	QCNCW1185AC2C	AF		C	Connector (23pin)	[CN104]
189	QCNCM1188AC0F	AC		C	Connector (6pin)	[CN105]
190	VHDMA724///-1	AD		B	Diode (MA724)	[CN106]
191	VHDDA204K///-1	AC		B	Diode (DA204K)	[D1]
192	VHDMA724///-1	AD		B	Diode (MA724)	[D2]
193	VHDMA724///-1	AD		B	Diode (MA724)	[D4]
194	VHDMA724///-1	AD		B	Diode (MA724)	[D5]
195	VHDMA724///-1	AD		B	Diode (MA724)	[D100]
196	RCORF6632RCZZ	AC		C	Core (B-02-R)	[D101]
197	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB2]
198	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB3]
199	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB4]
200	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB5]
201	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB6]
202	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB7]
203	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB8]
204	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB9]
205	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB10]
206	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB11]
207	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB12]
208	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB13]
209	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB15]
210	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB16]
211	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB100]
212	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB101]
213	RCORF1005ACZZ	AB		C	Core (BLM41A01)	[FB102]
214	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB103]
215	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB104]
216	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB105]
217	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB106]
218	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB107]
219	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB108]
220	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB109]
221	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB110]
222	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB111]
223	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB112]
224	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB113]
225	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB114]
226	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB115]
227	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB116]
228	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB117]
229	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB118]
230	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB119]
231	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB120]
232	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB121]
233	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB122]
234	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB123]
235	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB124]
236	RFILN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FB125]
237	RFILN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FL1]
238	RFILN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FL3]
239	RFILN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FL4]
240	RFILN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FL5]
				C	Filter (NFM41ROC470)(47pin)	[FL6]

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
241	RFiLN1010ACZZ	AD		C	Filter (NFM41ROC470)(47pin)	[FL7]
242	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL8]
243	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL9]
244	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL10]
245	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL11]
246	VHiSC14L01233	AU		B	IC (SC14L01233)	[IC1]
247	VHiSN74HC04DB	AD		B	IC (SN74HC04DB)	[IC2]
248	VHiSN74HC04DB	AD		B	IC (SN74HC04DB)	[IC3]
249	VHiSN74HC04DB	AD		B	IC (SN74HC04DB)	[IC4]
250	VHi80C51SL-BG	BF		B	IC (80C51SL-BG)	[IC5]
251	VHi74HC373DB	AG		B	IC (74HC373DB)	[IC6]
252	VHi360SLB1/-1	BZ	N	B	IC (360SLB1)	[IC7]
253	VHiTC8566AF-R	AX		B	IC (TC8566AF)	[IC8]
254	VHiTC55187-25	BF	N	B	IC (TC55187-25)	[IC9]
255	VHiAV9127-09	BB		B	IC (AV9127-09)	[IC10]
256	VHi28F020-150	BQ		B	IC (28F020-150)	[IC11]
257	VHi514400FTL8	BM		B	IC (514400FTL8)	[IC12]
258	VHi514400FTL8	BM		B	IC (514400FTL8)	[IC13]
259	VHi514400FTL8	BM		B	IC (514400FTL8)	[IC14]
260	VHi514400FTL8	BM		B	IC (514400FTL8)	[IC15]
261	VHiSN74HC74DB	AF		B	IC (SN74HC74DB)	[IC16]
262	VHiSN74HC02DB	AD		B	IC (SN74HC02DB)	[IC18]
263	VHiSN74HC10DB	AE		B	IC (SN74HC10DB)	[IC19]
264	VHiMM1060G/-1	AE		B	IC (MM1060G)	[IC20]
265	VHi74HC125DB	AE		B	IC (74HC125DB)	[IC21]
266	VHi74HC151NS	AG		B	IC (74HC151NS)	[IC100]
267	VHiALS245ANS	AK		B	IC (ALS245ANS)	[IC101]
268	VHiUPD4714GT1	AW		B	IC (UPD4714)	[IC102]
269	TLABE1290ACZZ	AB		D	ROM label	[IC103]
270	VHi27C256AA1D	BD	N	B	IC (27C256AA1D)	[IC104]
271	VHiIR2339N/-1	AE		B	IC (IR2339N)	[IC105]
272	VHiIR2339N/-1	AE		B	IC (IR2339N)	[IC106]
273	VHiALS38ANS	AE		B	IC (ALS38ANS)	[IC107]
274	QSO6C26433AC6H	AQ		C	IC socket (68pin)	[IC108]
275	VHiALS639ANS	AQ		B	IC (ALS639ANS)	[IC109]
276	VHi386SLB1-25	CS	N	B	IC (386SLB1-25)	[IC110]
277	VHi14L8AF1031	BE		B	IC (14L8AF1031)	[IC111]
278	VHiSN74HC04DB	AD		B	IC (SN74HC04DB)	[IC112]
279	VHiSN74HC14DB	AF		B	IC (SN74HC14DB)	[IC113]
280	VHiSN74HC00DB	AD		B	IC (SN74HC00DB)	[IC114]
281	VHi74ACT367FP	AG		B	IC (74ACT367FP)	[IC115]
282	VHi74ACT367FP	AG		B	IC (74ACT367FP)	[IC116]
283	VHi74ACT245FP	AK		B	IC (74ACT245FP)	[IC117]
284	VHi74ACT245FP	AK		B	IC (74ACT245FP)	[Q1]
285	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q2]
286	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q3]
287	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q4]
288	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[Q5]
289	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[Q6]
290	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q7]
291	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q8]
292	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q9]
293	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q10]
294	VSDTC114GK/-1	AB		B	Transistor (DTC114GK)	[Q11]
295	VS2SJ208-/-1	AD		B	Transistor (2SJ208)	[Q12]
296	VS2SJ208-/-1	AD		B	Transistor (2SJ208)	[Q13]
297	VS2SJ208-/-1	AD		B	Transistor (2SJ208)	[Q14]
298	VS2SJ208-/-1	AD		B	Transistor (2SJ208)	[Q15]
299	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q16]
300	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q17]
301	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q18]
302	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[Q20]
303	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q21]
304	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[R1]
305	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%)	[R2]
306	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R3]
307	VRS-TP2BD561J	AA		C	Resistor (1/8W 560Ω ±5%)	[R4]
308	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%)	[R5]
309	VRS-TS2AD106J	AA		C	Resistor (1/10W 10MΩ ±5%)	[R7]
310	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R8]
311	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R9]
312	VRS-CY1JD683G	AA		C	Resistor (0.063W 68KΩ ±2%)	[R10]
313	VRS-CY1JD153G	AA		C	Resistor (0.063W 15KΩ ±2%)	[R11]
314	VRS-TP2BD561J	AA		C	Resistor (1/8W 560Ω ±5%)	[R13]
315	VRS-CY1JD122J	AA		C	Resistor (0.063W 1.2KΩ ±5%)	[R14]
316	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R15]
317	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R17]
318	VRS-CY1JD472J	AA		C	Resistor (0.063W 4.7KΩ ±5%)	[R18]
319	VRS-CY1JD473J	AA		C	Resistor (0.063W 47KΩ ±5%)	[R20]
320	VRS-CY1JD103J	AA		C	Resistor (0.063W 10KΩ ±5%)	

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
321	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R21]
322	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%)	[R22]
323	VRS-CY1JD392J	AA		C	Resistor (0.063W 3.9KΩ ±5%)	[R23]
324	VRS-TP2BD561J	AA		C	Resistor (1/8W 560Ω ±5%)	[R24]
325	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R25]
326	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R27]
327	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%)	[R28]
328	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R29]
329	VRS-CY1JD472J	AA		C	Resistor (0.063W 4.7KΩ ±5%)	[R30]
330	VRS-TS2AD560J	AA		C	Resistor (1/10W 56Ω ±5%)	[R31]
331	VRS-CY1JD330J	AA		C	Resistor (0.063W 33Ω ±5%)	[R32]
332	VRS-CY1JD681J	AA		C	Resistor (0.063W 680Ω ±5%)	[R33]
333	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R35]
334	VRS-CY1JD103J	AA		C	Resistor (0.063W 10KΩ ±5%)	[R37]
335	VRS-CY1JD102J	AA		C	Resistor (0.063W 1.0KΩ ±5%)	[R100]
336	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R101]
337	VRS-CY1JD821J	AA		C	Resistor (0.063W 820Ω ±5%)	[R102]
338	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R103]
339	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R106]
340	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R107]
341	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R108]
342	VRS-CY1JD101J	AA		C	Resistor (0.063W 100Ω ±5%)	[R109]
343	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R110]
344	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R111]
345	VRS-CY1JD102G	AA		C	Resistor (0.063W 1.0KΩ ±2%)	[R112]
346	VRS-CY1JD100J	AA		C	Resistor (0.063W 10Ω ±5%)	[R113]
347	VRS-CY1JD223J	AA		C	Resistor (0.063W 22KΩ ±5%)	[R114]
348	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R115]
349	VRS-CY1JD750J	AA		C	Resistor (0.063W 75Ω ±5%)	[R118]
350	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW1]
351	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW2]
352	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW3]
353	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW4]
354	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW5]
355	XBBSD26P06000	AA		C	Screw (2.6×6)	[SCW6]
356	PGUMS1008ACZZ	AC		C	Rubber	[SW1]
357	QSW-Z1087ACZZ	AK		B	Dip switch (8pin)	[SW1]
358	QSW-Z1086ACZZ	AD		B	Switch (5pin)	[SW100]
359	RCRSP1057ACZZ	AH		B	Crystal (32.768KHz)	[X1]
360	RCRSP1056ACZZ	AH		B	Crystal (14.318MHz)	[X2]
361	RC-CZ1004ACZZ	AC	N	C	Capacitor (50WV 0.1μF)	[C168~C171]
(Unit)						
901	CPWBZ1225ACN4	**	N	E	Main PWB unit	

5 Display PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	RR-TZ1013ACZZ	AC		B	Block resistor (1.8KΩ×4)	[BR1]
2	RR-TZ1005ACZZ	AC		B	Block resistor (33Ω×4)	[BR100]
3	RR-TZ1005ACZZ	AC		B	Block resistor (33Ω×4)	[BR101]
4	RR-TZ1014ACZZ	AB		B	Block resistor (33Ω×4)	[BR102]
5	RR-TZ1005ACZZ	AC		B	Block resistor (33Ω×4)	[BR103]
6	RR-TZ1005ACZZ	AC		B	Block resistor (33Ω×4)	[BR104]
7	RR-TZ1005ACZZ	AC		B	Block resistor (33Ω×4)	[BR105]
8	RR-TZ1013ACZZ	AC		B	Block resistor (33Ω×4)	[BR106]
9	VCSAPJ1AE335M	AD		C	Capacitor (10WV 3.3μF)	[C1]
10	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C2]
11	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C3]
12	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33μF)	[C4]
13	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C5]
14	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33μF)	[C6]
15	VCCCTV1HH222J	AB	N	C	Capacitor (50WV 2200PF)	[C8]
16	VCCCTV1HH222J	AB	N	C	Capacitor (50WV 2200PF)	[C9]
17	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF)	[C10]
18	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF)	[C11]
19	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF)	[C12]
20	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C13]
21	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C14]
22	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C15]
23	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33μF)	[C16]
24	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C17]
25	VCSAPJ1AE335M	AD		C	Capacitor (10WV 3.3μF)	[C18]
26	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C19]
27	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C20]
28	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33μF)	[C21]
29	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33μF)	[C23]

5 Display PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
30	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C24]
31	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C25]
32	RC-SZ1001LCZZ	AF		C	Capacitor (10WV 33 μ F)	[C26]
33	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C100]
34	VCSAPJ1AE335M	AD		C	Capacitor (10WV 3.3 μ F)	[C101]
35	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C102]
36	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C103]
37	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C104]
38	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.01 μ F)	[C105]
39	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C106]
40	VCCSTV1HL102J	AA		C	Capacitor (50WV 1000PF)	[C107]
41	VCSAPJ1AE335M	AD		C	Capacitor (10WV 3.3 μ F)	[C108]
42	VCSAPJ1AE335M	AD		C	Capacitor (10WV 3.3 μ F)	[C109]
43	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C110]
44	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C111]
45	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C112]
46	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C113]
47	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C114]
48	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C115]
49	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C116]
50	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C117]
51	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C118]
52	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C119]
53	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C120]
54	VCCCTV1HH470J	AA		C	Capacitor (50WV 47pF)	[C121]
55	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C122]
56	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C123]
57	VCCCTV1HH330J	AA		C	Capacitor (50WV 33PF)	[C124]
58	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C125]
59	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C126]
60	VCCCTV1HH330J	AA		C	Capacitor (50WV 33PF)	[C127]
61	VCCCTV1HH330J	AA		C	Capacitor (50WV 33PF)	[C128]
62	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C129]
63	VCCCTV1HH330J	AA		C	Capacitor (50WV 33PF)	[C130]
64	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C131]
65	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C132]
66	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C133]
67	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C134]
68	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C135]
69	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C137]
70	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C138]
71	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10 μ F)	[C139]
72	VCCCTV1HH330J	AA		C	Capacitor (50WV 33PF)	[C140]
73	QCNCW1185AC2A	AF		C	Connector (21pin)	[CN1]
74	QCNCW1186ACA	AR		C	Connector (100pin)	[CN100]
75	QCNCW1187AC1E	AM		C	Connector (15pin)	[CN101]
76	VHPHLM-1790	AD		B	LED (HLMP-1790)	[D1]
77	VHPHLM-1790	AD		B	LED (HLMP-1790)	[D2]
78	VHPHLM-1790	AD		B	LED (HLMP-1790)	[D3]
79	VHPHLM-1790	AD		B	LED (HLMP-1790)	[D4]
80	VHPHLM-1790	AD		B	LED (HLMP-1790)	[D5]
81	VHPGL3ED8	AC		B	LED (GL3ED8)	[D7]
82	VHPGL3ED8	AC		B	LED (GL3ED8)	[D8]
83	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB1]
84	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB2]
85	RCORF1009ACZZ	AC	N	C	Core (BLM32A06)	[FB100]
86	RCORF1009ACZZ	AC	N	C	Core (BLM32A06)	[FB101]
87	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB102]
88	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB103]
89	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB104]
90	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB105]
91	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB106]
92	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB107]
93	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB108]
94	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB109]
95	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB110]
96	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB111]
97	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB112]
98	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB113]
99	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB114]
100	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB115]
101	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB116]
102	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB117]
103	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB118]
104	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB119]
105	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB120]
106	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB121]
107	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB122]
108	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB123]
109	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB124]

5 Display PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
110	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB125]
111	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB126]
112	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB127]
113	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB128]
114	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB129]
115	RCORF1008ACZZ	AB		C	Core (BLM21A05)	[FB130]
116	VHI82C456A/-1	BW		B	IC (82C456A)	[IC1]
117	VHI74HC125DB/-	AE		B	IC (74HC125DB)	[IC2]
118	VHI74HC125DB	AD		B	IC (SN74HC32DB)	[IC3]
119	VHI82C401A/-1	AY		B	IC (82C401A)	[IC4]
120	VHI74HCT245DB	AM		B	IC (74HCT245DB)	[IC5]
121	VHI74HCT541DB	AM	N	B	IC (74HCT541DB)	[IC6]
122	VHI74HCT541DB	AM	N	B	IC (74HCT541DB)	[IC7]
123	VHI74HCT245DB	AM		B	IC (74HCT245DB)	[IC8]
124	VHI511664BTL1	BA	N	B	IC (511664BTL1)	[IC100]
125	VHILZ98J13/-1	BB	N	B	IC (LZ98J13)	[IC101]
126	VHI511664BTL1	BA	N	B	IC (511664BTL1)	[IC102]
127	VHISN74HC04DB	AD		B	IC (SN74HC04DB)	[IC103]
128	VHIHD153119-1	BH		B	IC (HD153119)	[IC104]
129	VHITC7S08F/-1	AC		B	IC (TC7S08F)	[IC105]
130	VHITC7S08F/-1	AC		B	IC (TC7S08F)	[IC106]
131	RCILZ1013ACZZ	AC	N	C	Coil (LQH3C470K04)	[L1]
132	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q1]
133	VSDTC114YK/-1	AC		B	Transistor (DTC114YE)	[Q2]
134	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R2]
135	VRS-CY1JD000J	AA		C	Resistor (0.063W 0Ω ±5%)	[R5]
136	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R101]
137	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R102]
138	VRS-CY1JD752J	AA		C	Resistor (0.063W 7.5KΩ ±5%)	[R103]
139	VRS-CY1JD750J	AA		C	Resistor (0.063W 75Ω ±5%)	[R104]
140	VRS-CY1JD750J	AA		C	Resistor (0.063W 75Ω ±5%)	[R105]
141	VRS-TS2AD220J	AA		C	Resistor (1/10W 22Ω ±5%)	[R106]
142	VRS-CY1JD750J	AA		C	Resistor (0.063W 75Ω ±5%)	[R107]
143	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R108]
144	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R109]
145	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R111]
146	VRS-CY1JD821J	AA		C	Resistor (0.063W 820Ω ±5%)	[R112]
147	VRS-CY1JD330J	AA		C	Resistor (0.063W 33Ω ±5%)	[R113]
148	VRS-CY1JD330J	AA		C	Resistor (0.063W 33Ω ±5%)	[R114]
149	VRS-CY1JD104J	AA		C	Resistor (0.063W 100KΩ ±5%)	[R118]
150	PSHEZ1070ACZA	AC		C	Spacer sheet	[SHE1(FOR SW4)]
151	PSPAZ1061ACZZ	AA		C	LED spacer (1.5)	[SPA1(FOR D1)]
152	PSPAZ1061ACZZ	AA		C	LED spacer (1.5)	[SPA2(FOR D2)]
153	PSPAZ1061ACZZ	AA		C	LED spacer (1.5)	[SPA3(FOR D3)]
154	PSPAZ1061ACZZ	AA		C	LED spacer (1.5)	[SPA4(FOR D4)]
155	PSPAZ1061ACZZ	AA		C	LED spacer (1.5)	[SPA5(FOR D5)]
156	PSPAZ1062ACZZ	AA		C	LED spacer (9.2)	[SPA6(FOR D6)]
157	PSPAZ1062ACZZ	AA		C	LED spacer (9.2)	[SPA7(FOR D7)]
158	QSW-Z1085ACZZ	AE		B	Dip switch (4pin)	[SW1]
159	QSW-Z1085ACZZ	AE		B	Dip switch (4pin)	[SW2]
160	QSW-Z1086ACZZ	AD		B	Switch (5pin)	[SW3]
161	QSW-P1088ACZZ	AE		B	Switch (3pin)	[SW4]
(Unit)						
901	CPWBZ1239ACN1	CN	N	E	Display PWB unit	

6 Sub PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	RALMB1001ACZZ	AN		B	Buzzer	[BZ1]
2	VCSAPJ1AE225M	AC		C	Capacitor (10WV 2.2μF)	[C100]
3	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C101]
4	QCNCW1198AC1J	AQ		C	Connector (10pin)	[CN1]
5	QCNCW1184AC2J	AL		C	Connector (20pin)	[CN100]
6	VHDDAP202K/-1	AB		B	Diode (DAP202K)	[D100]
7	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL100]
8	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL101]
9	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL102]
10	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL103]
11	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL104]
12	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL105]
13	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL106]
14	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL107]
15	RFiLN1011ACZZ	AD		C	Filter (NFM41ROC221)(220pin)	[FL108]
16	VS2SC2412KS-1	AB		B	Transistor (2SC2412KS)	[Q100]
17	VRS-CY1JD182J	AA		C	Resistor (0.063W 1.8KΩ ±5%)	[R100]
18	XBBSD20P06000	AA		C	Screw (2×6)	[SCW1]

6 Sub PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
19	XBBSD20P06000	AA		C	Screw (2X6) [SCW2]
20	QSW-S1084ACZZ	AH		B	Slide switch [SW1]
21	LCHSM1028ACZZ	AF		C	Main chassis A
	(Unit)				
901	CPWBZ1227ACN1	CD		E	Sub PWB unit

7 Battery PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	MSPRP1024ACZZ	AD		C	Battery terminal A
2	MSPRP1025ACZZ	AD		C	Battery terminal B
3	QCNCW1183AC0F	AE		C	Connector (6pin)
	(Unit)				
901	DUNTK2704ACZZ	AX		E	Battery PWB unit

8 Power supply unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0BRNJD3335C3	AM	N	C	Capacitor (22 μ 20V) [C3AB,C22]
2	0BRNJD3335C4	AM	N	C	Capacitor (33 μ 10V) [C4AB]
3	0BRNJD3335C7	AM	N	C	Capacitor (6.8 μ 25V) [C7,C42]
4	0BRNJD3335C23	AM	N	C	Capacitor (3.3 μ 25V) [C23]
5	0BRNJD3335C5	AE	N	C	Capacitor (220 μ 6.3V) [C5]
6	0BRNJD3335C8	AE	N	C	Capacitor (100 μ 6.3V) [C8,C41]
7	0BRNJD3335F2	AM	N	A	Fuse (127V7A) [F2,3]
8	0BRNJD3335DS1	AR	N	B	Diode (FMB-24L SB100-05J) [DS1,2]
9	0BRNJD3178TR1	AX	N	B	FET (2SJ241) [TR1]
10	0BRNJD3178TR5	AV	N	B	FET (2SJ224) [TR5]
11	0BRNJD3335L1	AY	N	C	Choke coil [L1]
12	0BRNJD3335L2	BC	N	C	Choke coil [L2]
13	0BRNJD3335L3	AM	N	C	Choke coil [L3]
14	0BRNJD3178L4	AX	N	C	Choke coil [L4]
15	0BRNJD3335T1	BD	N	C	Transformer [T1]
16	0BRNJD3178CN1	AG		C	Connector (DF11-26DP-2DSA) [CN1]
17	0BRNJD3335CN2	BA	N	C	Harness [CN2]
18	0BRNJD3178CN3	AG		C	Connector (HEC0470-01-640) [CN3]
19	0BRNJD3335CN4	AE	N	C	Connector (B2B-EH) [CN4]
	(Unit)				
901	RDENC1027ACZZ	CA	N	E	Power supply unit

9 Inverter unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0IX7559-0269	AA	N	C	Resistor (4.7K Ω 1/10W) [R1,2,16,17,18,38,39,40,41]
2	0IX7558-4794	AA	N	C	Resistor (47K Ω 1/10W) [R3,33]
3	0IX7558-6849	AA		C	Resistor (CHP-R2-684JT)(680K Ω 1/10W) [R4,34]
4	0IX7558-1083	AA	N	C	Resistor (100K Ω 1/10W) [R5,6,36]
5	0IX7558-3329	AA		C	Resistor (CHP-R2-332JT)(3.3K Ω 1/10W) [R7]
6	0IX7559-0326	AB	N	C	Resistor (15K Ω 1/10W) [R8,27]
7	0IX7559-0271	AB	N	C	Resistor (3.9K Ω 1/10W) [R9,28]
8	0IX7558-1518	AB	N	C	Resistor (150 Ω 1/10W) [R10,19]
9	0IX7559-0315	AA	N	C	Resistor (1.8K Ω 1/10W) [R11]
10	0IX7558-1061	AA		C	Resistor (CHP-R2-102JT)(1.0K Ω 1/10W) [R12]
11	0IX7557-0085	AB	N	C	Resistor (330 Ω 1/8W) [R3,23,25]
12	0IX7557-0096	AB	N	C	Resistor (150 Ω 1/8W) [R14]
13	0IX7559-0293	AA	N	C	Resistor (180K Ω 1/10W) [R15,32]
14	0IX7559-0092	AA	N	C	Resistor (470 Ω 1/10W) [R20,21,22]
15	0IX7558-5610	AA	N	C	Resistor (560 Ω 1/10W) [R24,26]
16	0IX7559-0214	AB	N	C	Resistor (1.5K Ω 1/10W) [R29,30]
17	0IX7559-0304	AB	N	C	Resistor (820 Ω 1/10W) [R31]
18	0IX7558-1542	AA		C	Resistor (CHP-R2-154JT)(150K Ω 1/10W) [R35]
19	0IX7558-1529	AA	N	C	Resistor (1.5K Ω 1/10W) [R37]
20	0IX7572-5171	AD	N	C	Capacitor (180 μ F 16WV) [C1]
21	0IX7669-0113	AD		C	Capacitor (C320MD-E105HTC)(1 μ F) [C2,8,10,12,16,19]
22	0IX7678-0195	AB	N	C	Capacitor (0.01 μ F) [C3,6,11,13,18]
23	0IX7678-0140	AB		C	Capacitor (C210ME-B223KTC)(0.022 μ F) [C4]
24	0IX7678-0117	AB		C	Capacitor (C210MH-F104ZTC)(0.1 μ F) [C5,9,15]
25	0IX7572-3192	AE	N	C	Capacitor (100 μ F 6.3WV) [C7]

9 Inverter unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
26	0 i X 7 6 7 8 - 0 0 7 3 /	AC	N	C	Capacitor (0.047 μ F)
27	0 i X 7 5 7 2 - 5 1 1 4 /	AD	N	C	Capacitor (39 μ F 16WV)
28	0 i X 7 5 6 2 - 0 0 7 7 /	AH	N	C	Capacitor (0.22 μ F 100VDC)
29	0 i X 7 5 7 1 - 0 0 6 0 /	AD	N	C	Capacitor (22pF 3KVDC)
30	0 i X 7 5 3 2 - 2 0 8 0 /	AF		B	Transistor (2SA1213-Y-TR)
31	0 i X 7 5 3 2 - 2 0 1 3 /	AC		B	Transistor (2SC2712-GR-TL)
32	0 i X 7 5 3 2 - 5 0 4 2 /	AD	N	B	Transistor (2SA1162)
33	0 i X 7 5 3 2 - 2 2 0 3 /	AF	N	B	Transistor (FC112)
34	0 i X 7 5 3 2 - 5 0 2 9 /	AN		B	Transistor (2SA1795-A-4061)
35	0 i X 7 5 3 2 - 2 0 5 7 /	AF		B	Transistor (2SC2873-Y-TL)
36	0 i X 7 5 3 1 - 1 1 6 1 /	AE	N	B	Diode (SE014)
37	0 i X 7 5 3 1 - 1 5 4 1 /	AP	N	B	Diode (DE5SC4M)
38	0 i X 7 5 3 1 - 1 1 9 4 /	AC		B	Diode (1SS193-TL)
39	0 i X 7 5 3 1 - 1 2 6 1 /	AC	N	B	Diode (1SS184)
40	0 i X 7 5 3 1 - 1 4 3 9 /	AD	N	B	Diode (02CZ4.7)
41	0 i X 7 5 3 1 - 1 4 7 3 /	AD	N	B	Diode (02CZ9.1)
42	0 i X 7 5 3 1 - 1 4 5 1 /	AD	N	B	Diode (02CZ5.1)
43	0 i X 7 5 3 4 - 0 0 3 9 /	AN		B	IC (TL5001-TL)
44	0 i X 7 5 3 4 - 0 0 9 6 /	AK		B	IC (UPC155562-T1)
45	0 i X 7 5 9 9 - 1 9 7 5 /	AG	N	A	Fuse (SSFR 2.5A)
46	0 i X 7 5 9 9 - 3 7 0 7 /	AY	N	B	Transformer (EPS1368)
47	0 i X 7 5 9 9 - 3 7 1 8 /	AP	N	C	Inductor (CD105-181K)
48	0 i X 7 5 9 9 - 3 7 2 9 /	AP	N	C	Inductor (CD105-560K)
49	0 i X 7 5 9 9 - 1 9 4 2 /	AG	N	C	Connector (IL-Z-3PL-SMTY)
50	0 i X 7 5 9 9 - 1 9 6 4 /	AC	N	C	Connector (S2B-EH)
51	0 i X 7 5 9 9 - 1 9 5 3 /	AH	N	C	Connector (IL-Z-5PL-SMTY)
52	0 i X 7 5 9 9 - 1 9 3 1 /	AE	N	C	Connector (IL-G-3P-S3L2-E)
	(Unit)				
901	DUNTK 2 7 9 8 ACZZ	BR	N	E	CCFT inverter unit

10 FDD unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0 i EK 0 6 0 2 0 5 / / /	AK		C	Case
2	0 i EK 0 6 0 2 0 6 / / /	AE		C	Case cap
3	0 i EK 3 1 0 0 6 7 / / /	AA		C	Screw
4	0 i EK 0 6 0 2 0 3 0 4 /	AE		C	Front panel
5	0 i EK 0 6 0 2 0 2 0 4 /	AD		C	Shutter
6	0 i EK 2 2 0 1 6 3 / / /	AA		C	Shutter spring
7	0 i EK 3 2 0 0 4 1 0 4 /	AC		C	Button
	(Unit)				
901	DUNTK 2 6 8 8 ACZZ	BW		E	FDD unit

11 Track ball unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0 0 P 2 P 0 0 A A 0 1 2 /	AV		C	Ball
2	0 0 P 8 4 A A B 0 0 3 9 /	AM		C	Retainer
	(Unit)				
901	DUNT - 2 7 0 3 ACZZ	BM		E	Track ball unit

Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
[C]				
CCADZ1110AC01	3- 34	AN	N	D
CPWBZ1225ACN4	1- 30	**	N	E
//	4- 901	**	N	E
CPWBZ1227ACN1	1- 38	CD		E
//	6- 901	CD		E
CPWBZ1239ACN1	1- 45	CN	N	E
//	5- 901	CN	N	E
[D]				
DUNT-2679ACZZ	1- 35	BQ		E
DUNT-2680ACZZ	1- 35	BQ		E
DUNT-2681ACZZ	1- 35	BQ		E
DUNT-2703ACZZ	1- 44	BM		E
//	11- 901	BM		E
DUNTG2800ACZZ	2- 901	**	N	E
DUNT2688ACZZ	1- 24	BW		E
//	10- 901	BW		E
DUNT2704ACZZ	1- 22	AX		E
//	7- 901	AX		E
DUNT2736ACZZ	1- 23	**		E
DUNT2798ACZZ	2- 16	BR	N	E
//	9- 901	BR	N	E
DUNT2849ACZZ	2- 101	BX	N	E
[G]				
GCABA1092ACZZ	1- 6	BH		D
GCABB1091ACZZ	1- 31	BH		D
GCABC1095ACZZ	2- 22	BN	N	D
GCABD1096ACZZ	2- 3	BL	N	D
GCOVA1065ACZZ	1- 7	AK		D
GCOVA1068ACZZ	1- 55	AP	N	D
GCOVA1069ACZZ	1- 53	AL	N	D
GCOVH1061ACZZ	1- 11	AF		D
GCOVH1062ACZZ	1- 10	AE		D
GCOVH1063ACZZ	1- 34	AE		D
GCOVH1064ACZZ	1- 15	AH		D
GCOVH1067ACZZ	1- 1	AU		D
GLEGG1007DCZZ	1- 3	AA		C
[H]				
HBDGS1007ACZZ	2- 21	AP	N	D
[J]				
JBTN-1008ACZZ	1- 61	AC		C
JBTN-1009ACZZ	1- 60	AC		C
JBTN-1010ACZZ	1- 57	AD		C
JBTN-1011ACZZ	2- 7	AC		C
JBTN-1012ACZZ	2- 5	AC		C
JBTN-1013ACZZ	1- 8	AD		C
JHNDP2008SCZZ	3- 3	AB		C
JKNBP1018ACZZ	1- 32	AD		C
JKNBP1019ACZA	1- 4	AC		C
[L]				
LANGF1250ACZZ	2- 12	AE	N	C
LANGT1245ACZA	1- 20	AK		C
LANGT1246ACZZ	1- 25	AE		C
LANGT1247ACZA	1- 26	AF		C
LCHSM1028ACZZ	6- 21	AF		C
LCHSM1029ACZZ	1- 49	AL		C
LCHSM1030ACZZ	1- 48	AK		C
LCHSM1031ACZZ	1- 37	AK		C
LHLDN2101SCZZ	2- 24	AB		C
LHLDZ1029ACZB	1- 54	AH	N	C
LHLDZ1030ACZZ	4- 186	AS		C
LPLTF1037ACZZ	1- 14	AG		C
LPLTF1038ACZZ	1- 13	AG		C
LPLTP1040ACZZ	3- 25	AD		C
LX-BZ0406FCZZ	1- 18	AA		C
LX-BZ1047ACZZ	1- 17	AA		C
LX-BZ1048ACZZ	1- 50	AC		C
LX-BZ1050ACZZ	1- 43	AC		C
LX-BZ1051ACZZ	1- 19	AA		C
LX-BZ1052ACZZ	1- 27	AA		C
LX-BZ1053ACZZ	2- 2	AA		C
LX-BZ1054ACZZ	2- 20	AA		C
LX-BZ1147CCZZ	2- 15	AA		C
LX-BZ1187CCZZ	1- 21	AA		C
[M]				
MSPRC1022ACZZ	1- 58	AA		C
MSPRC1026ACZZ	2- 6	AB		C
MSPRP1024ACZZ	7- 1	AD		C
MSPRP1025ACZZ	7- 2	AD		C
[P]				

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
PCAPH1021ACZZ	2- 1	AA		D
PCUSS1056ACZZ	1- 66	AD		C
PCUSS1057ACZZ	1- 67	AE		C
PCUSS1058ACZZ	1- 70	AH		C
PCUSS1059ACZZ	1- 65	AK		C
PCUSS1060ACZZ	1- 69	AE		C
PCUSS1061ACZZ	1- 68	AC		C
PDMP-1010ACZZ	2- 14	AW	N	D
PDMP-1011ACZZ	2- 13	AW	N	D
PFI1W1017ACZZ	1- 59	AE		D
PFI1W1018ACZZ	1- 56	AD	N	D
PGUMS1008ACZZ	4- 356	AC		C
PGUMS1009ACZZ	2- 23	AE	N	D
PSHEZ1069ACZZ	1- 12	AD		C
PSHEZ1070ACZA	5- 150	AC		C
PSPA21061ACZZ	5- 151	AA		C
//	5- 152	AA		C
//	5- 153	AA		C
//	5- 154	AA		C
//	5- 155	AA		C
PSPA21062ACZZ	5- 156	AA		C
//	5- 157	AA		C
PSPA21063ACZZ	1- 73	AB		C
PSPA21065ACZZ	1- 72	AC		C
PTPEZ1030ACZZ	1- 76	AE		D
PTPEZ1031ACZZ	1- 75	AE		D
PZETZ1052ACZZ	1- 33	AB		D
PZETZ1053ACZZ	4- 182	AA		C
PZETZ1054ACZZ	2- 19	AC	N	C
[Q]				
QACCB7621QCZZ	3- 9	AN		B
QACCD7611QCZZ	3- 9	AT		B
QACCF7622QCZZ	3- 9	AX		B
QACCL7620QCZZ	3- 9	AW		B
QACCV6621QCZZ	3- 9	AT		B
QCNCM1188AC0F	4- 189	AC		C
QCNCM1191ACAJ	4- 172	AR		C
QCNCM1191AC2J	4- 178	AL		C
QCNCM1191AC5J	4- 180	AM		C
//	4- 181	AM		C
QCNCM1193AC6H	4- 187	AT		C
QCNCM1194AC0i	4- 174	AQ		C
QCNCW1183AC0F	7- 3	AE		C
QCNCW1184AC2J	6- 5	AL		C
QCNCW1185AC2A	5- 73	AF		C
QCNCW1185AC2C	4- 188	AF		C
QCNCW1185AC2J	4- 175	AE		C
//	4- 176	AE		C
QCNCW1186ACAJ	5- 74	AR		C
QCNCW1187AC1E	5- 75	AM		C
QCNCW1189AC0H	4- 179	AD		C
QCNCW1190AC2F	4- 177	AH		C
QCNCW1192AC0J	4- 183	AX		C
QCNCW1195AC2E	4- 173	AQ		C
QCNCW1196AC0i	4- 184	AE		C
QCNCW1197AC1E	4- 185	AE		C
QCNCW1198AC1J	6- 4	AQ		C
QCNCW-1347ACZZ	1- 42	AC		C
QCNCW-1349ACZZ	2- 17	AV	N	C
QCNCW-1350ACZZ	2- 10	AZ	N	C
QCNCW-1351ACZZ	2- 9	AM	N	C
QPWBM1234ACZZ	1- 16	AG		C
QPWBM1240ACZZ	1- 29	AZ		C
QPWBM1242ACZZ	1- 39	AY	N	C
QS0CZ6433AC6H	4- 274	AQ		C
QSW-P1088ACZZ	5- 161	AE		B
QSW-S1084ACZZ	6- 20	AH		B
QSW-Z1085ACZZ	5- 158	AE		B
//	5- 159	AE		B
QSW-Z1086ACZZ	4- 358	AD		B
//	5- 160	AD		B
QSW-Z1087ACZZ	4- 357	AK		B
[R]				
RADPA1024ACZQ	3- 14	BX	N	B
RADPA1024ACZZ	3- 14	BX	N	B
RADPA1025ACZZ	3- 14	BY	N	D
RALMB1001ACZZ	6- 1	AN		B
RC-CZ1004ACZZ	4- 361	AC	N	C
RC-SZ1001LCZZ	5- 12	AF		C
//	5- 14	AF		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
RC-SZ1001LCZZ	5- 23	AF		C
//	5- 28	AF		C
//	5- 29	AF		C
//	5- 32	AF		C
RCILZ1013ACZZ	5- 131	AC	N	C
RCORF1005ACZZ	4- 201	AB		C
//	4- 202	AB		C
//	4- 203	AB		C
//	4- 208	AB		C
//	4- 209	AB		C
//	4- 213	AB		C
RCORF1008ACZZ	4- 197	AB		C
//	4- 198	AB		C
//	4- 199	AB		C
//	4- 200	AB		C
//	4- 204	AB		C
//	4- 205	AB		C
//	4- 206	AB		C
//	4- 207	AB		C
//	4- 210	AB		C
//	4- 211	AB		C
//	4- 212	AB		C
//	4- 214	AB		C
//	4- 215	AB		C
//	4- 216	AB		C
//	4- 217	AB		C
//	4- 218	AB		C
//	4- 219	AB		C
//	4- 220	AB		C
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//	4- 222	AB		C
//	4- 223	AB		C
//	4- 224	AB		C
//	4- 225	AB		C
//	4- 226	AB		C
//	4- 227	AB		C
//	4- 228	AB		C
//	4- 229	AB		C
//	4- 230	AB		C
//	4- 231	AB		C
//	4- 232	AB		C
//	4- 233	AB		C
//	4- 234	AB		C
//	4- 235	AB		C
//	5- 83	AB		C
//	5- 84	AB		C
//	5- 87	AB		C
//	5- 88	AB		C
//	5- 89	AB		C
//	5- 90	AB		C
//	5- 91	AB		C
//	5- 92	AB		C
//	5- 93	AB		C
//	5- 94	AB		C
//	5- 95	AB		C
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//	5- 97	AB		C
//	5- 98	AB		C
//	5- 99	AB		C
//	5- 100	AB		C
//	5- 101	AB		C
//	5- 102	AB		C
//	5- 103	AB		C
//	5- 104	AB		C
//	5- 105	AB		C
//	5- 106	AB		C
//	5- 107	AB		C
//	5- 108	AB		C
//	5- 109	AB		C
//	5- 110	AB		C
//	5- 111	AB		C
//	5- 112	AB		C
//	5- 113	AB		C
//	5- 114	AB		C
//	5- 115	AB		C
RCORF1009ACZZ	5- 85	AC	N	C
//	5- 86	AC	N	C
RCORF6632RCZZ	4- 196	AC		C
RCRSP1056ACZZ	4- 360	AH		B
RCRSP1057ACZZ	4- 359	AH		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
RDENC1027ACZZ	1- 40	CA	N	E
//	8- 901	CA	N	E
RFILN1010ACZZ	4- 236	AD		C
//	4- 237	AD		C
//	4- 238	AD		C
//	4- 239	AD		C
//	4- 240	AD		C
//	4- 241	AD		C
RFILN1011ACZZ	4- 242	AD		C
//	4- 243	AD		C
//	4- 244	AD		C
//	4- 245	AD		C
//	6- 7	AD		C
//	6- 8	AD		C
//	6- 9	AD		C
//	6- 10	AD		C
//	6- 11	AD		C
//	6- 12	AD		C
//	6- 13	AD		C
//	6- 14	AD		C
//	6- 15	AD		C
RR-TZ1005ACZZ	4- 11	AC		B
//	4- 18	AC		B
//	4- 25	AC		B
//	5- 2	AC		B
//	5- 3	AC		B
//	5- 5	AC		B
//	5- 6	AC		B
//	5- 7	AC		B
RR-TZ1006ACZZ	4- 9	AB		B
//	4- 15	AB		B
//	4- 16	AB		B
//	4- 21	AB		B
RR-TZ1007ACZZ	4- 6	AC		B
//	4- 12	AC		B
//	4- 26	AC		B
//	4- 30	AC		B
//	4- 31	AC		B
//	4- 35	AC		B
RR-TZ1008ACZZ	4- 32	AE		B
//	4- 34	AE		B
RR-TZ1010ACZZ	4- 33	AE		B
RR-TZ1011ACZZ	4- 2	AE		B
RR-TZ1012ACZZ	4- 3	AE		B
//	4- 4	AE		B
RR-TZ1013ACZZ	5- 1	AC		B
//	5- 8	AC		B
RR-TZ1014ACZZ	4- 10	AB		B
//	4- 17	AB		B
//	5- 4	AB		B
RR-TZ1015ACZZ	4- 19	AC		B
//	4- 20	AC		B
//	4- 22	AC		B
RR-TZ1016ACZZ	4- 23	AB		B
//	4- 27	AB		B
RR-TZ1017ACZZ	4- 13	AB		B
RR-TZ1018ACZZ	4- 7	AC		B
//	4- 14	AC		B
RR-TZ1019ACZZ	4- 8	AB		B
//	4- 24	AB		B
RR-TZ1020ACZZ	4- 5	AB		B
//	4- 28	AB		B
RR-TZ1021ACZZ	4- 29	AC		B
[S]				
SPAKA2250ACZZ	3- 8	AE		D
SPAKA2251ACZZ	3- 12	AD		D
SPAKA2252ACZZ	3- 20	AB		D
SPAKA2279ACZZ	3- 15	AG		D
SPAKA2294ACZZ	3- 26	AH	N	D
SPAKA2295ACZZ	3- 4	AK	N	D
SPAKA2296ACZZ	3- 5	AK	N	D
SPAKA2303ACZZ	3- 13	AK	N	D
SPAKA5416SCZZ	3- 2	AB		D
SPAKC2298ACZZ	3- 1	AS	N	D
SPAKC2299ACZZ	3- 1	AR	N	D
SPAKP2288ACZZ	3- 19	AG		D
SSAKA1130QCZZ	3- 18	AA		D
SSAKA2010KCZZ	3- 31	AA		D
SSAKA3001CCZZ	3- 6	AA		D

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
[T]				
TCADZ1006DCZZ	3- 27	AW		D
TCADZ1075ACZZ	3- 29	AF		D
TCAUA1030ACZZ	1- 74	AB	N	D
TCAUS1028ACZZ	1- 63	AB		D
TCAUS1054CCZZ	3- 21	AB		C
TGANE0056FCZZ	3- 27	AF		D
TINSE1662ACZZ	3- 30	AX		D
TINSE1669ACZZ	3- 28	AY	N	D
TINSE1670ACZZ	3- 28	AY	N	D
TINSE1671ACZZ	3- 28	AY	N	D
TLABB1381ACZZ	3- 35	AC		D
TLABE1290ACZZ	4- 269	AB		D
TLABE1635ACZZ	3- 16	AF		D
TLABE1636ACZZ	3- 16	AF		D
TLABE1637ACZZ	3- 16	AF		D
TLABE1668ACZZ	3- 24	AH	N	D
TLABH1065DCZZ	2- 18	AA		D
TLABP1675ACZZ	3- 22	AB	N	D
TLABP1676ACZZ	3- 22	AB	N	D
TLABP1677ACZZ	2- 4	AG	N	D
TLABP1697ACZZ	1- 64	AD		D
TLABP1720ACZZ	3- 22	AA	N	D
TLABT1701ACZZ	1- 77	AC	N	D
TLABZ1640ACZZ	1- 71	AC		D
[U]				
UBATN1010ACZZ	1- 2	BN		B
"	3- 11	BN		B
UBATN1011ACZZ	4- 1	AT		B
UBNDA1008CCZZ	3- 7	AA		C
UFLPC1001ABUB	3- 17	BH	N	E
UFLPC1001ABVB	3- 17	BH	N	E
UFLPC1001ABWB	3- 17	BH		E
UFLPC1001ACTA	3- 23	BH		E
[V]				
VCCCTV1HH101J	5- 43	AA		C
"	5- 44	AA		C
"	5- 45	AA		C
"	5- 46	AA		C
"	5- 47	AA		C
"	5- 48	AA		C
"	5- 49	AA		C
"	5- 50	AA		C
"	5- 51	AA		C
"	5- 52	AA		C
"	5- 53	AA		C
VCCCTV1HH222J	5- 15	AB	N	C
"	5- 16	AB	N	C
VCCCTV1HH330J	5- 57	AA		C
"	5- 60	AA		C
"	5- 61	AA		C
"	5- 63	AA		C
"	5- 72	AA		C
VCCCTV1HH470J	5- 54	AA		C
VCCCTV1HH471J	5- 17	AA		C
"	5- 18	AA		C
"	5- 19	AA		C
VCCSTV1HL101J	4- 43	AA		C
"	4- 76	AA		C
"	4- 77	AA		C
"	4- 78	AA		C
"	4- 79	AA		C
"	4- 107	AA		C
"	4- 127	AA		C
"	4- 128	AA		C
VCCSTV1HL102J	4- 42	AA		C
"	4- 66	AA		C
"	4- 69	AA		C
"	4- 71	AA		C
"	4- 133	AA		C
"	4- 137	AA		C
"	5- 40	AA		C
VCCSTV1HL150J	4- 85	AA		C
"	4- 86	AA		C
VCCSTV1HL220J	4- 164	AA		C
VCCSTV1HL221J	4- 45	AA		C
"	4- 46	AA		C
"	4- 47	AA		C
"	4- 48	AA		C
"	4- 49	AA		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VCCSTV1HL221J	4- 50	AA		C
"	4- 51	AA		C
"	4- 52	AA		C
"	4- 53	AA		C
"	4- 54	AA		C
"	4- 108	AA		C
"	4- 109	AA		C
"	4- 110	AA		C
"	4- 111	AA		C
"	4- 112	AA		C
"	4- 113	AA		C
VCCSTV1HL300J	4- 106	AA		C
VCCSTV1HL470J	4- 61	AA		C
VCCSTV1HL560J	4- 168	AA		C
"	4- 169	AA		C
"	4- 170	AA		C
"	4- 171	AA		C
VCCSTV1HL680J	4- 60	AA		C
"	4- 105	AA		C
"	4- 166	AA		C
"	4- 167	AA		C
VCKYTV1EB103K	4- 67	AA		C
"	4- 80	AA		C
"	4- 154	AA		C
"	4- 156	AA		C
"	4- 158	AA		C
"	4- 160	AA		C
"	5- 38	AA		C
VCKYTV1EB104K	4- 155	AA		C
"	4- 157	AA		C
"	4- 159	AA		C
"	4- 161	AA		C
VCKYTV1HF104Z	4- 41	AA		C
"	4- 44	AA		C
"	4- 55	AA		C
"	4- 56	AA		C
"	4- 57	AA		C
"	4- 59	AA		C
"	4- 62	AA		C
"	4- 63	AA		C
"	4- 64	AA		C
"	4- 65	AA		C
"	4- 68	AA		C
"	4- 70	AA		C
"	4- 73	AA		C
"	4- 74	AA		C
"	4- 82	AA		C
"	4- 84	AA		C
"	4- 87	AA		C
"	4- 92	AA		C
"	4- 93	AA		C
"	4- 94	AA		C
"	4- 95	AA		C
"	4- 97	AA		C
"	4- 98	AA		C
"	4- 99	AA		C
"	4- 100	AA		C
"	4- 102	AA		C
"	4- 103	AA		C
"	4- 114	AA		C
"	4- 115	AA		C
"	4- 116	AA		C
"	4- 118	AA		C
"	4- 119	AA		C
"	4- 120	AA		C
"	4- 121	AA		C
"	4- 122	AA		C
"	4- 123	AA		C
"	4- 125	AA		C
"	4- 126	AA		C
"	4- 129	AA		C
"	4- 130	AA		C
"	4- 131	AA		C
"	4- 132	AA		C
"	4- 134	AA		C
"	4- 135	AA		C
"	4- 136	AA		C
"	4- 138	AA		C
"	4- 140	AA		C
"	4- 141	AA		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	REMARK
VCKYTV1HF104Z	4- 142	AA		C	
"	4- 146	AA		C	
"	4- 147	AA		C	
"	4- 148	AA		C	
"	4- 149	AA		C	
"	4- 150	AA		C	
"	5- 10	AA		C	
"	5- 11	AA		C	
"	5- 13	AA		C	
"	5- 20	AA		C	
"	5- 21	AA		C	
"	5- 22	AA		C	
"	5- 24	AA		C	
"	5- 26	AA		C	
"	5- 27	AA		C	
"	5- 30	AA		C	
"	5- 31	AA		C	
"	5- 33	AA		C	
"	5- 35	AA		C	
"	5- 36	AA		C	
"	5- 37	AA		C	
"	5- 39	AA		C	
"	5- 55	AA		C	
"	5- 56	AA		C	
"	5- 58	AA		C	
"	5- 59	AA		C	
"	5- 62	AA		C	
"	5- 64	AA		C	
"	5- 65	AA		C	
"	5- 66	AA		C	
"	5- 67	AA		C	
"	5- 68	AA		C	
"	5- 69	AA		C	
"	5- 70	AA		C	
"	5- 71	AA		C	
"	6- 3	AA		C	
VCSAPJ1AE106M	4- 36	AE		C	
"	4- 72	AE		C	
"	4- 75	AE		C	
"	4- 90	AE		C	
"	4- 96	AE		C	
"	4- 101	AE		C	
"	4- 117	AE		C	
"	4- 124	AE		C	
"	4- 139	AE		C	
"	4- 165	AE		C	
VCSAPJ1AE225M	4- 58	AC		C	
"	4- 81	AC		C	
"	4- 91	AC		C	
"	4- 104	AC		C	
"	4- 143	AC		C	
"	4- 151	AC		C	
"	4- 152	AC		C	
"	4- 153	AC		C	
"	4- 162	AC		C	
"	4- 163	AC		C	
"	6- 2	AC		C	
VCSAPJ1AE335M	5- 9	AD		C	
"	5- 25	AD		C	
"	5- 34	AD		C	
"	5- 41	AD		C	
"	5- 42	AD		C	
VCSAPJ1CE105M	4- 144	AC		C	
"	4- 145	AC		C	
VCSAPJ1CE336M	4- 37	AF		C	
"	4- 38	AF		C	
"	4- 39	AF		C	
"	4- 40	AF		C	
VCSAPJ1EE225M	4- 83	AD		C	
"	4- 88	AD		C	
"	4- 89	AD		C	
VHDDAP202K/-1	6- 6	AB		B	
VHDDA204K//--1	4- 191	AC		B	
VHDMA724//--1	4- 190	AD		B	
"	4- 192	AD		B	
"	4- 193	AD		B	
"	4- 194	AD		B	
"	4- 195	AD		B	
VHIALS245ANS/	4- 267	AK		B	
VHIALS38ANS//	4- 273	AE		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	REMARK
VHIALS639ANS/	4- 275	AQ		B	
VHIAV9127-09/	4- 255	BB		B	
VH1HD153119-1	5- 128	BH		B	
VH1IR2339N/-1	4- 271	AE		B	
"	4- 272	AE		B	
VH1LZ98J13/-1	5- 125	BB	N	B	
VH1MM1060G/-1	4- 264	AE		B	
VH1SC14L01233	4- 246	AU		B	
VH1SN74HC00DB	4- 280	AD		B	
VH1SN74HC02DB	4- 262	AD		B	
VH1SN74HC04DB	4- 247	AD		B	
"	4- 248	AD		B	
"	4- 249	AD		B	
"	4- 278	AD		B	
"	5- 127	AD		B	
VH1SN74HC10DB	4- 263	AE		B	
VH1SN74HC14DB	4- 279	AF		B	
VH1SN74HC32DB	5- 118	AD		B	
VH1SN74HC74DB	4- 261	AF		B	
VH1TC55187-25	4- 254	BF	N	B	
VH1TC7S08F/-1	5- 129	AC		B	
"	5- 130	AC		B	
VH1TC8566AF-R	4- 253	AX		B	
VH1UPD4714GT1	4- 268	AW		B	
VH114L8AF1031	4- 277	BE		B	
VH127C256AA1D	4- 270	BD	N	B	
VH128F020-150	4- 256	BQ		B	
VH1360SLB1/-1	4- 252	BZ	N	B	
VH1386SLB1-25	4- 276	CS	N	B	
VH1511664BTL1	5- 124	BA	N	B	
"	5- 126	BA	N	B	
VH1514400FTL8	4- 257	BM		B	
"	4- 258	BM		B	
"	4- 259	BM		B	
"	4- 260	BM		B	
VH174ACT245FP	4- 283	AK		B	
"	4- 284	AK		B	
VH174ACT367FP	4- 281	AG		B	
"	4- 282	AG		B	
VH174HCT245DB	5- 120	AM		B	
"	5- 123	AM		B	
VH174HCT541DB	5- 121	AM	N	B	
"	5- 122	AM	N	B	
VH174HC125DB/	4- 265	AE		B	
"	5- 117	AE		B	
VH174HC151NS/	4- 266	AG		B	
VH174HC373DB/	4- 251	AG		B	
VH180C51SL-BG	4- 250	BF		B	
VH182C401A/-1	5- 119	AY		B	
VH182C456A/-1	5- 116	BW		B	
VHPGL3ED8//--1	5- 81	AC		B	
"	5- 82	AC		B	
VHPHLMF-1790/	5- 76	AD		B	
"	5- 77	AD		B	
"	5- 78	AD		B	
"	5- 79	AD		B	
"	5- 80	AD		B	
VRS-CY1JD000J	4- 333	AA		C	
"	4- 338	AA		C	
"	4- 340	AA		C	
"	5- 134	AA		C	
"	5- 135	AA		C	
VRS-CY1JD100J	4- 346	AA		C	
VRS-CY1JD101J	4- 342	AA		C	
VRS-CY1JD102G	4- 310	AA		C	
"	4- 311	AA		C	
"	4- 341	AA		C	
"	4- 343	AA		C	
"	4- 344	AA		C	
"	4- 345	AA		C	
VRS-CY1JD102J	4- 305	AA		C	
"	4- 308	AA		C	
"	4- 322	AA		C	
"	4- 327	AA		C	
"	4- 335	AA		C	
VRS-CY1JD103J	4- 320	AA		C	
"	4- 334	AA		C	
VRS-CY1JD104J	4- 321	AA		C	
"	4- 348	AA		C	
"	5- 136	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VRS-CY1JD104J	5- 137	AA		C
"	5- 143	AA		C
"	5- 144	AA		C
"	5- 145	AA		C
"	5- 149	AA		C
VRS-CY1JD122J	4- 315	AA		C
VRS-CY1JD153G	4- 313	AA		C
VRS-CY1JD182J	6- 17	AA		C
VRS-CY1JD223J	4- 306	AA		C
"	4- 316	AA		C
"	4- 317	AA		C
"	4- 325	AA		C
"	4- 326	AA		C
"	4- 328	AA		C
"	4- 336	AA		C
"	4- 339	AA		C
"	4- 347	AA		C
VRS-CY1JD330J	4- 331	AA		C
"	5- 147	AA		C
"	5- 148	AA		C
VRS-CY1JD392J	4- 323	AA		C
VRS-CY1JD472J	4- 318	AA		C
"	4- 329	AA		C
VRS-CY1JD473J	4- 319	AA		C
VRS-CY1JD681J	4- 332	AA		C
VRS-CY1JD683G	4- 312	AA		C
VRS-CY1JD750J	4- 349	AA		C
"	5- 139	AA		C
"	5- 140	AA		C
"	5- 142	AA		C
VRS-CY1JD752J	5- 138	AA		C
VRS-CY1JD821J	4- 337	AA		C
"	5- 146	AA		C
VRS-TP2BD561J	4- 307	AA		C
"	4- 314	AA		C
"	4- 324	AA		C
VRS-TS2AD106J	4- 309	AA		C
VRS-TS2AD220J	5- 141	AA		C
VRS-TS2AD560J	4- 330	AA		C
VSDTA114YK/-1	4- 288	AC		B
"	4- 289	AC		B
"	4- 302	AC		B
"	4- 304	AC		B
VSDTC114GK/-1	4- 294	AB		B
VSDTC114YK/-1	4- 285	AC		B
"	4- 286	AC		B
"	4- 287	AC		B
"	4- 290	AC		B
"	4- 291	AC		B
"	4- 292	AC		B
"	4- 293	AC		B
"	4- 299	AC		B
"	4- 300	AC		B
"	4- 301	AC		B
"	4- 303	AC		B
"	5- 132	AC		B
"	5- 133	AC		B
VS2SC2412KS-1	6- 16	AB		B
VS2SJ208-/-1	4- 295	AD		B
"	4- 296	AD		B
"	4- 297	AD		B
"	4- 298	AD		B
[X]				
XBBS26P04000	1- 46	AA		C
XBBS26P06000	1- 62	AA		C
"	6- 18	AA		C
"	6- 19	AA		C
XBBS26P06000	1- 36	AA		C
"	2- 11	AA		C
"	4- 350	AA		C
"	4- 351	AA		C
"	4- 352	AA		C
"	4- 353	AA		C
"	4- 354	AA		C
"	4- 355	AA		C
XBBS26P12000	1- 41	AA		C
XBBSF20P06000	1- 5	AA		C
XBBSF26P06000	1- 9	AA		C
XBPSN20P04000	1- 47	AA		C
XJBS20P10000	1- 28	AA		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
[O]				
0BRNJD3178CN1	8- 16	AG		C
0BRNJD3178CN3	8- 18	AG		C
0BRNJD3178L4/	8- 14	AX	N	C
0BRNJD3178TR1	8- 9	AX	N	B
0BRNJD3178TR5	8- 10	AV	N	B
0BRNJD3335CN2	8- 17	BA	N	C
0BRNJD3335CN4	8- 19	AE	N	C
0BRNJD3335C23	8- 4	AM	N	C
0BRNJD3335C3/	8- 1	AM	N	C
0BRNJD3335C4/	8- 2	AM	N	C
0BRNJD3335C5/	8- 5	AE	N	C
0BRNJD3335C7/	8- 3	AM	N	C
0BRNJD3335C8/	8- 6	AE	N	C
0BRNJD3335DS1	8- 8	AR	N	B
0BRNJD3335F2/	8- 7	AM	N	A
0BRNJD3335L1/	8- 11	AY	N	C
0BRNJD3335L2/	8- 12	BC	N	C
0BRNJD3335L3/	8- 13	AM	N	C
0BRNJD3335T1/	8- 15	BD	N	C
0iEK06020204/	10- 5	AD		C
0iEK06020304/	10- 4	AE		C
0iEK060205///	10- 1	AK		C
0iEK060206///	10- 2	AE		C
0iEK220163///	10- 6	AA		C
0iEK310067///	10- 3	AA		C
0iEK32004104/	10- 7	AC		C
0iX7531-1161/	9- 36	AE	N	B
0iX7531-1194/	9- 38	AC		B
0iX7531-1261/	9- 39	AC	N	B
0iX7531-1439/	9- 40	AD	N	B
0iX7531-1451/	9- 42	AD	N	B
0iX7531-1473/	9- 41	AD	N	B
0iX7531-1541/	9- 37	AP	N	B
0iX7532-2013/	9- 31	AC		B
0iX7532-2057/	9- 35	AF		B
0iX7532-2080/	9- 30	AF		B
0iX7532-2203/	9- 33	AF	N	B
0iX7532-5029/	9- 34	AN		B
0iX7532-5042/	9- 32	AD	N	B
0iX7534-0039/	9- 43	AN		B
0iX7534-0096/	9- 44	AK		B
0iX7557-0085/	9- 11	AB	N	C
0iX7557-0096/	9- 12	AB	N	C
0iX7558-1061/	9- 10	AA		C
0iX7558-1083/	9- 4	AA	N	C
0iX7558-1518/	9- 8	AB	N	C
0iX7558-1529/	9- 19	AA	N	C
0iX7558-1542/	9- 18	AA		C
0iX7558-3329/	9- 5	AA		C
0iX7558-4794/	9- 2	AA	N	C
0iX7558-5610/	9- 15	AA	N	C
0iX7558-6849/	9- 3	AA		C
0iX7559-0092/	9- 14	AA	N	C
0iX7559-0214/	9- 16	AB	N	C
0iX7559-0269/	9- 1	AA	N	C
0iX7559-0271/	9- 7	AB	N	C
0iX7559-0293/	9- 13	AA	N	C
0iX7559-0304/	9- 17	AB	N	C
0iX7559-0315/	9- 9	AA	N	C
0iX7559-0326/	9- 6	AB	N	C
0iX7562-0077/	9- 28	AH	N	C
0iX7571-0060/	9- 29	AD	N	C
0iX7572-3192/	9- 25	AE	N	C
0iX7572-5114/	9- 27	AD	N	C
0iX7572-5171/	9- 20	AD	N	C
0iX7599-1931/	9- 52	AE	N	C
0iX7599-1942/	9- 49	AG	N	C
0iX7599-1953/	9- 51	AH	N	C
0iX7599-1964/	9- 50	AC	N	C
0iX7599-1975/	9- 45	AG	N	A
0iX7599-3707/	9- 46	AY	N	B
0iX7599-3718/	9- 47	AP	N	C
0iX7599-3729/	9- 48	AP	N	C
0iX7669-0113/	9- 21	AD		C
0iX7678-0073/	9- 26	AC	N	C
0iX7678-0117/	9- 24	AB		C
0iX7678-0140/	9- 23	AB		C
0iX7678-0195/	9- 22	AB	N	C
00P2P00AA012/	11- 1	AV		C

[illegible]

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	PRICE
1000	1000	1000	1000	1000	1000
1001	1001	1001	1001	1001	1001
1002	1002	1002	1002	1002	1002
1003	1003	1003	1003	1003	1003
1004	1004	1004	1004	1004	1004
1005	1005	1005	1005	1005	1005
1006	1006	1006	1006	1006	1006
1007	1007	1007	1007	1007	1007
1008	1008	1008	1008	1008	1008
1009	1009	1009	1009	1009	1009
1010	1010	1010	1010	1010	1010
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1012	1012	1012	1012	1012	1012
1013	1013	1013	1013	1013	1013
1014	1014	1014	1014	1014	1014
1015	1015	1015	1015	1015	1015
1016	1016	1016	1016	1016	1016
1017	1017	1017	1017	1017	1017
1018	1018	1018	1018	1018	1018
1019	1019	1019	1019	1019	1019
1020	1020	1020	1020	1020	1020
1021	1021	1021	1021	1021	1021
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1024	1024	1024	1024	1024	1024
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1099	1099	1099	1099	1099	1099

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SHARP CORPORATION
Information Systems Group
Quality & Reliability Control Center
Yamatokoriyama, Nara 639-11, Japan
1992 April Printed in Japan ©