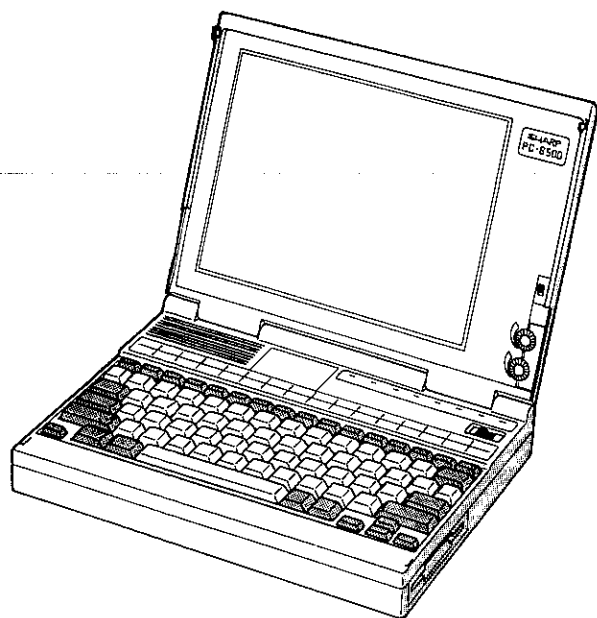


SHARP SERVICE MANUAL

CODE: 00ZPC6500SM-E



PERSONAL COMPUTER

PC-6541 MODEL PC-6521

CPU: 80C286 (12MHz)
Display: VGA
RAM: 1MB (standard)
HDD: 20MB/40MB
LCD: 640 x 480
OPTION: CE-651B (1MB RAM)
 CE-652B (2MB RAM)

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CHAPTER 1. OUTLINE

1-1. Features

1) Equipped with a 20MB/40MB hard disk as a standard component.

This model is equipped with a 20MB/40MB hard disk as a standard component.

This is great enough for salesmen to store customer information and product information and for busy business men to store conference materials, reports, and other information, allowing them to be retrieved at once when needed.

PC-6521: 20MB, PC-6541: 40MB

2) World's lightest, thinnest (letter size) book type personal computer with HDD.

This model is in letter size (8.5"(D) x 11.0"(W) x 1.8"(H)/216mm(D) x 279mm(W) x 46mm(H)), smaller than A4 size. Its thickness is only 46mm. It can be put in a half side of an attache case, and even in a clutch bag. Its light weight (3kg) and the battery drive system allows easy carrying in business trip.

6) System configuration

3) Black-and-white TST LCD with backlight

The black-and-white Triple Super Twist Liquid Crystal Display (TST LCD) with back light (side light) gives clear screen in 16 gradations, allowing to be used in a hotel room or other insufficiently illuminated place.

4) MODEM and, memory options available

Built-in options are available such as a MODEM board (2400bps, class 5). Max. 3MB additional memory can be added (total 4MB) without extending the external dimensions.

5) 3.5" FDD standard

This model has one Floppy disk drive (3.5") standard, it can write/read 1.44M byte and 720K byte diskette.

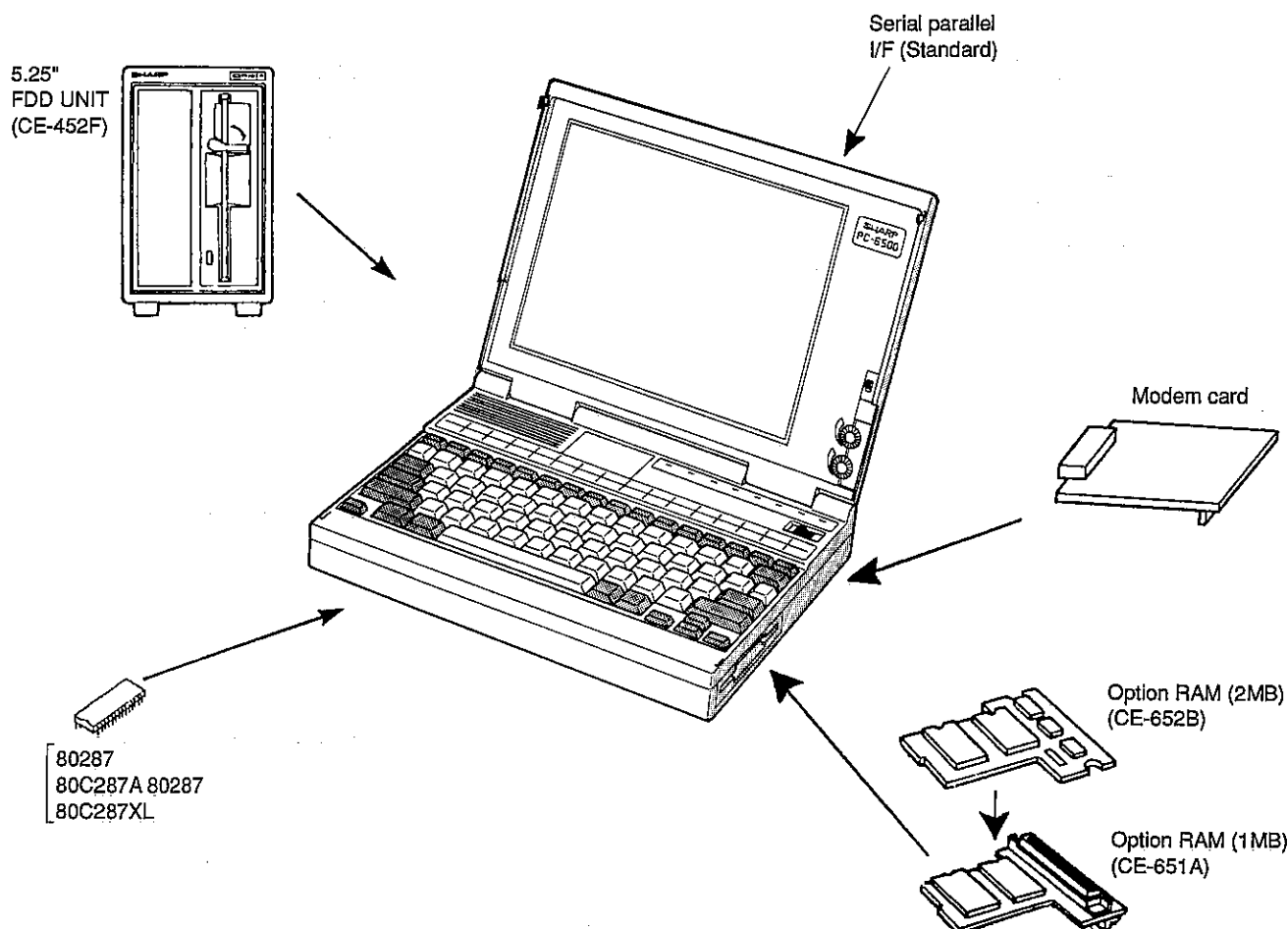


Fig.1-1

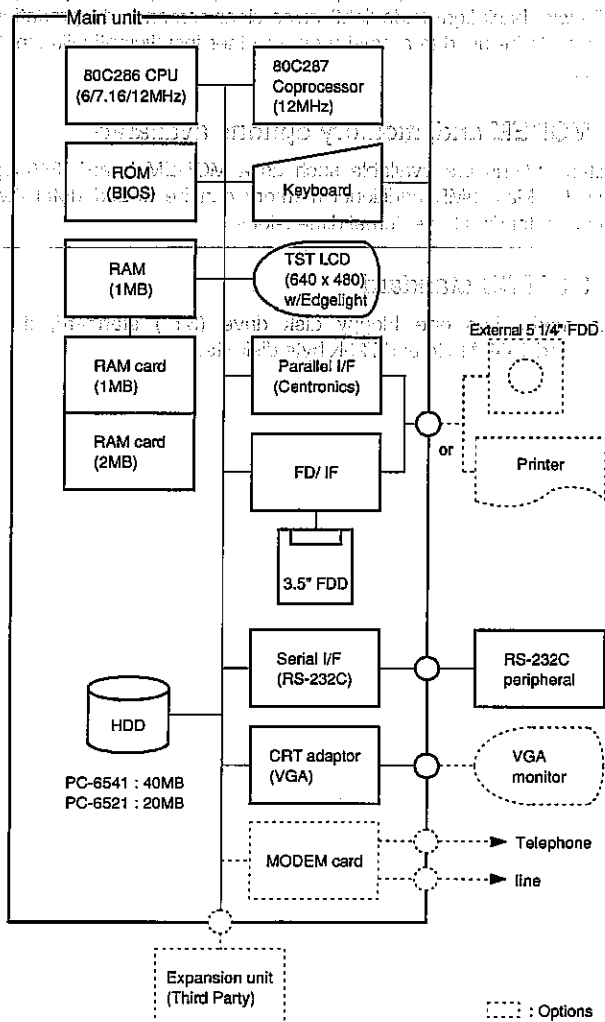


Fig.1-2

1-2. Specification

1) Hardware

- CPU:** 80C286 (6/7.16/12MHz)
- Clock speed can be changed in Setup screen.
- CO-PROCESSOR:** Socket for 80C287A, 80C287XL, 80287
- ROM:** 4M byte Mask ROM x 1
- Contents: IPL, Self check, Setup, AT BIOS, VGA BIOS, DOS system, Utility Software
- RAM:** 1M byte standard
- 4M bit PS-RAM x 2
 - 640K byte for conventional, 360K byte for Expanded or Extended memory
 - LIM/EMS 4.0 support
 - Bus width: 16 bit
 - 1 wait state (12MHz) 0 wait state (6/7.16MHz)
 - Expandable up to 4M byte in 1M byte increments by optional RAM card (CE-651B) and 2M byte more by optional RAM card (CE-652B)
 - CE-652B is connected on the CE-651B.
- DATA STORAGE:** 2.5 inch 20M/40M byte Hard disk drive
- Average access time: 23m sec.
 - PC-6521: 20M byte
 - PC-6541: 40M byte
- DISPLAY:** TST (Triple Super Twisted) LCD with CCFT (Cold Cathode Fluorescent Tube) backlight
- Resolution: 640 x 480 pixels
 - VGA compatible
 - 16 Gradations
 - Viewing area: 8" x 6"
 - Aspect ratio: 1:1
 - Dot pitch: 0.31 mm
 - LCD contrast and backlight brightness are adjustable by each volume.
 - Selectable normal/reverse screen by hardware switch.
- CRT interface:**
- Analog RGB output
 - VGA compatible
 - D-sub 15 pin female connector
 - Selectable LCD/CRT mode by Hardware switch.
 - LCD and CRT can not be used simultaneously.
 - Alternative use with MODEM card.
- KEYBOARD:** IBM 101/102 like keyboard layout
- 79 keys (US layout)
 - 80 keys (UK/German layout)
 - Integrated numeric keypad
 - 'Set Up' key for Setup screen
 - Fn key for special function
 - 12 programmable function keys
 - 19mm pitch (typewriter key part), 2mm stroke
 - Detachable structure for installing internal options. (Co-processor, RAM cards)
- INTERFACE:** Serial (RS-232C) x 1
- D-sub 9 pin male connector
 - Baud rate, data bits, stop bits and parity are selectable in Setup screen.
- Parallel (centronics)/Extend FDD x 1
- D-sub 25pin female connector
 - Selectable 'parallel' or 'Ext. FDD' by the

Dip-switch

Parallel port:	Selectable port address (378h/278h/ disable) by setup program Expansion bus - For the 3rd party - Without connector
SLOT/CONNECTOR:	1 slot for internal options - Optional MODEM card can be connected. 1 slots for RAM cards - Optional 1M byte RAM cards can be connected.
POWER SUPPLY:	Ni-Cd battery - Rechargeable and replaceable 9.6 V, 21.1 WH 2 hours fast charging in charge mode and trickle charging while operating. AC adaptor - Input: 100V – 240V AC 50/60Hz - Output: 15V DC - AC cord is detachable from AC adaptor.
BATTERY LIFE:	2.5H Hard disk always motor on, Floppy disk access 10% backlight maximum, without options.
POWER SAVE FUNCTION:	CPU: - Standby mode Hard disk drive: - Spindle motor off Backlight: - Backlight timeout
LOW BATTERY ALARM:	1st-step: With the battery in the normally charged state, LOW BATTERY indicator remains off. 2nd-step: When the battery is more than roughly 90% discharged, LOW BATTERY indicator turns red and an alarm beeps for about 15 seconds. 3rd-step: After LOW BATTERY indicator blinking and an alarm beeping for about 30 seconds, the system will shut off the power automatically.
CHARGING INDICATOR:	CHARGE indicator blinks while the battery is being charged, and illuminates when the battery is at least 90% charged.
POWER CONSUMPTION:	Typ. 7 W (without options)

2) Mechanical

CONNECTORS:

External connectors for:

Serial interface:	D-sub 9 pin connector
Parallel /EXT. FDD:	D-sub 25 pin connector
CRT:	D-sub 15 pin connector
AC adaptor:	2 conductor phone jack

Internal connectors for:

Modem card:	68 pin connector
RAM card	50 pin connector

SWITCHES: Power switch (slide switch)

LCD standard/reverse screen select switch
Low battery alarm switch
Speaker control switch
LCD/CRT switch
Parallel/Ext. FDD switch

VOLUMES: LCD contrast adjust volume (rotary volume)
LCD brightness adjust volume (rotary volume)

LEDS: Power indicator (green or orange)
Low battery indicator (red)
Charge indicator (green)
FDD indicator (green)
HDD indicator (green)
Caps lock indicator (green)
Num lock indicator (green)
Scroll lock indicator (green)

DIMENSIONS:

8.5"(D) x 11.0"(W) x 1.8"(H)
216mm(D) x 279mm(W) x 46mm(H)

WEIGHT: Approx. 2.9kg (6.4 lbs)
(Including battery, excluding AC adaptor)

Key board Layout

a) US version

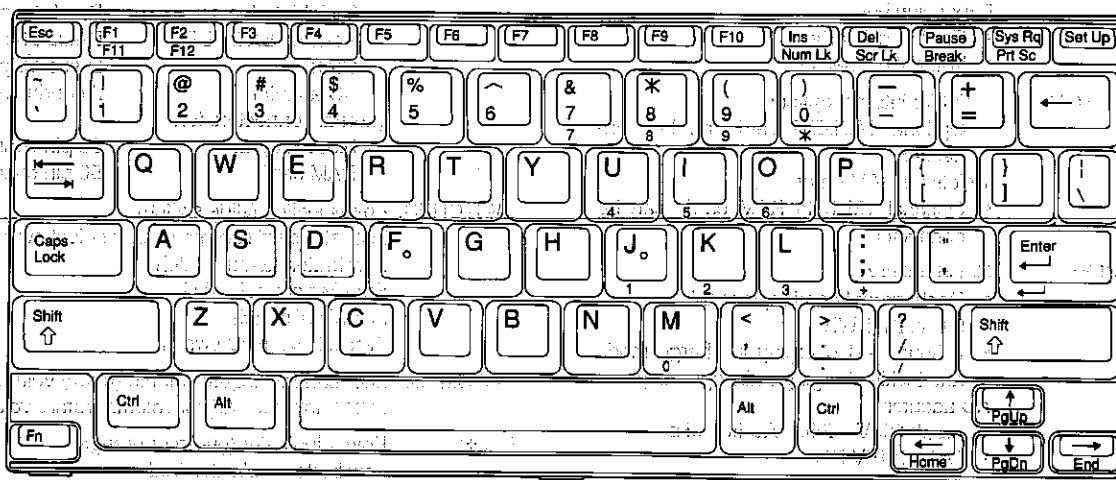


Fig.1-3

b) UK version

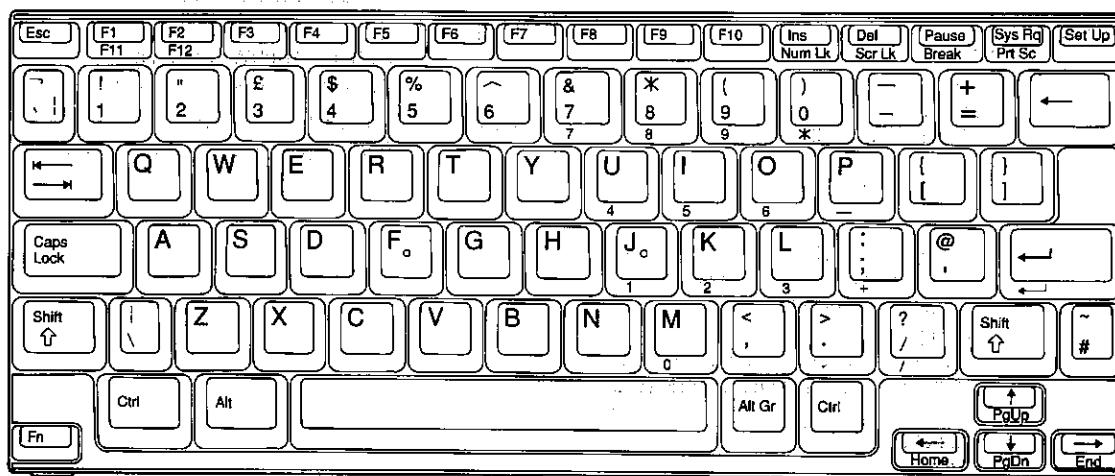


Fig.1-4

c) German version

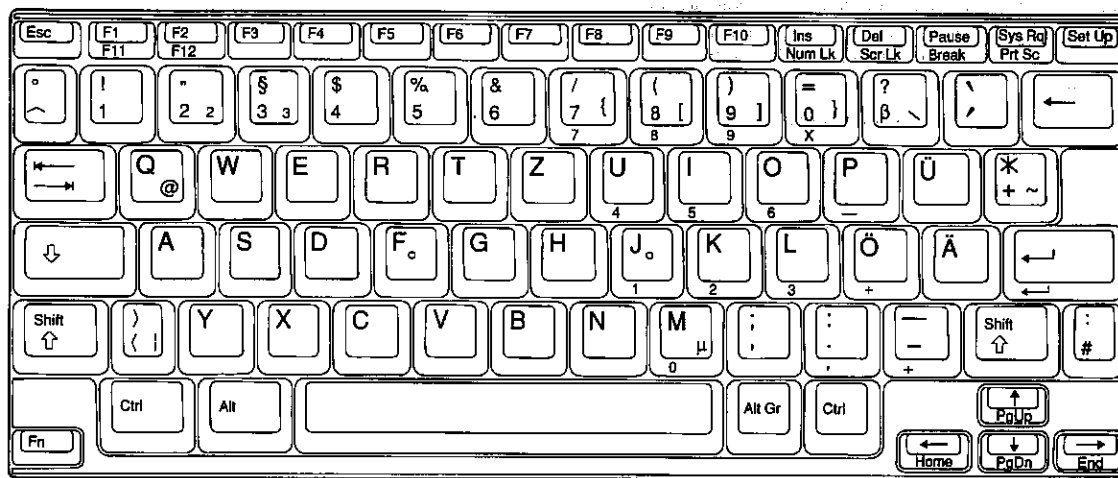


Fig.1-5

3) Software

OPERATING SYSTEM: MS-DOS 4.01

- Supplied by 2DD x 4 diskettes (Including one blank diskette)
- Including SHELL 1.01
- Including GW-BASIC 3.23
- Language: English, French, German

4) Operational and storage range

Operational range: 50 to 95 degrees F
10 to 35 degrees C
20 to 80% humidity (Non-condensing)

Storage range: -4 to 140 degrees F
-20 to 60 degrees C
10 to 90% humidity (non-condensing)

1-3. Software description

1) BIOS

The BIOS of this model is included in a 1Mbit EPROM.

The system BIOS and the video BIOS are stored in the EPROM and attached to a socket on the main PWB.

Special function of the BIOS this model are described below:

1-1) Power saving

This model is equipped with three levels of power saving.

- ① Display power saving
- ② Hard disk power saving
- ③ System power saving

These power saving functions are performed with the time-out values set by SETUP. The system power saving can be also executed by key input. Some application software may not work correctly with system power saving function. If there are any problems in the power saving function, Please disable the function by SET_UP.

1-2) Automatic setting of hardware

This model's hardware setting is performed for the following items.

- ① Built-in VGA mode setting
- ② Display adapter setting
- ③ Each device I/O port setting
- ④ FDD/HDD assignment
- ⑤ Built-in memory setting

The following items are automatically detected and proper settings are made automatically.

- ① FDD presence
- ② FDD type
- ③ HDD type
- ④ Main memory and expansion memory capacity

1-3) Special functions with key operation

- SETUP key : "SET UP" 0DH character line is displayed.
- CTRL + ALT + SETUP : Setup program execution
- Fn + SETUP : Displayed pallet number change
- (Fn + PAUSE) : System power saving execution/return
(CTRL + ALT + PAUSE)
- CTRL + ALT + ↑ : CPU clock UP (6 → 7.16 → 12 MHz)
- CTRL + ALT + ↓ : CPU clock down (12 → 7.16 → 6MHz)

2) Setup Program Page 1

SHARP PERSONAL COMPUTER SET-UP PROGRAM			
Version X.XX XXX XX, XXXX			
Page 1 of 3			
Time:	01:00:00 p.m.	Internal Memory Size:	1 MB
Date:	Mon Jan 01, 1991	Main Memory:	640 KB
Date Format:	U.S. (12-hours)	Extended Memory:	64 KB
		Expanded Memory:	320 KB
Drive A:	Internal 3.5"FDD	Disabled Memory:	0 KB
Drive B:	External 5.25"FDD	Boundary Address:	110000 h
CPU Speed:	12MHz	EMS Port Address:	218h-21Bh
BUS Speed:	6MHz		
Esc	F1	F2	Tab
Save/Exit	Help	Sys Info.	Category
			Field
			Value
			PgUp/PgDn
			Page

Clock

The computer contains a battery-operated clock that keeps track of the time and date. This category allows the current time and date to be set and modified.

Time This field specifies the current time. Time is set either in a 12-hour or a 24-hour clock format depending on the country setting. Press **Space Bar** or the + key to increase the time, or the - key to decrease it. With the 12-hour clock format, press the **Space Bar** to change between a.m. and p.m. This also resets the seconds to 00.

Date This field specifies the current date. The date is set either in the month-day-year or the day-month-year order depending on the next field, date format setting. The day of the week (Mon, Tue, Wed, etc.) is set automatically after the date is entered.

Date Format This field specifies the Time and Date format. Time can be set either in the 12-hour or 24-hour format, and Date can be set in either U.S. style or European style. The possible settings are: U.S. (12-hours), U.S. (24-hours), European (12-hours), or European (24-hours).

Note: The time and date only need to be set here when first running the setup program.

Floppy Disk

This category specifies the type of disk drive:

Drive A/Drive B These fields specify the FDD assignment. If DIP switch 4 on the rear panel is set to OFF, drive A is assigned to the internal 3.5" FDD, and drive B to the External 5.25" FDD, regardless of the setting here.

Speed

This category specifies the CPU and BUS speeds:

CPU Speed/BUS Speed These fields specify the CPU speed and bus speed used on power-up. The speeds are set as a pair and change simultaneously when you exit the setup program. The possible settings are: 12 MHz/6 MHz, 7.16 MHz/7.16 MHz, or 6 MHz/6 MHz.

Memory Configuration

This category specifies the configuration of the internal memory. By setting the internal memory size and boundary address, the system calculates each memory size.

Internal Memory Size

This field specifies the total amount of internal memory. The possible settings are: 1 MB, 2 MB, or 4 MB.

Main Memory This field always shows 640 KB.

Extended Memory This field shows the amount of internal Extended memory.

Expanded Memory This field shows the amount of internal Expanded memory.

Disabled Memory This field shows the amount of memory which is not available to the user.

Boundary Address Normally this field is specified automatically according to the upper three field settings. But you can also set this address as you prefer.

See Appendix A for the relationship between the settings in this category and each memory size.

EMS Port Address this field specifies the EMS device driver I/O port address (EMM4J.SYS).

You can continue to customize your PC-6500 by accessing two additional screens of selections within the setup program. Press **PgDn**, and the next screen will appear:

Setup Program Page 2

SHARE PERSONAL COMPUTER SET-UP PROGRAM Version x.xx xx xx, xxxxx			
Page 2 of 3			
Display Adaptor:	Internal VGA	Quick Boot:	Off
Display Mode:	VGA Mode	Standby Key:	Disable
Cursor Type:	Underline	Speed Key:	Enable
LCD Mode:	Standard		
Key Repeat Rate:	Fast	Display Timeout:	1 minute
		HDD Timeout:	1 minute
		System Timeout:	Always on
Caps Lock:	Off		
Num Lock:	Off		
Scroll Lock:	Off		

Esc	F1	F2	Tab	←→	Space	PgUp/PgDn
Save/Exit	Help	Sys Info.	Category	Field	Value	Page

Display

Display Adaptor This field always set to Internal VGA.

Display Mode Specifies the mode of the internal VGA controller. The possible settings are: VGA Mode, EGA Mode, CGA Mode, MDA Mode, and HGC Mode. The HGC Mode is effective only for an external CRT monitor.

Cursor Type The shape of the cursor can be changed to one of the following settings: Underline, Underbar, or Block.

LCD Mode The standard LCD screen has a resolution of 640 dots horizontally x 480 dots vertically. In MDA, CGA, and EGA display modes, however, the screen does not normally use all of the 480 dot vertical display area. For example, CGA normally displays text and images with 640 x 400 dots. Specifying expanded mode for these display modes expands the screen display vertically to use the full screen. Possible settings are: Standard or Expanded.

To use the entire display, set the LCD mode to Expanded. However, for some CGA and EGA-based applications where the aspect ratio is critical, it may be desirable to use the Standard setting.

Keyboard

This category specifies the key repeat rate and the state of three lock keys when the system is started.

Key Repeat Rate Specifies the default key repeat rate. Possible settings are: Fast or Standard.

Caps Lock Specifies the default state of the Caps Lock key. Possible settings are: On or Off.

Num Lock Specifies the default state of the Num Lk key. Possible settings are: On or Off.

Scroll Lock Specifies the default state of the Scr Lk key. Possible settings are: On or Off.

System Configurations

This category specifies three settings concerning the system configuration.

Quick Boot This field selects quick loading of the system. When this field is set to On, the system bypasses some of the power-on self checks (including memory check) when starting up. The possible settings are: On or Off.

Standby Key This field lets you enter the standby mode using the keyboard. Normally, the system enters the standby mode after a specified period of inactivity.

If this field is set to Enable, the system will enter standby mode when the **Fn-Pause** or **Ctrl-Alt-Pause** key combination is pressed. The possible settings are: Enable or Disable.

Note: The standby feature is designed to work with the vast majority of MS-DOS applications. However, this feature does not work with applications or operating environments which require the use of the 80286 "protected" memory mode. If this occurs, your application may be using the "protected" mode. In this case, set the System Timeout field to Always On, and Standby Key field to Disable.

Speed Key This field lets you change the CPU clock speed from the keyboard. If you set this field to Enable, you can change the CPU clock speed using the **Ctrl-Alt-↑** or **Ctrl-Alt-↓** key combination on the keyboard while using the computer. **Ctrl-Alt-↑** increases the CPU speed step by step in the 6 MHz - 7.16 MHz - 12 MHz order, and **Ctrl-Alt-↓** slows down the CPU speed step by step in the 12 MHz - 7.16 MHz - 6 MHz order. The possible settings are: Enable or Disable.

You will hear a high-pitched beep when pressing **Ctrl-Alt-↑**, and a lower pitched beep when pressing **Ctrl-Alt-↓**. The higher (lower) tone results from the higher (lower) CPU speed.

Note: In some cases, the above key functions (**Fn-Pause**, **Ctrl-Alt-Pause**, **Ctrl-Alt-↑** or **Ctrl-Alt-↓**) may not be effective even when Enable is set in the setup program. In this case, use the system timeout function or change the CPU Speed in the setup program.

Power Savings

This category specifies the period of three power saving functions.

Note: Each power saving function occurs within 1 minute from the specified period.

Display Timeout After a certain period of inactivity, with no input from the keyboard or no access to the disk drives, the system automatically shuts off the power to the LCD screen. Pressing any key on the keyboard turns the LCD back on. The length of the timeout period can be set or the LCD can be kept on continuously. Possible settings are: Always On, 1 minute, 2 minutes, 5 minutes, or 10 minutes.

HDD timeout In order to conserve battery life, the hard disk motor can be set turn off automatically after a certain idle period i.e. no access to the hard disk. The time from the last access until the motor is turned off can be set. Possible settings are: Always On, 1 minute, 2 minutes, 5 minutes, or 10 minutes.

Note: Although this conserves battery life, if you are constantly accessing the hard disk, disk access time will become slower if you set this timeout to a low value, because the motor power must be turned on before each access to the hard disk. Powering on the hard disk takes several seconds after the motor has been turned off. See the "Conserving Battery Power" section in Appendix B.

System Timeout After a certain period with no input from the keyboard, the system automatically enters the standby mode. Pressing the **Fn-Pause** or the **Ctrl-Alt-Pause** key combination on the keyboard returns the system to the active mode, the length of the timeout period can be set or the computer can be kept on continuously. The possible settings are: Always On, 1 minute, 2 minutes, 5 minutes, or 10 minutes.

Note: The standby feature is designed to work with the vast majority of MS-DOS applications. However, this feature does not work with applications or operating environments which require the use of the 80286 "protected" memory mode. If this occurs, your application may be using the "protected" mode. In this case, set the system Timeout field to Always On, and Standby Key field to Disable.

Pressing **PgDn** shows the next screen.

Setup Program Page 3

SHARP PERSONAL COMPUTER SET-UP PROGRAM
Version x.xx xxx xx, xxxx

Page 3 of 3

Internal Serial Port		Optional Serial Port	
Port Address:	Port 1 (3F8h)	Port Address:	Disable
Baud Rate:	9600	Baud Rate:	9600
Data Bits:	8	Data Bits:	8
Stop Bits:	1	Stop Bits:	1
Parity Bits:	None	Parity Bits:	None

Internal Parallel Port
Port Address: Port 1 (378h)

Esc	F1	F2	Tab	←→	Space	PgUp/PgDn
Save/Exit	Help	Sys Info.	Category	Field	Value	Page

Serial I/O Port

this category defines the communication setting for the standard and optional serial input/output (SIO) ports.

Port Address Possible settings are: Port 1 (3F8h), Port 2 (2F8h), or Disable.

Baud Rate Possible settings are: 110, 150, 300, 600, 1200, 2400, 4800, or 9600.

Date Bits Possible settings are: 7 or 8.

Stop Bits Possible settings are: 1 or 2.

Parity Possible settings are: None, Odd, or Even.

Internal Parallel Port

This category assigns a port number to the internal parallel port. The possible settings are: Port 1 (378h), Port 2 (278h), or Disable. Whenever DIP switch 4 on the rear panel is set to ON, the parallel port is disabled, regardless of the setting here.

1-4. BIOS POST (Power On Self Test) check

Error detection and report

When the system is started, BIOS POST program is executed.

In POST, operations of the system RAM interruption and various devices including peripheral devices are checked. The operation checks are classified into two groups according to error report.

- 1) Error report by I/O port 80h (MFG port) and beep sound
- 2) Error report by message displayed on the screen

For the tests which use the I/O port 80h (MFG port) and beep sounds, the test items and the output data to the port 80h are shown in the following table.

For the test item with "NONE" in the column of Beep sound, the system does not stop. For the other test items, when any error occurs, beep sound is generated and the system is stopped.

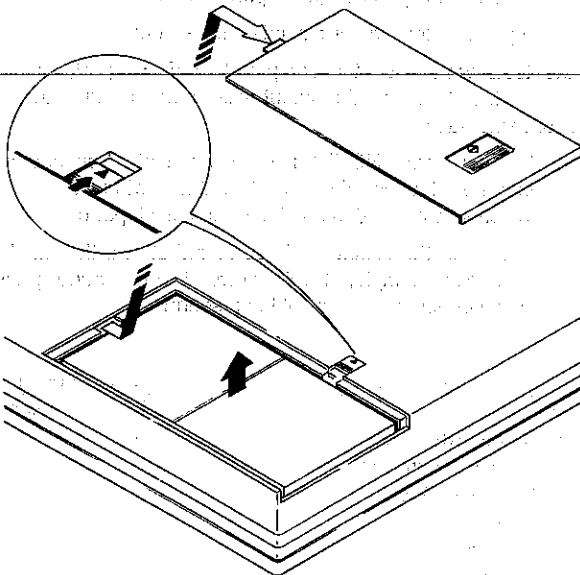
(Note) Figures in the column of beep sound shows the number of beep. For example, "1-3-4" shows "1 beep sound, pause, 3 beep sounds, pause, and 4 beep sound."

Test items	PORT 80h	Beep sound
CPU register test	01h	None
RTC RAM read/write test	02h	1-1-3
BIOS ROM check sum test	03h	1-1-4
System timer (8254) test	04h	1-2-1
DMAC initializing test	05h	1-2-2
DMA page register test	06h	1-2-3
RAM refresh test	08h	1-3-1
First 64KB system RAM test start	09h	None
First 64KB RAM plural data lines error	0Ah	1-1-1
First 64KB RAM control logic error	0Bh	1-3-4
First 64KB RAM address line error	0Ch	1-4-1
First 64KB RAM parity test	0Dh	1-4-2
First 64KB RAM data line error (BIT0)	10h	2-1-1
First 64KB RAM data line error (BIT1)	11h	2-1-2
First 64KB RAM data line error (BIT2)	12h	2-1-3
First 64KB RAM data line error (BIT3)	13h	2-1-4
First 64KB RAM data line error (BIT4)	14h	2-2-1
First 64KB RAM data line error (BIT5)	15h	2-2-2
First 64KB RAM data line error (BIT6)	16h	2-2-3
First 64KB RAM data line error (BIT7)	17h	2-2-4
First 64KB RAM data line error (BIT8)	18h	2-3-1
First 64KB RAM data line error (BIT9)	19h	2-3-2
First 64KB RAM data line error (BITA)	1Ah	2-3-3
First 64KB RAM data line error (BITB)	1Bh	2-3-4
First 64KB RAM data line error (BITC)	1Ch	2-4-1
First 64KB RAM data line error (BITD)	1Dh	2-4-2
First 64KB RAM data line error (BITE)	1Eh	2-4-3
First 64KB RAM data line error (BITF)	1Fh	2-4-4
Slave DMAC register test	20h	3-1-1
Master DMAC register test	21h	3-1-2
Master interrupt mask register test	22h	3-1-3
Slave interrupt mask register test	23h	3-1-4
Interrupt vector setting	25h	None
Keyboard controller test	27h	3-2-4
RTC RAM power check sum test	28h	None
RTC RAM content validation test	29h	None
Display memory (VRAM) test	2Bh	3-3-4
Display initialization test	2Ch	3-4-1
Display line signal test	2Dh	3-4-2
Display ROM searching	2Eh	None
Display test complete	30h	None
Monochrome display allowed to use	31h	None
Color display (40 columns) allowed to use	32h	None
Color display (80 columns) allowed to use	33h	None

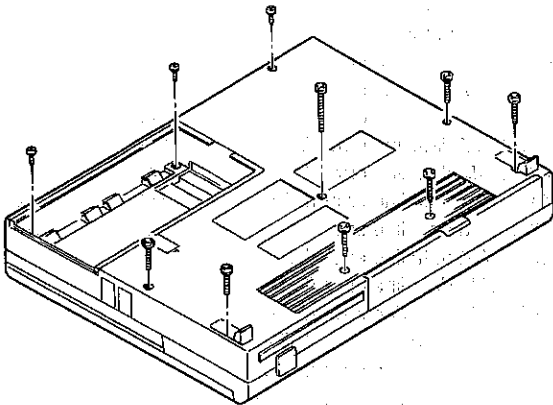
CHAPTER 2. DISASSEMBLY AND ASSEMBLY

Bottom cabinet

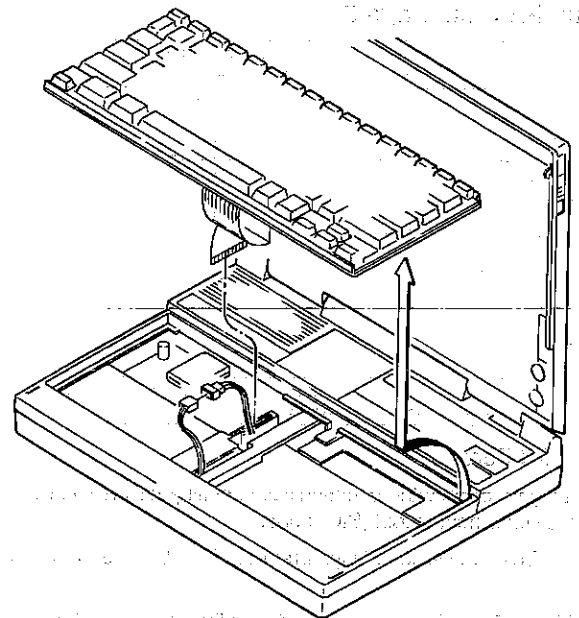
1. Move the stopper in the arrow direction, remove the battery cover, and remove the rechargeable battery cell.



2. Turn the machine upside down and remove ten screws. Note that there are screws of different sizes used.



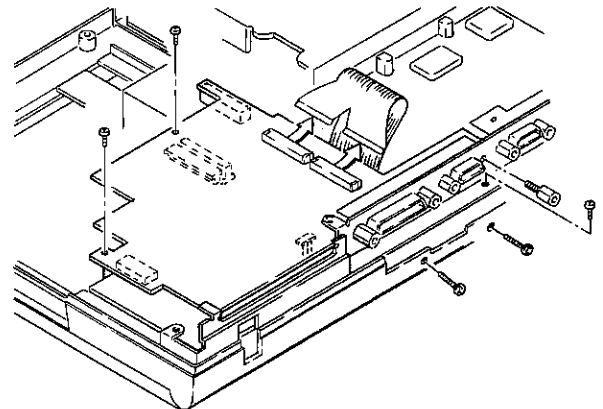
3. Remove the keyboard. Unfasten the 3-pin battery connector.



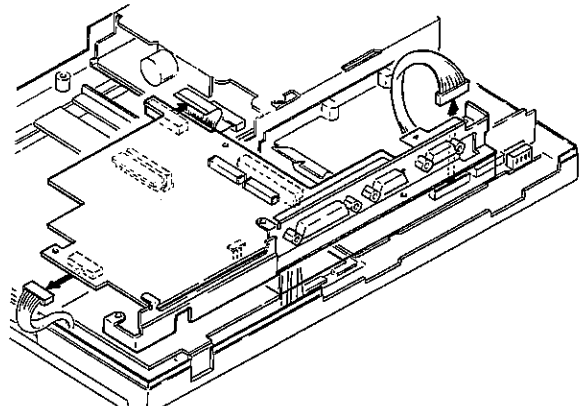
4. If a memory option is used, remove it.
5. Fasten the LCD, turn the machine upside down, and remove the bottom cabinet.

Main PWB

1. Remove the hard disk interfacing cable.
2. Remove two screws that hold the PWB.
3. Remove Allen screws of the RS-232C connector, then remove the screw that hold the angle.

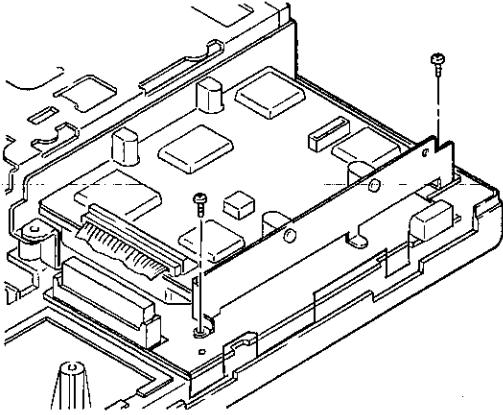


4. Slowly lift the main PWB and unfasten the connector connected to the display PWB.
5. Unfasten the power supply connector.
6. Unfasten the floppy disk connector.
7. Unfasten the VGA connector.

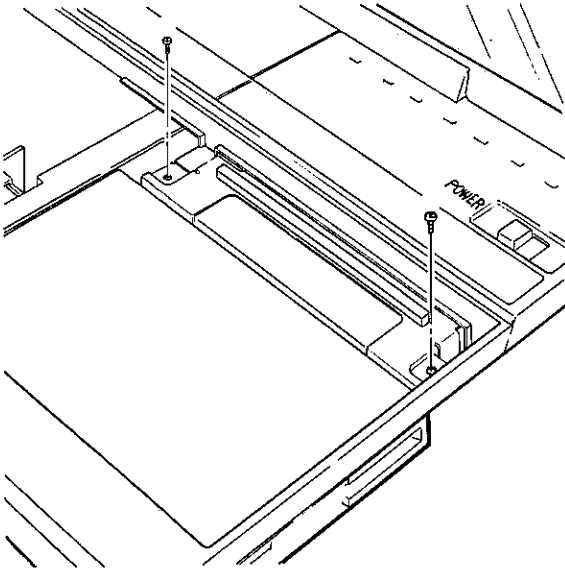


Hard disk drive

1. Remove the main PWB.
2. Remove two screws.

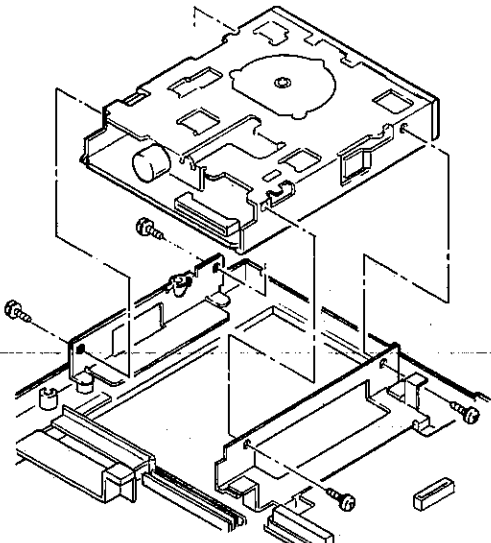


3. Turn it around and remove two screws from the keyboard side.
4. Carefully remove the hard disk drive.



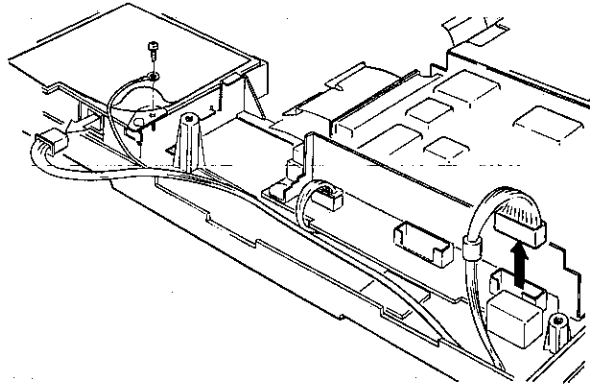
Floppy disk drive

1. Remove the main PWB.
2. Remove the hard disk drive.
3. Remove four screws and remove the floppy disk drive.

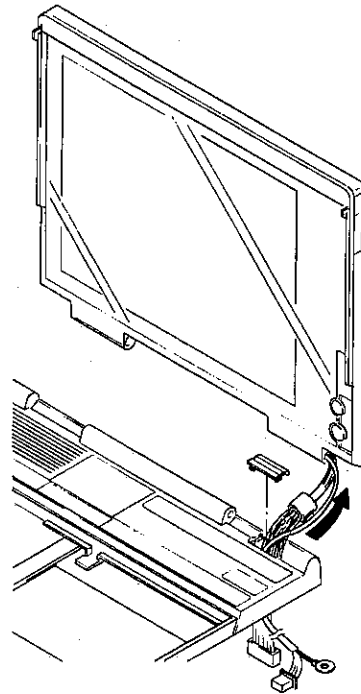


LCD

1. Remove the main PWB.
2. Remove the LCD connector from the display PWB. Remove the backlight cable from the power supply unit.

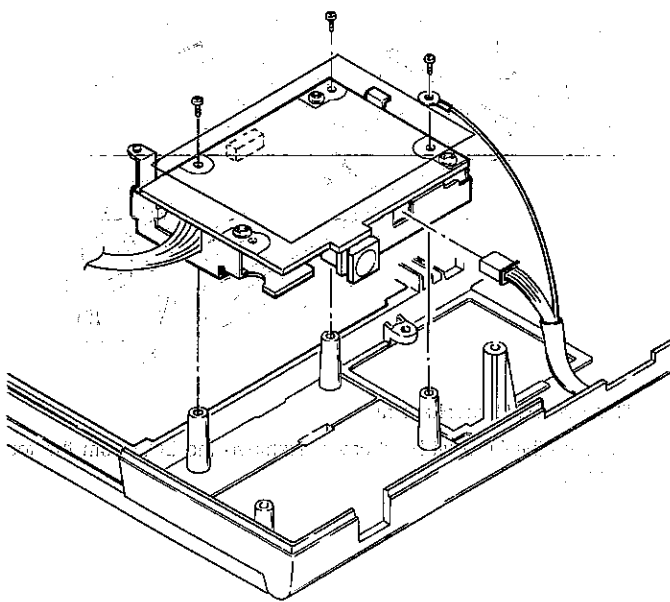


3. Remove the tilt mechanism.
4. Remove the LCD tilt blind cover. Remove the LCD from the top cabinet.



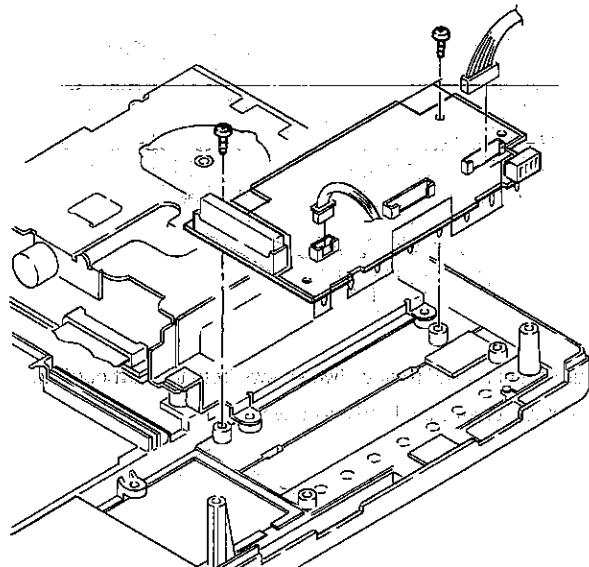
Power supply unit

1. Remove the main PWB.
2. Remove three screws, remove the backlight cable, then remove the power supply unit and power supply shield sheet.

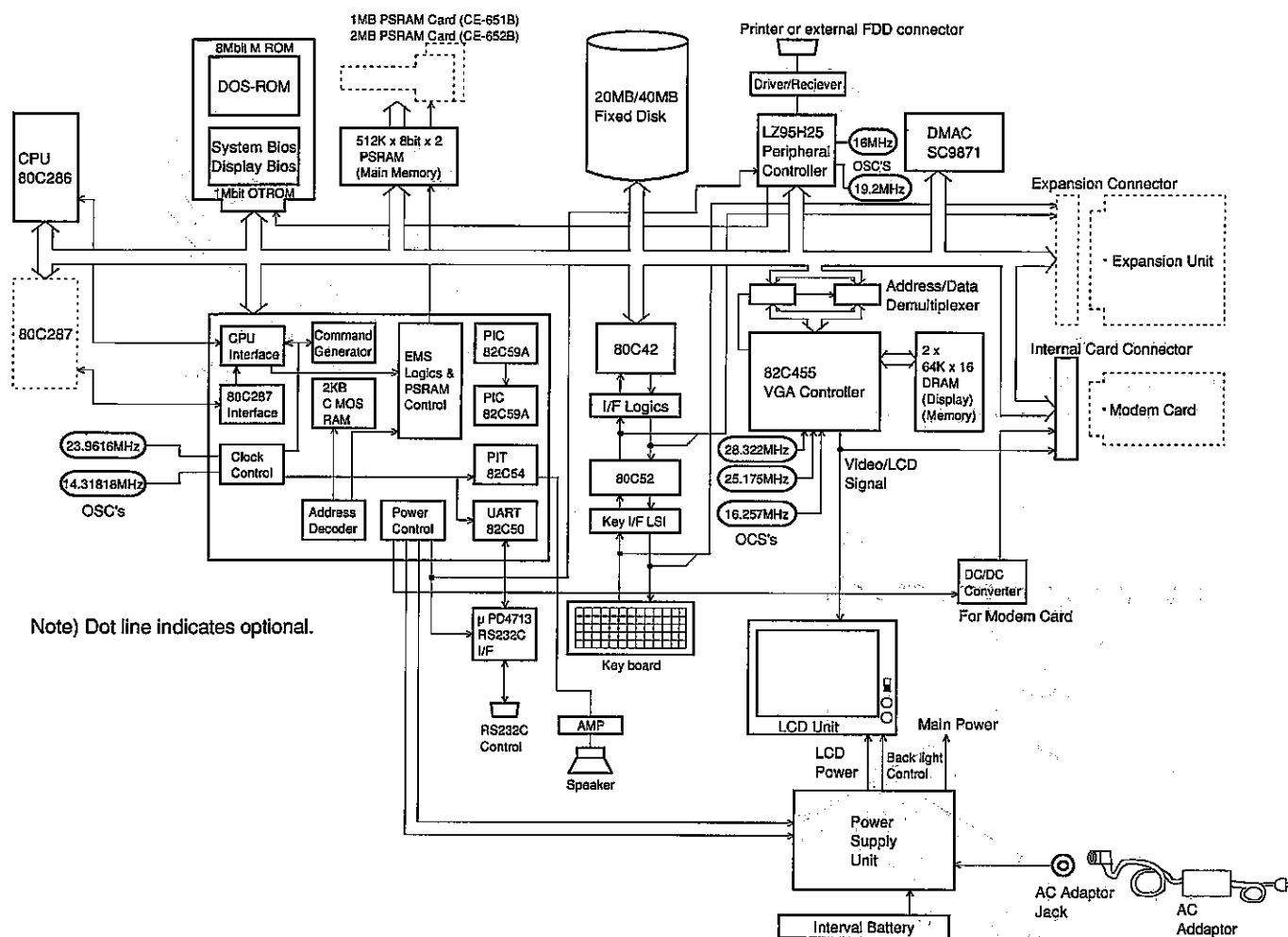


Display PWB

1. Remove the main PWB.
2. Remove the hard disk drive unit.
3. Unfasten the LCD cable, buzzer cable, and VGA cable.
4. Remove two screws, then remove the display PWB and shield sheet.



CHAPTER 3. System block diagram



CHAPTER 4. Theory of operation

4-1. Processor

4-1-1. CPU

This unit employs 12MHz version of 80C286 as the CPU, which operates at three speeds: 6MHz, 7.16MHz, and 12MHz. Its selection is possible at any time by writing into the port by the program.

One period from falling to next falling of a clock which is inputted to the CPU is called as "phase." There are two phases: phase 1 ($\phi 1$) and phase 2 ($\phi 2$). The CPU recognizes the next phase to the rising of a reset signal as phase $\phi 2$, and repeats phase 1 and phase 2 alternately until the reset signal rises again.

The combination of $\phi 1$ and $\phi 2$ is called as "state." There are four states: status state (Ts), command state (Tc), idle state (Ti), and hold state (Th). Ts shows the cycle where the CPU is trying to make status signal (*S0, *S1) active. Tc shows the cycle where command signals (*MEMW, *MEMR, *IOW, *IOR, *INTA) are made active to perform data transmission. (The signals, however, are not always made active.) When the CPU make access to a device, a continuous state composed of one Ts called cycle and one or more Tc's. One cycle is executed by repeating the following steps.

- ① First, the CPU generates address.
- ② Then the CPU generates status signal which shows the cycle to be executed. (TS)
- ③ The system control LSI (SC9889A/B) decodes address and status and outputs the necessary control signals (command signal, select signal of memory and each device). (TC)
- ④ The SC9889B controls each buffer according to data transmission direction, and transmits data from the CPU/device to the device/CPU. (Tc)
- ⑤ After completion of transmission, the SC9889B returns the ready signal to the CPU and completes the cycle. (The last Tc)

Fig. 4-1 shows the outline of the cycle.

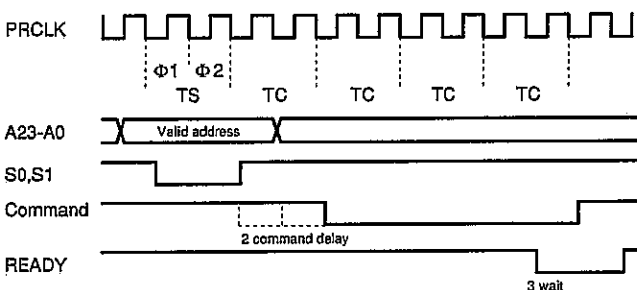


Fig. 4-1

• 80C286 Description

Features

- Compatible with NMOS 80286
- Static CMOS Design for Low Power Operation
 - ▶ ICCSB = 5mA Maximum
 - ▶ ICCOP = 220mA Maximum (80C286-12)
- High Performance Processor (Up to 12 Times the 8086 Throughput)
- Large Address Space:
 - ▶ 16 Megabytes Physical
 - ▶ 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes:

- ▶ 80C286 Real Address Mode
- ▶ Protected Virtual Address Mode

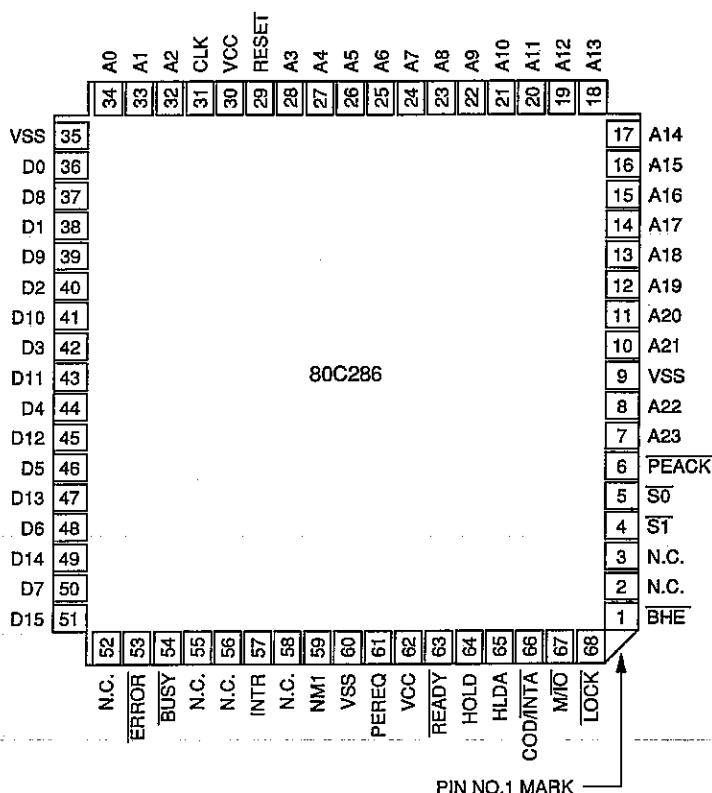
- Compatible with 80287 Numeric Data Co-processor
- Wide Range of Clock Rates:
 - ▶ DC to 12.5MHz (80C286-12)
- High Bandwidth Bus Interface (16 Megabyte/Sec)
- Available in 68 Pin PGA (Pin Grid Array) and PLCC (Plastic Leaded Chip carrier) Packages

Description

The Harris 80C286 is a static-CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12.5MHz 80C286 provides nine times or more throughput than the standard 5MHz 8086. The 80C286 includes memory management capabilities that map 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286 is upwardly compatible with 80C86 and 80C88 software (the 80C286 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286 real address mode, the 80C286 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 80C86 and 80C88 instructions.

The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.



Top view

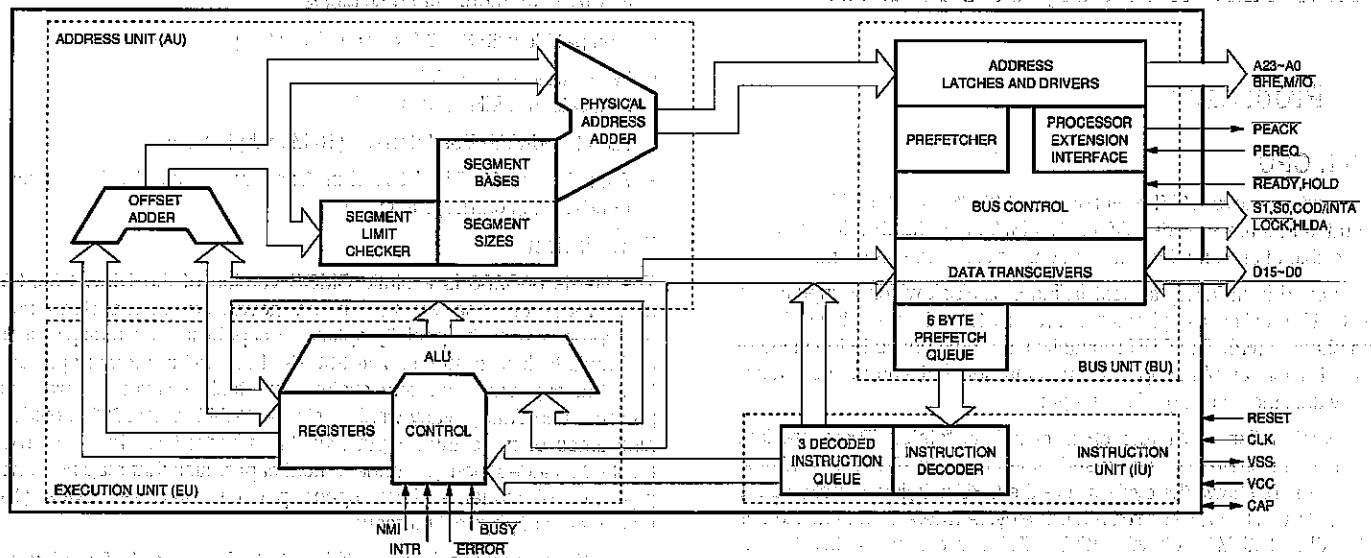


Table 4-1 80C286 Pin description

Signal	Pin No.	I/O	Name and Function																		
Vcc	30, 62	I	System power: +5V power supply.																		
Vss	9, 35, 60	I	System ground: 0V																		
RESET	29	I	System Reset clears the internal logic of the 80C286 and is active HIGH. The CPU may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET remains active, the output pins of the CPU enter the state shown below: <table border="1"><thead><tr><th colspan="2">80C286 Pin State During Reset</th></tr><tr><th>Pin Value</th><th>Pin Names</th></tr></thead><tbody><tr><td>1 (HIGH)</td><td>S0, ST, PEACK, A23 – A0, BHE, LOCK</td></tr><tr><td>0 (LOW)</td><td>M/IO, COD/INTA, HLDA</td></tr><tr><td>3-state OFF</td><td>D15 – D0</td></tr></tbody></table> Operation of the 80C286 begins after a HIGH to LOW transition of RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the CPU for internal initializations before the first bus cycle to fetch a code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.	80C286 Pin State During Reset		Pin Value	Pin Names	1 (HIGH)	S0, ST, PEACK, A23 – A0, BHE, LOCK	0 (LOW)	M/IO, COD/INTA, HLDA	3-state OFF	D15 – D0								
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3-state OFF	D15 – D0																				
CLK	31	I	System Clock provides the fundamental timing for 80L286 systems. It is divided by two inside the CPU to generate the processor clock. The internal divide-by two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.																		
D15-D0	51 – 36	I/O	Data Bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.																		
A23-A0	7, 8, 10 – 28 32 – 34	O	Address bus outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred pins D7-D0. A23-A16 are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.																		
BHE	1	O	Bus High Enable indicates transfer of data on the upper bytes of the data bus, D15-D8. Eight-bit oriented devices assigned to the upper bytes of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to 3-state OFF during bus hold acknowledge. <table border="1"><thead><tr><th colspan="3">BHE and A0 Encodings</th></tr><tr><th>BHE Valu</th><th>A0 Value</th><th>Fuaction</th></tr></thead><tbody><tr><td>L</td><td>L</td><td>Word transfer</td></tr><tr><td>L</td><td>H</td><td>Byte transfer on upper half of data bus (D15 – D8)</td></tr><tr><td>H</td><td>L</td><td>Byte transfer on lower half of data bus (D7 – D0)</td></tr><tr><td>H</td><td>H</td><td>Reserved</td></tr></tbody></table>	BHE and A0 Encodings			BHE Valu	A0 Value	Fuaction	L	L	Word transfer	L	H	Byte transfer on upper half of data bus (D15 – D8)	H	L	Byte transfer on lower half of data bus (D7 – D0)	H	H	Reserved
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H	L	Byte transfer on lower half of data bus (D7 – D0)																			
H	H	Reserved																			

Signal	Pin No.	I/O	Name and Function																																																																																										
$\overline{S1}, \overline{S0}$	4, 5	O	Bus Cycle status indicates initiation of a bus cycle and, along with $\overline{M/\overline{IO}}$ and $\overline{COD/\overline{INTA}}$, defines the type of bus cycle. The bus is a Ts state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge. <table><tr><th colspan="5">80C286 Bus Cycle Definition</th></tr><tr><th>$\overline{COD/\overline{INTA}}$</th><th>$\overline{M/\overline{IO}}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr><tr><td>L</td><td>L</td><td>L</td><td>L</td><td>Interrupt acknowledge</td></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>Reserved</td></tr><tr><td>L</td><td>L</td><td>H</td><td>L</td><td>Reserved</td></tr><tr><td>L</td><td>L</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr><tr><td>L</td><td>H</td><td>L</td><td>L</td><td>If A1 = 1 then halt; else shutdown</td></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td><td>Memory data read</td></tr><tr><td>L</td><td>H</td><td>H</td><td>L</td><td>Memory data write</td></tr><tr><td>L</td><td>H</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr><tr><td>H</td><td>L</td><td>L</td><td>L</td><td>Reserved</td></tr><tr><td>H</td><td>L</td><td>L</td><td>H</td><td>I/O read</td></tr><tr><td>H</td><td>L</td><td>H</td><td>L</td><td>I/O write</td></tr><tr><td>H</td><td>L</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr><tr><td>H</td><td>H</td><td>L</td><td>L</td><td>Reserved</td></tr><tr><td>H</td><td>H</td><td>L</td><td>H</td><td>Memory instruction read</td></tr><tr><td>H</td><td>H</td><td>H</td><td>L</td><td>Reserved</td></tr><tr><td>H</td><td>H</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr></table>	80C286 Bus Cycle Definition					$\overline{COD/\overline{INTA}}$	$\overline{M/\overline{IO}}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated	L	L	L	L	Interrupt acknowledge	L	L	L	H	Reserved	L	L	H	L	Reserved	L	L	H	H	None; not a status cycle	L	H	L	L	If A1 = 1 then halt; else shutdown	L	H	L	H	Memory data read	L	H	H	L	Memory data write	L	H	H	H	None; not a status cycle	H	L	L	L	Reserved	H	L	L	H	I/O read	H	L	H	L	I/O write	H	L	H	H	None; not a status cycle	H	H	L	L	Reserved	H	H	L	H	Memory instruction read	H	H	H	L	Reserved	H	H	H	H	None; not a status cycle
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$\overline{M/\overline{IO}}$	67	O	Memory-I/O Select distinguishes memory access from I/O access. If HIGH during Ts, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. $\overline{M/\overline{IO}}$ floats to 3-state OFF during bus hold acknowledge.																																																																																										
$\overline{COD/\overline{INTA}}$	66	O	Code/Interrupt Acknowledge distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. $\overline{COD/\overline{INTA}}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as $\overline{M/\overline{IO}}$.																																																																																										
$\overline{LOCK}$	68	O	Bus Lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80C286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.																																																																																										
$\overline{READY}$	63	O	Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge.																																																																																										
$\overline{HOLD}$ $\overline{HLDA}$	64 65	I O	Bus Hold Request and Hold Acknowledge control ownership of the 80C286 local bus. The $\overline{HOLD}$ input allows another local bus master to request control of the local bus. When control is granted, the 80C286 will float its bus drivers to 3-state OFF and then activate $\overline{HLDA}$, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until $\overline{HOLD}$ becomes inactive which results in the 80C286 deactivating $\overline{HLDA}$ and regaining control of the local bus. This terminates the bus hold acknowledge condition. $\overline{HOLD}$ may be asynchronous to the system clock. These signals are active HIGH.																																																																																										
$\overline{INTR}$	57	I	Interrupt Request requests the 80C286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80C286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, $\overline{INTR}$ must remain active until the first interrupt acknowledge cycle is completed. $\overline{INTR}$ is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. $\overline{INTR}$ is level sensitive, active HIGH, and may be asynchronous to the system clock.																																																																																										
$\overline{NMI}$	59	I	Non-Maskable Interrupt Request interrupts the 80C286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80C286 flag word does not affect this input. The $\overline{NMI}$ input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.																																																																																										
$\overline{PEREQ}$ $\overline{PEACK}$	61 6	I O	Processor Extension Operand Request and Acknowledge extend the memory management and protection capabilities of the 80C286 to processor extensions. The input requests the 80C286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. $\overline{PEREQ}$ is active HIGH and floats to 3-state OFF during bus hold acknowledge. $\overline{PEACK}$ may be asynchronous to the system clock. $\overline{PEACK}$ is active LOW.																																																																																										
$\overline{BUSY}$ $\overline{ERROR}$	54 53	I I	Processor Extension Busy and Error indicate the operating condition of a processor extension to the 80C286. An active $\overline{BUSY}$ input stops 80C286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80C286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80C286 to perform a processor extension interrupt when execution WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.																																																																																										

4-1-2. Numerical calculation processor (OPTION)

This unit can connect with the optional 80C287 numerical calculation processor (NPX). The NPX operates on 12MHz. The NPX is an expansion of the 80C286 CPU architecture. The CPU regards the NPX as an I/O device occupying 0F8h – 0FFh. The NPX itself has no bus control function. When, therefore, the NPX requires data, PEREQ signal is made active to request the CPU to transmit data. The CPU makes *PEREQ active to inform the NPX that it has accepted the request, then the CPU executes data transmission. For the NPX, data are transmitted as the form of IOR/IOW.

When the CPU meets a command to the NPX (ESC command in a certain format) during decoding, it informs the NPX of it as IOW. During the execution of this command, the NPX makes *BUSY signal active to control the CPU not to transmit ESC command any more. If there is any erroneous calculation during processing, the NPX makes *ERROR signal and *BUSY signal low simultaneously to show the error. The SC9889A/B LSI latches the *BUSY signal and informs the CPU, which stops processing of the commands following the error. The error is transmitted through interruption level 13 (IRQ13) to the CPU. The error treatment by the CPU differs from different application program, and the following two ports are used.

Address	Data	Operation
0F0h (IOW)	No meaning	Clears latched *BUSY signal.
0F1h (IOW)	No meaning	Hard reset the NPX in addition to the above.

The port is not effective when reading.

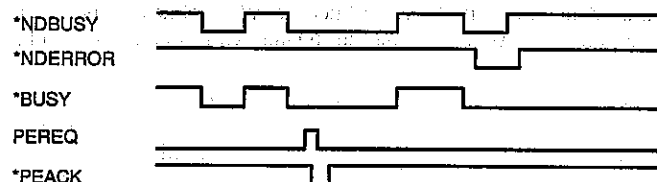


Fig. 4-2

4-2. System control LSI (SC9889B)

The LSI controls all the system using the following functions. The details of the functions are given later.

- CPU interface
- ROM access control
- RAM access control
- HOLD control
- Interruption controller
- Timer
- Serial interface
- RTC & C-MOS RAM
- PORT B
- Power control

4-2-1. CPU interface

This function is divided into the following five blocks:

- Clock control
- Ready control
- Reset control
- Command generator
- Data control

The clock control block forms PRCLK (which is supplied to the CPU) with 14.31818MHz and 23.9616MHz input clocks. With synchronizing the CPU operation phase, PRCLK is divided in 2/4 to generate DMACK. PRCLK is switched into 11.9808MHz, 14.31818MHz, and 23.9616MHz by the software. According to its selection, SYSCK and DMACK frequencies are changed. Table 4-2 shows the relationship.

CPU operating frequency	PRCLK	SYSCK	DMACK
6MHz	11.9808	5.9904	2.9952
7.16MHz	14.3182	7.1591	3.5795
12MHz	23.9616	5.9904	2.9952

Unit: MHz

Table 4-2

Clock used in this LSI includes PRCLK to moderate request for setup time of control signals from the CPU to the LSI.

Since This LSI has CLK stop function, clock before output is used for the circuit which must not be stopped. (SYSCK, DMACK, clock stop circuit, clock select circuit)

Fig. 4-3 shows synchronizing timing of PRCLK, SYSCK, and DMACK.

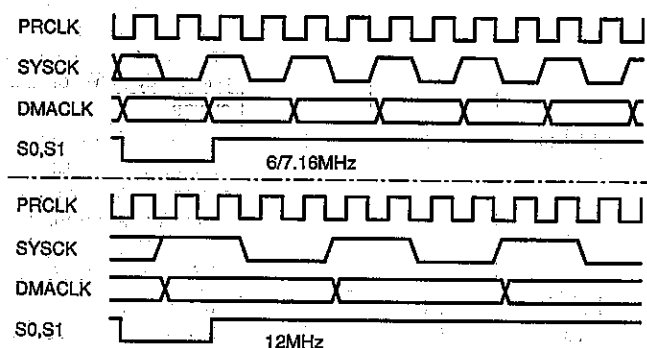


Fig. 4-3

The clock control section generates clocks which are supplied to the timer inside the LSI and the serial interface section. 14.31818MHz is divided into 12 and 1.19MHz is supplied to the timer section. 23.9616MHz is divided into 13 and 1.8432MHz is supplied to the serial interface section.

The ready control section controls cycle length and command signal start timing according to each device access time, address setup time and CPU operating clock. Table 4-3 shows the relationships between the cycle length (wait number) and command starting timing (command delay number) and CPU operating speed and device kinds.

Operating frequency (MHz)	12		7.16/6	
	Wait	Command delay	Wait	Command delay
Device				
Internal RAM (Conventional memory)	1	0	0	0
Internal RAM (Expanded/EMS)	2	0	0	0
ROM	1	0	0	0
V-RAM (8 bit)	7	0	4	0
V-RAM (16bit)	2	0	1	0
Other 8bit memory	11	3	4	0
Other 16bit memory	5	3	1	0
80C287	0	0	0	0
Display device (8bit), system I/O (0 - 0FFH)	7	2	4	1
Display device (16bit)	2	2	1	1
Other 8bit I/O	11	5	4	1
Other 16bit I/O	5	5	1	1
INTA	2	0	1	0

Table 4-3

The reset control section generates reset signal of the CPU and the system. The reset signal to the CPU are generated by the following three factors:

- (1) When PWRGOOD signal is low at power OFF or in case of abnormality.
- (2) When writing in the port by the software.
- (3) When shut down cycle is detected.

In the case of (1), when PWRGOOD signal becomes low, RESCPU signal is made high and kept high with external pull-up resistor (1Kohm). When PWRGOOD signal becomes high, RESCPU is driven high. In phase 2 after 128clock cycles, RESCPU falls to start the CPU.

In the case of (2), this process is performed by the software when the CPU mode is returned from the protect mode to the real mode. That is, when writing is made into I/O address 064h - 0FEh, the LSI decodes it and makes RESCPU line high for about 6 - 7ms to reset the CPU.

In the case of (3), the unit is started in a certain cycle of CPU, which is called shutdown cycle. This cycle is generated when the CPU cannot treat more processes in occurrence of an exception during double fault exception processing. The CPU informs external devices of this state using *S0 = 0, *S1 = 0, M/I/O = 1, and A1 = 1. The LSI detects this sign and makes RESCPU high for 16 clock cycles to reset the CPU.

BRESET signal (system reset) is made high only in the case of (1) to initialize the system. It remains low in the cases of (2) and (3).

The command generator section decodes status signal (*S0, *S1) and M/I/O signal from the CPU to form command signal required in the cycle, and output it according to command delay/wait numbers determined by the ready control section.

There are five command signals and their compositions are shown as follows in Table 4-4.

	*S0	*S1	M/I/O
•*MEMW	0	1	1
•*MEMR	1	0	1
•*IOW	0	1	0
•*IOR	1	0	0
•*INTA	0	0	0

Table 4-4

In this table, *INTA signal (interrupt acknowledge cycle) is used only in the LSI. So it does not output externally.

The data control section controls buffers according to data transmission direction in each operation mode of CPU operation, DMA operation, and MASTER operation. Fig. 4-4 shows the data bus configuration of this unit. (L), (I), (E), and (S) in Fig. 4-4 show device locations of Local, Internal, External, and Slot respectively.

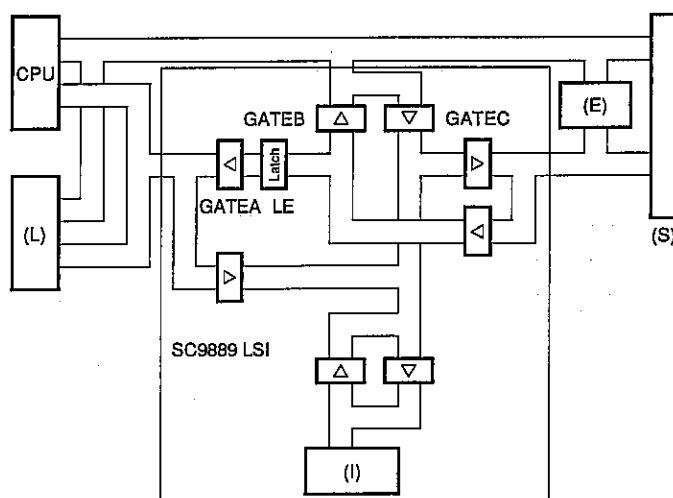


Fig. 4-4

Each device has its effective bus width. I/O device makes *IOCS16 low and memory makes *MEMCS16 low to transmit to the LSI. Address of internal I/O in the RAM or ROM, however, are fixed and decoded in side the LSI without using these signals.

The bus master makes three kinds of access to each device: word, even byte, and odd number byte. These kinds of access are classified as in Table 4-5.

Access kind	A0	-BHE
Word	0	0
Even number byte	0	1
Odd number byte	1	0
Invalid	1	1

Table 4-5

Table 4-6 shows how GATEA, GATEB, and GATEC are controlled by the combination of the following four factors:

- Data transmission direction (Bus master → device, bus master ← device, memory → IO, memory ← IO in DMA)
- Location on the data bus (L, I, E, S)
- Bus width (8 bit, 16 bit)
- Access kind (Word, even number byte, odd number byte)

High ("1") of GATEA/B/C means enable (bus drive).

CPU mode

Write (CPU → device)

In all combinations, GATEA = 0, GATEB = 0, GATEC = 1

Read (CPU ← device)

16/8	LOC	-BHE	A0	GA	GB	GC
16	L	0	0	0	0	0
		1	0	0	0	0
		0	1	0	0	0
	I	0	0	1	1	1
		1	0	1	0	1
		0	1	1	1	1
	E/S	0	0	1	0	0
		1	0	1	0	0
		0	1	1	0	0
8	I	0	0	1	1	1
		1	0	1	0	1
		0	1	1	1	1
	E/S	0	0	1	1	0
		1	0	1	0	0
		0	1	1	1	0

Table 4-6(a)

DMA mode

I/O → memory

16/8	LOC	-BHE	A0	GA	GB	GC
16	L/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	0	1
8	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1

Table 4-6 (b)

Memory → I/O

16/8	LOC	-BHE	A0	GA	GB	GC
16	L	0	0	1	1	0
		1	0	1	1	0
		0	1	1	1	0
	E/S	0	0	1	1	1
		1	0	1	1	1
		0	1	1	1	1
8	E/S	0	0	1	1	1
		1	0	1	1	1
		0	1	1	1	1

Table 4-6 (c)

MASTER mode

Write (Master → device)

16/8	LOC	-BHE	A0	GA	GB	GC
16	L/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1
8	I/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	0

Table 4-6 (d)

Read (Device → Master)

16/8	LOC	BHE	A0	GA	GB	GC
16	L	0	0	1	1	0
		1	0	1	1	0
		0	1	1	1	1
	I	0	0	0	0	0
		1	0	0	1	0
		0	1	0	0	0
	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1
8	I	0	0	0	1	0
		1	0	0	1	0
		0	1	0	0	0
	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	0	1

Table 4-6 (e)

4-2-2. Memory sub system

This unit is equipped with 1MB RAM, 64KB system BIOS ROM, and 32KB display BIOS ROM as standard system memory.

The RAM is composed of two pseudo-static RAM's of 512KB x 8. Optional 1MB memory and 2MB memory card cards can be added to expand memory to max. 4MB. System BIOS and display BIOS are provided in the ROM (128KB x 16). Fig. 4-5 shows the memory map.

Address

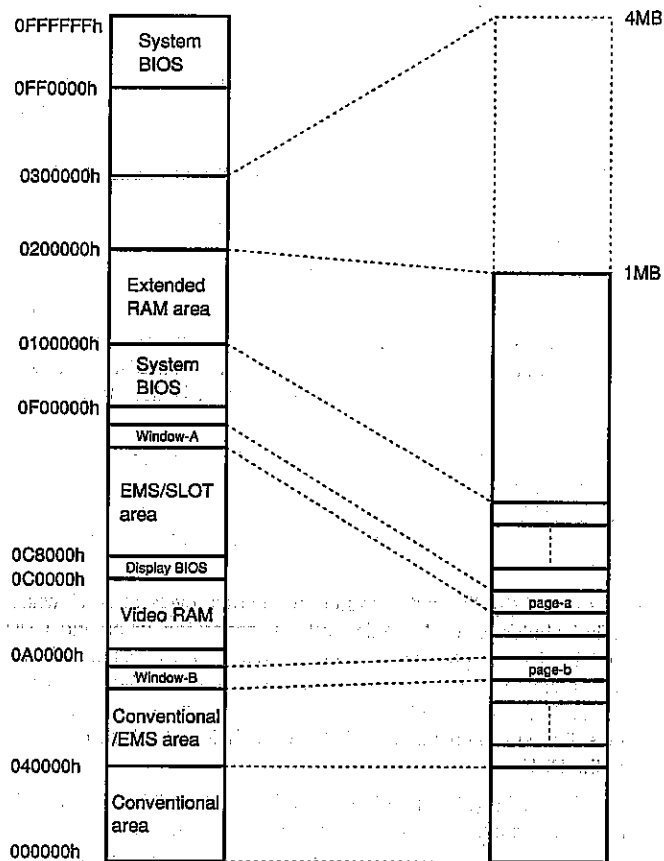


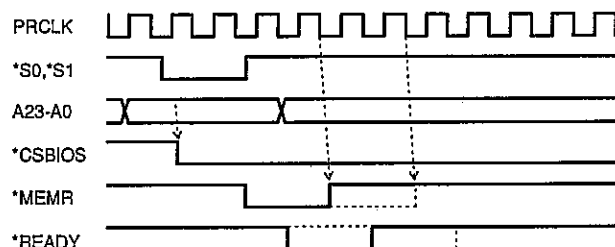
Fig. 4-3

(1) ROM

ROM address signal is supplied by latching the CPU address at the rising of the status signal by the peripheral control LSI (LZ95H25).

The reason why status signal instead of other signals is used for latch is to decrease weight by supplying outputs to the ROM. The upper side of data signal is connected to the CPU data. For the lower side of data, ROM access buffer is used to delay data transmission to reduce the weight number. The chip select signal (*CSBIOS) of ROM is generated by the SC9889A/B LSI.

Immediately after reset, the CPU makes access to the highest position (0FFFFFF0h) of address area. When JMP FAR command is executed, access is made near 00FFFF0h. At that time, the chip select signal becomes low at 0FF0000h – 0FFFFFFh and 00F0000h – 00FFFFFFh to select the same ROM. Since the display BIOS is included in the same ROM, the chip enable signal becomes active in the display BIOS area 00C0000h – 00C7FFFh. The output enable signal uses *MEMR signal. The data buffer enable signal in the lower side for only ROM reading uses ROM chip select signal and *MEMR signal. Fig. 4-6 shows ROM read timing.



Note: Waveform shown in dotted line is for 12MHz operation.

Fig. 4-4

(2) RAM

(2)-1. Pseudo-SRAM control

This chip supports control of a maximum 4MB of the pseudo-SRAM. Memory has three address spaces of the system area, EMS control area, and private area. The EMS control area can further be divided into three subsections of conventional area, extended area, and EMS area by the internal I/O register setting.

(1) System area

The area of 256KB is allocated to 000000H~03FFFFH as the conventional memory.

(2) EMS control area

Address can be allocated to three areas using the internal I/O register setting.

(a) Conventional memory setting

An address space of 384KB can be allocated to 040000 ~ 09FFFFH as a conventional memory area.

(b) Extended memory setting

Address space can be allocated after 100000H as an extended memory area.

(c) EMS area

To support the EMS version 4.0, 34 windows of 16KB increments can be mapped in 040000~09FFFFH and 0C8000H~0EFFFFH.

(3) Private area

Using the internal I/O register setting, a 256KB of address space is allocated to 0E0000H~0EFFFFH (accessed by bank select), which is to be used to save the VRAM contents during the resume and used by the system. The private area may be eliminated by the internal I/O register setting.

NOTE: With the current version of this LSI (TS1), it does not assure the interleave in the 12MHZ non-wait mode. Where, "0" must be written to INTLV of the SPRAMCFL register discussed later.

(2)-2. RAM configuration

(1) System area

Among 4MB memory area supported by the memory controller, a 256KB of address space 000000H~03FFFFH is allocated as a conventional memory, regardless of the internal I/O register setting.

(2) EMS control area

The maximum 4MB area, except for the system area and the private area, is allocated to the EMS control area, and mapped to the conventional area, extended area, and EMS area by the internal I/O register setting.

There are EMSCFR register, PSRAMCF register, and EMSSTAT register that controlled as the internal I/O registers and their bit definitions are shown next.

EMSCFR register

Bit	Signal name	Significance
0~2	SW0~2	EMS control register I/O address setting
3, 4	JP2, 3	Extended memory capacity setting (expansion)
5, 6	SW5, 6	Extended memory capacity setting
7		Reserved. Read/write possible

Table 4-7

PSRAMCF register

Bit	Signal name	Significance
0	RESERVED	Reserved. Read/write possible
1	INTVL	Pseudo-SRAM interleave access enable
2	*PCS3EN	256KB standard RAM usage setting
3, 4	JP0, 1	Extended memory capacity setting
5	VPTMEM	Private memory access enable
6, 7	MAP0, 1	Private memory bank select

Table 4-8

EMSSTAT register

Bit	Signal name	Significance
0~2	SW0~2	State of EMS control register I/O address allocation
3, 4	SW3, 4	Both SW3 and SW4 reads "1" at all times.
5, 6	SW5, 6	State of the extended memory capacity setting
7	EMSEN	EMS on/off setting

Table 4-9

The EMSCFR and PSRAMCF registers are allocated to 04H and 05H of the Sharp original port, and reset to "0" when reset.

SW0~2, and SW5~6 of the EMSSTAT register are read only bits which the data written in the EMSCFR register is read. EMSEN is a read/write bit that turns to "0" when reset.

When operated with the CPU clock at 24MHz, INTLV of the PSRAMCF register, is a bit which enables the non-wait access for the conventional memory and private memory interleave mode when the bit is set to "1".

(a) Conventional setting

To allocate the memory space 040000H~09FFFFH to a conventional memory, EMSEN of the EMSSTAT register must be set to "0" to disable the EMS.

(b) Extended setting

By setting SW5~6, JP2~3, of the EMSCFR register and JP0~1, and *PCS3EN of the PSRAMCF register, the memory space after 100000H can be allocated to the extended memory in a manner as shown next.

SW6	SW5	JP3	JP2	JP1	JP0	*PCS3EN	Extended memory
0	0	*	*	*	*	*	0MB
0	1	*	*	*	*	*	64KB (100000H~10FFFFH)
1	0	0	0	0	0	1	0MB
1	0	0	0	0	0	0	256KB (100000H~13FFFFH)
1	0	0	0	0	1	1	1MB (100000H~1FFFFFH)
1	0	0	0	0	1	0	1.25MB (100000H~23FFFFH)
1	0	0	0	1	0	1	2MB (100000H~2FFFFFH)
1	0	0	0	1	0	0	2.25MB (100000H~33FFFFH)
1	0	0	0	1	1	1	3MB (100000H~3FFFFFH)
1	0	0	0	1	1	0	3.25MB (100000H~43FFFFH)
1	0	0	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	0	1	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	0	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	0	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	1	*	*	0	3.25MB (100000H~43FFFFH)
1	1	*	*	*	*	*	512KB (100000H~17FFFFH)

Table 4-10

*: don't care

* PCS3EN is the bit employed to specify the usage of the 256KB area within the standard RAM which may be used as a private area when "1" and as an EMS control area when "0".

(c) EMS setting

To turn on the EMS, EMSEN of the EMSSTAT register must be set to "1". To support the EMS version 4.0, the EMSADR register and the EMSDAT register are provided as internal registers, whose bit definition is shown in Table 4-11 and Table 4-12 respectively.

EMSADR register

Bit	Signal name	Significance
0~7	EMSADR0~7	EMS mapping register address

Table 4-11

EMSDAT register (EMS mapping register),

Bit	Signal name	Significance
0~7	EMSDAT0~7	EMS mapping register data
8~14	—	Undefined. Reads "0" at all times.
15	EMSPEN	EMS page enable bit

Table 4-12

The EMS control register for the EMSADR register, EMSDAT register, including the EMSSTAT register, is I/O address allocated by SW0~2 of the EMSSTAT register, which are set as shown in table 4-13.

SW2	SW1	SW0	EMSSTAT	EMSADR	EMSDATL	EMSDATH
0	0	0	208H	209H	20AH	20BH
0	0	1	218H	219H	21AH	21BH
0	1	0	248H	249H	24AH	24BH
0	1	1	258H	259H	25AH	25BH
1	0	0	268H	269H	26AH	26BH
1	0	1	2A8H	2A9H	2AAH	2ABH
1	1	0	2B8H	2B9H	2BAH	2BBH
1	1	1	2E8H	2E9H	2EAH	2EBH

Table 4-13

When reset, SW0~2 are reset to "0".

The EMSADR register is a 8-bit read/write register which is employed to point the 34 EMS mappings using EMSADR2~7. EMSADR2~7 is automatically incremented when the high side of the EMSDAT register is accessed. "0" is always read from EMSADR0~1 and write is ignored.

The following shows the address setup range for the EMSADR register

40H, 44H, 48H, 4CH, 50H, 54H, 58H, 5CH, 60H, 64H, 68H, 6CH, 70H, 74H, 78H, 7CH, 80H, 84H, 88H, 8CH, 90H, 94H, 98H, 9CH, C8H, CCH, D0H, D4H, D8H, DCH, E0H, E4H, E8H, ECH

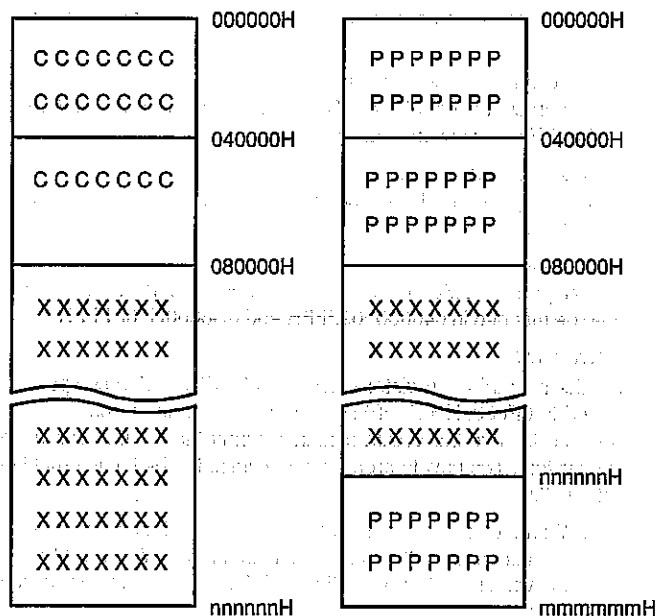
The EMSDAT register is a 16-bit read/write register in the CPU mode and 8-bit read/write register in the master mode, and there are 34 sections. The EMS mapping data is set in EMSDAT0~7 of the EMSDAT register and determines the page that mapped to the window of address space of 040000H~09FFFFH and 0C8000~0EFFFFH. Window can be set on or off for EMSPEN; sets on when "1". EMSDAT8~14 are read "0" at all times and write is ignored.

When the EMSADR register is out of the setup address range, EMSDAT0~15 is read "0" and write is ignored.

To obtain the EMS control area, subtract the system area and the private area from all memory area supported by the memory controller.

Its capacity is max. 3.75MB when the private memory is not used (*PCS3EN = 0).

Fig. 4-7 shows the mapping of the EMS control area.



Memory map for the conventional memory

Memory map for the EMS

Fig. 4-7

"C" represents conventional memory mapping, "X" represents extended memory mapping, and "P" represents expanded memory mapping. "nnnnnnH" is depends to the extended area setting, "mmmmmmH" to the actually installed memory capacity.

The actually installed memory capacity may be set to "nnnnnnH" when mapping the conventional memory. For an example, the extended area for the 4MB memory, it should be set to 3.25MB and "nnnnnnH" is 3DFFFFH (in case *PCS3EN=0).

When mapping the EMS memory, the capacity under the actual memory capacity should be set to "nnnnnnH". For the 4MB of actually installed memory, the EMS area should be set to 0~3.25MB. If 0MB was set, all are mapped as the EMS memory.

(3) Private area

It may be possible with the internal I/O register setting to reserve a 256KB private area out of the memory controller supported 4MB memory.

To reserve the private area, set *PCS3EN of the PSRAMCF register to "1" and set 256KB of the internal standard RAM as the private memory. Set EMSEN of the EMSSTAT register to "0" and PVTMEM of the PSRAMCF register to "1", which is then mapped to the address space of 0E0000H~0EFFFFH.

To access the 256KB private memory, four banks must be selected using MAP0~1 of the PSRAMCF register.

4-2-3. Hold mediation and sleep function

This function mediates DMA request, refresh request, and HOLD request during sleep and applies HOLD to the CPU. It also delivers acknowledge for each request. The mediate circuit is composed of three sets the D-F.F. connected in series in two stages. The first F.F. samples each request to process it by determining priority between requests which are under process and requests which are sampled. Then the requests are sent to the second F.F. If there is any request which is under process, the other requests are kept waiting until the process is completed. When two or more requests are made simultaneously, DMA request has the first priority, and sleep request has the last priority.

The second F.F. and the AND of HOLD and HLDA signals are used as acknowledge of the requests.

The sleep function stops the clock which is supplied to the CPU until the interruption line becomes active after HLT command is executed in order to reduce power consumption of memory. When the unit goes into the sleep mode, HOLD signal is made high to request bus hold to the CPU. When the acknowledge (HLDA) signal returns, the clock is stopped in the first phase 2. This is because the power consumption is minimized in that state. Then the hold request is cancelled, and delay of 3SYSCK cycle is made in the externally attached circuit to drop HLDA signal which is inputted to the LSI. Since the clock is stopped, the CPU is kept hold. The LSI returns to the normal state. Though there is DMA request or refresh request in the sleep, they can be processed without competition. When the CPU executes HLT command S0 and S1 are made low and M/IO and A1 are made high to show the hold state. The sleep controller detects it and the unit goes into the sleep mode in the following sequence.

- (1) HOLD request is delivered to the CPU. When refresh request or DMA request is overlapped, the mediate circuit will mediate it.
- (2) Hold acknowledge is confirmed to stop the CPU clock in synchronous with the falling of clock which is inputted to the controller in φ2.
- (3) HOLD request (HOLD signal) by the sleep is cancelled. In this case, the CPU is kept hold.
- (4) After the HOLD signal is made low by the external D-F.F. (3 stage), HLDA signal is delayed by 3 clocks of SYSCK. DMA in the sleep is transmitted and refresh is made in this state.

Escape from the sleep mode occurs when any interruption request including NMI is generated. When an interruption occurs, the CPU clock supply is resumed in synchronous with falling of the clock which is inputted to controller. The CPU starts execution of the command next to the HLT.

When the input from the EXPND terminal is low, it is regarded that the expansion unit is connected, and procedure (1) to (4) are prohibited and the sleep function is not performed.

4-2-4. Interrupt control

A pair of 82C59A interrupt controllers are internally contained in this chip for the interrupt control and supports 16 interrupt levels in conjunction with the cascade connection NMI. The NMI is port-B controlled.

As an 8-bit I/O device on the system bus (XD bus), a pair of 82C59A has address mapped to 020H~03FH on the master side and 0A0H~0BFH. In order to avoid contention with the CPU clock switch controlling I/O address 022H and 023H for the 82C59A on the master side, the selection is not done when the bit of the latch address is "1".

Table 4-14 shows the 82C59A interrupt outputs.

Master	Slave	Function
IRQ0		Timer output channel 0
IRQ1		Keyboard (output buffer full)
IRQ2		Interrupt from the slave side controller
	IRQ8	Real time clock interrupt
	IRQ9	VGA controller or INT0AH (IRQ2)
	IRQ10	Reserved (expansion slot)
	IRQ11	Reserved (expansion slot)
	IRQ12	Reserved (expansion slot)
	IRQ13	Co-processor
	IRQ14	Hard disk controller
	IRQ15	Reserved (expansion slot)
IRQ3		Serial port 2 (COM2)
IRQ4		Serial port 1 (COM1)
IRQ5		Parallel port 2
IRQ6		Floppy disk controller
IRQ7		Parallel port 1

Table 4-14

4-2-5. Timer

A single 82C54 interval timer is internally contained in this chip. The 82C54 is mapped to the I/O address 040H~05FH as an 8-bit I/O device on the system bus (XD bus). Three independent 16-bit counter on channels 0~2 of the 82C54 can be defined Table 4-15

Channel 0	System timer
GATE0	Fixed ON
CLKIN0	1/12 14.31818MHz clock
CLKOUT0	82C59A IRQ 0
Channel 1	Refresh request generator
GATE1	Fixed ON
CLKIN1	1/12 14.31818MHz clock
CLKOUT1	Refresh request cycle
Channel 2	Speaker tone generator
GATE2	Fixed ON
CLKIN2	1/12 14.31818MHz clock
CLKOUT2	Speaker drive

Table 4-15

4-2-6. Serial interface

The 82C50 UART is internally contained in this chip as a serial interface and supports a single channel RS-232C interface using the external RS-232C driver as an internal SIO. This also used for interface with the internal modem.

Two serial interfaces may be port allocated and set on or off, which the SIOCFR register is used for the RS-232C and the MDMCFR register for the internal modem. The SIOCFR register is a 7-bit read/write register which is allocated to 01H of the Sharp original port. The MDMCFR register is a 2-bit read/write register which is allocated to 03H of the Sharp original port.

Table 4-16 and 4-17 shows bit definition for SIOCFR and MDMCFR registers.

SIOCFR register

Bit	Signal name	Significance
0~2	FDD0~2	Reserved. Read/write possible.
3	*SIOEN	Internal SIO port allocation
4	SIO1/*2	Internal SIO on/off setting
5	*INTKEY	Reserved. Read/write possible.
6	*LCDEN	Display device selection
7	—	Undefined. Reads "0" at all times.

Table 4-16

MDMCFR register

Bit	Signal name	Significance
0	OUTSEL	MORSTN output signal selection
1~3	—	Undefined. Reads "0" at all times.
4	*MDMEN	Internal modem on/off setting
5~7	—	Undefined. Reads "0" at all times.

Table 4-17

When reset, *SIOEN of the SIO CFR register and *MDMEN of the MDMCFR register are set to "1" and all others are reset.

*SIOEN and SIO1/*2 of the SIOCFR register may be revised of their contents when written to "02" to the Sharp original port. The inverted bit 4 of the 02H port corresponds to SIO1/*2 and bit 5 to SIOEN.

Table 4-18 shows the ports that are allocated by the setting of SIOCFR and MDMCFR registers vs. active input to IRQ3 and IRQ4 of the 82C59A.

*SIOEN	*MDMEN	SIO1/*2	Internal SIO	Internal modem	IRQ3 input	IRQ4 input
0	0	0	COM2	COM1	Internal SIO	Internal modem
0	0	1	COM1	COM2	Internal modem	Internal SIO
0	1	0	COM2	OFF	Internal SIO	External IRQ4
0	1	1	COM1	OFF	External IRQ3	Internal SIO
1	0	0	OFF	COM1	External IRQ3	Internal modem
1	0	1	OFF	COM2	Internal modem	External IRQ4
1	1	0	OFF	OFF	External IRQ3	External IRQ4
1	1	1	OFF	OFF	External IRQ3	External IRQ4

Table 4-18

The RS-232C interface serial input/output and control signals can be inverted with POLINV of the VGACNT register. When POLINV is at "1", the polarity inverts. The VGACNT register is allocated to 0EH of the Sharp original port whose bit definition is shown in Table 4-19.

VGACNT register

Bit	Signal name	Significance
0	POLINV	RS-232C input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2, 3	PWRDWN1, 2	VGA controller mode setting
4~7	RESERVED	Reserved. Read/write possible

Table 4-19

When reset, all are reset to "0".

To reset the internal modem that can be installed within the machine, the output from the MORSTN line is used. The 1-bit output of the MORSTN output port can be switched with the port select signal output using OUTSEL of the MDMCFR register. When OUTSEL is at "1", the bit 3 of the I/O address 202H port is issued. When "0", the decoded signal of the I/O address 202H is issued as a port select signal. The 202H port is a read/write internal I/O register whose bit definition is shown Table 4-20.

202H port

Bit	Signal name	Significance
0~2	RESERVED	Reserved. Read/write possible
3	MORSTN	Internal modem reset signal
4	RESERVED	Reserved. Read/write possible
5~7	—	Undefined. Reads "0" at all times.

Table 4-20

When reset, bits 0~4 are reset.

4-2-7. RTC and CMOS RAM control

For this chip, RTC is controlled by AS, DS, R/W, and SCRTCN outputs. For setup expansion, a 2KB CMOS RAM is provided.

Among 11 bits address input of the 2KB CMOS RAM, the low 6 bits is connected to the I/O 070H port bits 0~5, and high 5 bits to the latch address bits 10~14. Which is to be selected, RTC or CMOS RAM, when the I/O 071H port is accessed is determined by the data in the I/O 70H bit 6. When "0", RTC is selected and "1" the CMOS RAM. See Fig. 4-8 for the mapping of the RTC and the CMOS RAM.

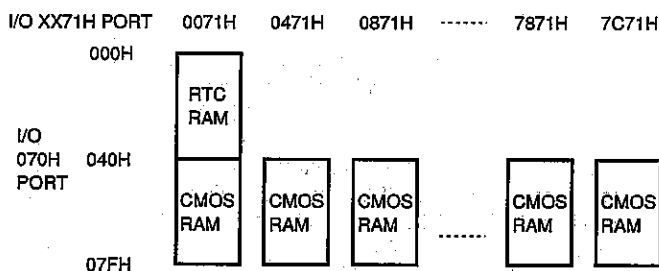


Fig. 4-8

4-2-8. Port-B

The port-B consists of a logic gate which is used for NMI occurrence control, speaker output control, and refresh detection by the parity and I/O channel checks.

4-2-9. Power control

The system power source is divided into several blocks to allow each block to be turned on/off separately. Therefore, the power control section is equipped with the port to turn off the power sections which are not used. For that purpose, VLCCNT, VBLCNT, VMDCNT, VIFCNT, VCCOFF, and *ONRSM are provided. The state where the power is supplied but no operation is requested is detected and if the state continues for a certain period, the power is automatically turned off.

For the power control port, a part of SOP (Sharp Original Port) assigned to 07Ch and 07Dh is used. Port number (called as index) is written into 07Ch of SOP and read/write is made with the data in 07Dh. When 07Dh is accessed, the index is cleared to be No. 0. therefore 07Ch must be set for each time. SOP related to the power control section is shown in Table 4-21 through 4-30.

PWRCNT register (Index 06Ch, R/W)

Bit	Signal name	Meaning
0	PCVIF	Printer/RS-232C interface IC control
1	PCVLCD	VGA controller and LCD power control
2	PCVCC	System power (Vcc) control
3	PCBL	Back light power control
4	PCVMD	MODEM power control
5 ~ 7	RESERVED	Reservation bit, Read/Write allowed

Table 4-21

When resetting, each bit of PCVIF, PCVCC, PCBL, and PCVMD are set to "1" and the others are reset.

ATSTBY register (Index 07Ch, R/W)

Bit	Signal name	Meaning
0	ASVIF	Auto I/F power off enable/disable setting
1	ASLCD	Auto power save enable/disable setting
2	ASVCC	Auto resume enable/disable setting
3 ~ 7	RESERVED	Reservation bit, Read/Write allowed

Table 4-22

When resetting, all are reset to "0."

RWRSTAT register (Index 08Ch, R/O)

Bit	Signal name	Meaning
0	PSVIF	Printer/RS-232C interface IC control state
1	PSLCD	LCD power (VLCD) state
2	PSVCC	System power (Vcc) state
3	PSBL	Back light power (VBL) state
4	PSVMD	MODEM power (VMDM) state
5 ~ 7	—	Reservation bit. Always reads "0."

Table 4-23

PWRTIM register (Index 09h, R/W)

Bit	Signal name	Meaning
0 ~ 3	PST0 ~ 3	Auto power save time setting
4 ~ 7	RESERVED	Reservation bit, read/write allowed.

Table 4-24

When resetting, PST3 ~ 0 are set to "1," and the others are reset.

RSMTIM register (Index 0Ah, R/W),

Bit	Signal name	Meaning
0 ~ 6	ART0 ~ 6	Auto resume time setting
7	RESERVED	Reservation bit, Read/Write allowed.

Table 4-25

When resetting, ART6 ~ 0 are set to "1," and bit 7 is reset.

RSMCNT register (Index 0Bh, R/W)

Bit	Signal name	Meaning
0	RSMEN	Resume mode setting
1	CIEN	Reservation bit, read/write allowed.
2	MRIEN	Reservation bit, read/write allowed.
3 ~ 7	RESERVED	Reservation bit, read/write allowed.

Table 4-26

When resetting, all are reset to "0."

RSTFCT register (Index 0Ch, R/O)

Bit	Signal name	Meaning
0	—	Not defined. Always reads "0."
1	RCR	System power (Vcc) OFF request effective state
2	RCCI	Internal SIO power ON factor state by CI input
3	RCMRI	Internal modem RI input power ON factor
4 ~ 7	—	Not defined. Always reads "0."

Table 4-27

EXSTAT register (Index 0Dh, R/O)

Bit	Signal name	Meaning
0	EXPND	Expansion unit contact state
1 ~ 7	—	Not defined. Always reads "0."

Table 4-28

VGACNT register (Index 0Eh, R/W)

Bit	Signal name	Meaning
0	POLINV	Internal SIO input/output polarity reversion
1	DISVGA	Internal VGA enable/disable setting
2	PWRDWN1	VGA controller mode setting (relax mode)
3	PWRDWN2	VGA controller mode setting (retire mode)
4 ~ 7	RESERVED	Reservation bit, read/write allowed.

Table 4-29

When resetting, all are reset to "0."

NMIFCT register (Index 0Fh, R/O)

Bit	Signal name	Meaning
0	RSMNMI	Resume NMI request effective state
1 ~ 7	—	Not defined. Always reads "0."

Table 4-29

Fig. 4-9 shows the outline of the power control section of this unit.

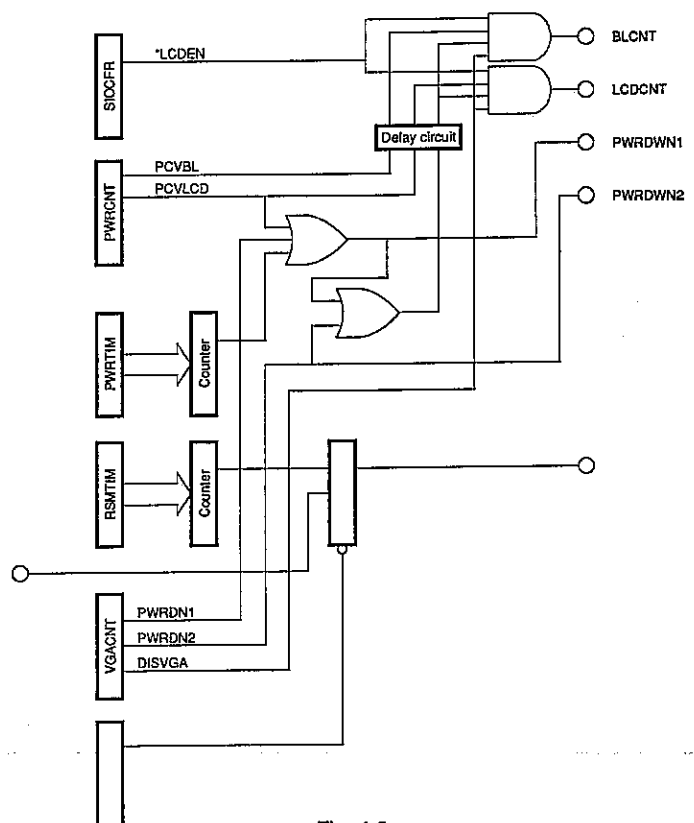


Fig. 4-9

The basic functions of the power control section are shown Table 4-31.

Control by the ports

Control item	Control signal	ON condition	OFF condition	Remarks	
LCD	*LCDEN	0	1	SOP1	bit 6
	DISVGA	0	1	SOPE	bit 1
	PCVLCD	1	0	SOP6	bit 1
	PWRDWN1	0	1	SOPE	bit 2
	PWRDWN2	0	1	SOPE	bit 3
	SHUT	1	0	Cover close external signal	
Back light	*LCDEN	0	1	SOP1	bit 6
	DISVGA	0	1	SOPE	bit 1
	PCVBL	1	0	SOP6	bit 3
	PWRDWN1	0	1	SOPE	bit 2
	PWRDWN2	0	1	SOPE	bit 3
	SHUT	1	0	Cover close external signal	
I/F power	PCVIF	1	0	SOP6	bit 0
Modem	PCVMD	1	0	SOP6	bit 4

Table 4-31

Control by the timer

This unit provides the following two functions using the basic functions in Table 4-32.

Control item	Control timer	Prohibit condition	Reload condition	
LCD back light	PWRTIM SOP9 Bit 3 - 0	ASLCD = 0 SOP7 bit 1	①	IRQ1 rising
			②	Internal SIO interruption
			③	Write to SOP6, 7, 9
I/F power	15 minutes fixed	ASVIF=0 SOP7 bit 0	①	Access to printer port
			②	Access to SIO
			③	Write to SOP6, 7
NMI	RSMTIM SOPA bit 6 - 0	ASVCC=0 SOP7 bit 2	①	IRQ1 rising
			②	Internal SIO interruption
			③	Write to SOP6, 7, A

Table 4-32

(1) Power save function

When the keyboard/mouse is not used for a certain period, LCD/back light power is turned off (auto power save). Each of LCD and back light power can be independently turned off by software.

(2) Standby function

The power to maintain the system state is kept ON and the other powers are turned off and the power consumption is minimized in the sleep mode. When an expansion unit is connected, this function cannot be used.

The power save function detects conditions which can be regarded as that the unit is not operated. If that conditions continues for a certain period, The LCD and the back light powers are automatically turned off. The power save controller includes one minute timer. Count is made when there is not interruption request from the key controller (8042), interruption from internal SIO set to COM2, or write access to SOP6, 7, 9. When a predetermined time is reached, LCDCNT signal and BLCNT signal are made low and the LCD and the back light are turned off. For versions outside Japan, PWRDWN1 signal is made high to set the VGA controller to the sleep mode and to stop the display cycle, reducing current consumption in V-RAM.

VGA controller operation mode can be directly set with internal I/O

register (SOP_VGACNT register). The Mediate mode and the sleep mode are set by PWRDWN1 and 2 of VGACNT register. In the sleep mode, the display cycle is stopped but read/write from the bus master is enabled. In the Mediate mode, cycles to V-RAM other than refresh are prohibited. When either of PWRDWN1 or 2 is made high, both LCDCNT and BLCNT signals are made low to turn off the power of LCD/Back light.

VGA controller operation mode is as follows according to PWRDWN1 and 2 in Table 4-33.

PWRDWN2	PWRDWN1	LCD power	BL power	VGA controller	Remark
0	0	ON	ON	Normal mode	
0	0	ON	OFF	Normal mode	PWRCNT register PCBL = 0
0	0	OFF	OFF	Relax mode	Auto power save or PWRCNT register PCLCD = 0
0	1	OFF	OFF	Relax mode	
1	0	OFF	OFF	Retire mode	
1	1	—	—	Prohibition	

Table 4-33

When the power save function is used, PWRDWN1, 2 are set to "0." DISVGA is set to "0" to make the internal VGA effective. SIOCPR register and *LCDEN is set to "0" and LCD is selected as the display device.

To directly turn off the LCD power and the back light power by software, write "0" to PCVLCD and PCBL of PWRCNT register. In this case, similarly to the auto standby, PWRDWN1 signal is driven to high and the VGA controller goes into the mediate mode. When, therefore, it is required to turn off the LCD/back light power in the CRT mode, *LCDEN is driven to high. In this case, PCVLCD must be kept to "1."

When the power save function (auto power save) by the timer is used, PCVLCD and PCBL of PWRCNT register are kept to "1." "1" is written into ASLCD of ATSTBY register to make the timer effective, and the time to require for PWRTIM register power save is set.

PWRTIM register sets auto power save time. Setting is made in the range of 0 to 15 minutes in increment of 1 minute by PST3 - 0. The actual time, however, is shorter than the set value by less than 1 minute. When all of PST3 - 0 are "1," the set value is 14 - 15 minutes. In read/write enable mode, the set value is read. When interruption request signal (IRQ1) from 8042 or internal SIO interruption signal set to COM2 rises before reaching the set time, the set value is reloaded to the timer and counting is restarted from the beginning. When the Sharp Original Port, PWRCNT register, ATSTBY register or PWRTIM register is written, the timer is reloaded.

To use the standby function, write "1" into RSMEN of the RSMCNT register to enable this function. To shift to the standby mode, there are following two cases:

- (1) Ctrl + Alt + Pause is pressed and rising waveform is inputted from the 8052 keyboard controller to the RSMSW terminal.
- (2) The keyboard or mouse is not operated for a certain period.

In the case of (1), high level signal is outputted from the NMI terminal at the rising edge of signal which is inputted from RSMSW terminal, and NMI is applied to the CPU. While in the case of (2), the timer in the resume controller keeps counting while there is no interruption request from 8042 or interruption request from internal SIO. When the set time is reached, NMI is generated. However, similarly to the sleep function, if the input from EXPND terminal is low, NMI output is prohibited and the resume function does not work. EXPND terminal

input state can be read by EXPND of the EXSTAT register.

When using the resume function (auto resume) by the timer, write "1" into ASVCC of the ATSTBY register to make the timer effective, and set the time to power down of the RSMTIM register. The RSMTIM register sets the auto resume time. The setting can be made from 0 to 127 minutes by increment of 1 minute by ART6 – 0. The actual time, however, is shorter than the set value by less than 1 minute. When all of ART 6 – 0 are "1," time is set to 126 – 127 minutes. In read/write enable, the set value is read. In the same manner as the auto power save, when interruption request signal (IRQ1) from 8042 or interruption request signal from internal SIO rises, the set value is reloaded into the timer and the counting is started from the beginning. When the Sharp Original Port PWRCNT register, ATSTBY register, or RSMTIM register is written, the timer is reloaded.

In either case of (1) or (2), the process after generation of NMI is the same, and must be supported by software.

To make power down in the resume mode, the following procedures are required in the NMI process routine.

- (1) Judge the NMI factor.
- (2) Stand the flag which shows generation of the NMI which requests standby.
- (3) Check this flag in the timer interruption (IRQ0) process routine, and judge if the unit may go into the standby mode. (During access of FD/HD, shift to the standby cannot be made.)
- (4) Operate the PWRCNT register to cut off each block power. Control the HD controller to cut off HD spindle motor.
- (5) Execute HLT command to go into the sleep mode.

To judge the NMI factor in (1), the NMIFCT register is read. When RSMNMI bit is "1," RSMSW input or NMI by resume timer is generated. Reset from the standby mode is made by pressing Ctrl + Alt + Pause keys. In this case also, the NMI is generated.

This unit is equipped with register group to reduce current consumption by turning off the printer/RS232C driver/receiver power. This function is called as the interface power off. This function enables to reduce current consumption of the interface IC when the printer and RS-232C are not used. The interface power off function works when there is no access to the printer or internal SIO for a certain period (auto interface power off), or when the internal I/O register is directly operated by software.

To directly operate the interface power off by software, write "0" into PCVIF of the PWRCNT register. In this case, the printer interface IC output becomes Hi-Z and the RS-232C line driver receiver goes into the standby mode, reducing the circuit current.

When the auto interface power off is used, PCVIF of the PWRCNT register is kept to "1," and "1" is written into ASVIF of the ATSTBY register to enable the timer. The timer is cleared when access is made to the internal printer and the internal SIO. The timer is cleared also when data are written into PWRCNT register of Sharp Original Port or into ATSTBY register. It takes 14 to 15 minutes until the power off function works after the timer is cleared.

As interface power off, the internal modem power can be controlled. To turn off the power (VMDM) of internal modem, write "0" into PCVMD of the PWRCNT register. By this, signal is outputted from the VMDCNT terminal to turn off the modem power.

In the case of auto power off or auto interface off, the power is automatically turned off by the timer and the CPU can read states of the LCD power, the back light power, and the printer/RS-232C control by reading the RWRSTA register. The PWRSTA register is a read-only register and assigned to 08H of the Sharp Original Port. Except for PSVIF, PSLCD, and PSBL, the power control data set by the PWRCNT register are read. When "0," it is OFF, and when "1," it is ON.

4-3. Peripheral control LSI (LZ95H25)

4-3-1. Printer interface

The printer port has three ports inside the LZ95H25, and the flipflop and input/output buffer between the LZ95H25 and the printer connector.

Printer ports, port-1 [378H] [379H] [37AH] and port-2 [278H] [279H] [27AH] can be selected by the Sharp original port.

No print data and printer control signals will be issued when the CNT_D from the printer connector is other than a low state.

4-3-2. VGA interface

There are two write only register in the LZ95H25 besides the display chip. Those registers limit the address used by the VRAM.

Write 06H in 3CEH, then write the data in 3CFH, which are set in Table 4-34.

I/O address		Bit allocation
3CEH	Graphics address	06H
3CFH	Miscellaneous register	Bit 3, 2

bit3	bit2	Address used
0	0	A0000H~BFFFFH
0	1	A0000H~AFFFFH
1	0	B0000H~BFFFFH
1	1	B8000H~BFFFFH

Table 4-34

4-3-3. Power save

As signal VIFCNT from the SC9889 controls the buffer between the serial interface and the printer interface, it saves the power equaling to the buffer.

4-3-4. Floppy Interface

There are FDD drive select circuit, oscillator switching circuit, FDC interface (16MHz or 19.2MHz) circuit and one of the Sharp original port which switch the external and the internal FDD.

4-4. Keyboard

Main parts of the keyboard interface is managed by two devices of the 80C42 and the 80C52. The 80C52 scan the keyboard matrix and its data is sent to the 80C42 in a serial form. Since the signal on the keyboard matrix is analog, depression of a key is informed by interrogating the voltage. In order to allow the 80C52 to handle this signal, there is a need of a digital to analog conversion which is carried out by the keyboard interface chip (3JD2CA1A). Not only the 80C42 converts it to the form that the scanned data may be handled by the processor (ASCII/JIS), an interrupt is caused to the processor via the IRQ1 line. The processor reads the keyboard data from the 80C42 within the interrupt routine and stores in the key buffer.

SIOCFR register (Index 02H, R/W)

Bit	Signal name	Significance
0~2	FDD0~2	Reserved bit, read/write possible
3	*SIOEN	Internal SIO on/off setting
4	SIO1/2	Internal SIO port allocation
5	*INTKEY	Internal key on/off setting
6	*LCDEN	Display device selection
7	—	Undefined

Table 4-35

4-5. Display circuit

This model has a 82C455 VGA display controller for both LCD and CRT display. In VGA (Video Graphics Array) mode, maximum resolution is 640 × 480, 256 colors out of 256k colors (in CRT), 16 gray scale for LCD. And also the backward compatibility (MDA, CGA, EGA HGC) is supported in this chip.

4-5-1. Overview of Display System

1) Display mode

The display mode of this model is not only compatible to VGA, but also EGA, CGA, MDA and HGC display adaptors.

In the cases of IBM VGA etc., some of CGA application softwares are not able to excuted properly though, with this model, even those application softwares can be excuted successfully.

2) VGA mode (Video Graphics Array)

An analog type display will be used with the VGA mode and can be displayed 256 colors simultaneously out of 256 thousands colors. And it supports 480 lines in the horizontal resolution in addition to current maximum resolution of 400 resolution.

3) EGA mode (Enhanced Graphics Adaptor)

A digital type display will be used with the EGA mode and can be displayed 16 colors simultaneously out of 64 colors. And it supports 350 lines in the horizontal resolution.

In the cases of VGA or EGA modes, the CG font will be given by the software when booting, the BIOS sets up the default of CG font.

4) CGA mode (Color Graphics Adaptor)

A digital type display will be used and it supports 200 lines in the horizontal resolution.

5) MDA mode (Monochrome Display Adaptor)

A monochrome digital display will be used, it only supports 720 × 350 dots resolution character mode. (in case of PC-6500, 640 × 350 dots resolution.)

6) HGC mode (Hercules Graphics Card)

A monochrome digital display is used with graphics card made by Hercules and has graphics function. The function of HGC itself is expanded version of MDA, and normally initiated at the same mode of MDA.

Since the graphics mode of HGC is 720 × 348 dots, the PC-6500 will only supports to CRT.

4-5-2. The relationship between each mode and display type

Display type \ Mode	VGA	EGA	CGA	MDA	HGC	Connector
Analog Display for VGA	○	○	○	○	○	Analog
Enhanced Color Display	×	○	○	×	×	Digital
Color Display	×	×	○	×	×	Digital
Monochrome Display	×	×	×	○	○	Digital
LCD	○	○	○	○	△	—

○ Support △ Functions as MDA × Not support

Table 4-36

In table 4-36 the display type and mode should be selected on the set-up menu, and effective when the system is booted. The selection of LCD and CRT can be switched by the slide switch located on the side of the main unit.

4-5-3. VGA mode control

The color display control of this model VGA mode.

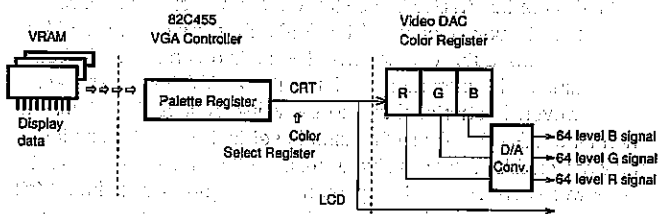


Fig. 4-10

Since the display to LCD is not through the Video DAC as shown in Fig. 4-10, the application software using Video DAC will only be effective to CRT.

4-5-4. Display toning this model

This model is capable to display 16 toning and selects the tone by giving the each toning data to the palette register.

The following method is used for managing 16 kinds of tone for this model.

In case of 16 tones, the basic frame frequency is normally 15 times. ON and OFF action of 1-dot on the LCD is made at the cycle 0/15, 1/15, 2/15, 15/15. However, because of the characteristic of the LCD, the display flickering is unavoidable at the cycle time of 1/15.

To reduce the flickering for this model, the following measures are taken;

- 1) Increases frame frequency
- 2) Increases basic cycle time
- 3) Shifts the ON/OFF cycle of neighboring dots

Even the above measures are taken for this model, there are still little flickering existed as follows;

- 1) Because of 16 toning, it is unavoidable to have some part of flickering tone.
- 2) It is not possible to shift the ON/OFF cycle of neighboring dot in the tile pattern display mode, therefore, at this mode, little flickering are shown.
- 3) Low resolution mode like 320 dots in width, 2 × 2 dots are used to display 1 dot on the LCD, since 2 × 2 dots make ON/OFF action at the same time. Thus, the flickering is noticeable.

4-5-5. Compensation capability

The resolution of the LCD is 640 × 480 dots though, only 640 × 400 dots resolution is used for text mode. In this case, all the dots of LCD is not used by doing centering operation.

Also, this model is capable to handle a full screen of 640 × 480 dots at Expanded mode of LCD.

The above function is called "Compensation capability", and there are two types of compensations. One is text compensation, and the other is graphic compensation. Text compensation is displayed in Fig. 4-11, and graphic compensation is in Fig. 4-11.

[Text Compensation]

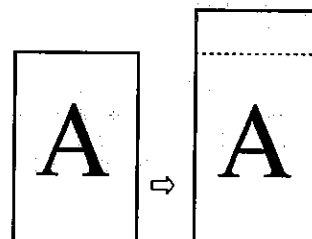


Fig. 4-11

At text mode, the 350 or 400 lines horizontal resolution is compensated by enlarging the most upper line of the character font.

However, since most CG fonts used in Europe countries, use the upper line is used also as character data. Therefore, if this method is applied to those fonts, the compensated character is changed to non-existent wrong character. This model does not use this method actually.

[Graphic Compensation]

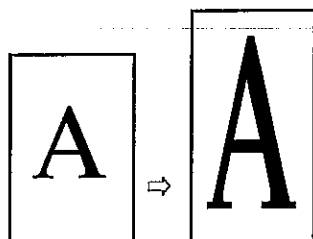


Fig. 4-12

The horizontal resolution is enlarged by duplicately 1-line per several lines over on all the screen. In this case however, since the duplicated line not always sets in between two characters. If a duplicated line sits on a character, the character looks distorted.

The graphic compensation function is originally used for graphic mode though, also used for text mode for this model.

4-5-6. Conventional CRT support (clock switching)

In VGA mode, analog CRT is used to present the beautiful color but in another mode CGA/MDA, digital (conventional) CRT is needed. In order to support these CRTs, clock pulses can be changed by the signal from 82C455 (ERMEN signal) Refer to Fig. 4-13.

When ERMEN signal is HIGH,
28.322 MHz (for VGA monitor)
25.175 MHz (for EGA monitor) are selected.

When ERMEN signal is LOW
16.257 MHz (for MDA monitor)
14.31818 MHz (for CGA monitor) are selected.

The ERMEN signal is set by the BIOS according to the CRT type assigned in the SETUP menu.

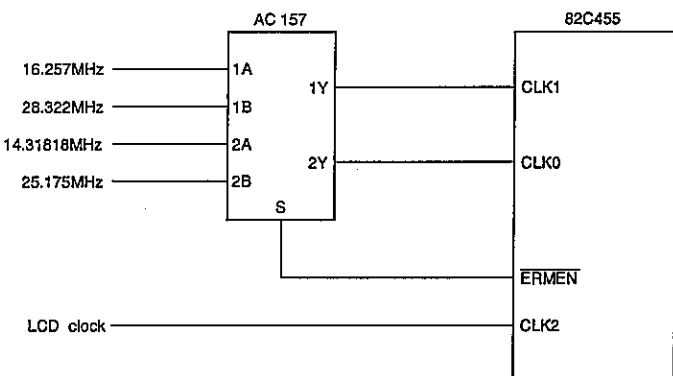


Fig. 4-13 clock switching

4-5-7. Address/Data multiplexer

The 82C455 uses several pins for address/data to reduce the number of the pins. So the address/data multiplexer is needed.

(Refer to Fig. 4-14)

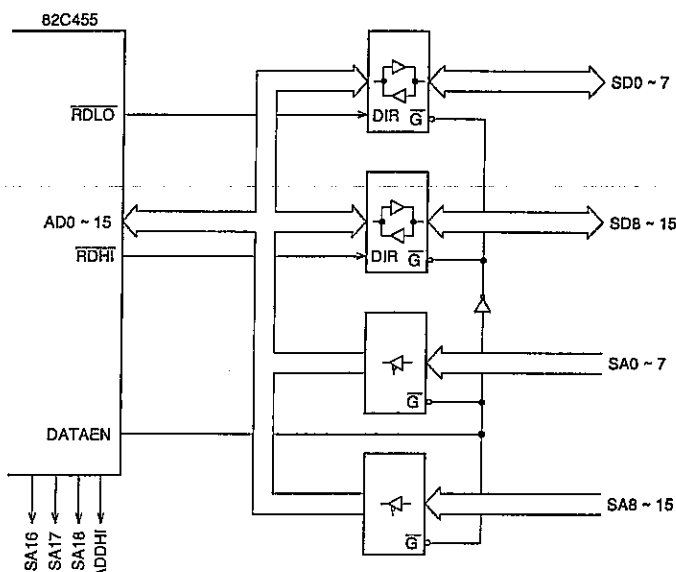


Fig. 4-14

Address/data multiplexer

4-6. Description of black/white liquid crystal backlight inverter (type: IV18106)

4-6-1. General

This PWB unit is employed to drive the LCD backlight (cold cathode ray tube) which will be directly installed to the plastic cabinet inside the display. Three connectors are used for the I/O and control signal interfacing.

- NOTES:
1. This unit drives the entire backlight circuit with the power supply only, except that it is connected with an external VR and control lines.
 2. Since it is an assembly unit, parts replacement and repair are not allowed. In case it has to be replaced with a new one, unfasten the connectors and remove screws.
 3. Pay attention to a high tension voltage of 1000V on the secondary side when operating. For wires that are exposed over and below the transformer, these must be treated with care as it may result in wire breakage.
 4. Since this unit is compact and low profile, the board height is low, width narrow, and long in the longitudinal direction, it would be liable to damage if subjected to twisting. So, never drop or twist it to avoid possible damage.

4-6-2. Electrical characteristics

(1) Maximum allowable ratings

Parameter	Symbol	Rating
Input voltage	Vin	16V
Input power	Pin	3.6W
Operating temperature	Ta	0~50°C
Storage temperature	Ts	-20~75°C
Operating humidity	RH	80% with maximum wet ball humidity at 35°C

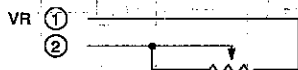
Table 4-37

(2) Electrical characteristics

Parameter	Symbol	Nominal	Note
Input voltage	V_{in}	DC12V	(9.0~16.0V)
Input current	I_{in}	0.24A	
No-load release voltage	V_s	AC100Vrms	Lamp load $V_{in}=12V$, $V_R=0\Omega$
Tube current	I_L	5.0mA	
Oscillation frequency	f	65kHz	
Chipping frequency	f_{ch}	60kHz	

Table 4-38

The following circuit is used for intensity adjustment.



(3) Connector pin layout

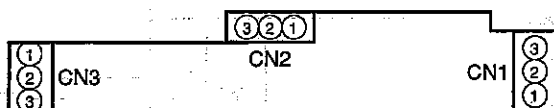


Fig. 4-15
PWB top view

(a) CN1 pin configuration

Pin No.	Signal name	Symbol
①	GND.	GND.
②	N.C	
③	OUT	OUT

(b) CN2 pin configuration

Pin No.	Signal name	Symbol
①	+B supply	+B
②	N.C	
③	GND.	GND.

(c) CN3 pin configuration

Pin No.	Signal name	Symbol
①	Intensity control VR	VR
②	GND.	GND.
③	Control	CONT

4-6-3. Circuit diagram

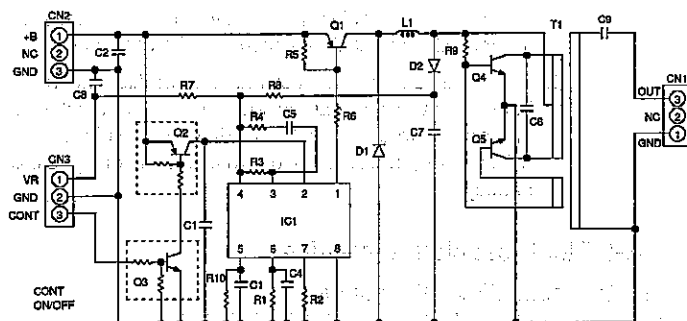


Fig. 4-16

CHAPTER 5. HDD

5-1. CP2024 (20MB HDD)

5-1-1. Introduction

The CP2024 is a high performance 2.5 inch low-profile (.69") 21.4 megabyte (formatted) disk drive with 23 ms average seek time (max) which is designed to operate on an IBM PC/XT & PC/AT or equivalent computer. The drive features a low 5V power requirement and high shock resistance, enabling battery operation in portable environments.

5-1-2. Key Features

- 2.5" Form factor
- Single 5 Volt supply
- Low power requirements
- 6.0 oz unit weight
- High performance rotary voice coil actuator with embedded servo system
- Single connector for power & interface
- Two of seven run length limited code
- High shock resistance.
- Sealed HDA with internal air filtration system
- Automatic actuator latch against inner stop upon power down
- Microprocessor-controlled diagnostic routines that are automatically executed at started-up
- Automatic error correction and retries.
- Block size 512 bytes
- PC XT/AT interface
- 1:1 Interleave
- 8K Buffer with Look-Ahead Read Capability
- Master/Slave option

5-1-3. Specification Summary

5-1-3-1. Capacity

Formatted Mbytes	21.4 Mbytes
------------------	-------------

5-1-3-2. Physical Configuration^{*1}

Actuator type	Rotary Voice-Coil
Number of Disks	1
Data Surfaces	2
Data Heads	2
Servo	Embedded
Tracks per Surface	654(zero to 653) user
Track Density(TPI)	1700TPI
Formatted Track Capacity(Bytes)	16,384 user
Bytes per Block	512
Blocks per Drive	41,856 user
Sectors per Track:	
physical	33
user	32

^{*1} The CP2024 defaults to a translate mode of 615 cylinders, 4 heads, and 17 sectors on power up.

5-1-3-3. Performance

Seek Times ^{*1}	Track to Track: 5.0 ms Average: 23 ms(max) ^{*2} Maximum: 40.0 ms
Average Latency	8.7 ms
Rotation Speed(+0.1%)	3433 RPM
Controller Overhead	1.0 ms
Data Transfer Rate (To/From Media)	1.25 MByte/second
Data Transfer Rate (To/From Buffer)	3.75 MByte/second
(0 RPM - Ready)	Typical: 7 seconds Maximum: 15 seconds ^{*3}
Stop Time (Power Down)	Typical: 3 seconds Maximum: 10 seconds
Start/Stop Cycles	40,000 min.
Interleave	1:1
Buffer Size	8K

^{*1} The timing is measured through the interface with the drive operating at nominal DC input voltages. The timing also assumes that:

- I/O driver overhead and system hardware dependency have been subtracted from timing measurements.

^{*2} The average seek time is determined by averaging the seek time for a minimum of 1000 seeks of random length over the surface of the disk

^{*3} Host system must allow a minimum of 60 seconds for drive electronic to facilitate retries for the READY line to become active. One retry is equal to 25 seconds.

5-1-3-4. Read/Write

Interface	XT/AT
Recording Method	2 of 7 RLL code
Recording Density(ID)	34K bits per inch
Flux Density(ID)	22.6K flux reversals per inch

5-1-3-5. Power Requirements (Typical)

	±5V (logic) ±5%	±5V motor ±10%	POWER
Read/Write/ Seek Mode	500 ma	100 ma	3.0 W
Idle Mode	200 ma	100 ma	1.5 W
Standby Mode	90 ma	0 ma	.45 W
Sleep Mode	50 ma	0 ma	.25 W
Spin-Up Mode	110 ma max	750 ma (3 seconds)	n/a

Read/Write/Seek Mode: occurs when data is being read from or written to the disk, or when the actuator mechanism is in motion.

Idle Mode occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.

Standby Mode occurs when the motor is stopped and actuator is parked. STANDBY MODE will occur after a programmable time-out since last host access occurs. The drive will leave STANDBY MODE upon receipt of a command which requires disk access or upon receipt of a spin up command.

Sleep Mode occurs when all electronics are disabled. Requires Host to reset to exit the SLEEP MODE.

Spin-Up Mode: occurs while the spindle motor is accelerating from its rest state to its operational speed. During the typical spin-up cycle, current on the 5 volt motor line may reach up to 900 mA for up to 500 microseconds. The specified current is the averaged value over the spin-up cycle.

Maximum noise allowed (DC to 1 MHz, with equivalent resistive load): +5V DC:2%

5-1-3-6. Physical Characteristics

Outline Dimensions $\pm .010"$	.69" x 2.75" x 4.00"
Weight	6.0 ounces

5-1-4. Environmental Characteristics

5-1-4-1. Temperature

Operating	5°C to 55°C
Non-operating	-40° to 60°C
Thermal Gradient	20°C per hour maximum

5-1-4-2. Humidity

Operating	8% to 80% non-condensing
Non-operating	8% to 80% non-condensing
Maximum Wet Bulb	26°C

5-1-4-3. Altitude (relative to sea level)

Operating	-200 to 10,000 feet
Non-operating (maximum)	40,000 feet

5-1-4-4. Reliability and Maintenance

MTBF	50,000 hours (POH)*1
MTTR	10 minutes typical
Preventive Maintenance	None
Component Design Life	5 years
Data Reliability	<1 non-recoverable error in 10^{12} bits read

*1population is minimum of 100 units

5-1-4-5. Shock and Vibration

Shock	1/2 sine pulse, 11 msec duration
Vibration	Swept sine, 1 octave per minute (measured without shock isolation)
Non-operating shock	100 G's (without non-recoverable errors)
Non-operating vibration	
5-31 Hz	.1 inch double amplitude
32-500 Hz	5 G's
Operating Shock	10 G's (without non-recoverable errors)
Operating Vibration	
5-10 Hz	.1 inch double amplitude
11-500Hz	.5G's (without non-recoverable errors or throughout degradation)

5-1-4-6. Magnetic Field

The disk drive will meet its specified performance while operating in the presence of an externally produced magnetic field under the following conditions:

Frequency	Field Intensity
0 to 700Khz	6 gauss maximum
700 KHz to 1.5 Mhz	1 gauss maximum

5-1-4-7 Acoustic Noise

The sound pressure level will not exceed 40 dBA at a distance of 1 meter from the drive.

5-1-5. Customer Options

PC XT/AT Interface

The CP2024 are designed to operate in either XT or AT interface single drive mode. On power up, the state of interface pin 44 (-XT/AT) is sampled and appropriate mode of operation is selected. An LED drive signal is provided via the interface

Master/Slave (AT only)

The CP2024 is designed to operate either as a master (C drive) or a slave (D drive) depending on the state of Jumper E2. The master/slave is not supported in XT mode. The drive will be configured as a master or single drive when its shipped. On power up, the state of jumper E2 is sampled and the appropriate role (master/slave) is selected. When jumper E2 is closed, the drive will assume the role of master. When jumper E2 is open, the drive will act on the slave. In single drive configurations, jumper E2 must be closed. For location of jumper E2, see outline drawing (Figure 5-1).

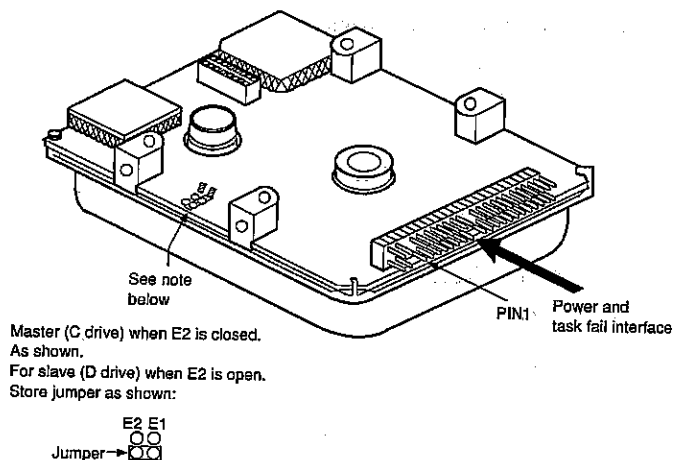


Figure 5-1. Customer Options

5-1-6. Interface Connector

The CP2024 has a 44 pin right angle interface/power connector mounted on the PCB. The recommended mating connector is DuPont Part Number: 69764-044 or equivalent. The maximum cable length is two feet.

5-1-6-1. Diagnostic Routines

The microprocessor performs diagnostics upon application of power. If an error is detected, the CP2024 will not come ready.

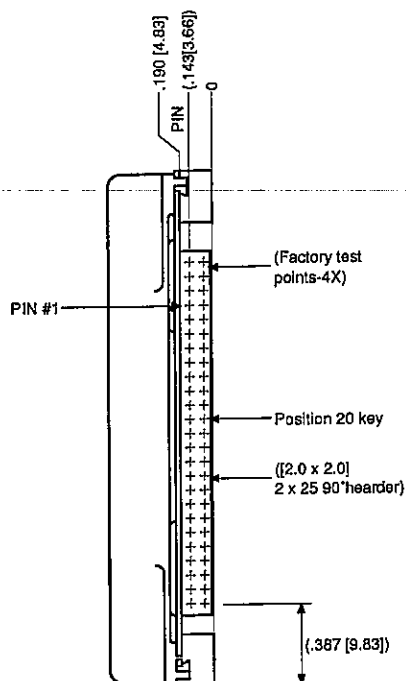


Figure 5-2. Connector

5-1-7. Electrical Description

5-1-7-1. Signal Levels

All signal levels are TTL compatible. A logic "1" is > 2.0 Volts. A logic "0" is from 0.00 Volts to .70 Volts. the drive capability of each of the inbound signals is described below.

5-1-7-2. Pin Descriptions

PIN	SIGNAL	PIN	SIGNAL
01	-HOST RESET	02	GND
03	+HOST DATA7	04	+HOST DATA8
05	+HOST DATA6	06	+HOST DATA9
07	+HOST DATA5	08	+HOST DATA10
09	+HOST DATA4	10	+HOST DATA11
11	+HOST DATA3	12	+HOST DATA12
13	+HOST DATA2	14	+HOST DATA13
15	+HOST DATA1	16	+HOST DATA14
17	+HOST DATA0	18	+HOST DATA15
19	GND	20	KEY
21	RESERVED	22	GND
23	-HOST IOW	24	GND
25	-HOST IOR	26	GND
27	RESERVED	28	+HOST ALE
29	RESERVED	30	GND
31	+HOST IRQ14	32	-HOST IO16
33	+HOST ADDR1	34	-HOST PDIAG
35	+HOST ADDR0	36	+HOST ADDR2
37	-HOST CS0	38	-HOST CS1
39	-HOST SLV/ACT	40	GND

Signal Name	Dir	Pin	Description
-RESET	0	1	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND		02, 19, 22, 24, 26, 30, 40, 43	Ground between the drive and the Host.
+DATA 0-15	I/O	3-18	16 bit bi-directional data bus between the host and the drive. In AT mode, the lower 8 bits, HD0-HD7, are used for register & ECC access. All 16 bits are used for data transfers. In XT mode, only the lower 8 bits are used. These are tristate lines with 10mA drive capability.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
RESERVED	0	21, 22	Reserved
-IOW	0	23	Write strobe, the rising edge of which clocks data from the host data bus into a register or the data register of the drive.
-IOR	0	25	Read strobe, which when low enables data from a register or the data register of the drive onto the host data bus. The rising edge of IOR latches data from the drive at the host.
-DACK	0	27	DMA hand shake signal used to select drive data register(XT only)
+DRQ	I	29	DMA hand shake signal used to request data byte transfer (XT only)
+IRQ	I	31	Interrupt to the Host system. In AT mode this signal is enabled only when the drive is selected, and the host activates the -IEN bit in the Digital Output Register. When the -IEN bit is inactive, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. In XT mode, this signal is enabled when the IRQ enable bit is set and the drive has completion status available for the host. This signal is a tristate line with 10 mA drive capacity.
-IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 mA drive capacity. (AT mode only).
-PDIAG	I	34	Passed diagnostic. This signal is ignored by the drive.
+A0, A1, A2	0	35, 33, 36	Bit binary coded address used to select the individual registers in the drive.
-CS0	0	37	Chip select decoded from the host address bus. Used to select some of the Host accessible registers. NOTE: This signal should be disabled by the Host when data transfers are in progress.
-CS1	0	38	Chip select decoded from the Host address bus. Used to select three of the registers in the Task File. AT mode only.
-ACTIVE	I	39	Signal from the drive used to drive an active LED whenever the disk is being accessed.
+5V (Logic)	0	41	5 volt +/-5% supply to drive circuitry.
+5V (Motor)	0	42	5 volt +/-5% supply to drive motors.
-XT/AT	0	44	Interface mode select. This signal is sampled on power up and will select XT or AT operating mode as requested by the Host.

5-2. MK1122FC (40MB HDD)

- Reduced power consumption by Power Control command

5-2-1. GENERAL DESCRIPTION

The MK1022FC/MK1122FC comprises a series of intelligent disk drives, hereinafter referred to as the MK1022FC/MK1122FC or simply as the drive.

The drive features an IBM PC-AT® embedded controller that requires a simplified adapter board for interfacing to an AT or AT compatible bus. The drives employ Winchester technology and a closed loop servo control system to realize recording density of more than 100Mbit/inch² and average access time of 23 mS with highest reliability.

It features smallest and lightest drive with 17mm height half space of market standard 3.5" micro FDD and 180gram of weight.

The MK1022FC/MK1122FC consists of an HDA (Head Disk Assembly) and a printed circuit board. The HDA is a sealed module and contains a disk spindle assembly, a head actuator assembly and an air filtration system. Reliability is enhanced through the use of Winchester technology. The actuator is a rotary voice coil motor and provides high-speed access.

The disk is driven directly by a DC spindle motor. Air filtration is provided by means of a high performance air filtration system using both breather and circulation filters.

The drive provides a carriage lock mechanism which activates automatically on power down, thus preventing head/media damage during non-operating or transportation conditions.

The printed circuit board is located externally to the HDA and contains all the electronic circuitry necessary to operate the drive except the head drivers. This board contains the power supply and interface signal connectors. Only the head control IC's are located within the HDA. The circuitry performs the following functions:

Read/Write, Task File Control, Spindle Motor Control, Seek and Head Positioning Servo Control and Abnormal Condition Detection.

5-2-2. KEY FEATURES

* High capacity in smallest size

- Single platter of world smallest 2.5" accommodating formatted capacity of 40MB.
- Slim (17mm height) and light (180gram weigh) design

* Fast access and fast transfer

- Quick spin up of Spindle Motor - 3 S
- 23 msec average access time realized by optimized balance and effective magnet of Rotary VCM
- Bus transfer rate up to 5.0 megabytes/second and disk transfer 12Mbit/second (40MB model)
- Read ahead cache improved system throughput

* Intelligent Interface

- Emulation of IBM PC AT Task File and all AT commands plus additional commands.
- Any drive configuration is applicable by translation mode
- Quick address conversion in translation mode

* Data integrity

- Automatic retry and corrections for read errors.
- 56 bit computer generated ECC polynomial with 11 bit burst error correction capability.
- Defect free product by defect alternation during format

* High reliability

- Powerful self-diagnostic capability.
- Fail-safe power down return heads to landing zone with automatic carriage lock realized high immunity to shock.

* Low power consumption

5-2-3. BASIC SPECIFICATION

	MK1122FC
Capacity (Megabytes)	
Formatted	43.0
Actuator type	Rotary Voice Coil Motor
Servo method	Sector Servo
Format	Hard Sector
Number of disks	1
Number of data heads	2
Number of user data cylinder	977
Track capacity (formatted)	22,016
Bytes per sector	512
Number of sectors per track	44
Number of sectors per track	43
Number of sectors per unit	84,022
Recording method	1-7 RLL
Recording density	
TPI	2,000
BPI	51,891
FRPI	38,918

5-2-4. PERFORMANCE

Access time (msec)*1	
Track to track seek*2	5
Average seek*3	23
Max. seek	40
Rotation speed (RPM)	3,200 ± 1%
Average Latency Time (msec)	9.4
Internal Transfer rate (M bits/sec)	12
Host Transfer rate	5.0 Mbyte/sec
Sector Interleave	1:1
Track skew	yes
Buffer size	32kByte
Cache	Read Ahead Cache
Start time	
upto Drive Ready	3 sec. (TYP.), 15 sec. (MAX.)
Stop time (when power switched off)	4 sec. (TYP.), 8 sec. (MAX.)
Recovery time from S stand-by	3 sec. (TYP.)

(*1) Under the condition of normal voltage, 25°C normal temperature and of placing bottom side down

(*2) Average time to seek to all possible adjacent track without head switching

(*3) Average time to travel between all possible combination of track

5-2-5. POWER REQUIREMENTS

5-2-5-1. Supply voltage

(1) Supply for Logic

Allowable voltage range	5V $\pm$ 5%
Allowable noise/ripple	100mvp-p or less
Current	
Starting	200 mA
Seeking	220 mA
Reading/Writing	230 mA
Idle	210 mA
Stand-by	60 mA
Sleep	42 mA

(2) Supply for Motor

Allowable voltage range	5V $\pm$ 5%
Allowable noise/ripple	100mvp-p or less
Current	
Starting	500 mA
Seeking	100 mA
Reading/Writing	90 mA
Idle	75 mA
Stand-by	3m A
Sleep	3m A

5-2-5-2. Power consumption

	Average (note 3)	Max (note 4)
Starting	3.5 W	4.5 W
Reading/Writing	1.6 W	1.8 W
Seeking	1.6 W	1.8 W
Idle (note 1)	1.4 W	1.6 W
Stand-by (note 2)	0.3 W	0.4 W
Sleep	0.2 W	0.3 W

(note 1) Motor is rotating in normal speed but none of Reading, Writing or Seeking is executed.

(note 2) Motor is not rotating and head is parking on CSS (Contact Start Stop) zone.

(note 3) Under nominal condition (25°C, 1,013mb) and 5V $\pm$ 0%

(note 4) 5V $\pm$ 5%

5-2-5-3. Power Sequence

If the 5V Logic is separated from 5V Motor, both line should be turned on and off within a second longest.

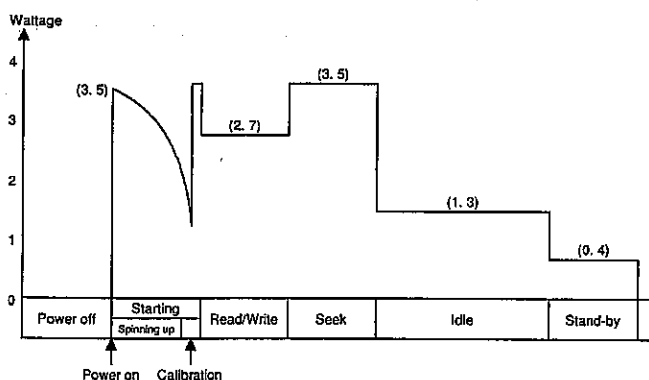


Fig. 6.1 Power Consumption Profile

5-2-6. Mechanical Specification

5-2-6-1. Dimension

Width : 2.76" (70.0 mm)

Height : 0.67" (17.0 mm)

Depth : 3.94" (100.0 mm)

tolerance: ± 0.4 mm

Fig. 7.1 shows an outline of the drive.

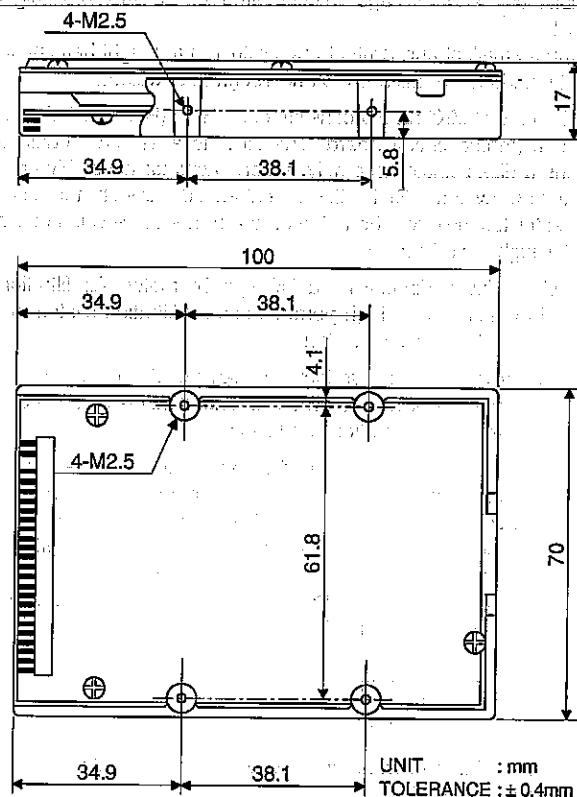


Fig. 7.1 MK1022FC/MK1122FC Dimensions (Metric screw)

5-2-7. Pin Assignment

The following table describes all of the pins on the Task File Interface. Header on control PC board has 4 option pins next to Pin 1 as shown in Fig. 10.1.

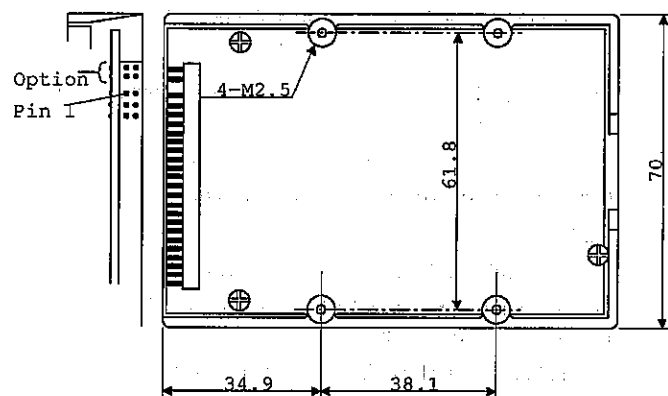


Fig. 10.1. Pin position

PIN NO.	SIGNALS	PIN NO.	SIGNALS
1	–HOST RESET	2	GROUND
3	HOST DATA 7	4	HOST DATA 8
5	HOST DATA 6	6	HOST DATA 9
7	HOST DATA 5	8	HOST DATA 10
9	HOST DATA 4	10	HOST DATA 11
11	HOST DATA 3	12	HOST DATA 12
13	HOST DATA 2	14	HOST DATA 13
15	HOST DATA 1	16	HOST DATA 14
17	HOST DATA 0	18	HOST DATA 15
19	GROUND	20	KEY
21	RESERVED	22	GROUND
23	–HOST IOW	24	GROUND
25	–HOST IOR	26	GROUND
27	RESERVED	28	HOST ALE
29	RESERVED	30	GROUND
31	HOST IRQ14	32	–HOST IO16
33	HOST ADDR 1	34	–HOST PDIAG
35	HOST ADDR 0	36	HOST ADDR 2
37	–HOST CS0	38	–HOST CS1
39	–HOST SLV/ACT	40	GROUND
41	+5V (LOGIC)	42	+5V (MOTOR)
43	GROUND	44	RESERVED

5-2-8. SIGNAL

SIGNAL NAME	DIR	PIN	DESCRIPTION
–HOST RESET	O	1	Reset signal from host system; active low during system power-up or detection of voltage fault.
GROUND		2, 19 22, 24 26, 30 40, 43	Ground between the drive and the host system.
+HOST DATA 0-15	I/O	3-18	16 bit bi-directional data bus between the host system and the drive. The lower 8 bits, HD0-HD7, are used for register and ECC access. All 16 bits are used for data transfers.
KEY	N/C	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
–HOST IOW	O	23	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data register of the drive.
–HOST IOR	O	25	Read strobe, low state enables data from a register or the data of the drive onto the host data bus, HD0 through HD15. The rising edge of –HOST IOR latches data from the drive at the host system.
–HOST IRQ14	I	31	Interrupt to the host system, enabled only when the drive is selected and the host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive high, or the drive is not selected, this output is in a high impedance state, regardless to the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero when host reads the Status register or a write to the command register.
RESERVED		21, 27 28, 29 44	Reserved for future use. no connection
+HOST IO16	I	32	Indication to the host system that the 16bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word (open drain).
+HOST ADDR 1	O	33	Address line from the host system to select the registers of the drive.
–HOST PDIAG	I/O	34	In Master/Slave mode, reporting the presence of slave drive to master drive and passing diagnostic result between master drive and slave drive.
+HOST ADDR 0	O	35	Address line from the host system to select the registers of the drive.
+HOST ADDR 2	O	36	Address line from the host system to select the registers of the drive.
–HOST CS0	O	37	Chip select decoded from the host address bus. Used to select one of two groups of host accessible registers.
–HOST CS1	O	38	Chip select decoded from the host address bus. Used to select another group of host accessible registers.
–HOST SLV/ACT	I	39	Signal from the drive used either: – to drive an external LED whenever the drive is being accessed – or reporting of slave drive presence to master drive when it is configured as master/slave
+5V (LOGIC)		41	power line for logic and analog circuit
+5V (MOTOR)		42	power line for the driving of motor

'I' is from the drive to the host system, 'O' is from the host system to the drive, and I/O is bidirectional.

5-3. PRAIRIETEK MODEL 242 (40MB HDD)

1.0 Introduction

The PrairieTek Model 242 is a 2.5 inch ruggedized high performance disk drive optimized for an IBM PC-AT or XT compatible laptop or portable computer. The Model 242 contains an on-board controller with selectable interface that requires a simplified adapter board for interfacing to an AT or XT compatible bus.

1.2 Key Features

- Unique ramp loading mechanism for loading and unloading the disk heads during power-downs and periods of inactivity.
- User invoked low power modes and power-downs for power sensitive applications.
- High performance rotary voice coil actuator with embedded servo system.
- On-board controller for direct connection to a 44-pin interface.
- Microprocessor - controlled diagnostic routines that are automatically performed at power-up.
- Internal air filtration and dessicant system.
- Automatic error detection and correction.

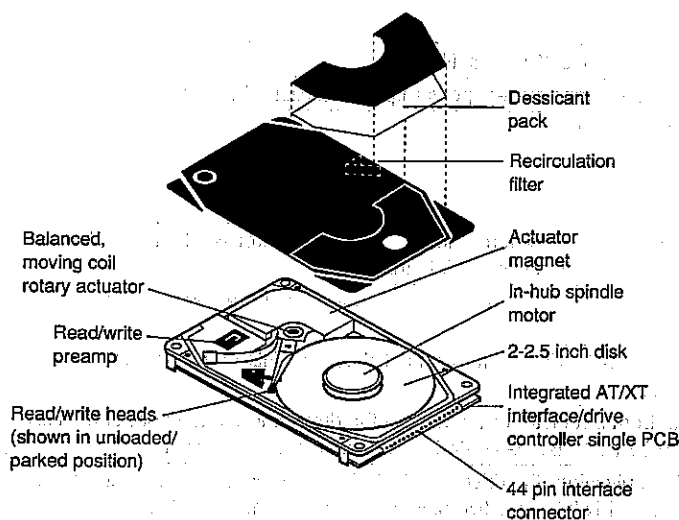


Figure 1: PrairieTek Model 242

2.0 Specification Summary

2.1 Capacity

Formatted	42.8 MBytes
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2.2 Configuration

Actuator Type	Rotary Moving Coil
Number of Disks	2
Data Surfaces	4
Data Heads	4
Servo System	Embedded
Tracks per Surface	615
Track Capacity	17,408 bytes
Bytes per Block	512
Blocks per Track	34
Blocks per Drive	83,640

2.3 Performance

Seek Times	
Track to Track	8ms
Average	23ms
Maximum	45ms
Average Latency	9.1ms
Rotation Speed	3,307 RPM
Controller Overhead	1ms
Data Transfer Rates	
To/From the Buffer	
Burst (max)	5.50MB/sec
Sustained	4.25MB/sec
To/From the Media	1.25MB/sec
Start Time	2 sec (typical)
Stop Time	NA (refer to functional description)
Interleave	Programmable

2.4 Read/Write

Interface	AT or XT 44 pin
Recording Method	2 of 7 RLL Code
Track Density	1,350 TPI
Recording Density (ID)	38,452 BPI
Flux Density (ID)	25,634 FCI

2.5 Power Requirements

Typical Power Dissipation	
Spin Up	3.50 watts
Ready	1.10 watts
Seeks	1.25 watts
R/W	2.50 watts
Power Save Mode	0.7 watts
Standby Mode	0.06 watts
DC Input	
+5 Volts $\pm 5\%$ D.C., 1 amp max.	
Maximum ripple allowed is 2% with equivalent resistive load	

2.6 Physical Characteristics

Outline Dimension	0.75" x 2.75" x 4.00" (19.0mm x 69.9mm x 101.6mm)
Weight	7.94 ounces (225 grams)

2.7 Environmental Characteristics

Temperature	
Operating	5°C to 55°C
Non-Operating	-40°C to 70°C
Thermal Gradient	20°C/hour max
Humidity	
Operating	10% to 90% non-condensing
Non-Operating	10% to 90% non-condensing
Max Wet Bulb	30°C
Altitude (relative to sea level)	
Operating	≈ 1000 to 10,000 feet
Non-Operating (max.)	40,000 feet

2.8 Reliability and Maintenance

MTBF	100,000 POH
MTTR	5 minutes typical
Start/Stops	250,000
Preventive Maintenance	None
Component Design Life	5 years
Data Reliability	< 1 non-recoverable error in 10^{12} bits read

2.9 Shock and Vibration

Shock	(1/2 sine pulse, 11 ms duration)
Non-Operating	100 G
Operating	5 G
Vibration	(swept sine, 1 octave per minute, 10-400Hz)
Non-Operating	5 G peak to peak
Operating	1 G peak to peak
(without non-recoverable errors)	

2.10 Magnetic Field

An externally induced magnetic flux density may not exceed 10 gauss as measured at the external drive surface.

2.11 Acoustic Noise

Sound pressure level at 1 meter - 39 dBA. (Ready Mode)

2.12 Safety Standards

The Model 242 disk drive is designed to comply with relevant product safety standards such as:

- UL1950 Electronic Data Processing Units and Systems
- CSA C22.2 No. 154 Data Processing Equipment
- VDE 0804 Regulations for Telecommunications Apparatuses including Information Processing Equipment
- IEC 435 Safety Requirements for Data Processing Equipment

The following table describes all of the pins on the 44 Pin Interface Connector (J1) in AT Mode. AT Mode is designated by pin 44.

I/O PIN	SIGNAL	I/O PIN	SIGNAL
01	-HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	Not Used	22	GND
23	-HOST IOW	24	GND
25	-HOST IOR	26	GND
27	Not Used	28	Not Connected
29	Not Used	30	GND
31	+HOST IRQ	32	-HOST IO16
33	+HOST ADDR 1	34	-PDIAG
35	+HOST ADDR 0	36	+HOST ADDR 2
37	-HOST CS0	38	-HOST CSI
39	-ACTIVE/SLAVE PRESENT	40	GND
41	+5V Supply	42	+5V Supply
43	+5V Return	44	+AT/-XT

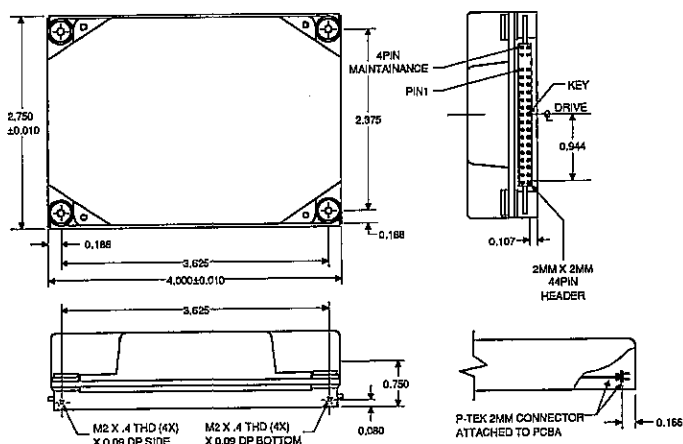


Figure 2A: 242 Mounting Specifications/Dimensions

SIGNAL NAME	DIR	PIN	DESCRIPTION
-HOST RESET	O	01	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	—	02	Ground between the drive and the Host.
+HOST DATA	I/O	03-18	16 bit bi-directional data bus between the Host and the drive. The lower 8 bits, HD0-HD7, are used for register & ECC byte access. All 16 bits are used for data transfers. These are tri-state lines with 24 ma drive capability.
GND	—	19	Ground between the drive and the Host.
KEY	—	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
Not Used	—	21	Not Used
GND	—	22	Ground between the drive and the Host.
-HOST IOW	O	23	Write strobe, the trailing edge of which clocks data from the Host data bus, HD0 through HD15, into a register or the Data register of the drive.
GND	—	24	Ground between the drive and the Host.
-HOST IOR	O	25	Read strobe, which when low enables data from a drive register onto the Host data bus, HD0 through HD15. The trailing edge of -HOST IOR latches data from the drive at the Host.
GND	—	26	Ground between the drive and the Host.
Not Used	—	27	Not used
Not Connected	—	28	Not connected
Not Used	—	29	Not used
GND	—	30	Ground between the drive and the Host.
+HOST IRQ	I	31	Interrupt to the Host system, enabled only when the drive is selected, and the Host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive high, or the drive is not selected, this output is in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by drive microcontroller. IRQ is reset to zero by a Host read of the Status register or a write to the Command register. This signal is a tri-state line with 24 ma drive capacity.
-HOST IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 ma drive capacity.
-PDIAG	I	34	Passed diagnostic. Output by the drive if it is the slave drive. Input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command.
+HOST A0, A1, A2	O	33, 35, 36	Three bit binary coded address lines used to select the individual registers in the task file.
+HOST CS0	O	37	Chip select decoded from the Host address bus. Used to select low-order Host accessible registers.
-HOST CS1	O	38	Chip select decoded from the Host address bus. Used to access the three high order registers in the Task File.
-ACTIVE/SLAVE PRESENT	I/O	39	Signal from the drive used to drive an active LED whenever the disk is being accessed. This signal is active low when the drive is busy and has a drive capability of 48 ma. In a two drive system, this signal is driven low by the Slave drive to indicate its presence to the Master drive.
GND	—	40	Ground between the drive and the Host.
+5V SUPPLY		41, 42	+5 Volt drive supply
+5V RETURN		43	+5 Volt P.S. ground
+AT / -XT		44	When connected to +5V or left open this signal will enable AT Mode.

Chapter 6. LCD (LM64N674)

6-1. Structure

Structure: The 640 x 480 full dot liquid display graphic display unit consists of an LCD panel, electronic component printed circuit board, and the film carrier LSI that electrically connected.

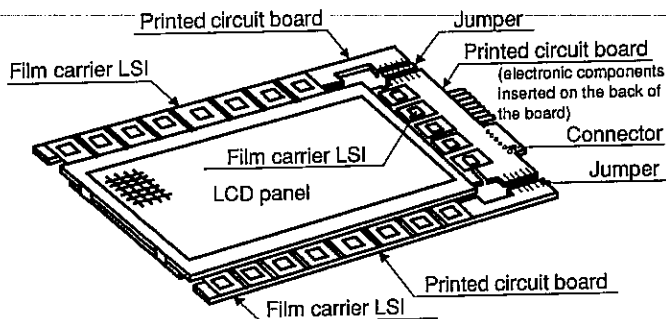


Fig. 6-1

6-2. BLOCK DIAGRAM

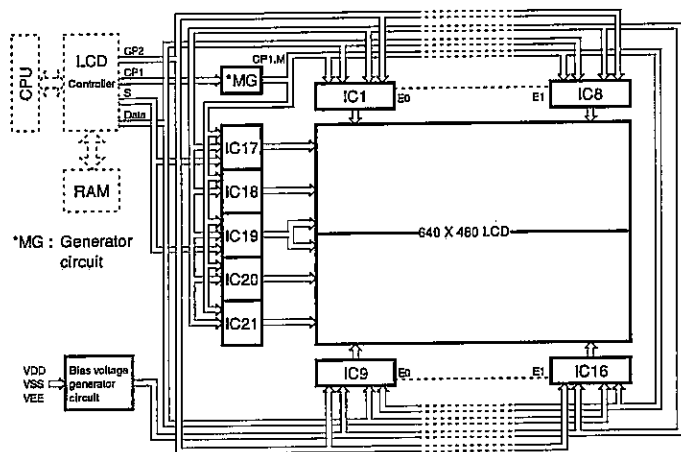


Fig. 6-2

6-3. Specification

Tbl. 6-1

Item	Characteristics	Unit
*1 Physical dimensions	244(W) x 195(H) x 7MAX(D)	mm
Effective display area	205(W) x 155(H)	mm
Display format	640(W) x 480(H) full dot	—
Dot size	0.28 x 0.28	mm
Dot space	0.03	mm
*2 Dot color	White *3	—
*2 Background color	Black	—
Weight	About 240	g

*1: The physical dimensions of the unit excludes the LCD sealed portion.

*2: The color of the LCD panel may vary according to the environmental temperature due to the characteristic of the LCD panel.

*3: Data "H" → ON=white When the RV line is established when the RV line is connected to the VDD line.
Data "L" → OFF=black is open.

6-4. Absolute maximum rating

(1) Absolute electrical maximum rating

Tbl. 6-2

Item	Symbol	Minimum	Maximum	Unit	Note
For logic circuit	$V_{DD} - V_{SS}$	0	6.0	V	$T_a = 25^\circ\text{C}$
For liquid crystal drive circuit	$V_{DD} - V_{EE}$	0	33.0	V	$T_a = 25^\circ\text{C}$
Input voltage	V_{IN}	0	V_{DD}	V	$T_a = 25^\circ\text{C}$
For liquid crystal drive	$V_{DD} - V_O$	0	28.0	V	$T_a = 25^\circ\text{C}$

(2) Environmental requirements

Tbl. 6-3

Item	Storage		Operating		Note
	Minimum	Maximum	Minimum	Maximum	
Temperature	-25°C	$+60^\circ\text{C}$	0°C	$+45^\circ\text{C}$	
Humidity	NOTE(1)		NOTE(1)		Free of moisture condensation

NOTE(1): $T_a \leq 40^\circ\text{C}$... 95%RH, max.
 $T_a > 40^\circ\text{C}$... Absolute humidity must be 59%RH with $T_a = 40^\circ\text{C}$.

6-4. Electrical characteristics

(OPTIONAL) CO. 100101

(1)

Tbl. 6-4

 $T_a = 25^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$

Item	Symbol	Condition	Minimum	Maximum	Unit	Note
For logic circuit supply voltage	$V_{DD} - V_{SS}$		4.75	5.0	5.25	V
For liquid crystal drive circuit supply voltage	$V_{DD} - V_{EE}$		TBD	TBD	TBD	V
Liquid crystal drive voltage	$V_{DD} - V_O$	(NOTE)	18.0	21.2	25.7	V
Input voltage	V_{IN}	High level	$0.8V_{DD}$	—	V_{DD}	V
		Low level	0	—	$0.2V_{DD}$	V
Input leak current	I_{IL}	High level	—	—	25	μA
		Low level	-25	—	—	μA
For logic circuit supply current	I_{DD}	$V_{DD}=5V$, $V_{DD}-V_O=F=75\text{Hz}$ 21.2V High frequency pattern	—	25	35	mA
For liquid crystal circuit supply current	I_{EE}		—	15	25	mA
Power consumption	P_d		—	600	900	mW

NOTE: The view angle (θ) of a maximum contrast may be obtained by changing the liquid crystal drive voltage ($V_{DD}-V_O$).
 Maximum and minimum limits of the rating show the maximum and minimum voltages at the operating temperature range ($0^\circ\text{C}-45^\circ\text{C}$).
 "Standard" shows the nominal voltage.

(2) Input capacity

Tbl. 6-5

Signal name	Input capacity
S	40pF TYP
CP1	250pF TYP
CP2	200pF TYP
UDO~UD3	200pF TYP
LDO~LD3	200pF TYP

(3) Interfacing signals

[1] Connector 1 (IL-Y-15P-S15L2-EF)

Pin No.*	Symbol	Function	Active signal level
1	S	Scan start	"H"
2	CP1	Input data latch	H→L
3	CP2	Data input lock	H→L
4	BLoff	Backlight control	Connected with the pin-2 of connector 2
5	V_{DD}	Logic circuit power supply (+5V)	—
6	V_{SS}	Ground potential	—
7	V_{EE}	Liquid crystal drive power supply (—)	—
8	DUO	Display data (upper half)	H(ON), L(OFF)
9	DU1	"	"
10	DU2	"	"
11	DU3	"	"
12	LD0	Display data (lower half)	H(ON), L(OFF)
13	LD1	"	"
14	LD2	"	"
15	LD3	"	"

Tbl. 6-6

[2] Connector 2 (IL-Y-5P-S15L2-EF)

Pin No.*	Symbol	Function	Active signal level
1	RV	Logic reverse control signal	Open or shorted with VDD
2	BLoff	Backlight control	Connected with the pin-4 of connector 1
3	VDD	+5V	Must be connected with the contrast calibration circuit.
4	V ₀	Liquid crystal drive voltage	
5	VEE	Liquid crystal supply voltage (-)	

Tbl. 6-7

6-5. Driving method**1) Circuit configuration**

Fig.6-2 shows the block diagram of the circuit configuration.

2) Display configuration

To obtain high contrast display by decreasing the duty, the area of 640 x 480 dots display is divided into two sectors, each sector (640 x 240 dots) is driven by 1/240 duty.

3) Input data and control signals

The LCD driver is 80-bit LSI that consists of latch circuit and LCD drive circuit.

A 4-bit parallel data is supplied to one line (640 dots) of both display sectors at a time, starting from the upper left corner of the display, via the shift register with the clock pulse CP2.

Upon receiving one line input data (640 dots), 640 signals are latched as parallel data at a high to low transition of the latch signal CP1 to supply dot drive signals corresponding to 640 electrodes of the LCD panel.

Since the scan start signal S sent to the scan signal drive circuit has been transferred to the first line of the scan electrode, the contents of the data signals are displayed on the first line of the display screen by a combination of the LCD scan electrode and the voltage added to signal electrode.

While the first line display data are being displayed, the second line data are received. Upon transferring the 640 dots data and latched at a high to low transition of CP1, the second line data are now displayed.

When data transfer is repeated down to the 240th line in this manner using the multiplex mode from the upper to lower lines, a single cycle of a full data display (1 frame) is completed, then again starts to accept the data from the first line. The scan start signal S is a horizontal electrode drive signals.

To avoid display flicker for this model, the operation with the frequency shown in the table next is recommended.

If a DC voltage was added to the LCD panel, a chemical reaction takes place in the liquid crystal of the LCD panel which may result in LCD fatigue. The driving waveform must be reversed in a certain cycle to avoid the generation of such a DC voltage. This is performed by the async M signal circuit which converts the driving waveform into AC signal M.

Source frequency	50	60	50/60
Operating frequency	50±1	60±1	72±1

(Unit: Hz)

On account of the characteristics of the CMOS driver LSI, the power consumption of the unit increases proportionate to the increase of the CP2 clock frequency. Therefore, to decrease the CP2 clock data transfer speed, the driver LSI incorporates the system to 4 bits transfer parallel data through 4 shift registers. Use of this LSI abates the power consumption of the unit.

For this circuit configuration, a 4-bit display data are supplied from data input lines of UD0~3 for the upper half and DL0~3 for the lower half.

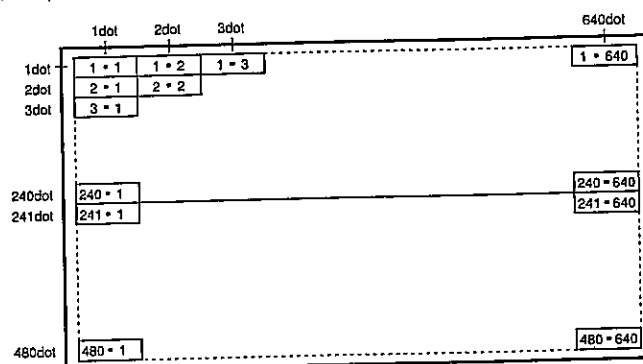
Aside from this, a data input bus line system is adopted for less power consumption. With this system, data inputs from LSI function only when appropriate data are sent.

The following shows the a full screen signal electrode data inputs and the driver LSI chip select functions.

First, when the driver LSI at the left is selected to send 80-dot data (20CP2), the right side driver close to it is selected. This action continues until the data have been sent to the driver LSI at the right. This process takes place at the same time with the signal electrode drive LSI for both screen sectors.

In this manner, data for both screen sectors are supplied through the 4-bit bus line one at a time.

Because this graphic display unit does not have the internal refresh RAM, it is necessary to supply the data and its timing pulse.



NOTE: 1.2 "1" represent the first vertical dot and "2" the second horizontal dot.

Fig. 6-5 Dot chart of Display Area

CHAPTER 7. POWER SUPPLY UNIT

7-1. Technical characteristics

1) Inputs

i) AC adaptor input

Rated voltage: 15.3V

Working voltage range: 14.24~16.5V

ii) Battery input

Rated voltage: 9.6V

Working voltage range: 8.0~12.8V

2) Outputs

i) Output

Circuit name	5V Vcc	5V VBu1	5V VBu2	-24V VLCD	*1 VBT
Rated load	2.12A	*2 0.1A	*3 0.01A	0.022A	2.7W

*1: VBT is an input voltage through circuit.

*2: VBu1 is battery backed up.
If Vcc is not, the load current is 0.01A.

*3: VBu2 is battery backed up.

ii) Recharge output

There are two modes of recharge; quick recharge and trickle recharge, which gets in action when the power is off to the personal computer.

Mode	Quick recharge	Trickle recharge
Charge current	1.32A	0.11A
Charge time	2 Hr	Continuous

7-2. Operational description

This DC/DC converter consists of two boards; one of which is the control PWB and the other is power supply PWB.

2-1) Input filter

Fig.7-1 shows the input filter.

It is a high pass type filter that consists of C1, C2, and L1. Noise on the input line, radio interference from within the converter, and conduction noise are suppressed in this circuitry.

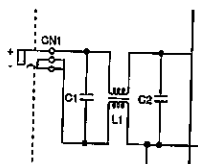


Fig. 7-1

2-3) 5V, VCC circuit

Fig.7-2 shows the 5V, VCC circuit.

8~16.5VDC supplied from the AC adaptor or the battery is dropped to 5V in TR4 to supply the regulated 5V. The transistor TR4 is switched at 110KHz using the control signal from IC1 of the control PWB to convert the DC input into high frequency square waveform, then rectified and smoothed by D2, L3, and C10.

To regulate the output voltage, a fluctuation in the supply line is detected and divided by means of the resistors R1, R2, and VR1 within the control PWB which is then sent to the comparator input in IC1 where the ON-width of TR4 is controlled by the drive signal that error amplified by the error amp within IC1.

On and off of Vcc is controlled by CPU (IC5).

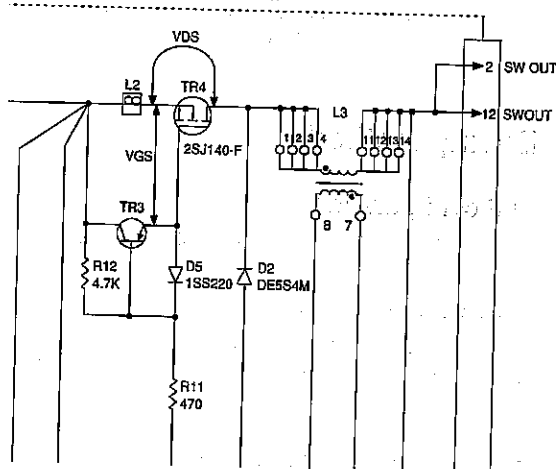


Fig. 7-2

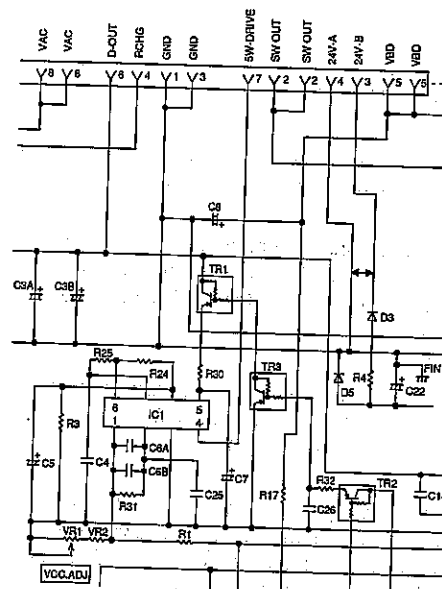


Fig. 7-3

2-3) 5V, VBU1 circuit

Fig.7-4 shows the 5V, VBU1 circuit.

For VBU1, the VCC output and the 3-pin regular IC2 outputs are OR-ed by the diode using DS1. If VCC was present, the VCC voltage is sent out straight. If not, output is obtained from IC3.

It has relationship of IC3 output < Vcc.

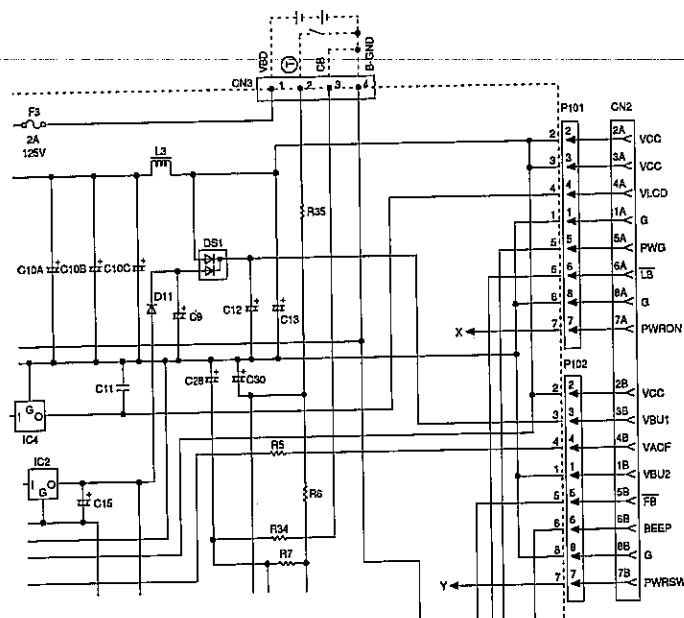


Fig. 7-4

2-4) -24V, VLCD circuit

Fig.7-2, 7-3 and 7-4 shows the -24V, VLCD circuit.

Current flowing in the ON period of TR4 of the Vcc circuits charged in the primary circuit coil and released from the secondary circuit coil during the off period, to supply energy to the load.

A square waveform generated in the secondary side coil L3 is rectified and smoothed by D3 and C22 to obtain the DC current of about 40V. This then dropped to -24V by the 3-pin regulator IC4 to be used as the LCD power supply.

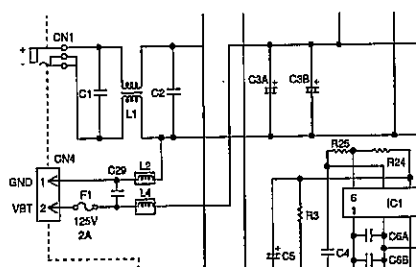


Fig. 7-5

2-5) VBT circuit

Fig.7-5 shows the VBT circuit.

VBT is an input through circuit from which derived the voltage same as the DC input. F1 is a short circuit protect fuse.

2-6) Recharge circuit

There are two types of the recharge circuits; the quick recharge circuit that operates when the switch is off and the trickle recharge circuit which the current flows at all times during the time the AC adaptor is used. Fig. 7-6 shows the power switch circuit.

i) Quick recharge circuit

With the IC1 drive signal within the power supply PWB is switched at about 50KHz using TR1 which is then rectified and smoothed by D4, L1, and C3 to recharge the battery.

Recharge of the battery is entirely controlled by IC5 within the control PWB.

IC5 is a 4-bit microcomputer that not only controls battery recharge but handles signal transfer with the main unit.

ii) When AC input is added to the AC adaptor, the current is kept supplied to the battery via R9.

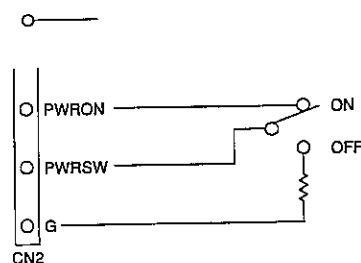


Fig. 7-6

CHAPTER 8. KEYBOARD

8-1. Input/output data

1) Start/stop, half-duplex transfer mode for the clock and data lines.

2) Transfer format

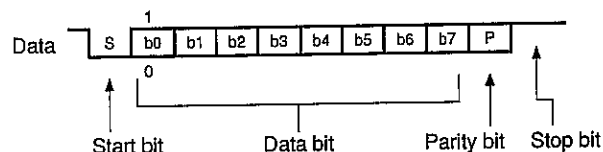


Fig. 8-1

3) Transmit rate

For both send and receive, it depends on the clock signal sent from the keyboard which will be 14300bps.

4) Output

The output (data, clock) is directly connected with the 80C52 controller.

8-2. Data send/receive control

Prior to sending and receiving of data on the keyboard, the clock and data lines are checked of their conditions.

Clock	Data	
1	1	Keyboard data ready to send
1	0	Keyboard data receive request
0	0 or 1	Send/receive disabled
0 ... Low	1 ... High	

NOTE: After completion of the keyboard data, "1" is sent onto the clock and data signal lines.

1) Keyboard data output (KB→Host)

If there is data in the keyboard internal buffer with a high state of clock and data, these signals are driven in the timing shown separately to send the data. In case the clock signal is at a low (0) with "1" sent on the clock line, that is, the clock (0) is sent by the host, the clock and data signals are fixed to "1" and the data output is interrupted.

2) Keyboard input (Host→KB)

If clock is at a high (1) and the data low (0), the host assumes that data is going to be sent to the keyboard, and the clock signal is driven in the timing separately shown and data are received in synchronization with it.

If a parity or framing error is involved, the RESEND command is issued from the keyboard and becomes ready for an input again.

8-3. Key code

A key code is sent to the FIFO buffer in the keyboard and the contents of FIFO are sent when it becomes ready to send after handshake. The SET 2 mode is established after the power was turned on. The key code can be selected by the SELECT SCAN command (FO, 00-03) and it is possible to select SET 1, SET 2, and SET 3 for the output code. Except for special code keys shown in a separate listing, it produces a "MAKE" code and a "BREAK" code.

Set 1 mode

Make code Value in the code table 1 byte

Break code Value in the code table + 80hex 1 byte

Example: MAKE code = 20 hex produces BREAK code = A0 hex

Set 2, Set 3 mode

Make code Value in the code table 1 byte

1st Break code F0hex

2nd Break code Value in the code table 2 byte

Example: MAKE code = 20 hex produced BREAK code = F0, 20 hex

NOTE: If a key code that needs to be sent is occurred when the FIFO buffer is fully occupied, the OVERRUN code is provided after waiting until a vacancy is obtained in the buffer, then the key code is set. In this event, either MAKE/BREAK code may not be lacking.

8-4. Repeat operation

When the same key is kept depressed, it produces the key code repeatedly sent to the FIFO buffer. The following is established for the repeated key.

If the same key was kept depressed, that particular key code is repeated to issue and stored in the FIFO buffer. All keyboard keys are subject to this in the SET 1 and SET 2 modes, except for the SET 3 mode where the following keys are effective for repeat.

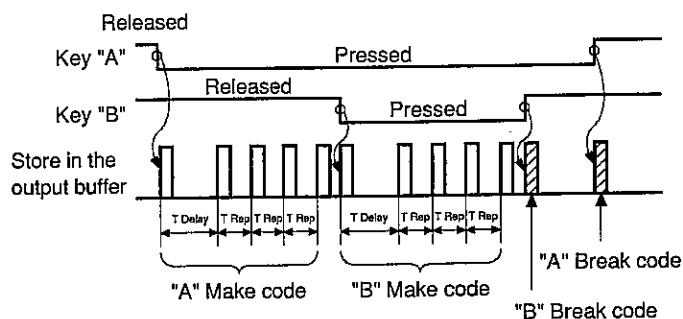


Fig. 8-2

Repeat takes place in the following sequence.

1. Wait for depression of a repeat (TYPEMATIC) key.
2. When a TYPEMATIC key is pressed, the MAKE code of that key is stored in the output buffer.
3. Step 2 is repeated until the MAKE code is accepted to the output buffer.
4. The key by which the MAKE code is produced is temporarily stored in the latest output buffer.

5. It waits for the time TDelay that programmed by the SET TYPOMATIC RATE/DELAY command. If a new key depression was made in this period, it returns to Step 2. If the key that stored the key code latest in the output buffer is released, it returns to Step 1 after storing the BREAK code of that key in the output buffer. If the other key than that stored the MAKE code latest in the output buffer is released, the BREAK code of that key is stored in the output buffer.
6. If the key that stored the MAKE code latest in the output buffer without a new key depression, the MAKE code that temporarily stored is sent to the output buffer.
7. It waits for the repeating time TRep that programmed by the SET TYPOMATIC RATE/DELAY command. If a new key is pushed in this period, it returns to Step 2. If the key that stored the MAKE code latest in the output buffer, the BREAK code of that key is stored in the output buffer and returns to Step 1. If a key other than stored the MAKE code latest in the output buffer is released, the BREAK code of that key is stored in the output buffer.
8. If the key that stored the MAKE code latest in the output buffer is released without a new key depression, it returns to Step 6.

8-5. Fn key

Operational description

The Fn key (key No.128) is the key employed to emulate the 24 key which was removed from the IBM AT 101/102 keyboard in regard to the US, GE, and UK keyboard. It is also used to generate the key code that expanded from the original 101/102 keyboard.

Key code shown next will be issued when the following key is pressed while depressing the Fn key or the Fn key is pressed while the following key is depressed.

Key combination (US keyboard)	Emulation key (AT101/102 keyboard key No.)
Fn + Esc (110)	Blank/5(Ten key for Cursor) (97)
Fn + F1 (112)	F11 (122)
Fn + F2 (113)	F12 (123)
Fn + F3 (114)	←(Ten key for Cursor) (92)
Fn + F4 (115)	→(Ten key for Cursor) (102)
Fn + F5 (116)	↑(Ten key for Cursor) (96)
Fn + F6 (117)	↓(Ten key for Cursor) (98)
Fn + F7 (118)	PageUp(Ten key for Cursor) (101)
Fn + F8 (119)	PageDown(Ten key for Cursor) (103)
Fn + F9 (120)	Home(Ten key for Cursor) (91)
Fn + F10 (121)	End(Ten key for Cursor) (93)
Fn + Ins (75)	Num Lock (90)
Fn + Del (76)	Scroll Lock (125)
Fn + SysReq (124)	Print Screen (124)
Fn + Setup (127)	Alternate Setup (NEW)
Fn + Pause (126)	Sleep (NEW)

8-6. Typing timing

1) Normal typing timing

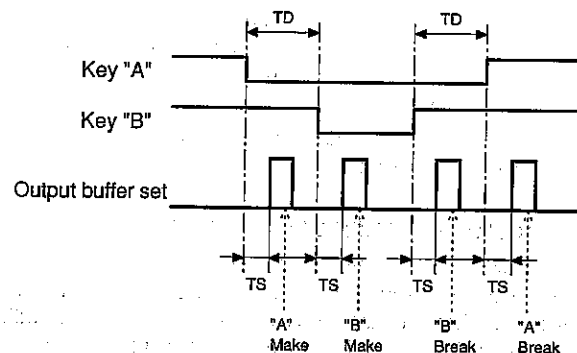


Fig. 8-3

Ts: 10~20msec (NOTE)

But, if it is shorter than the time required to prevent chattering by TD, the order of outputs "A" and "B" may be inverted depending on the sequence of sampling.

NOTE: For this period is required to prevent chattering, and is the parameter that may vary according to keyboard mechanical characteristics. The parameter shown above is the one when the bounce convergence time.

Shown below is the expression to obtain Ts.

Min Ts = Maximum bounce convergence time

Max Ts = 2 x (maximum bounce convergence time)

Key combination (US keyboard)	Emulation key (AT101/102 keyboard key No.)
Fn + 7/& (Key No. 8)	7(Ten key for Number) (91)
Fn + 8/* (9)	8(Ten key for Number) (96)
Fn + 9/((10)	9(Ten key for Number) (101)
Fn + 0/ (11)	*(Ten key) (100)
Fn + \ / (14)	Ins(Ten key for Cursor) (99)
Fn + ←(BackSpace) (15)	Del(Ten key for Cursor) (104)
Fn + U (23)	4(Ten key for Number) (92)
Fn + I (24)	5(Ten key for Number) (97)
Fn + O (25)	6(Ten key for Number) (102)
Fn + P (26)	-(Ten key) (105)
Fn + J (37)	1(Ten key for Number) (93)
Fn + ; / : (40)	+(Ten key) (106)
Fn + _ (Enter) (43)	Enter(Ten key) (108)
Fn + M (52)	0(Ten key for Number) (99)
Fn + . / > (54)	.(Ten key for Number) (104)
Fn + / ? (55)	/ (Ten key) (95)
Fn + ← (79)	Home(Cursor key) (80)
Fn + ↑ (83)	PageUp(Cursor key) (85)
Fn + ↓ (84)	PageDown(Cursor key) (86)
Fn + → (89)	End(Cursor key) (81)

2) Power on timing with a key depression or key code output timing at RESET command input

When power is turned on with a key depressed or the key code of the key pushed after sending the BAT completion code (AAH) is sent after the RESET command has been processed.

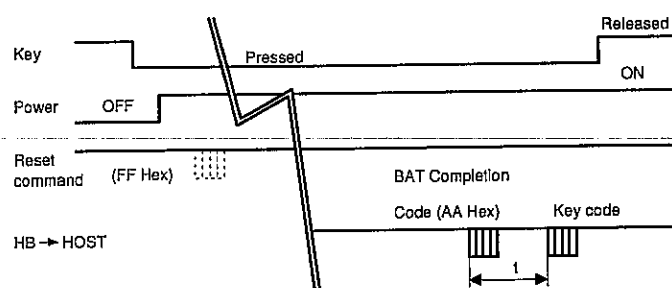


Fig. 8-4

8-9. Multiple key depression including the emulation key

(1) In case a normal key is pressed while the emulation key is being pressed and that the normal key is released first.

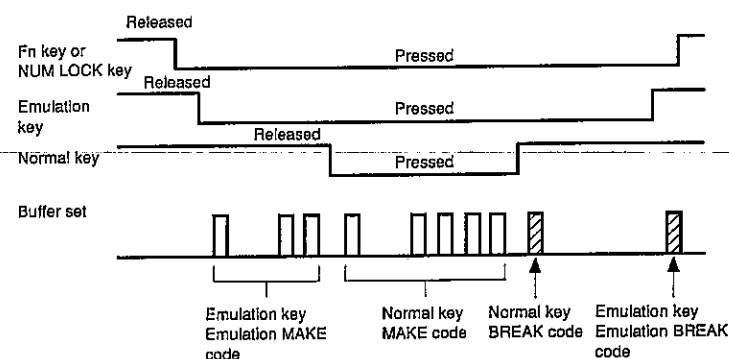


Fig. 8-5

(2) When the normal key is pressed while the emulation key is being pressed and that the emulation is released first.

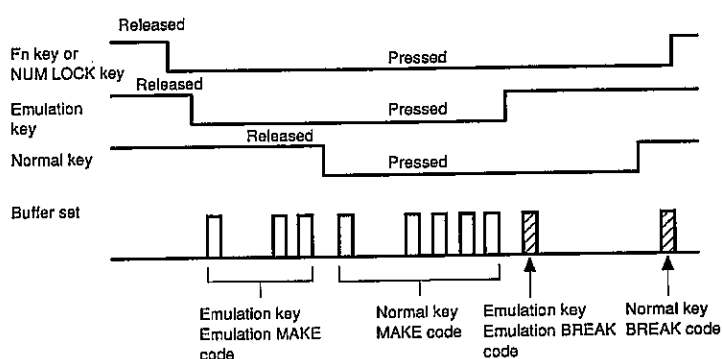


Fig. 8-6

(3) When the normal key is released while the emulation key is being depressed and that the Fn key, emulation key, and normal key are released in this order.

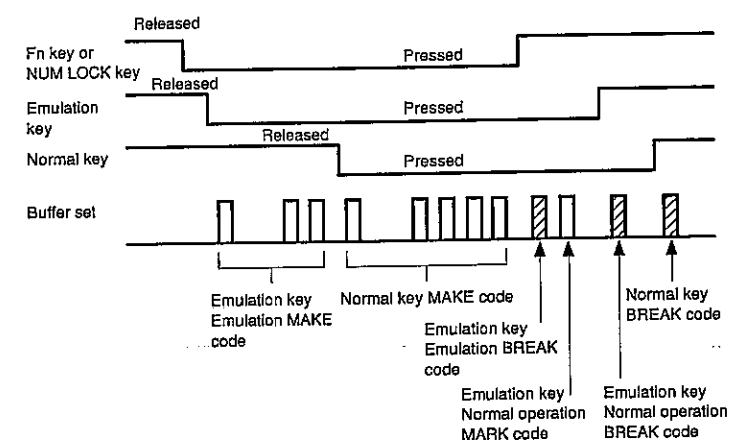


Fig. 8-7

8-7. Input/output commands

1) Input command (host→keyboard controller)

When a command given in the command list is inputted, the process takes place. The response signal to the host should be returned within 20msec, except for the response to the RESET command. If there is no such a command, the RESEND command is returned to the host.

2) Output command (keyboard controller→host)

The keyboard controller sends the command code to the host except the key scan code.

3) Newly employed command codes

DISABLE SLP command.....E2 hex
 ENABLE SLP command.....E4 hex
 RESET SLP command.....E0 hex
 SET SLP command.....E1 hex

8-8. N-key rollover

The keyboard controller itself does the N-key rollover. A resistance method matrix is used for the key matrix, and the return data is sent to the controller via the rollover chip (VHi3JD2CA1A-1) made by Alps. Because of this, a complete N-key rollover may not be attained owing to the limit to the key numbers, it has been so made as to secure the 10 key rollover. Adoption of the N-rollover chip would not generate the overrun code caused by multiple key depression.

- (4) When the normal key is pressed while the emulation key is being pressed and that the Fn key, normal key, and emulation key are released in this order.

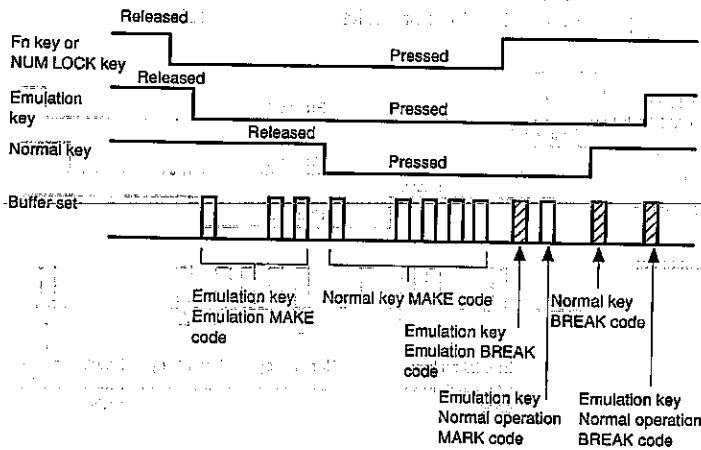


Fig. 8-8

- (5) When the normal key is pressed with the shift key while the emulation key is being pressed and that the normal key, shift key, and emulation key are released in this order.

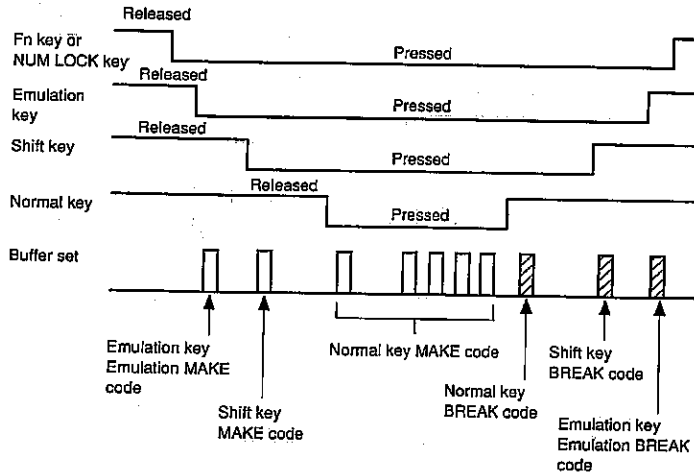


Fig. 8-9

- (6) When the normal key is pressed with the shift key while the emulation key is being pressed and that the emulation key, normal key, shift key, and Fn key are released in this order.

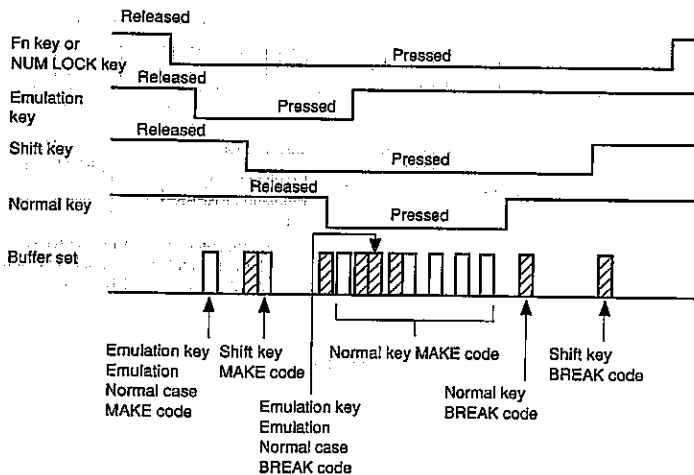


Fig. 8-10

- (7) When the normal key is pressed with the shift key while the emulation key is being pressed and that the normal key, emulation key, and shift key are released in this order.

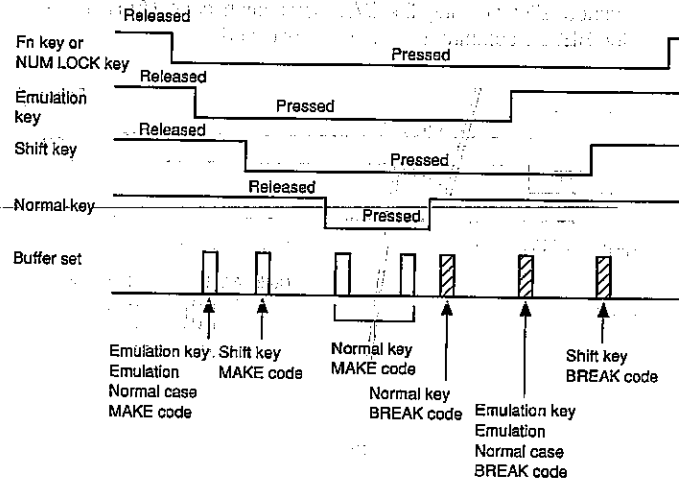


Fig. 8-11

8-10. Resistor membrane method

(1) Configuration

The resistor membrane N-key rollover circuit consists of:

- ① a membrane switch that has the resistor matrix (printed),
- ② scan circuit that convert the unselected row to ground level, and,
- ③ comparator that recognizes the receive signal level.

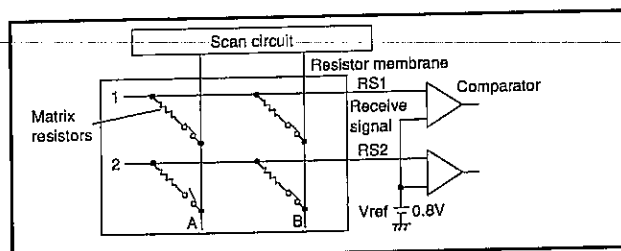


Fig.2 Resistor membrane N-key configuration

(2) Operation

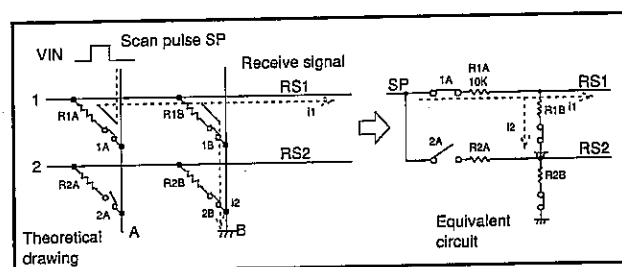


Fig.3 Theoretical drawing

(2)-1 Removal of phantom key by line separation

- Each key switch constitutes a serial matrix resistors RA1–R2B.
- Using those resistors, the not selected by the scan pulse is set to ground level.
- This way, line is isolated in terms of circuits (see Fig.3 Equivalent circuit).
- So, there would be no phantom key generated caused by line to line interference as seen in the conventional configuration.

(2)-2 Receive signal level recognition

- With this method, there would be no generation of phantom key caused by line to line interference.
- But, if there was a rollover operation in the same line of the matrix, the scan pulse peak value VIN is divided by the matrix resistors R1A and R1B to decrease the receive level.
- So, the comparator KM1 (KM2) is used to recognize the level.
- So, if assumed that occurrence of comparator threshold value Vref as many as the maximum rows of the matrix rows, the N-key rollover can be attained by setting it to the minimum receive level.

CHAPTER 9. EXPLANATION OF LSI

bottom: enhancement: 10/10/88 (0)

9-1. 80C287 80-Bit HMOS NUMERIC PROCESSOR EXTENSION (80C287)

revision: 3.0.0

- High Performance 80-Bit Internal Architecture
- Implements Proposed IEEE Floating Point Standard 754
- Expands iAPX 286/10 Datatypes to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands
- Object Code Compatible with 8087
- Built-In Exception Handling
- Operates in Both Real and Protected Mode iAPX 286 Systems
- 8x80-Bit Individually Addressable, Numeric Register Stack
- Protected Mode Operation Completely Conforms to the iAPX 286 Memory Management and Protection Mechanisms
- Directly Extends iAPX 286/10 Instruction Set to Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Datatypes
- Compatible with 80386 CPU
- Available in EXPRESS—Standard Temperature Range
- Available in 40 pin-Cerdip package (see Packaging Spec: Order #231369)

The Intel® 80C287 is a high performance numerics processor extension that extends the iAPX 286/10 architecture with floating point, extended integer and BCD data types. The iAPX 186/20 computing system (802C86 with 802C87) fully conforms to the proposed IEEE Floating Point Standard. Using a numerics oriented architecture, the 80C287 adds over fifty mnemonics to the iAPX 286/20 instruction set, making the iAPX 286/20 a complete solution for high performance numeric processing. The 80287 is implemented in N-channel, depletion load, silicon gate technology (HMOS) and packaged in a 40-pin cerdip package. The iAPX 286/20 is object code compatible with the iAPX 86/20 and iAPX 88/20.

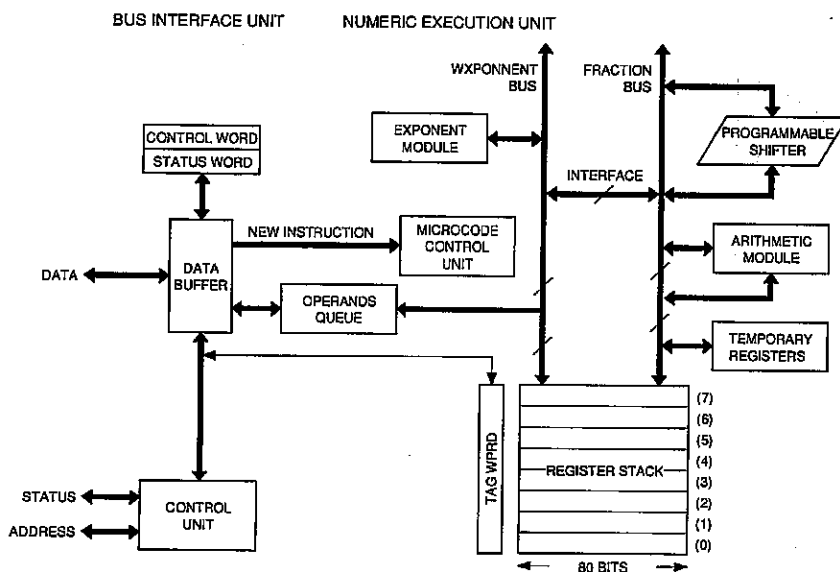
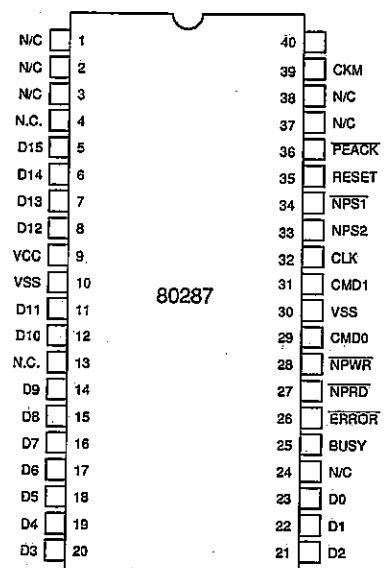


Fig. 9-1. 80C287 block diagram



NOTE:
NC PINS MUST NOT BE CONNECTED.

Fig. 9-2. 80C287 pin configuration

Table 9-1. 80C287 pin description

Symbol	Type	Name and Function
CLK	I	Clock input: this clock provides the basic timing for internal 80C287 operations. Special MOS level inputs are required. The 82284 or 8284A CLK outputs are compatible to this input.
CKM	I	Clock Mode signal: indicates whether CLK input is to be divided by 3 or used directly. A HIGH input will cause CLK to be used directly. this input may be connected to Vcc or Vss as appropriate. this input must be either HIGH or LOW 20 CLK cycles before RESET goes LOW.
RESET	I	System Reset: causes the 80C287 to immediately terminate its present activity and enter a dormant state. RESET is required to be HIGH for more than 480287 CLK cycles. For proper initialization the HIGH-low transition must occur no sooner than 50 μ s after Vcc and CLK meet their D.C. and A.C. specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the 80287 clock.
BUSY	O	Busy status: asserted by the 80287 to indicate that it is currently executing a command.
ERROR	O	Error status: reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	O	Processor Extension Data Channel operand transfer request: a HIGH on this output indicates that the 80C287 is ready to transfer data. PEREQ will be disabled upon assertion of PEACK or upon actual data transfer, whichever occurs first, if no more transfers are required.
PEACK	I	Processor Extension Data Channel operand transfer ACKnowledge: acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. PEACK may be asynchronous to the 80287 clock.
NPRD	I	Numeric Processor Read: Enables transfer of data from the 80287. This input may be asynchronous to The 80C287 clock.
NPWR	I	Numeric Processor Write: Enables transfer of data to the 80C287. This input may be asynchronous to the 80C287 clock.
NPS1, NPS2	I	Numeric Processor Selects: indicate the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., NPS1 is LOW and NPS2 is HIGH) enables the 80C287 to perform floating point instructions. No data transfers involving the 80C287 will occur unless the device is selected via these lines. these inputs may be asynchronous to the 80C287 clock.
CMD1, CMD0	I	Command lines: these, along with select inputs, allow the CPU to direct the operation of the 80C287. These inputs may be asynchronous to the 80C287 clock.

9-2. SC9889

9-2-1. General

This LSI incorporates two 82C59A interrupt controllers, 82C54 timer, 82C50 UART, and CMOS RAM, with a random gate to control the system operation and pseudo-SRAM control based on the AT/AX architecture.

Features

- AT/AX compatible machine system controller
- Internal peripheral controller
 - 82C59A interrupt controller x 2
 - 82C54 timer x 1
 - 82C50 UART x 1
- Internal 2KB CMOS RAM

- AT/AX compatibility
 - 80C286 interface
 - Clock control
 - Ready control
 - Reset control
 - Command generator
 - Data control
 - Hold control
 - 80C287 interface
 - Interrupt control by the 82C59A (internal = 3, external = 14)
 - System timer, refresh request, and speaker tone generation by 82C54
 - RS-232C interface by 82C50
 - Modem control
 - RTC interface
 - Including 2KB CMOS RAM
 - Pseudo-SRAM control (conventional memory, extended memory, EMS memory)
 - Port-B control
- Special functions
 - Sleep function
 - Power save function
 - Resume function (not used for the PC-6220)
 - Interface power off
- 184-pin QFP

9-2-2. Block diagram

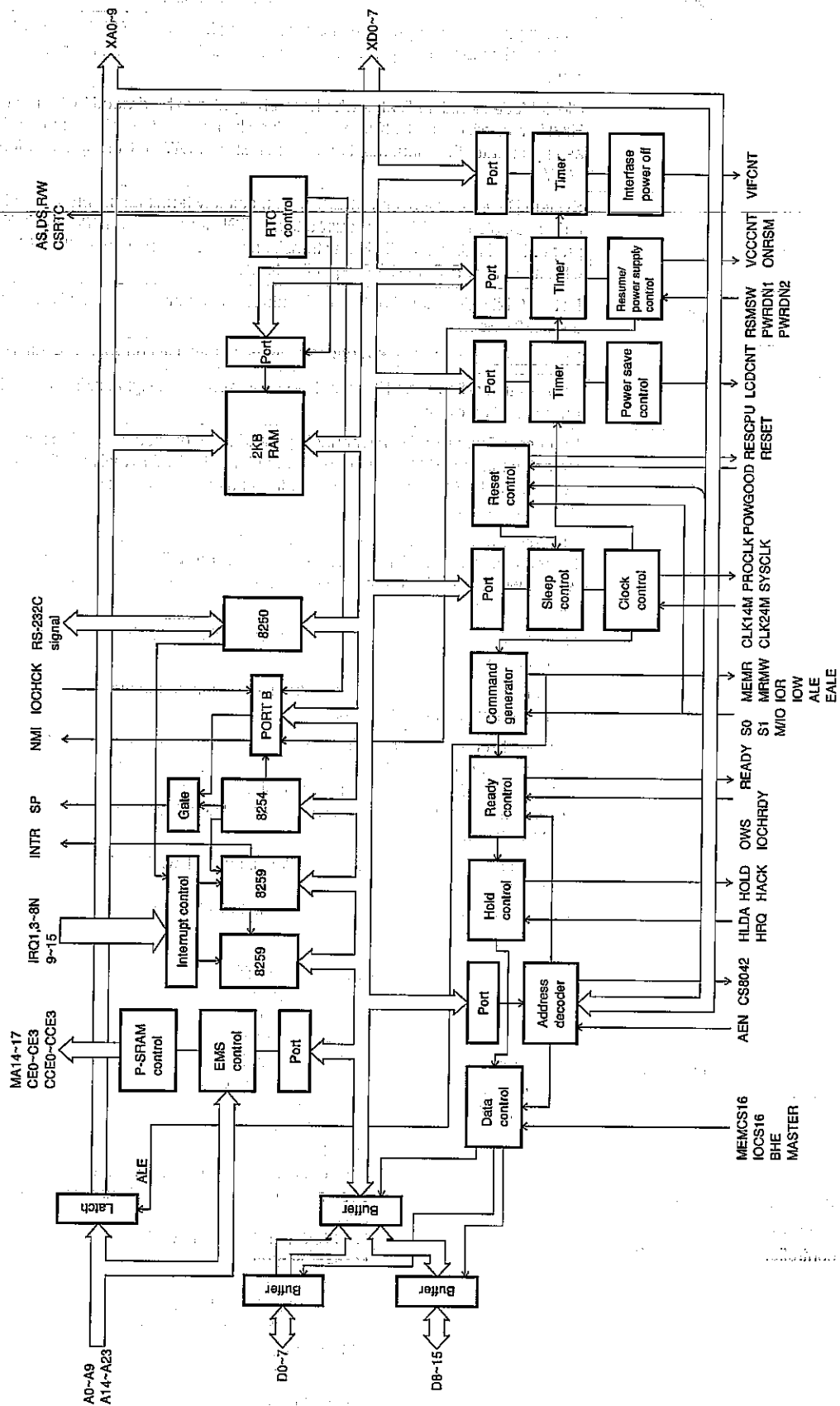


Fig. 9-3

9-2-3. Signal description

Signal name	IN/OUT	Function
CLK14M	IN	A 14.31818MHz clock input used for the CPU clock and also used for the timer clock after dividing it to 1/12.
CLK24M	IN	A 23.9616MHz clock input used for the CPU clock and also used for the 82C50A UART clock after dividing it to 1/13.
SYCLK	OUT	I/O slot strobe signal. A 1/2 CLK14M or 1/4 CLK24M is delivered.
PRCLK	OUT	CPU clock. A CLK14M or CLK24M input or 1/2 CLK24M is delivered with the clock selection.
S1-0	IN	Bus cycle status signal input from the CPU.
MIO	OUT	Memory and I/O select from the CPU.
ALE	OUT	Strobe to externally latch the CPU output address.
MEMR	IN/OUT	Memory read signal. During the memory read cycle and refresh cycle, a low state of strobe signal is issued, except when reading the memory signal on the local bus.
MEMW	IN/OUT	Memory write signal. Except for the memory write of the local bus, a low state of strobe signal is issued during the memory write cycle.
IOR	IN/OUT	I/O read signal. A low state of strobe is issued during the I/O read cycle.
IOW	IN/OUT	I/O write signal. A low state of strobe is issued during the I/O write cycle.
LMSEL	OUT	Indicates accessing of address below 1MB which is used to generate SMEMR or SMEMW in the external circuit.
EALE	OUT	Address latch signal used by the expansion unit employed to emulate a 6MHz bus cycle.
PWRGOOD	IN	Input from the power supply unit to indicate that the supply voltage is normal.
RESCPU	OUT	Reset signal issued when returning from the protect mode to the real mode, or when exiting from the shut down cycle. Connected only to the CPU.
BRESET	OUT	System reset signal.
READY	OUT	Signal used to inform the CPU the end of the cycle currently executed.
OWS	IN	Signal used to request the system to terminate the bus cycle currently executed by the device on the I/O slot.
IOCHRDY	IN	Signal used to request the system to extend the bus cycle currently executed by the device on the I/O slot.
HOLD	OUT	Signal used to request the CPU to hand down the bus.
HLDA	IN	Acknowledge to the CPU for its hold request.
HREQ	IN	Bus request signal from the DMAC.
HLDAK	OUT	Acknowledge request to the DMAC.
AEN	OUT	Signal used to indicate that it is a DMA cycle not by the master. A high on this line indicate the DMA cycle.
MA21-14	OUT	Pseudo-SRAM high address. For MA21~19, the address from the CPU is internally latched for output.
PCSL0 PCSH0 PCSL1 PCSH1	OUT	Pseudo-SRAM chip select. Four chip selects are used to access 16 bits of 2-bank pseudo-SRAM. Low byte High byte Bank0 PCSL0 PCSH0 Bank1 PCSL1 PCSH1
PSOE	OUT	Pseudo-SRAM output enable signal.
PSWE	OUT	Pseudo-SRAM write enable signal.
REFR	OUT	Pseudo-SRAM refresh signal.
CSBIOS	OUT	Display BIOS chip select signal.
NMI	OUT	Non-maskable interrupt signal to the CPU.
IOCHCKN	IN	Signal used to inform an error in I/O slot.
PCKN	IN	Parity check error signal.
INTR	OUT	Interrupt request signal to the CPU.
IRQ1 IRQ3-7 IRQ8N IRQ9-12 IRQ14-15	IN	Interrupt request signal from an external device.
LA23-0	IN/OUT	CPU side address signal.
SA9-0	IN/OUT	System side address signal.
BHE	IN/OUT	Data bus access signal, high side.
SBHE	IN/OUT	Latched data bus access signal, high side.
D7-0	IN/OUT	CPU side data bus, low side.
D15-8	IN/OUT	CPU/system side data bus, high side.
XD7-0	IN/OUT	System side data bus, low side.

Table 9-2 (a)

Signal name	IN/OUT	Function						
RDI	IN	Receive data.						
CII	IN	Calling tone detect signal.						
CTSI	IN	Send enable signal.						
DSRI	IN	Modem signal ready signal.						
CDI	IN	Carrier detect signal.						
SDI	OUT	Send data.						
RTSI	OUT	Send request signal.						
DTRI	OUT	Terminal ready signal.						
SP	OUT	Speaker tone output signal.						
RFRSHN	IN/OUT	Refresh timing signal to external bus.						
BCNT1 BCNT2 BCNT3 BCNT4	OUT	External buffer control signal. <table><tr><td>Enable</td><td>Direction</td></tr><tr><td>BCNT3</td><td>BCNT4</td></tr><tr><td>BCNT1</td><td>BCNT2</td></tr></table>	Enable	Direction	BCNT3	BCNT4	BCNT1	BCNT2
Enable	Direction							
BCNT3	BCNT4							
BCNT1	BCNT2							
EXPND	IN	Connected with GND of the expansion unit when connected need to pull-up externally.						
SELTM	IN	Signal used to inform selection of external gate array.						
DACK2	IN	Signal used to inform transfer on DMA channel 2.						
AS	OUT	Strobe signal for the RTC to latch address.						
DS	OUT	Strobe output for RTC to read.						
RW	OUT	Strobe output for RTC to write.						
CSRTCN	OUT	RTC chip select signal. A low state of signal is issued to select RTC.						
VIFCNT	OUT	Printer and RS-232C interface IC control signal.						
VCCOFF	OUT	Shuts off the unwanted power supply during the resume.						
LDCNT	OUT	Controls the LCD power supply.						
VMDCNT	OUT	Control the modem power supply.						
BLCNT	OUT	Control the backlight power supply.						
RSMSW	IN	Resume switch status input.						
ONRSM	OUT	Signal used to inform the resume state.						
MANOFF	IN	Indicates the main power supply status.						
SHUT	IN	Top cabinet close alarm signal. A high state of signal is an input normally by the external pullup resistor. When the top cabinet is closed, the microswitch is closed to have a low level input signal.						
BUSY	OUT	Signal used to indicate to the CPU that NDP is busy.						
BUSYNDP	IN	Signal from the NDP to indicate the busy state.						
ERRNDP	IN	Signal used to indicate occurrence of an error from NDP.						
RSTNDP	OUT	Signal used to initialize NDP.						
CSNDP	OUT	NDP select signal.						
PWRDWN2-1	OUT	Signal used to select the VGA controller operating mode.						
CSMDMN	OUT	Internal modem select signal.						
MINT	IN	Interrupt request from the internal modem.						
MORSTN	OUT	Internal modem reset signal.						
MRI	IN	RI signal from the internal modem.						
MEMCS16	IN/OUT	Indicates that the currently accessed memory is a 16-bit device.						
IOCS16	IN	Indicates that the currently accessed I/O is a 16-bit device.						
MASTER	IN	Indicates that the bus control is requested by an external master.						
DMACLK	OUT	DMAC clock which is 1/2 of SYSCLK.						
CLKSM	OUT	Key controller clock. 1/3 of CLK24M is supplied in 50% duty.						
ADS	N.C.	Reserved. ADS signal input pin when the 80386SX is used.						
MA23-22	N.C.	Reserved. Memory address high order 2 bits (corresponds to 4M RAM).						
TEXT	IN	Test input. With a high state of this signal, the test mode is established.						
VDD		Power supply.						
GND		GND						

Table 9-2 (b)

9-2-4. Function of block

4.1. Clock control

In this clock controller, the system clock supplied to the CPU, internal circuits, and I/O slot is derived from the clock input. Also, the input clock to the 82C54/82C50 serial controller and the minute-increment timer used by a special function is derived.

Two kinds of input clocks are supplied at all times; 14.31818MHz and 23.9616MHz. 1.8432MHz (After dividing 23.9616MHz to 1/13) is supplied to the internal timer. The CPU clock can be changed to 3 kinds software-wise. The I/O address 022H and 023H are used for the selection of the CPU clock. 04H is written to the port 022H, then the data are write to the port 023H. When 023H is once accessed, 04H needs to be written to 022H again. See the table next for the bit definition of the port 023H.

Bit	Signal name	Significance
0, 1	RESERVED	Reserved.
2, 3	CKSEL1, 2	CPU clock selection
4-7	RESERVED	Reserved.

When reset, all are reset except for CLSEL2 is set to "1".

Shown next is the CPU clock and the system clock when CKSEL1 and 2 are set for the port 023H.

CKSEL2	CKSEL1	CPU clock	CPU operating frequency	System clock
0	0	11.9808 MHz	5.9904 MHz	5.9904 MHz
0	1	14.31818 MHz	7.15909 MHz	7.15909 MHz
1	0	23.9616 MHz	11.9808 MHz	5.9904 MHz
1	1	Prohibited		

4.2. Ready control

In the ready controller, waits during the CPU access is determined. Shown below is the number of waits when accessing device.

Device	Waits	
	5.9904MHz/ 7.15909MHz	11.9808MHz
Main memory, private memory	0	1
Extended memory, EMS memory	0	1
BIOS ROM	0	1
VRAM (8-bit)	4	7
VRAM (16-bit)	1	2
DOS ROM, 8 bits	4	11
DOS ROM, 16 bits	1	5
80287	0	0
VGA (8-bit)	4	7
System I/O (000H-0FFH)		
VGA (16-bit)	1	2
Internal I/O, 8-bit I/O	4	11
HDC, EMS register, 16-bit I/O	1	5
Interrupt acknowledge cycle	1	2

4.3. Reset control

The CPU and system reset signal is created from the signal PWRGOOD.

When the CPU went into the shut down cycle, the reset signal is issued to the CPU. The data bus is monitored when the reset CPU command is sent to the keyboard controller (80C42) and the reset signal is sent to the CPU without receiving the signal from the 8042.

4.4. Command generator

The command signal is created by receiving the 286 CPU status signal. Also, the signal ALE is issued.

For a device that requires the command recovery time in the I/O cycle, the command delay is automatically inserted.

Shown next is the CPU clocks for the command delay when accessing a device.

Device	Command delay/CPU clocks	
	5.9904MHz/ 7.15909MHz	11.9808MHz
Main memory, private memory	0	0
Extended memory, EMS memory	0	0
BIOS ROM	0	0
VRAM (8-bit)	0	0
VRAM (16-bit)	0	0
Dictionary ROM, 8 bits	0	3
Dictionary ROM, 16 bits	0	3
80C287	0	0
VGA (8-bit)	1	2
System I/O (000H-0FFH)		
VGA (16-bit)	1	2
Internal I/O, 8-bit I/O	1	5
HDC, EMS register, 16-bit I/O	1	5
Interrupt acknowledge cycle	0	0

4.5. Data control

The internal/external data bus buffer is controlled and 8 bits to 16 bits and 16 bits to 8 bits conversion is carried out.

4.6. Address decoder

Internal device port select signal is created from the address. Also, chip select signal is issued for some of external devices.

Since the address input is latched by ALE, it may not be needed to be fully established during the cycle and may use CPU local address cycle.

4.7. Hold control

DMA request and refresh request are arbitrated and a hold is applied to the CPU.

When going into the sleep mode, the hold state is established before stopping the CPU clock. After this, the hold request is cancelled. For the clock is at a halt, the CPU stays in the hold state. Therefore, DMA request or refresh request during the sleep mode can be performed without contention.

4.8. Special functions

- (1) Sleep function
The CPU clock is suspended to supply when the HLT command is executed.
 - (2) Power save function
With this feature, the power supply to the LCD and backlight is turned off after a lapse of a certain time (auto power save feature). It is also possible to directly shut off the power supply to the LCD and backlight independently.
 - (3) Resume function (not used for the PC-6500)
With this feature, the memory contents are backed up when the power is turned off so that the previous state may be recovered when the power is turned on.
 - (4) Interface power off
With this feature, power consumption is abated when not required for the RS-232C interface IC and internal modem.
- (1) and (3) functions mentioned above are not able to use when connecting the expansion unit.

4.8.1. Sleep function

The sleep function is completely supported by the hardware once the HLT command has been executed. When the HLT command is executed, the CPU sets S0 and S1 low and M/IO and A1 high to inform the existence of the hold state to externals. As the sleep controller recognize it, the sleep mode will be established in the following sequence.

- (1) Hold request is issued to the CPU. If the refresh request or DMA transfer request is issued at the same moment, it will be handled by the arbitrary circuit.
- (2) After recognizing the halt acknowledge, the CPU clock is suspended to supply in synchronization with a high to low transition of the clock input to the controller in $\phi 2$ cycle.
- (3) The hold request is cancelled by the sleep. Since the CPU is at a hold state, the DMA transfer and refresh during the sleep continue to perform.

An interrupt request is issued including NMI, it exits from the sleep mode. When the interrupt occurred, the clock is resumed to supply to the CPU in synchronization with a high to low transition of the clock input to the controller and the CPU starts executing the command that follows HLT.

When the input to EXPND line is at a low, connection of an expansion is assumed and prohibits steps (1)~(3) so that the sleep function does not take place. The state of the EXPND line input can be known by scanning EXPND of the EXSTAT register. When EXPND is at "0", the expansion unit is in connection. The EXSTART register is a read only register which is allocated to 0DH of the Sharp original port. The table below shows its bit definition.

EXSTAT register

Bit	Signal name	Significance
0	EXPND	State of expansion unit connection
1~7	—	Undefined. Reads "0" at all times.

4.8.2. Power save function

The power save function automatically turns off the power supply to the LCD and backlight when there was no key operation met for a period of the given time. So, it has a timer within the power save controller which continues to count the time as long as there is no interrupt request from the 8042 key controller. When the prescribed time is reached, the signal is issued from the LCDCNT and BLCNT line to turn off the LCD and the backlight power. At the same time, the VGA controller goes into the relax mode.

The VGA controller operating mode can be directly set by the internal I/O register. PWRDWN1 and 2 of the VGACNT register are used to set the relax mode and retire mode. DISVGA of the VGACNT register is used to set active or inactive of the internal VGA, which is active "0". The VGACNT register is allocated to 0EH of the Sharp original port and its bit definition is shown next.

VGACNT register

Bit	Signal name	Significance
0	POLINV	Internal SIO input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2	PWRDWN1	VGA controller mode setting (relax mode)
3	PWRDWN2	VGA controller mode setting (retire mode)
4~7	RESERVED	Reserved. Possible to read/write.

When reset, all are reset to "0".

The table next shows the VGA controller operation mode set by PWRDWN1 and 2.

PWRDWN 2	PWRDWN 1	LCD power supply	BL power supply	VGA controller	Note
0	0	ON	ON	Normal mode	
0	0	ON	OFF	Normal mode	
0	0	OFF	OFF	Relax mode	PWRCNT register, PCBL=0
0	1	OFF	OFF	Relax mode	
1	0	OFF	OFF	Retire mode	
1	1	OFF	OFF	Prohibited	

When the power save feature is used, both PWRDWN1 and 2 need to be set to "0". The DISVGA is set to "0" to set the internal VGA active, and *LCDEN of the SIOCPR register needs to be set to "0" to select the LCD as a display device.

To directly turn off the LCD or backlight power supply by means of software, "0" must be written to PCVLCD and PCBL of the PWRCNT register. The PWRCNT register is an 8-bit read/write register employed to control power supplies which is allocated to 06H of the Sharp original port, whose bit definition is as shown next.

PWRCNT register

Bit	Signal name	Significance
0	PCVIF	Printer, RS-232C interface IC control.
1	PCVLCD	VGA controller and LCD power supply control
2	PCVCC	System power supply control (VCC)
3	PCBL	Backlight power supply control
4	PCVMD	Modem power supply control
5~7	RESERVED	Reserved. Read/write possible.

When reset, each bit of PCVIF, PCVCC, PCBL, and PCVMD is set "1" and others are reset.

When using the power save function (auto power save) by means of the timer, PCVLCD and PCBL of the PWRCNT register must be set to "1". Then write "1" to ASLCD of the ATSTBY register to put the timer effective, then set in the PWRTIM register the time the power save should function.

The ATSTBY register is an 8-bit read/write register with which programmed to put control functions in effect, which the timer becomes effective when set to "1". It is allocated to 07H of the Sharp original port whose bit definition is as given next.

ATSTBY register

Bit	Signal name	Significance
0	ASVIF	Auto interface power off on/off setting
1	ASLCD	Auto power save on/off setting
2	ASVCC	Auto resume on/off setting
3~7	RESERVED	Reserved. Read/write possible

All are reset to "0" when reset.

The PWRTIM register is used to program the time for auto power save that it may be set in increment of one minute in a range of 0 to 15 minutes. However, the actual time is shorter than the programmed time within a minute. When PST3-0 are all "1", the setting will be 14-15 minutes. It is possible to read/write and the set value is read. It is allocated to 09H of the Sharp original port whose bit definition is given next.

PWRTIM register

Bit	Signal name	Significance
0-3	PST0-3	Auto power save time setting
4-7	RESERVED	Reserved. Read/write possible.

When reset, PST3-0 are set to "1" and others are reset.

When IRQ1 which is the interrupt request from the 8024 goes high before the set time, the set value is reloaded in the timer and starts to count from the start all over again. The timer will be reloaded even if the PWRCNT register, ATSTBY register or PWRTIM register of the Sharp original port is written.

4.8.3. Resume function (not used for the PC-6500)

To use the resume function, it has to be enabled by writing "1" in RSMEN of the RSMCNT register. The RSMCNT register is an 8-bit read/write register which is allocated to 0BH of the Sharp original port whose bit definition is given next.

RSMCNT register

Bit	Signal name	Significance
0	RSMEN	Resume mode setting
1	CIEN	Reserved. Read/write possible.
2	MRIEN	Reserved. Read/write possible.
3-7	RESERVED	Reserved. Read/write possible.

When reset, all are reset to "0".

In the resume mode (RSMEN=1), there are two cases that moves to the power down state by shutting the power supply (Vcc) off with the memory backed up.

(1) Input of a low to high transition signal from the RSMS line.

(2) No key operation is done within the prescribed time.

In the case of (1), a high state of signal is issued from the NMI line at a low to high transition of the signal input from the RSMSW line to apply NMI to the CPU. On the other hand, in the case of (2), the resume controller internal timer continues to count while there is no interrupt request from the 8042. When the programmed time is reached, the NMI is caused. But similar as the sleep function, a low on the EXPND input prohibit the NMI and the resume function does not take place. The state of the EXPND input can be scanned on EXPND of the EXSTAT register.

When using the resume function by the timer (auto resume), the timer must be turned on after writing "1" to ASVCC of the ATSTBY register and the time that the power down is expected must be set in the RSMTIM register. It would be possible to program it in increments of one minute within a range of 0 to 127 minutes, actual time is shorter than the programmed time within a minute. When ART6-0 are all "1", the setting will be 126-127 minutes. It is possible to read/write and the set value is read. It is allocated to 0AH of the Sharp original port whose bit definition is given next.

PWRTIM register

Bit	Signal name	Significance
0-6	ART0-6	Auto resume mode setting
7	RESERVED	Reserved. Read/write possible.

When reset, ART6-0 are all set to "1" and the bit 7 is reset. Similar as the auto power save, an interrupt request from the 8042 (IRQ) turns high before the programmed time, the set value is loaded in the timer and the count starts all over again from the beginning. The timer will be reloaded when the PWRCNT register, ATSTBY register, or RSMTIM register of the Sharp original port is written.

In either case of (1) and (2), occurrence of NMI does the same process and requires software support. The following are required in the NMI routine in order to power down during the resume mode.

- (1) Judges the NMI cause.
- (2) All I/O registers of the device (VCC supply) installed to the system must be saved to the expanded CMOS RAM.
- (3) If the VRAM contents may not be retained, it has to be saved in the pseudo-SRAM private area (256KB).
- (4) All CPU registers at NMI occurrence must be saved to the stack and SS:SP must be written in the CMOS RAM.
- (5) In order to shut down the system power supply, "0" must be written in PCVCC of the PWRCNT register.

To judge the cause of NMI at (1), RSMNMI of the NMIFCT register must be scanned. If "1", an NMI occurrence is indicated by the RSMSW input or the resume timer. The NMIFCT register is a read only register which is used to judge the NMI cause which is allocated to 0FH of the Sharp original port whose bit definition is shown next.

NMIFCT register

Bit	Signal name	Significance
0	RSMNMI	On state of the resume NMI request
1-7	—	Undefined. Reads "0" at all times.

To restore from the power down state in the resume mode, the system power must be turned on and PWRGOOD input must change from low to high. Because a reset is applied in this instance, the following process takes place in the initialization routine after the reset.

- (1) Reset cause is judged.
- (2) The contents of I/O registers saved in the CMOS RAM and are loaded to devices.
- (3) The contents of the VRAM are loaded from the private area of the pseudo-SRAM (in case the contents of the VRAM may not be retained).
- (4) SS:SP is read from the CMOS RAM and all CPU registers are restored from the stack.

To judge the reset cause in (1), RCR of the RSTFCT register is scanned. If "1", it indicates to turn off the VCC supply by software in order to power down in the resume mode. The RSTFCT register is a read only register used to judge the reset cause. When this register is scanned, each bit of RCR, RCCI, and RCMRI is reset to "0". It is allocated to 0CH of the Sharp original port whose bit definition is shown next.

RSTFCT register

Bit	Signal name	Significance
0	—	Undefined. Reads "0" at all times.
1	RCR	On state of the system power (VCC) off request
2	RCCI	State of the power on cause by the CI input of the internal SIO.
3	RCMRI	State of the power on cause by the RI input of the internal modem.
4-7	—	Undefined. Reads "0" at all times.

RCCI and RCMRI of the RSTFCT register is used to support the auto sensor from the internal SIO and the internal modem.

When the system power turns on, a reset is applied, and the GPU reads the RSTFCT register during the initialization routine. If RCCI or RCMRI is "1", it indicates that power on took place by the auto answer. Reading it again resets RCCI and RCMRI.

4.8.4. Interface power off

With the interface power off function, the power consumption of the interface IC may be held down when not using the printer or RS-232C. The time the interface power off feature functions is when the printer or the internal SIO was not accessed within the given time, or, the internal I/O register is directly accessed by means of software.

To directly turn off the interface power by software, "0" must be written to PCVIF of the PWRCNT register. When written, the printer interface IC output goes high impedance and the RS-232C line driver receiver goes into a standby mode to decrease the circuit current.

To use the auto interface power off feature, PVCIF of the PWRCNT register must be set to "1", then write "1" to ASVIF of the ATSTBY register to turn on the timer. The timer will be cleared when the internal printer and internal SIO is accessed. It may also be cleared by writing the PWRCNT register or ATSTBY register of the Sharp original port. The time power off feature comes active after the timer has cleared for 14 to 15 minutes.

It is also possible to control the power supply to the internal modem using the interface power off function. To shut off the power supply to the internal modem (VMDM), write "0" to PCVMD of the PWRCNT register. With this, the signal employed to shut off the modem power supply appears on the VMDCNT line.

4-8-5. Power status

Since the power is automatically shut down for the auto power save timer, and auto interface power off functions by means of the timer. The CPU will recognize the status of the LCD power, backlight power, and printer-RS-232C control by scanning the PWRSTAT register. The PWRSTAT register is a read only register which is allocated to 08H of the Sharp original port. Except for PSVIF, PSLCD, and PSBL, the power supply control data set to the PWRCNT register are read. "0" means off and "1" on. See the table next for the bit definition of the PRSTAT register.

PWRSTAT register

Bit	Signal name	Significance
0	PSVIF	State of printer and RS-232C interface IC control
1	PSLCD	State of LCD power supply (VLCD)
2	PSVCC	State of system power supply (VCC)
3	PSBL	State of backlight power supply (VBL)
4	PSVMD	State of modem power supply (VMDM)

4-9. Interrupt control

A pair of 82C59A interrupt controllers are internally contained in this chip for the interrupt control and supports 16 interrupt levels in conjunction with the cascade connection NMI. The NMI is port-B controlled.

As an 8-bit I/O device on the system bus (XD bus), a pair of 82C59A has address mapped to 020H-03FH on the master side and 0A0H-0BFH. In order to avoid contention with the CPU clock switch controlling I/O address 022H and 023H (refer to paragraph 4.1) for the 82C59A on the master side, the selection is not done when the bit of the latch address is "1".

The table below shows the 82C59A interrupt outputs.

Master	Slave	Function
IRQ0		Timer output channel 0
IRQ1		Keyboard (output buffer full)
IRQ2		Interrupt from the slave side controller
	IRQ8	Real time clock interrupt
	IRQ9	VGA controller or INT0AH (IRQ2)
	IRQ10	Reserved (expansion slot)
	IRQ11	Reserved (expansion slot)
	IRQ12	Reserved (expansion slot)
	IRQ13	Co-processor
	IRQ14	Hard disk controller
	IRQ15	Reserved (expansion slot)
IRQ3		Serial port 2 (COM2)
IRQ4		Serial port 1 (COM1)
IRQ5		Parallel port 2
IRQ6		Floppy disk controller
IRQ7		Parallel port 1

4.10. Timer

A single 82C54 interval timer is internally contained in this chip.

The 82C54 is mapped to the I/O address 040H-05FH as an 8-bit I/O device on the system bus (XD bus). Three independent 16-bit counter on channels 0-2 of the 82C54 can be defined as follows:

Channel 0	System timer
GATE0	Fixed ON
CLKIN0	1/12 14.31818MHz clock
CLKOUT0	82C59A IRQ0
Channel 1	Refresh request generator
GATE1	Fixed ON
CLKIN1	1/12 14.31818MHz clock
CLKOUT1	Refresh request cycle
Channel 2	Speaker tone generator
GATE2	Fixed ON
CLKIN2	1/12 14.31818MHz clock
CLKOUT2	Speaker drive

4.11. Serial interface

The 82C50 UART is internally contained in this chip as a serial interface and supports a single channel RS-232C interface using the external RS-232C driver as an internal SIO. This also used for the interface with the internal modem.

Two serial interfaces may be port allocated and set on or off, which the SIOCFR register is used for the RS-232C and the MDMCFR register for the internal modem. The SIOCFR register is a 7-bit read/write register which is allocated to 01H of the Sharp original port. The MDMCFR register is a 2-bit read/write register which is allocated to 03H of the Sharp original port.

The table next shows bit definition.

SIOCFR register

Bit	Signal name	Significance
0-2	FDD0-2	Reserved. Read/write possible.
3	SIO1/*2	Internal SIO port allocation
4	*SIOEN	Internal SIO on/off setting
5	*INTKEY	Reserved. Read/write possible.
6	*LCDEN	Display device selection
7	—	Undefined. Reads "0" at all times.

MDMCFR register

Bit	Signal name	Significance
0	OUTSEL	MORSTN output signal selection
1-3	—	Undefined. Reads "0" at all times.
4	*MDMEN	Internal modem on/off setting
5-7	—	Undefined. Reads "0" at all times.

When reset, *SIOEN of the SIO CFR register and *MDMEN of the MDMCFR register are set to "1" and all others are reset.

*SIOEN and SIO1/*2 of the SIOCFR register may be revised of their contents when written to "02" to the Sharp original port. The inverted bit 4 of the 02H port corresponds to SIO1/*2 and bit 5 to SIOEN.

The table below shows the ports that allocated by the setting of SIOCFR and MDMCFR registers vs. active input to IRQ3 and IRQ4 of the 82C59A.

*SIOEN	*MDMEN	SIO1/*2	Internal SIO	Internal modem	IRQ3 input	IRQ4 input
0	0	0	COM2	COM1	Internal SIO	Internal modem
0	0	1	COM1	COM2	Internal modem	Internal SIO
0	1	0	COM2	OFF	Internal SIO	External IRQ4
0	1	1	COM1	OFF	External IRQ3	Internal SIO
1	0	0	OFF	COM1	External IRQ3	Internal modem
1	0	1	OFF	COM2	Internal modem	External IRQ4
1	1	0	OFF	OFF	External IRQ3	External IRQ4
1	1	1	OFF	OFF	External IRQ3	External IRQ4

The RS-232C interface serial input/output and control signals can be inverted with POLINV of the VGACNT register. When POLINV is at "1", the polarity inverts. The VGACNT register is allocated to 0EH of the Sharp original port whose bit definition is as shown next.

VGACNT register

Bit	Signal name	Significance
0	POLINV	RS-232C input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2, 3	PWRDWN1, 2	VGA controller mode setting
4-7	RESERVED	Reserved. Read/write possible

When reset, all are reset to "0".

To reset the internal modem (that can be installed within the machine), the output from the MORSTN line is used. The 1-bit output of the MORSTN output port can be switched with the port select signal output using OUTSEL of the MDMCFR register. When OUTSEL is at "1", the bit 3 of the I/O address 202H port is issued. When "0", the decoded signal of the I/O address 202H is issued as a port select signal. The 202H port is a read/write internal I/O register whose bit definition is shown next.

202H port

Bit	Signal name	Significance
0-2	RESERVED	Reserved. Read/write possible
3	MORSTN	Internal modem reset signal
4	RESERVED	Reserved. Read/write possible
5-7	—	Undefined. Reads "0" at all times.

When reset, bits 0-4 are reset.

4.12. RTC and CMOS RAM

For this chip, RTC is controlled by AS, DS, R/W, and SCRTCN outputs. For setup expansion, a 2KB CMOS RAM is provided.

Among 11 bits address input of the 2KB CMOS RAM, the low 6 bits is connected to the I/O 070H port bits 0-5, and high 5 bits to the latch address bits 10-14. Which is to be selected, RTC or CMOS RAM, when the I/O 071H port is accessed is determined by the data in the I/O 70H bit 6. When "0", RTC is selected and "1" the CMOS RAM. See the figure below for the mapping of the RTC and the CMOS RAM.

4.13. Pseudo-SRAM control

This chip supports control of a maximum 4MB of the pseudo-SRAM. Memory has three address spaces of the system area, EMS control area, and private area. The EMS control area can further be divided into three subsections of conventional area, extended area, and EMS area according to the internal I/O register setting.

(1) System area

The area of 256KB is allocated to 000000H-03FFFFH as the conventional memory.

(2) EMS control area

Address can be allocated to three areas using the internal I/O register setting.

(a) Conventional area

An address space of 384KB can be allocated to 040000-09FFFFH as a conventional memory.

(b) Extended area

Address space can be allocated after 100000H as an extended memory.

(c) EMS area

To support the EMS version 4.0, 34 windows of 16KB increments can be mapped in 040000-09FFFFH and 0C8000H-0EFFFFH.

(3) Private area

Using the internal I/O register setting, 2 256KB of address space is allocated to 0E0000H-0EFFFFH (access by bank select), which is to be used to save the VRAM contents during the resume and used by the system. It is possible to eliminate the private area by the internal I/O register setting.

4.13.1. System area

Among 4MB memory area supported by the memory controller, a 256KB of address space 000000H-03FFFFH is allocated as a conventional memory, regardless of the internal I/O register setting.

4.13.2. EMS control area

The maximum 4MB area from which excluded the system area and the private area is allocated to the EMS control area, and mapped to the conventional area, extended area, and EMS area by the internal I/O register setting.

There are EMSCFR register, PSRAMCF register, and EMSSTAT register as the internal I/O register controlled, whose bit definition is shown next.

EMSCFR register

Bit	Signal name	Significance
0-2	SW0-2	EMS control register I/O address setting
3, 4	JP2, 3	Extended memory capacity setting (expansion)
5, 6	SW5, 6	Extended memory capacity setting
7	RESERVED	Reserved. Read/write possible

PSRAMCF register

Bit	Signal name	Significance
0	RESERVED	Reserved. Read/write possible
1	INTLV	Pseudo-SRAM interleave access enable
2	*PCS3EN	256KB standard RAM usage setting
3, 4	JP0, 1	Extended memory capacity setting
5	VPTMEM	Private memory access enable
6, 7	MAP0, 1	Private memory bank select

EMSSTAT register

Bit	Signal name	Significance
0-2	SW0-2	State of EMS control register I/O address allocation
3, 4	SW3, 4	Both SW3 and SW4 reads "1" at all times.
5, 6	SW5, 6	State of the extended memory capacity setting
7	EMSEN	EMS on/off setting

The EMSCFR and PSRAMCF registers are allocated to 04H and 05H of the Sharp original port, and reset to "0" when reset.

SW0-2, and SW5-6 of the EMSSTAT register are read only bits which the data written in the EMSCFR register is read. EMSEN is a read/write bit that turns to "0" when reset.

When operated with the CPU clock at 24MHz, INTLV of the PSRAMCF register, is a bit which enables the non-wait access for the conventional memory and private memory interleave mode when the bit is set to "1".

(a) Conventional area

To allocate the memory space 040000H-09FFFFH to a conventional memory, EMSEN of the EMSSTAT register must be set to "0" to disable the EMS.

(b) Extended area

By setting SW5-6, JP2-3, of the EMSCFR register and JP0-1, and *PCS3EN of the PSRAMCF register, the memory space after 100000H can be allocated to the extended memory in a manner as shown next.

SW6	SW5	JP3	JP2	JP1	JP0	*PCS3EN	Extended memory
0	0	*	*	*	*	*	OMB 64KB (100000H-10FFFFH)
0	1	*	*	*	*	*	OMB 256 KB (100000H-13FFFFH)
1	0	0	0	0	0	1	OMB 1MB (100000H-1FFFFFH)
1	0	0	0	0	0	0	1.25MB (100000H-23FFFFH)
1	0	0	0	0	1	1	2MB (100000H-2FFFFFH)
1	0	0	0	1	0	1	2.25MB (100000H-33FFFFH)
1	0	0	0	1	0	0	3MB (100000H-3FFFFFH)
1	0	0	0	1	1	1	3.25MB (100000H-43FFFFH)
1	0	0	1	*	*	1	3MB (100000H-3FFFFFH)
1	0	0	1	*	*	0	3.25MB (100000H-43FFFFH)
1	0	1	0	*	*	1	3MB (100000H-3FFFFFH)
1	0	1	0	*	*	0	3.25MB (100000H-43FFFFH)
1	0	1	1	*	*	1	3MB (100000H-3FFFFFH)
1	0	1	1	*	*	0	3.25MB (100000H-43FFFFH)
1	1	*	*	*	*	*	512KB (100000H-17FFFFH)

* : don't care

*PCS3EN is the bit employed to specify the usage of the 256KB area within the standard RAM which may be used as a private area when "1" and as an EMS control area when "0".

(c) EMS area

To turn on the EMS, EMSEN of the EMSSTAT register must be set to "1". To support the EMS version 4.0, the EMSADR register and the EMSDAT register are provided as internal registers, whose bit definition is shown next.

EMSADR register

Bit	Signal name	Significance
0-7	EMSADR0-7	EMS mapping register address

EMSDAT register

Bit	Signal name	Significance
0-7	EMSDAT0-7	EMS mapping register data
8-14	—	Undefined. Reads "0" at all times.
15	EMSPEN	EMS page enable bit

The EMS control register for the EMSADR register, EMSDAT register, including the EMSSTAT register, is I/O address allocated by SW0-2 of the EMSSTAT register, which are set as shown in the table.

SW2	SW1	SW0	EMSSTAT	EMSADR	EMSDATL	EMSDATH
0	0	0	208H	209H	20AH	20BH
0	0	1	218H	219H	21AH	21BH
0	1	0	248H	249H	24AH	24BH
0	1	1	258H	259H	25AH	25BH
1	0	0	268H	269H	26AH	26BH
1	0	1	2A8H	2A9H	2AAH	2ABH
1	1	0	2B8H	2B9H	2BAH	2BBH
1	1	1	2E8H	2E9H	2EAH	2EBH

When reset, SW0-2 are reset to "0".

The EMSADR register is a 8-bit read/write register which is employed to point the 34 EMS mappings using EMSADR2-7. EMSADR2-7 is automatically incremented when the high side of the EMSDAT register is accessed. "0" is always read from EMSADR0-1 and write is ignored.

The following shows the address setup range for the EMSADR register

40H, 44H, 48H, 4CH, 50H, 54H, 58H, 5CH, 60H, 64H, 68H, 6CH, 70H, 74H, 78H, 7CH, 80H, 84H, 88H, 8CH, 90H, 94H, 98H, 9CH, C8H, CCH, D0H, D4H, D8H, DCH, E0H, E4H, E8H, ECH,

The EMSDAT register is a 16-bit read/write register and there are 34 sections. The EMS mapping data is set in EMSDAT0-7 of the EMSDAT register and determines the page that mapped to the window of address space of 040000H-09FFFFH and 0C8000-0EFFFFH. Window can be set on or off for EMSPEN; sets on when "1" an. EMSDAT8-14 are read "0" at all times and write is ignored.

When the EMSADR register is out of the setup address range, EMSDAT0-15 is read "0" and write is ignored.

The EMS control area equals to the memory controller supported all memory but the system area and the private area, of which capacity is a maximum 3.75MB when the private memory is not used (*PCS3EN=0).

The following shows the mapping of the EMS control area.

"C" represents conventional memory mapping, "X" extended memory mapping, and "P" expanded memory mapping. "nnnnnnH" is depends to the extended area setting, "mmmmmmH" to the actually installed memory capacity.

The actually installed memory capacity may be set to "nnnnnnH" when mapping the conventional memory. For an example, the extended area for the 4MB memory, it should be set to 3.25MB and "nnnnnnH" is 3DFFFFH (in case *PCS3EN=0).

When mapping the EMS memory, the capacity under the actual memory capacity should be set to "nnnnnnH". For the 4MB of actually installed memory, the EMS area should be set to 0-3.25MB. If 0MB was set, all are mapped as the EMS memory.

4.13.3. Private area

It may be possible with the internal I/O register setting to reserve a 256KB private area out of the memory controller supported 4MB memory.

To reserve the private area, set *PCS3EN of the PSRAMCF register to "1" and set 256KB of the internal standard RAM as the private memory. Set EMSEN of the EMSSTAT register to "0" and PVTMEM of the PSRAMCF register to "1", which is then mapped to the address space of 0E0000H-0EFFFFH.

To access the 256KB private memory, four banks must be selected using MAP0-1 of the PSRAMCF register.

4.14. Port-B

The port-B consists of a logic gate which is used for NMI occurrence control, speaker output control, and refresh detection by the parity and I/O channel checks.

4.15. Sharp original port

To access the Sharp original port, I/O addresses 07CH and 07DH are used. First, set the pointer to 07CH port and read and write the pointer specified port with 07DH. Unless the pointer is set with 07CH, it may not permit to access the Sharp original port of 07DH. Once 07DH has accessed, it needs to set the pointer again.

See the table below for the Sharp original port used by this chip.

Pointer address	Register name	R/W
01H	SIOCFR (SIO Configuration Register)	R/W
02H	PRICNT (Peripheral Control Register)	W/O
03H	MDMCFR (Modem Configuration Register)	R/W
04H	EMSCFR (EMS Configuration Register)	R/W
05H	PSRAMCF (PSRAM Configuration Register)	R/W
06H	PWRCNT (Power Control Register)	R/W
07H	ATSTBY (Auto Stand-by Control Register)	R/W
08H	PWRSTAT (Power Status Register)	R/O
09H	PWRTIM (Power Save Timer Register)	R/W
0AH	RSMTIM (Auto Resume timer Register)	R/W
0BH	RSMCNT (Resume Control Register)	R/W
0CH	RSTFCT (Reset Factor Register)	R/O
0DH	EXSTAT (Expansion Unit Status Register)	R/O
0EH	VGACNT (VGA Control Register)	R/W
0FH	NMIFCT (MNI Factor Register)	R/O

Chips port map (Si)

[1] Access method

① Write the pointer address in the I/O address 22H.

② Read or write the data in the I/O address 23H.

After the 23H has accessed, it may not permit to access the pointer again unless the pointer is set again.

SIGNAL DESCRIPTIONS

The block diagram in Figure 9-5, shows the pin connection with the major internal functions of the MC146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{DD}, V_{SS}

DC power is provided to the part on these two pins, V_{DD} being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2—TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant.

AT cut crystal at 4.194304 MHz or 1.048576 MHz frequencies.

CKOUT—CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 9-3.

CKFS—CLOCK OUT FREQUENCY SELECT, INPUT

When the CKFS pin is tied to V_{DD} it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

Table 9-3. Clock output frequencies

SQW—SQUARE WAVE, OUTPUT

The SQW pin can output a signal from one of the 15 taps provided by the 22 internal-divider stages. The frequency of the SQW may be altered by programming Register A. The SQW signal may be turned on and off using the SQWE bit in Register B.

AD0—AD7—MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the MC146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the MC146818 latches the address from AD0 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or WR pulses. In a read cycle, the MC146818 outputs eight bits of data during the latter portion of the DS or RD pulses, then ceases driving the bus (returns the output drivers to the high-impedance state) when DS falls in the Motorola case of MOTEL or RD rises in the other case.

AS—MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the MC146818. The automatic MOTEL circuit in the MC146818. The automatic MOTEL circuit in the MC146818 also latches the state of the DS pin with the falling edge of AS or ALE.

DS—DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/O}$ emanating from the competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the MC146818, latches the state of the DS pin on the falling edge of AS/ALE. When the Motorola mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the Motorola multiplexed bus processors. To ensure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

R/W—READ/WRITE, INPUT

The MOTEL circuit treats the R/W pin in one of two ways. When a Motorola type processor is connected, R/W is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/W while DS is high, whereas a write cycle is a low on R/W during DS.

The second interpretation of R/W is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/O}$ from competitor type processors. The MOTEL circuit in this mode gives R/W pin the same meaning as the write (W) pulse on many generic RAMs.

$\overline{\text{CE}}$ —CHIP ENABLE, INPUT

The chip-enable ($\overline{\text{CE}}$) signal must be asserted (low) for a bus cycle in which the MC146818 is to be accessed. $\overline{\text{CE}}$ is not latched and must be stable during DS and AS (Motorola case of MOTEL) and during $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (in the other MOTEL case). Bus cycles which take place without asserting $\overline{\text{CE}}$ cause no actions to take place within the MC146818. When $\overline{\text{CE}}$ is high, the multiplexed bus output is in a high impedance state.

When $\overline{\text{CE}}$ is high, all address, data, DS, and R/W inputs from the processor are disconnected within the MC146818. This permits the MC146818 to be isolated from a powered-down processor. When $\overline{\text{CE}}$ is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{\text{CE}}$ when the main power is off. When $\overline{\text{CE}}$ is not used, it should be grounded.

$\overline{\text{IRQ}}$ —INTERRUPT REQUEST, OUTPUT

The $\overline{\text{IRQ}}$ pin is an active low output of the MC146818 that may be used as an interrupt input to a processor. The $\overline{\text{IRQ}}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{\text{IRQ}}$ pin, the processor program normally reads Register C. The $\overline{\text{RESET}}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{\text{IRQ}}$ level is in the high-impedance estate. Multiple interrupting devices may thus be connected to an $\overline{\text{IRQ}}$ bus with one pullup at the processor.

$\overline{\text{RESET}}$ —RESET, INPUT

The $\overline{\text{RESET}}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{\text{RESET}}$ pin must be held low for the specified time, t_{RLH} , in order to allow the power supply to stabilize.

When $\overline{\text{RESET}}$ is low the following occurs:

- a) Periodic Interrupt Enable (PIE) bit is cleared to zero.
- b) Alarm Interrupt Enable (AIE) bit is cleared to zero.
- c) Update ended Interrupt Enable (UIE) bit is cleared to zero.
- d) Update ended Interrupt Flag (UF) bit is cleared to zero.
- e) Interrupt Request status Flag (IRQF) bit is cleared to zero.
- f) Periodic Interrupt Flag (PF) bit is cleared to zero.
- g) The part is not accessible.

9-4. 82C455 VGA FLAT PANEL/CRT CONTROLLER DATA SHEET

- VGA-Compatible flat panel controller optimized for laptop computer applications.
- Supports CRT, LCD, Plasma and Electro-Luminescent displays of varying resolutions.
- Single chip implementation tightly couples to the CHIPS/250 and CHIPS/280 and interfaces with 8 and 16 bit PC bus and MCA (an interface compatible with the MicroChannel™).
- Up-to-40-MHz dot-clock-speed-for-graphics-and-text-modes.
- Can utilize an external palette DAC with up to 16 million colors.
- Provides intelligent backward compatibility to the EGA, CGA, Hercules™, and MDA on Flat Panel displays.

The 82C455 Graphics Controller provides a complete solution for implementing a Video Graphics Array-compatible controller. The 82C455 is supplied in a 144-pin PFP package. It can be used in 8 and 16-bit PC bus and in 16-bit MCA bus environments.

Display Types Supported

CGA, EGA, MDA, Multifrequency, IBM PS/2™ and other monitors can be used. The choice of flat panel displays includes EL, plasma, as well as single panel/single drive, dual panel/single drive and dual panel/double drive LCDs. Both gray scale and monochrome panels are supported; a proprietary frame rate control algorithm provides gray scale capability on monochrome panels.

CHIPS/250 and CHIPS/280 Interface

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective solution for PS/2 compatible systems. When used with one of these CHIPSets®, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

Backward Compatibility

The 82C455 is compatible with IBM's EGA, CGA and MDA, in addition to offering a Hercules monochrome-graphics-compatible mode. On-chip compensation registers permit software designed for low resolution displays to utilize the entire screen area on a flat panel with higher resolution.

Hardware Support for Context Switching

Multitasking and windowing environments can be implemented easily since all internal registers of the 82C455 can be read and written.

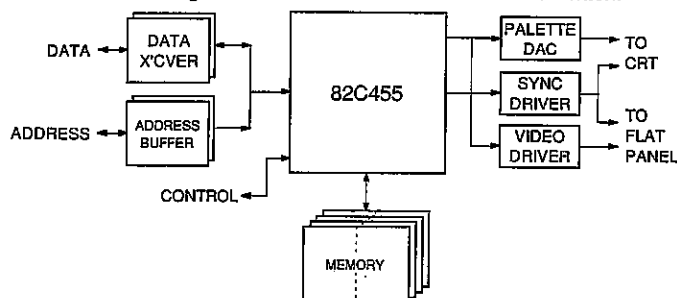


Fig. 9-7 82C455 System Implementation

82C455 Functional Description

The 82C455 offers a complete solution for implementing a VGA/MCGA/EGA/CGA/MDA/Hercules-compatible display system. By integrating all necessary logic the device ensures that total chip count for a VGA-compatible solution can be as low as 14 chips (includes 82C455, display memory, buffers and drivers).

Any one of a variety of CRT monitors or flat panel displays can be driven. Internal compensation registers ensure that industry-standard software designed for different displays can be executed on the single

flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software. The 256 Kbytes of display memory size is comprised of 8 64K*4 DRAMs. Display memory refresh is controlled by the 82C455; it is transparent to the CPU.

For support of multitasking environments and context switching, the entire state of the 82C455 (internal registers and latches) is readable and writeable. This feature is 100% compatible to IBM's VGA.

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations and generation of the necessary control signals.

The 82C455 contains 16 color palette registers. It also interfaces directly to an external Immos G171 (or compatible) color palette and D/A converter. Like the VGA, it is capable of display resolutions of 640*480 with 16 on-screen colors (internal palette) and 320*200 with 256 on-screen colors from an external palette of 256 thousand (or 16 million) colors. The 82C455 can also be programmed for higher resolutions up to 800*600 in 16 colors.

The 82C455 integrates four different modules as follows:

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies to the Attribute Controller display memory data for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and an attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access and contains mask registers which can prevent writes of individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and graphic modes the 4-bit pixel data acts as an index into a set of internal palette registers which generate a 6-bit stream. Two additional bits of color data are added if 256-color mode is enabled. Text blink, underline and cursor are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Pin Description Table

Flatpack Pin No.	Name	Type	Active	Description
63	AD0	I/O	Both	SYSTEM ADDRESS and DATA Bits 0-15. These bits are used to address display memory and the I/O mapped 82C455 internal registers. They also transfer data between the CPU bus and display memory and 82C455 registers. Addresses must be valid when output signal DATAEN is low and data must be held until \VGACMD (COMMAND) is low. Addresses are latched internally.
62	AD1	I/O	Both	
61	AD2	I/O	Both	
60	AD3	I/O	Both	
59	AD4	I/O	Both	
58	AD5	I/O	Both	
57	AD6	I/O	Both	
56	AD7	I/O	Both	
53	AD8	I/O	Both	
52	AD9	I/O	Both	
51	AD10	I/O	Both	
50	AD11	I/O	Both	
49	AD12	I/O	Both	
48	AD13	I/O	Both	
47	AD14	I/O	Both	
46	AD15	I/O	Both	
44	A16	I	Both	SYSTEM ADDRESS Bits 16-18 and AUXILIARY DATA Bits 0-2. These bits transfer a high-order address when DATAEN is low. The auxiliary data bits on pins A16, A17, and A18 respectively are read into Bits 0-2, respectively, of the DIP Switch register when that register is accessed by the CPU. The address bits are latched internally and are ignored for I/O cycles.
43	A17	I	Both	
42	A18	I	Both	
72	\BHE	I	Low	BYTE HIGH ENABLE and AUXILIARY DATA Bit. \BHE low indicates that the high order byte at the current word address is being accessed. If active, \BHE must be valid when DATAEN is low. The pin is also an auxiliary data input which is read into Bit 3 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This data bit is latched internally on the falling edge of \VGACMD (\IOR).
41	ADDHI	I	High	ADDRESS HI and AUXILIARY DATA Bit. This high order memory address enable input is generated external to the 82C455 by decoding system addresses A19-A23. As an address, it must be valid when DATAEN is low, is latched internally and specifies that the current memory address is valid for the 82C455. This pin is an auxiliary data bit read into Bit 4 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This input pin is ignored during I/O cycles.
67	DATAEN	O	High	DATA ENABLE. The DATAEN output controls external multiplexing of the system address/data bus. DATAEN low selects address and DATAEN high selects data. In an MCA interface, DATAEN is low when \VGACMD is high and DATAEN is high when \VGACMD is low. In a PC or PC/AT bus interface DATAEN is low when all \MEMR, \MEMW, \IOR, and \IOW are high. DATAEN is high when any one of \MEMR, \MEMW, \IOR or \IOW is low.
65	\RDLO	O	Low	READ LO. This output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address/data bus. It is low when data is read from the 82C455 and high when data is written to 82C455. DATAEN can be used to enable the external transceiver.
64	\RDHI	O	Low	READ HI. This output operates in a fashion identically to the \RDLO output except that it controls direction for the high order byte (Bits 8-15) of the address/data bus. RDHI is low when data is read from 82C455 and high when data is written to 82C455.
71	M/IO (AEN)	I	Both	MEMORY/IO or ADDRESS ENABLE and AUXILIARY DATA input. In MCA interfaces, the M/IO input pin selects either a memory or an I/O transfer. M/IO high selects a memory cycle and low selects an I/O cycle. When defined as M/IO, it must be valid when the DATAEN input is low. In PC-Bus interfaces, this input is renamed AEN. When low, it indicates a valid I/O address when DATAEN is low. The M/IO (AEN) signal is latched internally. In both MCA and PC-Bus environments this pin serves as an auxiliary data bit input. It is read into Bit 5 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
69	\S0 (\MEMW)	I	Low	S0 or MEMORY WRITE. \S0 is the memory and I/O write input from the MCA bus. In PC-Bus interface applications, this input is named \MEMW. It must be low for CPU writes to display memory.
70	\S1 (\MEMR)	I	Low	S1 or MEMORY READ. \S1 is the memory and I/O read input from the MCA bus. In PC-Bus interface applications, this input is named \MEMR. It must be low to permit the CPU to read display memory.
79	\VGASETUP (\IOW)	I	Low	VGA SETUP or I/O WRITE. In an MCA environment this active low \VGASETUP input allows configuration registers at I/O Addresses 100-104h to be accessed. All other memory and I/O functions are disabled. In PC-BUS interface applications, this input is named \IOW. It must be low to permit the CPU to write to an 82C455 I/O register.
68	\VGACMD (\IOR)	I	Low	VGA COMMAND or I/O READ. In an MCA environment this active low \VGACMD indicates a command bus cycle. \VGACMD must not be asserted during system memory refresh cycles. In a PC-Bus environment this input is named \IOR. It must be low to permit the CPU to read an I/O register.

Table 9-4 (a)

Flatpack Pin No.	Name	Type	Active	Description															
80	VGAENAB (REFRESH)	I	High/Low	VGA ENABLE or REFRESH and AUXILIARY DATA. In an MCA environment this active high VGAENAB input signal enables memory and I/O accesses. In the PC-Bus interface, REFRESH high indicates a valid memory cycle. This pin also serves as an auxiliary data bit input which is read into Bit 6 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.															
78	VGAREQ (IOSC16)	O	Low	VGA REQUEST or I/O SELECT 16. In an MCA environment this output indicates that a FAST memory cycle can be executed (this feature can be disabled through a register). In a PC-Bus environment this active low \IOSC16 signal indicates a valid 16 bit I/O cycle.															
74	VGARDY	O	Low	VGA READY. when low this output indicates that the current CPU read/write cycle must be extended with wait states.															
77	VGADS16 (MEN16)	O	Low	VGA ADDRESS SELECT 16 or MEMORY ENABLE 16. In an MCA environment this active low VGADS16 output indicates that a 16-bit memory or I/O transfer cycle is occurring. In a PC-Bus environment this active low \MEN16 signal indicates a 16-bit memory cycle transfer is enabled. This signal should be used in external logic to decode the high order address and generate \MEMCS16 for the PC-AT bus.															
75	VGAACK (WR46E8)	O	Low	VGA ACKNOWLEDGE or WRITE-46E8h. In an MCA environment this active low \VGAACK output indicates a valid CPU access (memory and I/O) to the 82C455. In a PC-Bus environment this active low \WR46E8 signal indicates a valid I/O write to address 46E8h.															
113	VGAINT	O	Either	VGA INTERRUPT. This pin is asserted whenever the vertical sync signal goes active. This pin can be configured to be active high (EGA) or active low (VGA) through the Emulation Mode register (XR14).															
114	RESET	I	High	RESET. An active high input which resets the 82C455.															
38	TEST	I	High	TEST. This input is used for factory testing only. It should be tied low.															
40 111	PWRDN2 PWRDN1	I I	Both Both	POWER DOWN 2, 1. The POWER DOWN input pins select the Normal, Relax, and Retire modes of operation as follows: <table><tr><td>PWRDN2</td><td>PWRDN1</td><td>OPERATION</td></tr><tr><td>0</td><td>0</td><td>Normal Operation</td></tr><tr><td>0</td><td>1</td><td>Relax Mode</td></tr><tr><td>1</td><td>0</td><td>Retire Mode</td></tr><tr><td>1</td><td>1</td><td>Illegal</td></tr></table>	PWRDN2	PWRDN1	OPERATION	0	0	Normal Operation	0	1	Relax Mode	1	0	Retire Mode	1	1	Illegal
PWRDN2	PWRDN1	OPERATION																	
0	0	Normal Operation																	
0	1	Relax Mode																	
1	0	Retire Mode																	
1	1	Illegal																	
105 104 103	CLK0 CLK1 CLK2	I I I	Both Both Both	CLKCK 2-0. Video Clock inputs. One of these dot clock inputs is selected by the Miscellaneous Output Register.															
101	MCLK	I	Both	MASTER CLOCK. This clock input is used to sequence internal 16-bit I/O cycles.															
108	SENSE	I	Both	SENSE. The state of this input pin can be read in Input Status Register 0, Bit 4.															
100	\PALRD	O	Low	PALETTE READ. This output is active low during an I/O read to an address in the range 3C6-3C9h and is connected to the Read input of an external Immos G171 Palette/DAC.															
99	\PALWR	O	Low	PALETTE WRITE. This output is active low during an I/O write to an address in the range 3C6-3C9h and is connected to the Write input of an external Immos G171 Palette/DAC.															
142 3 7 12 16 24 28 33	M0D0 M0D1 M0D2 M0D3 M0D4 M0D5 M0D6 M0D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 0 DATA. Display memory data bus for Plane 0 (Map 0).															
144 5 10 14 22 26 31 35	M1D0 M1D1 M1D2 M1D3 M1D4 M1D5 M1D6 M1D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 1 DATA. Display memory data bus for Plane 1 (Map 1).															
115 118 120 122 124 128 130 132	M2D0 M2D1 M2D2 M2D3 M2D4 M2D5 M2D6 M2D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 2 DATA. Display memory data bus for Plane 2 (Map 2).															

Table 9-4 (b)

Flatpack Pin No.	Name	Type	Active	Description
116 119 121 123 125 129 131 133	M3D0 M3D1 M3D2 M3D3 M3D4 M3D5 M3D6 M3D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 3 DATA. Display memory data bus for Plane 3 (Map 3).
143 4 8 13 21 25 29 34	AA0 AA1 AA2 AA3 AA4 AA5 AA6 AA7	O O O O O O O O	Both Both Both Both Both Both Both Both	ADDRESS PLANES 0, 1. Display memory address bus for DRAM planes 0 and 1.
141 2 6 11 15 23 27 32	BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7	O O O O O O O O	Both Both Both Both Both Both Both Both	ADDRESS PLANES 2, 3. Display memory address bus for DRAM Planes 2 and 3.
20	\RAS	O	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	\CAS0	O	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	\CAS1	O	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	\CAS2	O	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	\CAS3	O	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.
139	\WE	O	Low	WRITE ENABLE. Active low write enable signal for all display memory banks/planes.
97	HSYNC	O	Both	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (Bit 6 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the horizontal polarity bit is high.
98	VSNC	O	Both	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (Bit 7 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the vertical polarity bit is high.
96	BLANK	O	Both	BLANK is a programmable output for blanking the CRT or Flat Panel. Its polarity is programmable. It can be redefined as the Display Enable signal.
85 86 87 88 89 93 94 95	VIDEO0 VIDEO1 VIDEO2 VIDEO3 VIDEO4 VIDEO5 VIDEO6 VIDEO7	O O O O O O O O	Both Both Both Both Both Both Both Both	VIDEO 0-7. Eight video outputs to drive a color or monochrome display devices. Color values for digital CRT interface are assigned as follows: Video0 B Blue Video1 G Green Video2 R Red Video3 BS/V Secondary Blue/Monochrome Video4 GS/I Secondary Green/Intensity Video5 RS Secondary Red Video6 User Defined Video7 User Defined
92	SHIFTCLK	O	High	SHIFT CLOCK. Output pixel clock to which video output data is synchronized.
83	WGTCLK	O	High	WEIGHT CONTROL CLOCK. Gray scale reference clock for Panels with Pulse Width Modulation support.
17	ACDCLK	O	High	LCD CLOCK. A 50% duty cycle square-wave with programmable period. Used to back bias LCD panels.
140	\ERMEN	O	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C455 to refresh the display. A high indicates display device access and a low is CPU access. This signal can be redefined as a general purpose output.
112	\TRAP	O	Low	TRAP. This active low output indicates a TRAP condition requiring special CPU assistance. It can be redefined as a general purpose output pin.
82	PTMC	I	Both	PTMC. this input selects the type of CPU interface. PTMC low selects an MCA interface and high selects a PC-Bus interface. This input must always be valid.

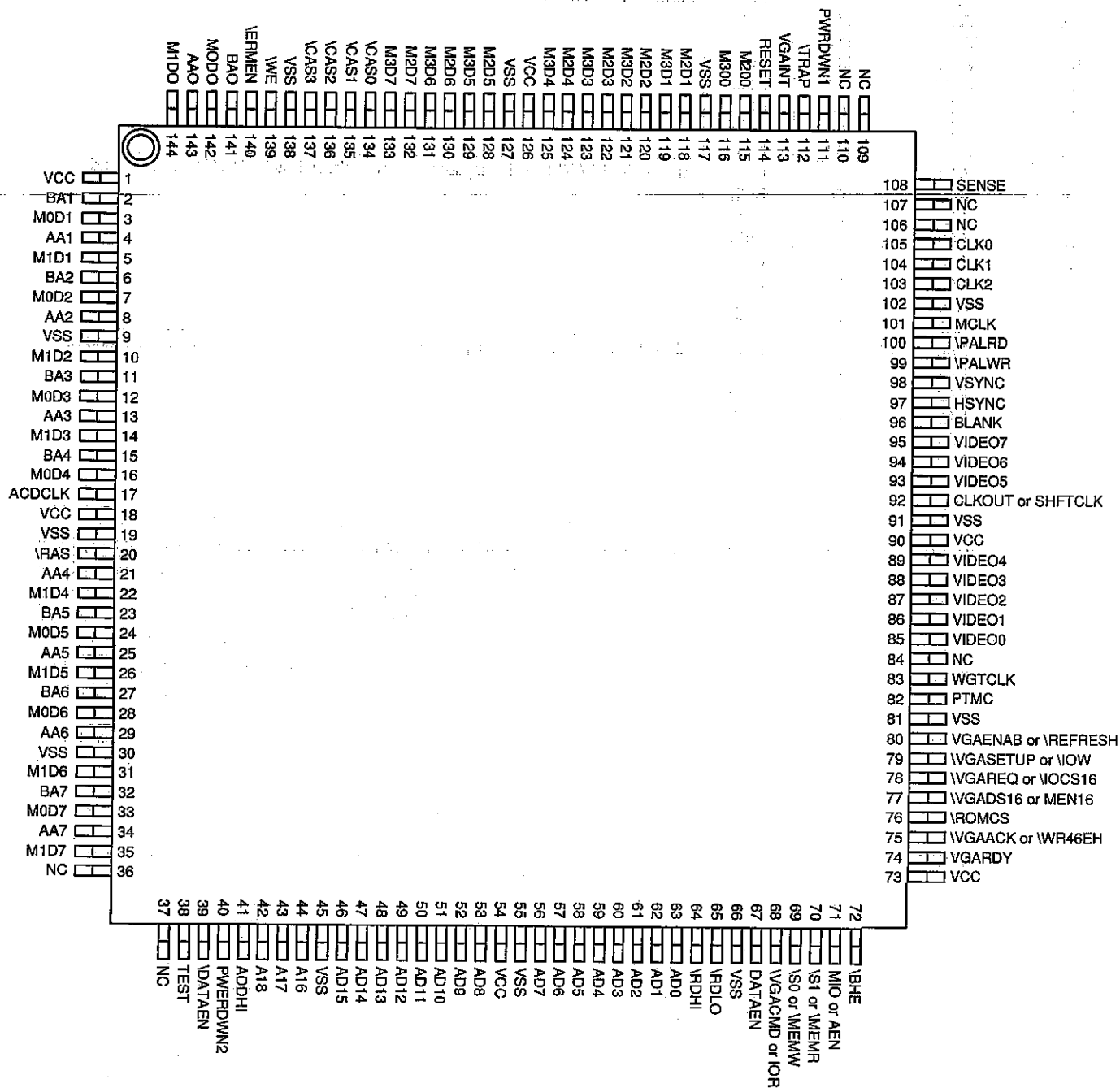


Fig. 9-8 Top view

9-5. μ PD80C42 Universal peripheral interface

Features

- Instruction cycle: 1.25 μ s/12MHz
- Program memory (ROM): 2K x 8 bits
- Data memory (RAM): 128 x 8 bits
- I/O port: 2 x 8 bits
- Async slave master interface
 - Two data registers (DBBIN,, DBBOUT)
 - 8-BIT STATUS
- Internal timer/counter: 8 bits
- A pair of working registers
- 8-level stack
- Internal clock oscillation circuit
- Interrupt function
- DMA function
- Expandable I/O port
- Single step operation

Block diagram

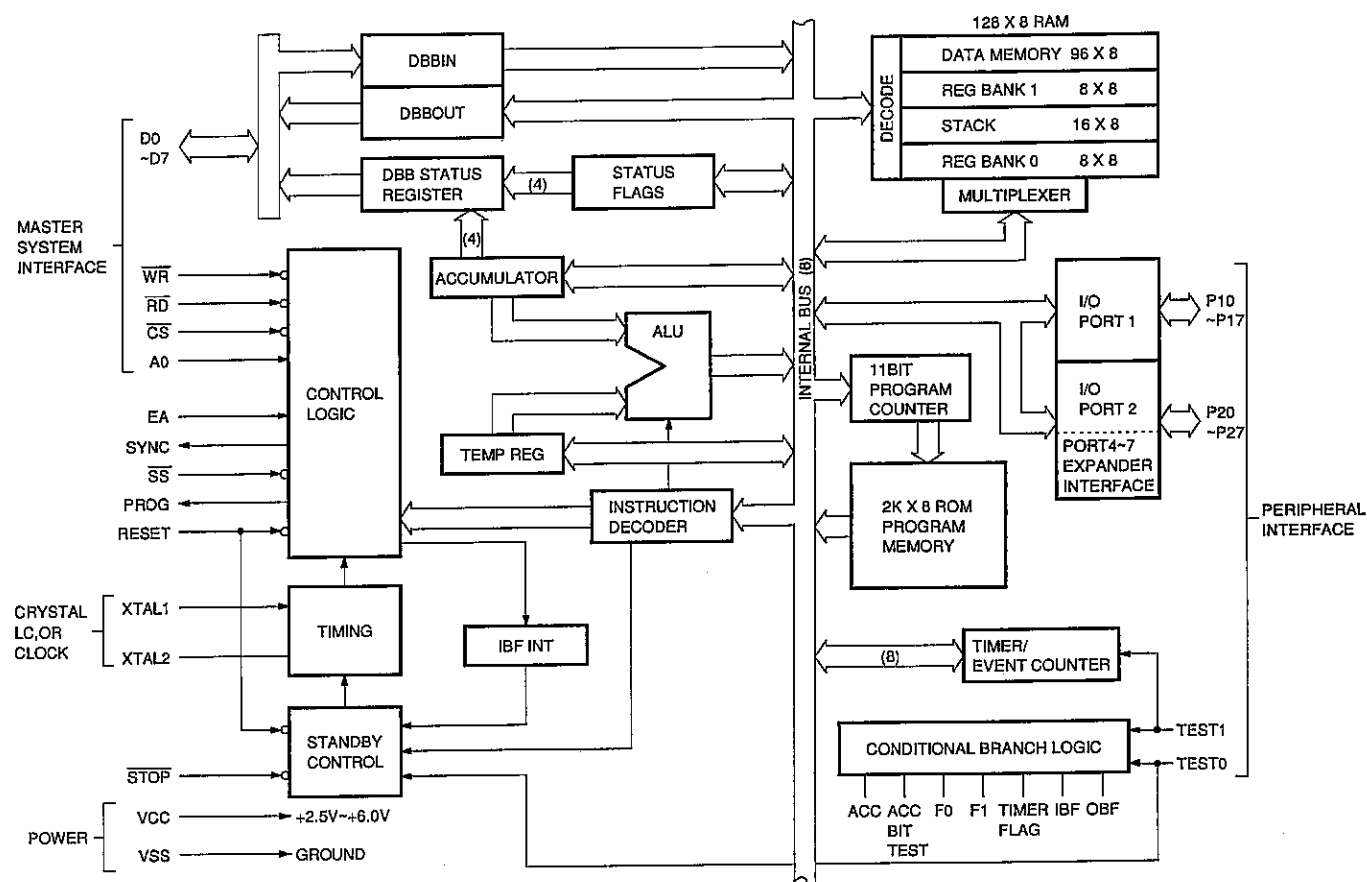


Fig. 9-9

9-6. TC51128AFL-80 CMOS PSEUDO-STATIC RAM (131,072 WORDS X 8 BITS)

General

The TC51128AFL is a single 5V operated 131,072 words x 8 bits pseudo-static RAM. It realized a large capacity, high speed, and low power dissipation by a combination of single transistor type dynamic memory cell and peripheral CMOS static circuit. With the TC51128AFL, auto refresh and self-refresh can easily be achieved with $\overline{\text{RFSH}}$ input, and, similar as an async static RAM, the R/W input is accepted at a low to high transition of R/W , which enhances easier interface with microcomputer.

The TC51128AFL is pin compatible with 1MB static RAM (JEDEC standard) and a package of 0.3" wide, 32-pin SOP mini-flat static package is used.

Refresh can be done by selecting 512 address (A0-A8) within 8ms.

Features

tCEA	Access time	80ns
tOE	$\overline{\text{OE}}$ access time	35ns
tRC	Cycle time	130ns
P _D	Operating power dissipation	385mW
	Self-refresh current	1mA/220μA

- Large capacity: 131,072 words x 8 bits
- High speed, low power dissipation
- Single 5V supply: $5V \pm 10\%$
- Auto refresh possible by the internal counter
- Self-refresh possible by the internal counter
- All input/output are TTL compatible
- 512 refresh cycle/8ms
- Adoption of the auto refresh power down function
- Pin compatible with 1M static RAM (JEDEC standard)
- 32-pin mini-flat package

Pin configuration

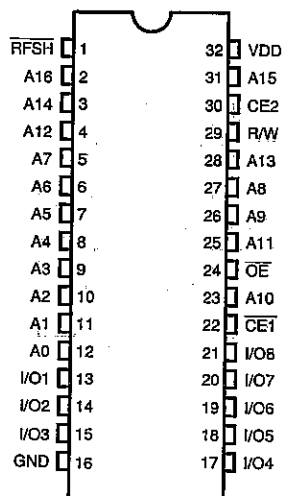


Fig. 9-10

Pin name

A0-A16	Address input
R/W	Read/write input
$\overline{\text{OE}}$	Output enable input
$\overline{\text{RFSH}}$	Refresh input
$\overline{\text{CE1}}, \overline{\text{CE2}}$	Chip enable input
I/O1-I/O8	Data input/output
V _{DD}	Power supply
GND	GND

Block diagram

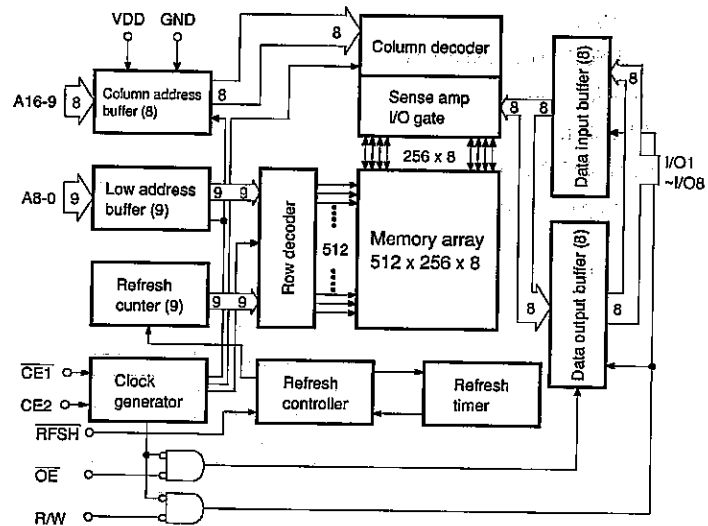


Fig. 9-11

9-7. SC9871 DMAC

9-7-1. DMAC general description

The DMAC function is stored in the SC9871.

Two 8237 DMACs are contained in this controller which supports 7 DMA channels. The DMA controller-1 operates as a slave to carry out the DMA transfer for CH0~3 in byte increment. The DMA controller-2 operates as a master to carry out the DMA transfer for CH4~7 in 16-bit increment. CH4 is used for the cascade connection. The rate transferred at a time is 64KB for CH0~3 and 128KB for CH4~7. The transfer area is 16MB whose high order area is set to the page register within the superintegration.

Channel allocation

CH0 : I/O slot

CH1 : I/O slot

CH2 : Floppy disk + I/O slot

CH3 : I/O slot

CH4 : For cascade connection

CH5 : I/O slot

CH6 : I/O slot

CH7 : I/O slot

I/O address

Described next is I/O address.

00H : CH0 base, current address

01H : CH0 base, current address

02H : CH1 base, current address

03H : CH1 base, current address

04H : CH2 base, current address

05H : CH2 base, current address

06H : CH3 base, current address

07H : CH3 base, current address

08H : DMAC 1 command, status register

09H : DMAC 1 request register

0AH : DMAC 1 single mask register

0BH : DMAC 1 mode register

0CH : DMAC 1 clear byte point register

0DH : DMAC 1 master clear

0EH : DMAC 1 clear mask register

0FH : DMAC 1 all mask register

C0H : CH4 base current address

C2H : CH4 base current address

C4H : CH5 base current address

C6H : CH5 base current address

C8H : CH6 base current address

CAH : CH6 base current address

CCH : CH7 base current address

CEH : CH7 base current address

D0H : DMAC 2 command, status register

D2H : DMAC 2 request register

D4H : DMAC 2 single mask register

D6H : DMAC 2 mode register

D8H : DMAC 2 clear byte point register

DAH : DMAC 2 master clear

DCH : DMAC 2 clear mask register

DEH : DMAC 2 all mask register

DMAC 1 address and count must be set in increment of a byte. The address of DMAC 2 is possible for DMA due to a 16-bit word environment and a half of the actual address is used to set.

Page register

87H : DMAC CH0 page address

83H : DMAC CH1 page address

81H : DMAC CH2 page address

82H : DMAC CH3 page address

8BH : DMAC CH5 page address

89H : DMAC CH6 page address

8AH : DMAC CH7 page address

8FH : High address during DRAM refresh

80H : MFG port

84, 85, 86, 88, 8C, and 8EH are reserved.

In the page register is set the DMA address A23~16. But, for the DMAC 2, the LSB of the page register is insignificant because the DMAC is an output for A16.

DREQ/DACK signal are connected to the I/O slots, but, the internal FDC is connected for the channel 2 of the slave when the bit 3 of the 3F3H/372H port is at "1".

9-7-2. DMAC block diagram (SC9871)

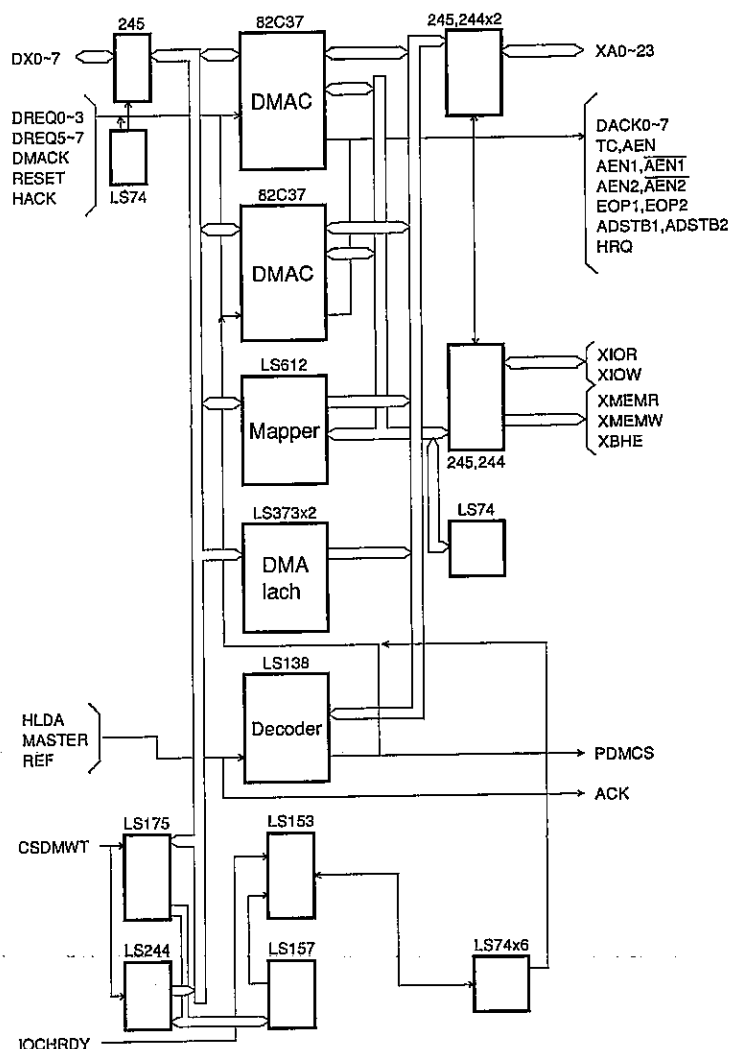


Fig. 9-13

9-7-3. Configuration register

Can be accessed when the register number is set in the configuration register 22H and the set value is outputted to the address 23H.

- 22H: Register number (write only)
- 23H: Value to be set in the register (read/write possible).

There are some registers provided, but explanation will be given here for the register number 01H which is DMAC related.

Register number 01H (read/write port)

7							0
X	X	16W1	16W0	8W1	8W0	X	X

Default ALL "0"

The register to which set the DMA wait control.

Table

Set value		DMAC 2 waits
16W1	16W0	
0	0	1 wait
0	1	2 waits
1	0	3 waits
1	1	4 waits

Set value		DMAC 1 waits
8W1	8W0	
0	0	1 wait
0	1	2 waits
1	0	3 waits
1	1	4 waits

DMAC 2 is for 16-bit transfer (master DMAC)

DMAC 1 is for 8-bit transfer (slave DMAC)

9-7-4. SC9871 DMAC signal descriptions

PIN No.	NAME	I/O	Function
1-5	TXA0-5		Not used.
6-7	XA0-1	B	System address bus
9-15	XA2-8	B	
17	XA9	B	
18-24	XA10-16	0	
26-32	XA17-23	0	
33-36	DACK0-3	0	Response to 8-bit transfer request for DREQ0-3.
37	DACK4	0	Not used.
38-40	DACK5-7	0	Response to 16-bit transfer request for DREQ5-7.
42	AEN	0	Not used.
43	AEN1	0	Not used.
44	AEN2	0	Not used.
45	AEN1B	0	Address enable
46	AEN2B	0	Not used.
47	ADSTB1	0	Not used.
48	ADSTB2	0	Not used.
49	EOP1	0	Not used.
50	EOP2	0	Not used.
51	TC	0	DMA complete signal
52	HRQ	0	Hold request, to system gate array
53	HRQ	0	Not used.
54	ACK	0	Not used.
55	TEST	I	Fixed LOW
56	GATERDY	0	Not used.
58	XIOR	B	I/O read
59	XIOW	B	I/O write
60	TXIOR		Not used.
61	TXIOW		Not used.
62	XBHE	0	Byte high enable
63	XD0	B	System data bus
65-71	XD1-7	B	
73-80	TXD0-7		Not used.
81	XMEMR	0	System bus memory read MEMRC
82	XMEMW	0	System bus memory write MEMWC
83	TEST CK	I	Fixed LOW
84	TSTNORT	I	Fixed HIGH
85	IOCHRDY	I	AT bus IOCHRDY signal
86	CSDMWT	I	Indicates the configuration register access inside the DMAC that indicates the 23H is accessed following to 22H 01.
87	REF	I	Indicates the refresh cycle.
88	MASTER	I	AT bus master signal input. Indicates that the AT bus has become the bus master.
89	RESET	I	Reset
91-94	DREQ0-3	I	8-bit DMA request signal
95-97	DREQ5-7	I	16-bit DMA request signal
98	DMACLK	I	4MHz DMA clock
99	HACK	I	Hold acknowledge
100	HLDA	I	CPU HLDA signal that indicates that the CPU released the bus.

9-8. LZ95H25

9-8-1. General

The VGA, and printer interface are contained in a single chip for the PC-6500.

- (1) DOS-ROM interface
Supports the same features as the ROM board.
- (2) VGA interface
Creates the memory and I/O chip select signals.
- (3) Printer interface
Supports the parallel port functions of the IBM serial/parallel board. Ports 1 and 2 are set by the Sharp original port.
- (4) 8042 hard disk interface select signal generation
- (5) Floppy interface
Floppy drive select signal generation clock switching
- (6) Others
Drive select signal generation
Key board select signal generation
CRT display select signal generation
Drive access LED internal/external key selection
Hold signal for 80C286 generation
HLDA signal for SC9889B generation

9-8-2. I/O address

The following I/O ports exist in the gate array.

- ① Sharp original port
- ② DOS-ROM interface port
- ③ Printer interface port
- ④ Hard disk interface, 8042 decoder
- ⑤ FDD control signal port

See the table next for the relationship between address and port

AEN	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX	
1	X	X	X	X	X	X	X	X	X	X	XXX	Not selected
0	0	0	0	1	1	1	1	1	0	0	7C	Sharp port pointer (WO)
0	0	0	0	1	1	1	1	1	0	1	7D	Sharp port data (R/W)
0	0	1	#	#	#	#	1	0	0	0	1#8	DOSROM port pointer (WO)
0	0	1	#	#	#	#	1	0	0	1	1#9	DOSROM port data (R/W)
0	0	1	#	#	#	#	1	0	1	0	1#A	DOSROM port reserved (R/W)
0	0	1	#	#	#	#	1	0	1	1	1#B	DOSROM port ID (R/W)
0	1	\$	0	1	1	1	1	0	0	0	\$78	Printer port data (R/W)
0	1	\$	0	1	1	1	1	0	0	1	\$79	Printer port status (RO)
0	1	\$	0	1	1	1	1	0	1	0	\$7A	Printer port control (R/W)
0	1	1	1	1	0	0	1	1	1	0	3CE	VGA port
0	1	1	1	1	0	0	1	1	1	1	3CF	VGA port
0	0	0	0	1	1	0	0	X	0	0	60, 64	-CS8042 signal output
0	0	1	%	1	1	1	0	X	X	X	1F0~7	-HDCS0 signal output
0	1	1	%	1	1	1	0	1	1	X	3F6,7	-HDCS1 signal output
0	1	1	1	1	1	1	0	0	1	0	3F2	FDD select signal output
0	1	1	1	1	1	1	0	1	1	1	3F7	FDD port data (R/W)
0	1	1	1	1	1	1	0	X	X	X	3F0~7	-SELIFDD signal output

#: Set by the Sharp original port 12H.

\$: Set by the Sharp original port 02H.

?: Set by the Sharp original port 02H.

X: Don't care

9-8-3. Sharp original port

① Access method

After setting the register number in the pointer port of 7CH, make access through 7DH. For the pointer of 7CH is cleared after the data port of 7DH is accessed, the register number needs to be set to the pointer port of 7CH again in order to access the data port of 7DH once more.

② Register 01H [W/O]

Read port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*								Not Used
		*							-LCD, CRT
			*						-INTKEY
				*					SIO SEL (Not used in this GA)
					*				SIO EN
						*			FDD SEL 2 (Not used in this GA)
							*		FDD SEL 1 (Not used in this GA)
								*	FDD SEL 0

-LCD, CRT 0: LCD MODE 1: CRT MODE

-INTKEY 0: INTERNAL KEYBOARD ENABLE
1: INTERNAL KEYBOARD DISABLE (IF EXTERNAL KEYBOARD INSTALLED)

SIO EN 0: INTERNAL SIO ENABLE
1: INTERNAL SIO DISABLE
SIO_EN can also be changed by the register 2.

FDD SEL This register can be read from
0: Drive A is INT-FDD STRX pin, Drive B is EXT-FDD
1: Drive A is EXT-FDD, Drive B is INT-FDD

② Register 02H [R/W] Write port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*								HD EN
		*							HD SEL
			*						SIO EN
				*					SIO SEL (Not used in this GA) @
					*				PRT EN
						*			PRT SEL
							*		IMS EN (Not used in this GA) @
								*	IMS SEL(Not used in this GA) @

HD EN 0: HD port enable 1: HD port disable

HD SEL 0: Primary setting 1: Secondary setting

PRT EN 0: Printer port enable 1: Printer port disable

PRT SEL 0: Port 1 setting
(378H~37AH) 1: Port 2 setting
(278H~27AH)

SIO EN 0: Internal SIO enable 1: Internal SIO disable See register 1.

NOTE @: A bit exists in the register.

③ Register 0EH [W/O] Read port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					PRINTER BUSY CONTROL
					*	*			PWRDWN2, PWRDWN1 (Not used in this GA)
							*		VGA_EN

VGA_EN 0: Internal VGA enable 1: Internal VGA disable

Printer busy control 0: Normal, busy in the status port indicates the state of the line.
1: Forced to the busy state by the strobe and cancelled by -ACK.

④ Register 11H [R/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Reserved. PRINTER PORT (Not used) @ * FDD/PRN

FDD/PRN 0: 25 pin DSUB connector is used as FDD
1: 25 pin DSUB connector is used as PRINTER

NOTE @: Treat this bit as reserved.

⑤ Register 12H [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Reserved. ID2SW3~0

ID2SW3~0: The value "X" is set for the port address 1X8~BH.

⑥ The register 14~1FH is kept for software address.

9-8-4. DOSROM port (Not used)

① Access method

After the register number is set to the pointer port of 1X8H, access is made through 1X9H.

Existence of the DOSROM port is recognized by the 1XBH port.
The value "X" is set by the Sharp original port (pointer 12).

② Register group

Pointer register (1X8H)	Data register (1X9H)
00h	Memory data read/write
01h	Chip select register
02h	Memory mapper register
03h	Address register 1
04h	Address register 2
05h	Address register 3

Control register: 1XAH

ID register: 1XBH

③ Explanation of register

◦ Pointer register: 1X8H

BIT	7	6	5	4	3	2	1	0	
				*	*	*	*	*	Data register pointer Reserved. Test bit Reset

Data register The register to be accessed through the data register pointer 1X9H.

Test bit For counter clear, normally set to "0".

Reset 1: Same function as the hardware reset. The 1X9H related register keeps the reset state.
0: During normal operation

Reserved Normally set to "0"

NOTE: Since the pointer set is kept until written next, it needs no setting when the same register is to be read or written next.

◦ ROM data read: Pointer 00H [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory data

ROM data port when accessing the I/O.

Write is valid only when the RAM is installed.

◦ Chip select register: Pointer 01H

BIT	7	6	5	4	3	2	1	0	
	*		*	*	*	*	*	*	Chip select Reserved. Reserved @. Address auto increment

• Chip select

010: DOSROM1 (enabled only for 8-bit access)

011: DOSROM2 (enabled only for 8-bit access)

100: Reserved

101: Reserved

110: Reserved

111: Reserved

• Address auto increment

0: The contents of the address register are not incremented when the I/O is accessed.

1: The contents of the address register are incremented when the I/O is accessed.

NOTE: Set to 00H when reset.

NOTE @: A bit exists in the register.

◦ Memory map register: Pointer 02H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory base address 8/16 access Memory access enabled

Within the 1MB system address space, the base address is set for a 64KB window at a boundary of 16KB.

Setting is possible 010000~111100.

With the software,

101100 B0000~BFFFF (Disabled depending on the display mode)

110100 D0000~DFFFF

110101 D4000~E3FFF

110110 DS000~E7FFF

110111 DC000~EBFFF

111000 E0000~EFFFF 6 kinds of setting enabled

Disabled addresses are:

00XXXX 00000~3FFFF

C0000~CFFFF (disabled)

1111XX F0000~FFFFF

8/16 access

Selection is made whether the 64KB space set operate as an 8-bit memory or 16-bit memory.

0: Only 8-bit access is enabled.

1: 16-bit access is enabled.

Memory access enable/disable 0: Disable 1: Enable

NOTE: Set to 38H when reset and CPU is reset (test cycle detection of FEH to I/O 64H)

◦ Address pointer 1: Pointer 03H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Expansion address Reserved.

Expansion address, EA20~EA16 Specified which 64KB sector of a 2MB memory card is to be mapped to a window.

Reserved. Set to "0" when writing, and "0" when reading

NOTE: Set to 00H when reset.

◦ Address register 2: Pointer 04H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory address, AD15~AD08

Memory card address AD15~AD08 when accessing the ROM.

NOTE: Set to 00H when reset.

◦ Address register 3: Pointer 05H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory address

Memory card address AD07~AD00 when accessing the DOSROM.

The address registers 2 and 3 are auto incremented according to the setting when accessing I/O. (Subsequent address is turned to 0H when the contents of the address registers 2 and 3 are 0FFFFH and carry is not reflected to the address register 1. In the test mode, count increments at every digit.

NOTE: Set to 00H when reset.

◦ Control register 1XAH [R/W]

BIT	7	6	5	4	3	2	1	0	
	*								Serial in (not used)
		*	*	*	*				Reserved.
						*			IDMEME
							*		RESCPUE
								*	Serial out (not used)

RESCPUE 0: Reset CPU monitor enable

The 1X9 and 1XA registers within this gate array are reset when FEH is written in the address 64H.

1: Reset CPU monitor disable

The 1X9 and 1XA registers within this gate array are not reset when FEH is written in the address 64H.

IDMEME 0: Memory access enabled when ID changed.

1: Memory access disabled when ID changed.

Others Reserved.

NOTE: Set to 00H when reset.

◦ ID register: 1XBH

BIT	7	6	5	4	3	2	1	0	
	1	1	0	0	1	1	0	1	LSI code
	0	0	0	0	0	0	1	0	Board ID

LSI code and ID code are read alternately. The LSI code is read immediately after reset.

LSI code: CDH

Board code: 02H

Any board to be developed next will be allocated with 03H through 0FH.

When the board ID is written in the ID register, the board is enabled. If disabled, read/write to any register is not enabled.

* Recognition method

02H → ID register

ID register read x 2 OCDH&02h → Yes → interface exists

9-8-5. Printer port

The printer port consists of three internal ports and external input/output. The board address can be selected using the Sharp port bit PRT_EN and PRT_SEL, as shown in the table below.

PRT_EN	PRT_SEL	I/O address	Port name
1	X	Not selected	
0	0	37xH	Printer port 1
0	1	27xH	Printer port 2

◦ Print data (I/O address, 378H/278H) [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Printer output data

◦ Printer status (I/O address, 379H/279H) [R/O]

BIT	7	6	5	4	3	2	1	0	
	*								-BUSY
		*							-ACK
			*						PE
				*					SELECT
					*		*	*	-ERROR

-BUSY: Printer busy signal 0: Busy

-ACK: Printer acknowledge signal 0: Acknowledge

PE: Paper empty signal 1: Paper empty

SELF: Printer select signal. Selection of the printer is informed to the gate array. 1: Printer selected

-ERR: Printer error 0: Printer error.

A printer error is informed to the gate array.

x: Don't care.

◦ Printer control (I/O address, 37AH/27AH) [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Don't care
				*					ENIR
					*				SEL
						*			-INIT
							*		AUTFDX
								*	STROBE

ENIR: Printer port interrupt enable 1: Interrupt enabled with -ACK.

SEL: Printer select 1: Printer selected

-INIT: Printer initialization 0: Initialization (50μs/min)

ATFD: Auto feed 1: Linefeed with a CR code (CR/LF)

STB: Printer data strobe signal

Don't care: Not affected (during write) 0: (During read)

9-8-6. Hard disk selection

Generates the AT bus interface hard disk drive select signal.

HD_EN	HD_SEL	-HDCS0	-HDCS1
1	X	Not active	Not active
0	0	Active through 1F0~1F7	Active through 3F6~3F7
0	1	Active through 170~177	Active through 376~377

9-8-7. FDD selection (I/O address: 3F2H) [W/O]

BIT	7	6	5	4	3	2	1	0	
	*								DRIVE D MOTOR ENABLE (Not used)
		*							DRIVE C MOTOR ENABLE (Not used)
			*						DRIVE B MOTOR ENABLE
				*					DRIVE A MOTOR ENABLE
					*				ENABLE IRQ & DMA (Not used)
						*			FDC RESET (Not used)
							*	*	DRIVE SELECT (Not used)

When the FDD is selected, (BIT 5, BIT 4) = (1, 0), (0, 1), (1, 1).

To turn on the floppy disk access lamp, set FDSELF to "1".

NOTE: Set to 00H when reset.

9-8-8. FDD/HDD port (I/O address: 3F7) [R/O]

BIT	7	6	5	4	3	2	1	0	
	*		*		*		*		FDD DISK CHANGE
		*		*		*		*	HDD WRITE GATE (Not used) @
			*		*		*	*	HDD HEAD SELECT 3 (Not used) @
				*		*		*	HDD HEAD SELECT 2 (Not used) @
					*		*	*	HDD HEAD SELECT 1 (Not used) @
						*		*	HDD HEAD SELECT 0 (Not used) @
							*	*	HDD DRIVE SELECT 1 (Not used) @
								*	HDD DRIVE SELECT 0 (Not used) @

NOTE: READY pin of FDC is always high. Disk change should be decided by DC signal.

@: High impedance

[W/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Reserved
							*	*	MS1
								*	MS0

MS1	MS0	Transfer rate	Media	Drive
0	0	500Kbps	2HD	Internal (3.5" 1.44MB), External (5¼" 1.2MB)
0	1	300Kbps	2DD, 2D	External (1.2MB drive 640KB, 320KB read only)

9-8-9. VGA port (I/O address: 3CEH, ECFH) [W/O]

Working range of the display memory is set.

① Access method

Write the pointer 06H in the register of 3CEH to put the 3CFH port active.

② Register group

3CEH Graphic address

3CFH Miscellaneous register

③ Explanation of register

Graphics address 3CEH [W/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					NOT USED
					*	*	*	*	INDEX TO GRAPHICS CONTROLLER DATA REGISTERS

Index: 0110: 3CFH is enabled to write.

Other: 0110: 3CFH is disabled to write.

(Reference): Because this gate array consists of a 1-bit register, no signal is assumed for other than 06H.

Miscellaneous register 3CFH [W/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					NOT USED
					*				MEMORY MAP 1
						*			MEMORY MAP 0
							*		CHAIN ODD EVEN PLANES (Not used in this GA)
								*	GRAPHICS/TEXT MODE (Not used in this GA)

VRAM address is specified by the memory map.

MAP 1	MAP 0	Address used
0	0	A0000H~BFFFFH
0	1	A0000H~AFFFFH
1	0	B0000H~BFFFFH
1	1	B8000H~BFFFFH

NOTE: Set to 00H when reset.

9-8-9. Signal descriptions

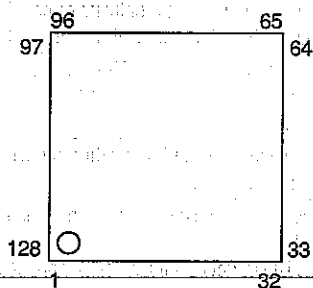
- ① The signal name preceded with a "-" represents active low signal.
② The column next to the signal name indicates: (I) for input, (O) for output, (I/O) for input/output.

Signal name	I/O	Explanation
-LMSEL	(I)	When all addresses A20~A23 are at 0, this signal turns low and cannot be latched by ALE when the CPU accesses. Used for the memory decode enable signal.
A19~A1	(I)	Memory address 19~1. Not ALE latched when the CPU accesses. Incorporates a pullup resistor.
XA0	(I)	Memory address 0. Latched by ALE when the CPU accesses. Incorporates a pullup resistor.
AEN	(I)	Address enable signal that goes high during the DMA access. With a "0" state of the signal, it is used for the enable signal of the I/O decode circuit.
XD7~XD0	(I/O)	CPU side data bus (low side).
-MEMR	(I)	Memory read command. Output for any space of 16MB.
-MEMW	(I)	Memory write command. Output for any space of 16MB.
-IOR	(I)	I/O read command.
-IOW	(I)	I/O write command.
RESET	(I)	System reset command. Schmidt input.
-SELTm	(O)	I/O select signal for within the gate array. Turns active when accessing the printer I/O, RAM I/O, hard disk I/O, floppy disk I/O, -SELMD, -SELEXIO and ROM memory.
-SELMD	(I)	Select return signal from the modem connector. In the case of a device other than the modem, the select signal needs to be added to this line. Incorporates a pullup resistor.
-SELEXIO	(I)	Select return signal from an expansion unit. When using the XD0~7 bus by the expansion unit, the select signal must be an input to this line. Incorporates a pullup resistor. If the signal is active when the internal printer port is selected, it treated invalid as the expansion unit side port takes preference by the internal printer logic.
-SELIFDD	(O)	Chip select signal for FDC Turns active when accessing the address 3F0 ~ 3F7h.
-MEMCS16	(O)	16-bit memory access request signal. Turns active when accessing the VGA VRAM and accessing the ROM memory with the memory mapper register bit 6 is at "1". Open drain output.
-MEN16	(I)	VRAM 16-bit access enable signal (VGA). 0: Enabled (MEMCS16 issued) 1: Disabled (MEGA) Enables the VGA to access the 16-bit. Controls MEMCS16.
-RMEM16	(I)	ROM memory access enable signal. Controls MEMCS16. 0: Enabled (MEMCS16 issued). 1: Disabled
IRQ7	(O)	Parallel port 1 interrupt request signal. High impedance when not used.
IRQ5	(O)	Parallel port 2 interrupt request signal. High impedance when not used.
-CS8042	(O)	8042 key controller chip select signal. Active address 60H, 64H.
-HDCS0	(O)	Hard disk chip select signal.
-HDCS1	(I)	Hard disk chip select signal. HD_EN HD_SEL -HDCS0 -HDCS1 1 X Not active. 0 0 1F0~1F7 3F6~3F7 0 1 170~177 376~377

Signal name	I/O	Explanation
-INTKEY	(O)	Internal keyboard enable signal. Contents of the Sharp original port 01, bit 5. 0: Internal 1: External
-EN_CRT	(O)	CRT display enable signal. Turns active when the VGA_EN bit is "0" with the contents of the Sharp original port 01 bit 6 in the CRT mode. L: CRT display mode -LCD/CRT inversion issued.
VGAAEN	(O)	VGA chip select signal. Turns low when the bit 1 of the AEN input is at a "0" with the bit 1 of the Sharp original port 0E (VGA_EN) at "0".
VGACS	(O)	VGA memory chip select signal. Turns "1" when the bit 1 of the Sharp original port 0E (VGA_EN) is at a "0" with -LMSEL at 0, A19 at 1, A18 at 0 and A17 at 1.
-READY	(I)	VRAM ready signal.
IOCHRDY	(O)	System ready signal. Open drain output. Turns low with a "0" state of the -READY signal.
AD0~7	(I/O)	Address multiplex bus. Hands down the address and data to the ROM and the printer. AD0 is an input when word accessing to DOSROM. In the normal operation mode, XA0 and A1~7 latch signals are issued. When accessing the ROM I/O, the contents of the address register 3 is issued. When the printer data is written, XD0~7 are issued. When printer control is written, the printer data is issued. When the printer status is read, it is in the input mode in the floating mode.
AD8~15	(O)	In the normal operating mode, A8~15 latch signal. When ROM I/O is accessed, the contents of the address register 2 are issued. When accessing the ROM, AD14 and 15 are converted. Low order two bits of the mapping register. 00 01 10 11 00→00 01→00 10→00 11→00 A14, A15→AD14, AD15 01→01 10→01 11→01 00→01 10→10 11→10 00→10 01→10 11→11 00→11 01→11 10→11
EA16~20	(O)	In the normal operating time, A16~19, -LMSEL latch signal. When accessing the ROM I/O, the contents of the address register 1 are issued.
-MEMWE	(O)	Memory write enable signal for Sharp memory
-MEMOE	(O)	Memory out enable signal for Sharp memory
-MEMCE0~3	(O)	Memory chip enable signal for Sharp memory. Refer to ROM port chip select register.
BYTE	(O)	Turns to "1" when MEMCS16 has turned to "0" by the ROM memory access. ALE latched signal.
VIFCNT	(I)	1: Printer/re232C driver enable. 1 if the printer is connected.
-PRT_EN	(O)	0: Printer driver enable
PRT_EN	(O)	1: Printer driver enable
-STBY	(O)	0: RS232C driver enable
-PDCLK	(O)	Printer data latch clock. Issued when -IOW with address 378, 278H.
-PDIN	(O)	Printer status input. Issued when IOR with address 379/279 or 37A/27A.
STROBE	(O)	Printer strobe signal (externally inverted). The contents of the printer control register bit 0.
AUTFDX	(O)	Printer auto linefeed signal (externally inverted). The contents of the printer control register bit 1.
INIT	(O)	Printer initialize signal (externally inverted). The contents of the printer control register bit 2.

Signal name	I/O	Explanation
SLCTIN	(O)	Printer select signal (externally inverted). The contents of the printer control register bit 3.
-ACK	(I)	Printer acknowledge signal. Used for the interrupt signal from the printer. Incorporates a pullup resistor (inside the chip).
FDSEL	(O)	FD access signal for LED activation (active when the motor on bit of DOR).
FALE	(O)	Address latch enable signal when making access to the CPU. Fixed to HIGH when other than making access to the CPU. To generate this signal, HLDA (signal with countermeasure against SC9889B bug) instead of HLDACPU is used as the HLDA signal.
-S0	(I)	Bus cycle status signal (I/O read, etc.)
-S1	(I)	Bus cycle status signal (I/O write, etc.)
HOLDS1	(I)	HOLD request output signal issued by SC9889B.
HLDACPU	(I)	HLDA signal issued by 80C286. Shows the HOLD state of the CPU.
HOLD	(O)	HOLD request output signal to the CPU (80C286). (HOLD signal with countermeasure against 80C286 errata)
HLDA	(O)	HLDA signal outputted to SC9889B (to prevent against SC9889B bug). To generate this signal, HOLD (signal with countermeasure against 80C286 errata) instead of HOLDS1 is used as HOLD signal.
RESCPU	(I)	RESET signal to the CPU. Schmidt input.
SYSClk	(I)	System CLOCK input
CLK16M	(I)	16MHz CLOCK input
CLK19M	(I)	19.2MHz CLOCK input
CLKOUT	(O)	CLOCK output to the FDC (Floppy Disk Controller). Outputs reversed waveforms of the input. Duty ratio of the clock output is; L: H=9:11.
-HDI	(O)	Specifies the kind of floppy disk media. 0: Floppy media 2HD (Standard floppy disk) 1: Floppy media 2DD, 2D (Mini floppy disk) I/O address Write data CLOCKOUT -HDI 3F7h 00h 16 MHz 0 3F7h 01h 19.2MHz 1
-DCH	(I)	Disk change signal from the FDD (Floppy Disk Drive).
STRX	(O)	Floppy disk drive number set signal Sharp original port is set with the register 01h/bit 0. 0: Drive A: INT-FDD Drive B: EXT-FDD 1: Drive A: EXT-FDD Drive B: INT-FDD
PRN/FDD	(I)	Select status signal input of 25 pin DSUB connector with pull-up resistor inside the chip. 0: FDD select 1: Printer select
ENID	(I)	Output allow signal to the interruption request signal (DRQ2, INT6) from the FDC (Floppy Disk Controller).
IDREQ2	(I)	Interruption request signal input from the FDC.
IIRQ6	(I)	Interruption request signal input from the FDC.
DRQ2	(O)	Interruption request signal from the FDC. HI-Z when not used.
INT6	(O)	Interruption request signal from the FDC. HI-Z when not used. ENID IDREQ2 IIRQ6 DRQ2 INT6 0 X X HI-Z HI-Z 1 0 0 0 0 1 0 1 0 1 1 1 0 1 0 1 1 1 1 1

9-8-10. Pin description



NO.	SIGNAL	BUF	NO.	SIGNAL	BUF	NO.	SIGNAL	BUF	NO.	SIGNAL	BUF
1	GND		33	CLK16M	IBF	65	AD9	OBF	97	-S1	IBF
2	-FDSEL	OBF2M	34	CLK19M	IBF	66	AD10	OBF	98	AEN	IBF
3	-SELMD	IBFU	35	GND		67	AD11	OBF	99	FALE	OBF
4	-READY	IBF	36	CLKOUT	OBF	68	AD12	OBF	100	-LMSEL	IBF
5	-MEN16	IBF	37	-CS8042	OBF2M	69	AD13	OBF	101	A19	IBFU
6	VGAEN	OBF2M	38	-INTKEY	OBF2M	70	AD14	OBF	102	GND	
7	VGACS	OBF2M	39	ENID	IBFD	71	GND		103	A18	IBFU
8	DRQ2	TOBF	40	HLDACPU	IBF	72	AD15	OBF	104	A17	IBFU
9	INT6	TOBF	41	HOLDSI	IBF	73	EA16	OBF	105	A16	IBFU
10	IDREQ2	IBFD	42	RESCPU	IBFS	74	EA17	OBF	106	A15	IBFU
11	IIRQ6	IBFD	43	HOLD	OBF2M	75	EA18	OBF	107	A14	IBFU
12	XD0	IOBF	44	-HDI	OBF2M	76	EA19	OBF	108	A13	IBFU
13	XD1	IOBF	45	STRX	OBF2M	77	EA20	OBF	109	A12	IBFU
14	XD2	IOBF	46	-MEMCS16	OBFN6M	78	-BYTE	OBF2M	110	A11	IBFU
15	XD3	IOBF	47	INT7	TOBF	79	-MEMWE	OBF	111	A10	IBFU
16	VCC		48	INT5	TOBF	80	VCC		112	VCC	
17	GND		49	GND		81	GND		113	GND	
18	XD4	IOBF	50	VCC		82	-MEMOE	OBF	114	A9	IBFU
19	XD5	IOBF	51	-SELEXIO	IBFU	83	-MEMCE0	OBF2M	115	A8	IBFU
20	XD6	IOBF	52	-SELIFDD	OBF2M	84	-MEMCE1	OBF2M	116	A7	IBFU
21	XD7	IOBF	53	PRN/FDD	IBFU	85	-MEMCE2	OBF2M	117	A6	IBFU
22	PDCLK	OBF	54	-DCH	IBF	86	-MEMCE3	OBF2M	118	A5	IBFU
23	-PDIN	OBF2M	55	ADO	IOBF	87	-RMEM16	IBF	119	A4	IBFU
24	-ACK	IBFSU	56	AD1	IOBF	88	-MEMR	IBF	120	A3	IBFU
25	SLCTIN	OBF2M	57	AD2	IOBF	89	-MEMW	IBF	121	A2	IBFU
26	INIT	OBF2M	58	AD3	IOBF	90	-IOR	IBF	122	A1	IBFU
27	AUTFDX	OBF2M	59	AD4	IOB	91	-IOW	IBF	123	XA0	IBFU
28	STROBE	OBF2M	60	AD5	IOBF	92	GND		124	IOCHRDY	TOBF
29	SYSCLK	IBF	61	AD6	IOBF	93	RESET	IBFS	125	VIFCNT	IBF
30	-PRT_EN	OBF2M	62	AD7	IOBF	94	-SELTm	OBF2M	126	-HDCS0	OBF
31	PRT_EN	OBF	63	GND		95	HLDA	OBF6M	127	-HDCS1	OBF
32	-STBY	OBF	64	AD8	OBF	96	-S0	IBF	128	-ENCRT	OBF2M

IBF : TTL level input buffer

IBFS : TTL level schmidt trigger input buffer

IBFSU : TTL schmidt trigger input buffer with a pull up resistor

OBF : Output buffer IOL=4mA

OBF2M : Output buffer IOL=2mA

OBFN6M : Nch open drain output buffer IOL=6mA

IOBF : TTL level input/output buffer

TOBF : Tri-state output buffer

9-9. μ PD4714GT (RS-232C DRIVER)

Block diagram/pin configuration (top view)

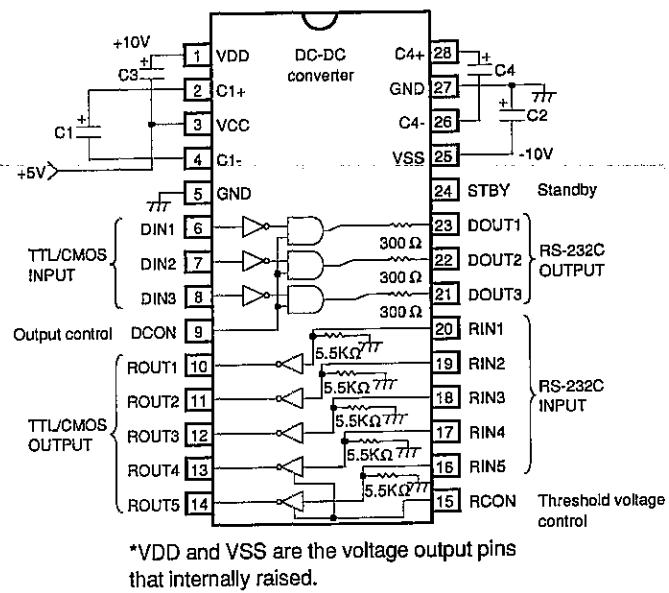


Fig. 9-14

Standby line is internally pulled down.

Voltage withstand of C1~C4 must be above 16V.

Truth table

STBY	DCON	DIN	DOUT	Note
H	X	X	Z	Standby mode
L	L	X	L	MARK level output
L	H	H	L	MARK level output
L	H	L	H	SPACE level output

STBY	RIN	ROUT
H	X	Z
L	H	L
L	L	H

H: High level L: Low level Z: High impedance X: H or L

9-10. Sharp original port map (SOP)

9-10-1. Access method

- ① Write the pointer address in the I/O address 7CH.
- ② Read or write the data in the I/O address 7DH.

9-10-2. Register groups

Pointer	Register name		
01	FD, etc. control	SI (R/W)	GA (W/O)
02	Device control	SI (W/O)	GA (R/W)
03	Modem control	SI (R/W)	
04	EMS control	SI (R/W)	
05	PSRAM control	SI (R/W)	
06	Power supply control	SI (R/W)	
07	Auto standby control	SI (R/W)	
08	Power supply status	SI (R/O)	
09	Power save timer	SI (R/W)	
0A	Auto resume timer	SI (R/W)	
0B	Resume enable	SI (R/W)	
0C	RSTCPU cause register	SI (R/O)	
0D	Expansion unit	SI (R/O)	
0E	VGA control	SI (R/W)	GA (W/O)
0F	NMI cause register	SI (R/O)	
10	Reserved		
11	Reserved		
12	ROM support control		GA (R/W)
13	Reserved		
1F			

9-10-3. Explanation of registers

Pointer **01** FD, etc. control SI (R/W) GA (W/O)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*							DISPLAY MODE (-ENCR)
			*						KEY ASSIGN
				*					SIO SELECT
					*				SIO ASSIGN
						*	*	*	FDD ASSIGN

DISPLAY MODE 0: LCD MODE 1: CRT MODE

KEY ASSIGN 0: INTERNAL KEY ENABLE
1: INTERNAL KEY DISABLE

SIO SELECT 0: PORT 1 1: PORT 2

SIO ASSIGN 0: ENABLE 1: DISABLE

FDD ASSIGN

BIT	INT-FDD		EXT-FDD	
210	0	1	0	1
000	0	1	2	3
001	2	1	0	3
010	0	3	1	2
011	1	3	0	2
100	2	3	0	1
101	0	2	1	3
110	2	3	0	1
111	0	2	1	3

SIO SELECT affects the pointer 02 setting.

Pointer **02** Device control SI (W/O) GA (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								HD EN
		*							HD SEL
			*						SIO EN
				*					SIO SEL
					*				PRT EN
						*			PRT SEL
							*		IMS EN (Inport Mouse)
7								*	IMS SEL

HD EN 0: INTERNAL HD ENABLE

1: INTERNAL HD DISABLE

HD SEL 0: PRIMARY

1: SECONDARY

SIO EN 0: INTERNAL SIO ENABLE

1: INTERNAL SIO DISABLE

SIO SEL 0: PRIMARY

1: SECONDARY

PRT EN 0: INTERNAL PRT ENABLE

1: INTERNAL PRT DISABLE

PRT SEL 0: PRIMARY

1: SECONDARY

IMS EN 0: INTERNAL IMS ENABLE (Not used)

1: INTERNAL IMS DISABLE

IMS SEL 0: PRIMARY

1: SECONDARY (Not used)

IMS=INPORT MOUSE

Pointer **03** Modem control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					MODEM_EN
					*	*	*		Not used
							*		OUTSEL

MODEM EN 0: INTERNAL MODEM ENABLE

1: INTERNAL MODEM DISABLE

OUTSEL 0: MORST signal is issued

1: 202H decode signal output

Model port selection is set opposite to the internal SIO port setting.

Pointer **04** EMS control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*	*						SW6, 5
				*	*				JP3, 2
						*	*	*	SW2, 1, 0 2x8~2xB (X16=XXX02)

SW6,5 Extended memory area setting

SW2,1,0 EMS control register I/O address setting

JP3,2 Pointer 05 JP1, 0 expansion

Pointer **05** PSRAM control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*							MAP1, 0
			*						PVTMEM
				*	*				JP1, 0
						*			PCS3EN
							*		INTVL
								*	Not used

MAP2,1 Private memory bank selection

PVTMEM 1: Private memory access enable (E0000H~EFFFFH)
0: Disable

PCS3EN Standard RAM capacity setting
1: 256KB used for a private memory area

INTLV 1: PSRAM interleave access enable
0: Disable

Pointer **06** Power supply control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					VMDM CNT
					*				VBL CNT
						*			VCC CNT
							*		VLCD CNT
								*	VIF CNT

VMDMCNT 0: Off 1: On Modem power supply

VBLCNT 0: Off 1: On Backlight power supply

VCCCNT 0: Off 1: On System power supply

VLCD CNT 0: Off 1: On LCD power supply

VIFCNT 0: Off 1: On Printer/RS232C driver power supply

LCD and backlight power on needs to be in the LCD mode with the pointer 01 and display circuit enabled with the pointer 0E.

Pointer **07** Auto standby control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*				Not used
						*			VCC STB
							*		VLCD SAVE
								*	VIF SAVE

VCCSAVE 0: Auto resume disabled (with timer) 1: Enabled

VLCD SAVE 0: Auto power save disabled (with timer) 1: Enabled

VIFSAVE 0: Auto driver power save disabled 1: Enabled

Pointer **08** Power supply status SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					VMDM STS
					*				VBL STS
						*			VCC STS
							*		VLCD STS
								*	VIF STS

VMDMSTS 0: Off state 1: On state

VBLSTS 0: Off state 1: On state

VCCSTS 0: Off state 1: On state

VLCDSTS 0: Off state 1: On state

VIFSTS 0: Off state 1: On state

(Even though set to on by the power supply control, off is established by the auto standby.

Pointer **09** Power save timer SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*	*	*	*	PST3~0 0=0 min.~1 min. F=15 min.~16 min.

PST3~0 VLCD, VBL off timer count time is set between 0 and 15 minutes. The set value is read when read.

Pointer **0A** Auto resume timer SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*	*	*	*	*	*	*	ART6~0

ART6~0 VCC off time-out time is set between 0 and 127 minutes. The set value is read when read.

Pointer **0B** Resume enable SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*				Not used
						*			MRI
							*		CI
								*	RE

MRI 1: Enabled to return from resume by the RI signal from the modem.

CI 1: Enabled to return from resume by the CI signal from the 232C.

RE 1: Resume enabled

Pointer **0C** RSTCPU cause register SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*				MRI
						*			CI
							*		R
								*	Not used

MRI 1: Resume return BY MRI

CI 1: Resume return by CI

R 1: Resume return by the resume switch

Pointer **0D** Expansion unit SI (R/O)

BIT	7	6	5	4	3	2	1	0	
*	*	*	*	*	*	*	*	*	Not used
								*	EXU

EXU 0: Expansion unit exists

1: Expansion unit does not exist

Pointer **0E** VGA control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*				PWRDWN2
						*			PWRDWN1
							*		VGA EN
								*	SIO_POL

PWRDWN2,1 0 0 Normal operation

0 1 Relax mode

Though power turns down, R/W is enabled for VRAM and REG.

1 0 Retire mode

Power turns down and R/W is not enabled for VRAM and REG. Needs refresh timer to set.

VGA EN 0: VGA enable
1: Disable

SIO_POL 0: Normal 1: 232C input/output polarity inverted

Pointer **0F** NMI cause register SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Not used
								*	RSNNMI

RSMNMI 0: Resume request NMI does not occur

1: Resume request NMI occurred.

Pointer 0B Cleared by setting the bit 0 of RE sets to 0.

Pointer **12** ROM port control GA (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*	*	*	*	IOA3~0

IOA3~0 Specifies the part of "X" of the I/O address 1X8~BH that set by the dip switch for the UE-1R06/06 (AX dictionary ROM board).

9-11. IMS G176L

High performance CMOS Colour look-up table

9-11-1. Features

- Compatible with the RS170 video standard.
- Pixel rates up to 66MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun.
- Composite blank on all three channels.
- Low DAC glitch energy.
- Video signal output into 37.5 Ω .
- Up to 8 bits per pixel.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V power supply.
- Low power dissipation, 950mW max at maximum pixel rate.
- Standard 600 mil 28 pin DIL or 32 pin or 44 pin Plastic LCC.
- Pin compatible with IMS G171.
- Power down capability.

9-11-2. General Description

The IMS G176/L integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 28 pin DIL, 32 pin or 44 pin PLCC package. The IMS G176L is a power down version of the IMS G176.

The device is capable of driving a doubly-terminated 75 Ω line with no external buffering, and composite blank signals can be generated all three outputs.

Capable of displaying 256 colours from a total of 262, 144 colours, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

9-11-3. Pin assignment

32 pin plastic leaded-chip-carrier package

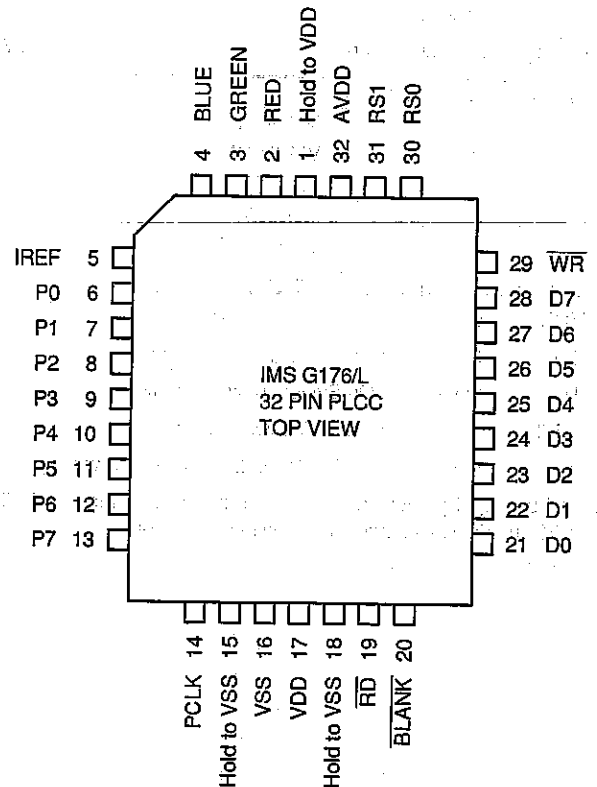


Figure 9-14 IMS G176/L 32 pin PLCC J-bend package pinout

9-11-4. Block diagram

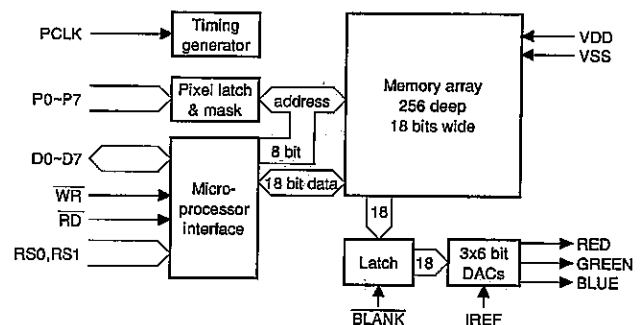


Fig. 9-15

9-11-5. Pin designations

9-11-5-1. Pixel Interface

Signal	Pin number	I/O	Signal name	Description
	PLCC			
	32			
PCLK	14	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of Values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
P ₀ -P ₇	6-13	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
BLANK	20	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

9-11-5-2. Analogue Interface

Signal	Pin number	I/O	Signal name	Description
	PLCC			
	32			
RED BLUE GREEN	2 3 4	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. the number of current sources active is controlled by the 6 bit binary value applied.
IREF	5	I	Reference Current	The reference current drawn from VDD (or AVDD) via the IREF pin determines the current sourced by each of the current sources in the DACs.

9-11-5-3. Microprocessor

Signal	Pin number	I/O	Signal name	Description
	PLCC			
	32			
$\overline{WR}$	29	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	19	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The read and Write enable signals should not be asserted at the same time.
RS ₀ , RS ₁	30, 31	I	Register Select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
D ₀ -D ₇	21-28	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G176/L under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

9-11-5-4 Power supply

Signal	Pin number	Signal name	Description
	PLCC		
	32		
VDD	17	Digital supply	Digital and analogue supply pads are bonded out separately on the PLCC package to give highest possible noise immunity. Due to package size limitations the decoupling capacitor must be provided externally (see section on 'Power supply decoupling')
AVDD	32	Analogue supply	
VSS	16	Ground	

9-11-5-5. Internal registers

RS1	RS0	Size (bits)	Register name	Description
0	0	8	Address (Write mode)	There is a single Address register within the IMS G176/L. This register can be accessed through either register select 0, 0 or 1, 1 Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1, 1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the colour look-up table. b) Loads the Colour Value register with the contents of the location in the look-up table addressed and then increments the Address register. A read from register 0,0 is functionally equivalent to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits D ₀ -D ₅ are used. When a byte is read only the least significant six bits contain information – the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the Colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the Colour look-up table replaces the normal pixel mapping operations of the IMS G176/L for a single pixel.
1	0	8	Pixel Mask	The pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P ₀ -P ₇). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

9-11-6. Device description

The IMS G176/L is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 x 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 66 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G176/L. This signal acts on all three of the analogue outputs. The BLANK signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

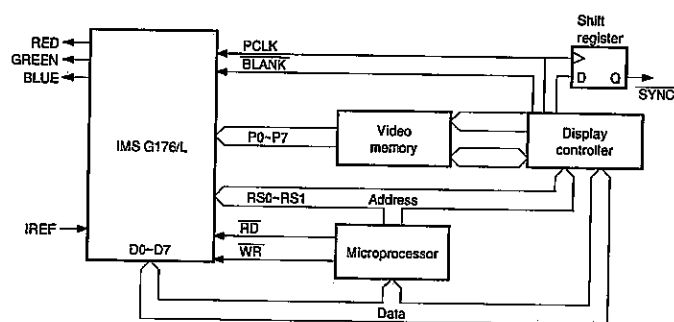


Figure 9-16 Typical IMS G176/L application

9-11-6-1. Video path

P₀-P₇ and BLANK inputs are sampled on the rising edge of Pixel Clock. Their effect appears at the analogue outputs after three further rising edges of pixel clock (see figure 9-17)

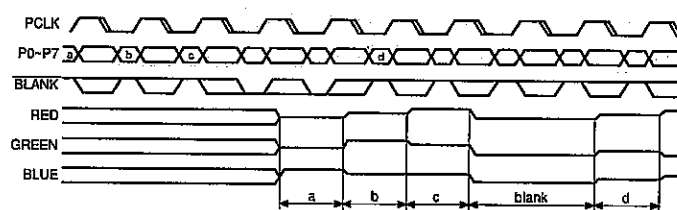


Figure 9-17

9-11-6-2. Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 9.07 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load (REFFECTIVE) of 37.5Ω.

The BLANK input to the IMS G176/L acts on all three of the analogue outputs. When the BLANK input is low a binary zero is applied to the inputs of the DACs.

The expression of calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAKWHITE}}{2.058 \times REFFECTIVE}$$

Note that for all values of IREF and output loading:

$$V_{BLACK LEVEL} = 0$$

9-11-6-3. Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G176/L and the four locations through which they can be accessed:

RS ₁	RS ₀	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transferred from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity value can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G176/L. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronised to the Pixel Clock by internal logic. This is done in the period between microprocessor accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers or modifications to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

CHAPTER 10. DIAGNOSTICS

10-1. Introduction

This diagnostics is used to check the operating state of the system unit, keyboard and peripheral units, when an option device is interfaced to the PC-6500 or when there is a state of error.

The following twelve kinds of diagnostics are provided to trace the exact cause.

Memory diagnostics

This diagnostics tests the standard and optional memory.

Real time clock & CMOS RAM diagnostics

This diagnostics tests the real time clock function and CMOS RAM.

Keyboard diagnostics

This diagnostics tests the keyboard functions.

Serial I/O diagnostics

This diagnostics tests the RS-232C line of the standard serial I/O.

Printer diagnostics

This diagnostics tests the printer function.

LCD diagnostics

This diagnostics tests the LCD.

Video subsystem diagnostics

This diagnostics tests the video subsystem function.

Coprocessor diagnostics

This diagnostics tests the coprocessor function

Modem diagnostics

This diagnostics tests the modem function.

Floppy disk drive diagnostics

This diagnostics tests the floppy disk drive function.

Hard disk drive diagnostics

This diagnostics tests the hard disk drive function.

10-2. Starting up the diagnostic program

Set the diagnostic diskette to the floppy disk drive and supply power. Then the diagnostic program is automatically started and the following screen is displayed.

Move the highlighting to the diagnostics you want to select, and press ENTER.

PC-6500 Series Service-man Diagnostics

Memory diagnostics
Real time clock & CMOS RAM diagnostics
Keyboard diagnostics
Serial I/O diagnostics
Printer diagnostics
LCD diagnostics
Video subsystem diagnostics
Coprocessor diagnostics
Modem diagnostics
Floppy disk drive diagnostics
Hard disk drive diagnostics

10-3. Diagnostic program loader

This diagnostic program loader is used to select and execute the each device diagnostic program.

Upon the start of the program loader, the diagnostic main menu is displayed. When one of twelve choice is selected, the respective diagnostic program is loaded from the floppy disk onto the main memory area. After it has been completed, the control moves to the diagnostic program to execute.

When the ESC is pushed in the diagnostic main menu, the program terminates and the control returns to the MS-DOS.

10-4. Check program

All check programs are stored on the diagnostic program disk and used to check the state of a device after it has been installed or a specific device is tested when an error is reported.

In general, the valid keys at that time are displayed at the lowest line on the screen.

10-4-1. Memory diagnostics

This program tests the standard memory and the optional memory.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Memory Diagnostics

Marching check
Display error table

10-4-1-1. Marching check

The marching check for the all memory area is executed in the following manner:

1. Test data 5555H are written in the area to be checked.
2. The test data are read/compare at every word and test data AAAAH are written in the area to be checked.
3. The test data are read/compare at every word and test data 5555H are written in the area to be checked.
4. Test data 0000H are written in the area to be checked.
5. The test data are read/compare at every word and test data FFFFH are written in the area to be checked.
6. The test data are read/compare at every word and test data 0000H are written in the area to be checked.

The main memory is checked the following procedure:

1. The area from the address 40000H to 9FFFFH is tested by the marching test in an increment of 64KB.
2. The data in the address 00000H through 3FFFFH are copied onto the area after the address 40000H, then the address 00000H through 3FFFFH is tested by the marching test in an increment 64KB.

The extended memory is checked the following procedure:

1. The area after the address 100000H is tested by the marching test in an increment 64KB.

The expanded memory is checked the following procedure:

1. The expanded memory area is tested by the marching test in an increment 16KB (page frame)

• OPERATION

Specify the memory to be checked.

Check main memory ? [Yes No]
Check extended memory ? [Yes No]
Check expanded memory ? [Yes No]

Move the highlighting to the memory you want to check and press ENTER.

If an error occurs while executing the test, specify whether to abort or continue the test.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

• Error message

The current error message is displayed on the lower side of the screen when an error is occurred during the executing of the task.

• **Range** shows absolute address at which an error occurred.

• **Page** shows page frame at which an error occurred.

• **Bits** shows bits at which an error occurred.

10-4-1-2. Display error table

This item displays the information of errors in the form of a table. The parameters shown on the screen are described below.

Mode shows memory mode at which an error occurred.

Range shows absolute address at which an error occurred.

Page shows page frame at which an error occurred.

Bits shows bits at which an error occurred.

Count shows number of errors.

10-4-2. Real time clock & CMOS RAM diagnostics

This program tests the real time clock function and CMOS RAM.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Real Time Clock & CMOS RAM Diagnostics

Real time clock check

CMOS RAM check

Dump CMOS RAM

10-4-2-1. Real time clock check

This test checks RTC timer function and RTC clock function. RTC timer check tests if the timer interrupt occurs correctly. RTC clock check tests if the clock works correctly.

10-4-2-2. CMOS RAM check

This test item tests RTC CMOS RAM and setup CMOS RAM.

• Depression of ESC terminates the aging

This test writes the specified data to the CMOS RAM, reads the data from CMOS RAM, and then compares them. The specified data to be written are 55h, AAh and 55h. Also this test checks checksum and banks are selected correctly.

• Operation

Specify whether to repeat or do only once the test in the following message.

Aging mode ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When selection "Yes", the test will be repeated. On the other hand, when selecting "No", the test will be done only once.

10-4-2-3. Dump CMOS RAM

This test dumps contents of RTC C-MOS RAM and bank 0-in-Setup C-MOS RAM are displayed.

10-4-3. Keyboard diagnostics

This program tests the keyboard and speaker functions.

The following menu appears when this test program is selected.

Keyboard Diagnostics

U.S. English keyboard check

Other keyboard check

Move the highlighting to the keyboard type you want to select, and press ENTER. Depression of ESC terminates the test.

10-4-3-1. Keyboard check

The keyboard check begins with a graphic representation of the keyboard layout displayed on the screen. To test whether a particular key functions as it should, press the key. A square should display on the keyboard layout at that position if the key is working correctly. The test terminates when the ESC is pressed twice consecutively.

10-4-4. Serial I/O diagnostics

This program tests the function of the serial I/O with the loopback connector in use.

No.3 (SD) ☐
 No.2 (RD) ☐
 No.7 (RTS) ☐
 No.8 (CTS) ☐
 No.4 (DTR) ☐
 No.1 (CD) ☐
 No.9 (RI) ☐
 No.6 (DSR) ☐
 9 pins female connector

The following shows how wires are connected.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Serial I/O Diagnostics

Line check

Parameters check

Character transport check

10-4-4-1. Line check

This item tests the following RS-232C line.

• SD – RD line

The program causes 256 bytes of data from 00H to FFH to be transmitted in the asynchronous mode, receives the data from the receive data line, compare that the transmitted data is the same as the received data. When the program considers that both data are the same, it transmits the next data.

• RTS – CTS line

By turning on/off the RTS signal, the program checks that the CTS signal function normally.

• DTR – DSR – CD – RI line

By turning on/off the DTR signal, the program checks that the DSR, CD, RI signal function normally.

10-4-4-2. Parameter check

This test checks the serial I/O function by changing the baud rate, parity bit, stop bit and word length.

Parameters check is checked the following order.

The data 0 to 7FH is used for the word length 7 bits and 0 to FFH for the word length 8 bits.

Each parameter at that time is display on the screen.

10-4-4-3. Character transport check

This test checks the character data entered on the keyboard are sent and received via the loopback connector and the received data are displayed on the screen.

As entry of characters to be transmitted will be prompted as shown below after the program started, you may enter 40 strokes of any character at a maximum. Depression of the ENTER starts the test and transmission takes place. The received data are displayed.

Sending data : ■
Receiving data :

- **Error message**

The error message is displayed on the lower side of the screen when an error is occurred during the executing of the task.

- **SD time out error**

Response to the transmit data is not found within the prescribed time.

- **RD time out error**

response to the receive data is not found within the prescribed time.

- **Transmit register not empty**

The transmit shift register failed to go empty.

- **Overrun error**

Character is received when the receive buffer is fully occupied with characters.

- **Framing error**

0 is found for the stop bit.

- **Parity error**

A parity error is met.

- **Data compare error**

Received data did not match with the transmit data.

10-4-5. Printer diagnostics

This program tests the printer interface and the printer connector with main unit.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Printer Diagnostics
Status check
Print check

10-4-5-1. Status check

The printer's status signals are checked and displayed. The following status categories are checked:

Bsy checks the printer's busy signal.

Ack checks that the printer can handshake with the main unit.

Pe checks that paper is set.

Sel shows when the printer is on-line.

loe checks that the printer's mechanics are OK.

An asterisk is displayed above a category when it's check completes normally.

10-4-5-2. Print check

The test printing will not start until the five status categories in the status check all show an asterisk (above the categories). If a true hardware malfunction is detected, you will not be able to obtain an asterisk in that category. In that case, you will not be able to do a test print either.

10-4-6. LCD diagnostics

This program tests the LCD by displaying the test pattern on the screen.

The following menu appears when this test program is selected. Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

LCD Diagnostics
Checker pattern check
Stripe pattern check
Shades of gray check
Frame check

10-4-6-1. Checker pattern check

This test displays the checker pattern on the screen.

First, all display dots are displayed. Next, the test patterns of single dot, two dots, four dots and eight dots intervals are displayed and their reverse videos. The above procedure is repeated again.

10-4-6-2. Stripe pattern check

This test displays the stripe pattern on the screen.

The vertical and horizontal stripes are displayed including reverse video. The above procedure is repeated again.

10-4-6-3. Shades of gray check

This test displays the 16 shades of gray on the screen.

10-4-6-4. Frame check

The frame line is displayed in each display mode. The above procedure is repeated again.

- **Operation**

When SPACE is pressed during the test, the test execution suspends. With the depression of the SPACE again, the test resumes. The test terminates by the depression of ESC.

10-4-7. Video subsystem diagnostics

This program tests video subsystem function.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Video Subsystem Diagnostics
Video memory check
DAC check
Attribute check
Character set check

10-4-7-1. Video memory check

This test checks the buffer in the video subsystem.

The video memory is tested by the marching test for four buffer bank (64KB).

The marching test for the all video memory area is executed in the following manner:

1. Test data 5555H are written in the area to be checked.
2. The test data are read/compare at every word and test data AAAAH are written in the area to be checked.
3. The test data are read/compare at every word and test data 5555H are written in the area to be checked.
4. Test data 0000H are written in the area to be checked.
5. The test data are read/compare at every word and test data FFFFH are written in the area to be checked.
6. The test data are read/compare at every word and test data 0000H are written in the area to be checked.

- **Operation**

Specify whether to repeat or do only once the test in following message.

Aging mode? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

If an error occurs while executing the test, specify whether to abort or continue the test.

Error stop? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

The test terminates by the depression of ESC.

• Error message

The current error message is displayed on the lower side of the screen when an error is occurred during the executing task.

Map shows map at which an error occurred.

Bits shows bits at which an error occurred.

10-4-7-2. DAC check

This program tests the digital-to-analog converter in the video subsystem.

10-4-7-3. Attribute check

This program displays 16 foreground, 8 background and 8 blinking shades of gray.

BLACK BLUE GREEN CYAN RED MAGENTA BROWN LIGHT_GRAY DARK_GRAY LIGHT_BLUE LIGHT_GREEN LIGHT_CYAN LIGHT_RED LIGHT_MAGENTA YELLOW WHITE		BLACK BLUE GREEN CYAN RED MAGENTA BROWN LIGHT_GRAY	(B)
		BLACK BLUE GREEN CYAN RED MAGENTA BROWN LIGHT_GRAY	(C)

The following figure is displayed on the screen.
 The portion (A) shows 16 foreground shades of gray.
 The portion (B) shows 8 background shades of gray
 The portion (C) shows 8 blinking shades of gray

10-4-7-4. Character set check

This program displays characters on the screen normally on an 80 × 25 test mode display.

Example: The following figure will be displayed on the screen.

Decimal Value	→	0	16	32	48	64	80	96	112	128	144	160	176	192	208	224	240
↓	Hexa decimal Value	0-	1-	2-	3-	4-	5-	6-	7-	8-	9-	A-	B-	C-	D-	E-	F-
0	-0																
1	-1																
2	-2																
3	-3																
4	-4																
5	-5																
6	-6																
7	-7																
8	-8																
9	-9																
10	-A																
11	-B																
12	-C																
13	-D																
14	-E																
15	-F																

10-4-8. Coprocessor diagnostics

This program tests the coprocessor function.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Coprocessor Diagnostics
Function check

10-4-8-1. Function check

This test has the following four items.

Initialize check checks that the coprocessor is initialized, when the initialize command was issued.

Arithmetic check checks that the coprocessor can calculate, when the arithmetic command was issued.

Interrupt check checks the interrupt occurs in the coprocessor, when the division by 0 command was issued.

Reset check checks the coprocessor is reseted, when the reset command was issued.

10-4-9. Modem diagnostics

This program tests modem (CE-621M).

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Modem Diagnostics
Analog loop back check

10-4-9-1. Analog loop back check

This program tests the modem by sending, receiving and comparing the data in the analog loop back mode. Then the optional modem port must be installed:

• Operation

Move the highlighting to the baud rate you want to check, and press ENTER. Depression of ESC terminates the test.

Set baud rate ? [300 1200 2400]

- **Error message**

The error message is displayed on the lower side of the screen when an error is occurred during the executing of the task.

- **SD time out error**

Response to the transmit data is not found within the prescribed time.

- **RD time out error**

Response to the receive data is not found within the prescribed time.

- **Transmit register not empty**

The transmit shift register failed to go empty.

- **Overrun error**

Character is received when the receive buffer is fully occupied with characters.

- **Framing error**

0 is found for the stop bit.

- **Parity error**

A parity error is met.

- **Data compare error**

Received data did not match with the transmit data.

10-4-10. Floppy disk drive diagnostics

This program tests the internal 3-1/2" floppy disk drive and the external 5-1/4" floppy disk drive.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Floppy Disk Drive Diagnostics

Read drive status

Write, read & compare check

Read only check

00 track sensor adjustment

Target sector read check

Display error table

10-4-10-1. Read drive status

This item displays the current status of the floppy disk drive(s). While this program is executing, the system periodically detect some status change, it causes the buzzer to sound and displays the new status on the screen.

- **Operation**

Pressing any key, the test terminates.

10-4-10-2. Write, read & compare check

This test checks the write/read operation.

The system writes the specified data to the floppy disk, reads the same data from the floppy disk, and then compares them.

The specified data to be written is 00H to FFH increment pattern when the pass count is '0', otherwise the data is 2bytes repetitive pattern of "B6DBH".

- **Caution**

When this test is executed, all the contents stored in the floppy disk are destroyed. So be very careful with this test. In addition, it is necessary to release "Write Protect".

- **Operation**

When this test is selected, the following message is displayed.

Please insert the formatted scratch disk in the drive.

At the time, insert the test disk in the drive to be checked and press

ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

Drive not ready.

Specify whether to check the drive or not in the following message.

Drive_A (1.44MB) test ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. The string in the parenthesis represents the capacity of the disk.

Specify the range of cylinders to be checked in the following message.

Cylinder range ?

Drive_A [00 ↔ 79] = ■

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.

Specify the number of sector accessed by one instruction in the following message.

Sector count ?

Drive_A [1, 3, 18] = ■

Type the sector count in the displayed count and press ENTER.

Specify the number of retrial in the following message, when an error has occurred.

Retry count ? [0 ↔ 4] = ■

Type the retry count in the displayed range and press ENTER.

Specify whether to stop or continue the test, when an error has occurred.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the checked drive". On the other hand, when entering "Yes", starts the test.

While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.

The lower left screen shows pass count and test point represented by physical address as follows:

Pass count = ■■■■■■

Test point = TT.H.SS

"TT" means the track, "H" means the head and "SS" means the sector.

In addition, the lower right screen shows the test mode and the test drive.

Test mode: Write Test drive: Drive_A

• Error processing

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter.

If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "12-4-10-7. Error message".

10-4-10-3. Read only check

This test checks that data is properly read from the floppy disk drive.

• Operation

When this test is selected, the following message is displayed.

Please insert the formatted scratch disk in the drive.

At the time, insert the test disk in the drive to be checked and press ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

Drive not ready.

Specify whether to check the drive or not in the following message.

Drive_A (1.44MB) test ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. The string in the parenthesis represents the capacity of the disk.

Specify the range of cylinders to be checked in the following message.

Cylinder range ?
Drive_A [00 ↔ 79] = ■■

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.

Specify the number of sector accessed by one instruction in the following message.

Sector count ?
Drive-A [1, 3, 18] = ■■

Type the sector count in the displayed count and press ENTER.

Specify the number of retrial in the following message, when an error has occurred.

Retry count ? [0 ↔ 4] = ■

Type the retry count in the displayed range and press ENTER.

Specify whether to stop or continue the test, when an error has occurred.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.

While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.

The lower left screen shows pass count and test point represented by physical address.

Pass count = ■■■■■
Test point = TT.H.SS

"TT" means the track, "H" means the head and "SS" means the sector.

In addition, the lower right screen shows the test mode and the test drive.

Test mode: Read Test drive: Drive_A

• Error processing

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter.

If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "12-4-10-7. Error message".

12-4-10-4. 00 Track sensor adjustment

This program checks the 00 track sensor which detects the cylinder 0. The system moves the head from the cylinder 0 to cylinder 4 and returns the head to the cylinder 0. With such an operation, the system can observe a signal from the 00 track sensor as a pulse.

• Operation

Specify the drive to be checked in the following message.

Test drive ? [Drive_A]

Move the highlighting to the drive you want to select, and press ENTER.

Specify whether to repeat or do only once the test in the following message.

Aging mode ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When selecting "Yes", the test will be repeated. On the other hand, when selection "No", the test will be done only once.

Specify whether to execute the test or not.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.

In the aging mode, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test.

Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test. Otherwise, by pressing ESC, the test terminates. However, by pressing ENTER, the test is repeated again.

- **Error processing**

While the system executes the test, if an error occurs, the system displays the kind of error at the lower screen. In this state, by pressing any key, the test terminates. For details of error message, see "12-4-10-7. Error message".

10-4-10-5. Target sector read

This test is used to continue reading the specific sector.

- **Operation**

Specify the disk to be checked in the following message.

Please insert the alignment or formatted disk in the drive.
What kind of the test disk do you use ?
[Alignment_disk Formatted_disk]

At the time, insert the test disk in the drive to be checked and move the highlighting to the disk you inserted, and press ENTER. If the drive is not ready or the test disk isn't inserted in the drive, the following message is displayed and the test terminates.

Drive not ready.

Specify the drive to be checked in the following message.

Test drive ? [Drive_A]

Move the highlighting to the drive you want to select, and press ENTER.

Specify the cylinder number to be checked in the following message.

Cylinder number ? [00 ↔ 79] = ■■

Type the cylinder number to be checked in the displayed range and press ENTER.

Specify the head number to be checked in the following message.

Head number ? [0 ↔ 1]

Type the head number to be checked in the displayed range and press ENTER.

Specify the sector range to be checked in the following message.

Sector range ? [1 ↔ 18] = ■■ - ■■

Type the first sector number and the last sector number of the cylinder range to be checked and press ENTER.

NOTE: When the alignment disk is selected, this specification of sector range is not displayed.

Specify whether to stop or continue the test if an error occurs while executing test.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. when selecting "No", control exits to "specification of the checked drive". On the other hand, when selecting "Yes", starts the test.

While the system executes the test, by pressing SPACE, it stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depression of ESC is always effective during this test.

The lower left screen shows pass count and test point represented by physical address.

Pass count = ■■■■■■
Test point = TT.H.SS

"TT" means the track, "H" means the head and "SS" means the sector. In addition, the lower right screen shows the test mode and the test drive.

Test mode: Read Test drive: Drive_A

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on the lower right screen and increments the right-hand error counter. If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information at the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER the system continues the test. On the other hand, by pressing ESC, the test terminates. For details of error message, see "12-4-10-7. Error message".

10-4-10-6. Display error table

All error kinds, locations and counts are displayed for "Write-read check" and "Read only check". However, this error information is limited to 40 locations.

- **Operation**

By pressing any key, the test terminates.

10-4-10-7. Error messages

- **FDC busy**

A read or write command is in process.

- **FDC seek error**

The system received a FAULT signal from the device or the seek operation was abnormally completed.

- **Communication error**

Handshake error occurred between the CPU and FDC.

- **Equipment check**

The system received a FAULT signal from a device or did not detect a track 00 signal in the specified time period while the recalibrate operated.

- **Missing address mark**

The address mark in the ID section was not detected.

- **FDC no data**

The ID without CRC error was not detected.

- **FDC invalid command**

A command written to the FDC was invalid.

- **Drive not ready**

The device being specified was in the not ready state.

- **Record not found**

The sector specified in the ID field could not be detected in the track

- **DMA boundary error**

DMA error across 64KB boundary.

- **Write protected error**

The system detected write protection.

- **Seek error**

Shows the occurrence of an error during seek.

- **Bad controller**

Shows the occurrence of any abnormality in the controller.

- **Bad address mark**

Shows the occurrence of an address mark read error.

- **Bad CRC error**

Shows the occurrence of a CRC error during data error.

- **Bad command error**

A command was specified which was not in BIOS.

- **Compare error**

Data being written did not accord with data being read.

- **Others error**

Shows the occurrence of other errors not described above.

10-4-11. Hard disk drive diagnostics

This program tests the hard disk drive.

The following menu appears when this test program is selected.

Move the highlighting to the item you want to select, and press ENTER. Depression of ESC terminates the test.

Hard Disk Drive Diagnostics

Drive type check

Write, read & compare check

Read only check

Random seek check

Dump and Patch

Disk controller check

Display error table

10-4-11-1. Drive type check

This test item checks the specification of the drive if the drive is ready. The capacity, cylinder numbers, head numbers and sector numbers are displayed.

- **Operation**

Depression of any key terminates the test.

10-4-11-2. Write, read & compare check

This item checks the write/read operation.

The system writes the specified data to the hard disk, reads the same data from the floppy disk, and then compares them.

The specified data to be written is 00H to FFH increment pattern when the pass count is 0, otherwise the data is 2bytes repetitive pattern of "CB33".

- **Caution**

When this test is executed, all the contents stored in the disk are destroyed. So be very careful with this test.

- **Operation**

Specify the range of cylinders to be checked in the following message.

Cylinder range ?
[000 ↔ 613] = ■■■ - ■■■

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER. Specify the number of sector accessed by one instruction in the following message.

Sector count ?
[01 ↔ 17] = ■■

Type the sector count in the displayed range and press ENTER. Specify the number of retrial in the following message; when an error has occurred.

Retry count ?
[0 ↔ 4] = ■

Type the retry count in the displayed range and press ENTER.

Specify whether to stop or continue the test in the following message, when an error has occurred.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not in the following message.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.

While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.

the lower left screen shows the pass count and the test point represented by physical address as follows:

Pass count = ■■■■■■
Test point = CCC.HH.SS

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.

In addition, the lower right screen shows the test mode.

Test mode: Write

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.

If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates. For details of error message, see "12-4-11-8. Error message".

10-4-11-3. Read only check

The test checks if the read operation is normal by reading the data on the hard disk.

- **Operation**

Specify the range of cylinders to be checked in the following message.

Cylinder range ?
[000 ↔ 613] = ■■■■ - ■■■■

Type the starting cylinder number at first and press ENTER. Then type the ending cylinder number and press ENTER.

Specify the number of sector accessed by one instruction in the following message.

Sector count ?
[01 ↔ 17] = ■■

Type the sector count in the displayed range and press ENTER. Specify the number of retrial in the following message, when an error has occurred.

Retry count ?
[0 ↔ 4] = ■

Type the retry count in the displayed range and press ENTER.
Specify whether to stop or continue the test in the following message,
when an error has occurred.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not in the following message.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER: when entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.

While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.

The lower left screen shows the pass count and the test point represented by physical address as follows:

Pass count = ■■■■■
Test point = CCC.HH.SS

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.

In addition, the lower right screen shows the test mode.

Test mode: Read

• Error processing

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.

If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates. For details of error message, see "12-4-11-8. Error message".

10-4-11-4. Random seek check

The test checks if the seek operation is normal by accessing the hard disk at random.

• Operation

Specify whether to stop or continue the test in the following message, when an error has occurred.

Error stop ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

Specify whether to execute the test or not in the following message.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the cylinder range". On the other hand, when entering "Yes", starts the test.

While executing the test, by pressing SPACE, the system stops the test. At the time, by pressing SPACE again, the system continues the test. Also by pressing ESC, the test terminates. The depressing of ESC is always effective during this test.

The lower left screen shows the pass count and the test point represented by physical address as follows:

Pass count = ■■■■■
Test point = CCC.HH.SS

"CCC" means the cylinder, "HH" means the head and "SS" means the sector.

In addition, the lower right screen shows the test mode.

Test mode: Read

• Error processing

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen and increments the right-hand error counter.

If the error stop is set to "No", the system updates the error counter every time an error occurs and continues to execute the test. The system only displays the newest error information in the lower right screen. On the other hand, if the error stop is set to "Yes", the system stops the test if an error occurs. At the time, by pressing ENTER, the system continues the test and by pressing ESC, the test terminates. For details of error message, see "12-4-11-8. Error message".

10-4-11-5. Dump and Patch

The contents of the disk, the hexadecimal figure with the ASCII character, are displayed on the screen and are patched up. The contents of a sector (512KB) is displayed in two parts: the first half (256KB) and the second half (256KB).

• Operation

Specify the physical address to be dumped and patched.

Physical address = CCC.HH.SS

Type the cylinder number displayed by "CCC" and press ENTER. Type the head number displayed by "HH" and press ENTER. Type the sector number displayed by "SS".

When the entries have been complete, the screen appears with the data of the specified sector on the screen.

At this time, by pressing PGDN, a next sector or a second half of the sector is displayed and by pressing PGUP, a previous sector or a first half of the sector is displayed on the screen.

Moreover, by pressing SPACE, control exits "specify the physical address" and by pressing ESC, the test terminates.

To patch up, move the highlighting to the location you want to patch and type the figure with hexadecimal and press ENTER. The following message display on the lower screen. At this time, specify whether to update or not.

Update data ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER.

• Error processing

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen. For details of error message, see "12-4-11-8. Error message".

10-4-11-6. Disk controller check

The test checks the disk controller.

• Operation

Specify whether to repeat or do only once the test in the following message.

Aging mode ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When selection "Yes", the test will be repeated. On the other hand, when selecting "No", the test will be done only once. Specify whether to execute the test or not in the following message.

Test start ? [Yes No]

Move the highlighting to the mode you want to select and press ENTER. When entering "No", control exits to "specification of the aging mode". On the other hand, when entering "Yes", starts the test. Depression of ESC terminates the aging.

- **Error processing**

If the system detects an error while it executes the test, it displays the kind of error and where the error occurs on lower right screen. For details of error message, see "12-4-11-8. Error message".

10-4-11-7. Display error table

All error kinds, locations and counts are displayed for "Write-read check", "Read only check" and "Random seek check". However, this error information is limited to 40 locations.

- **Operation**

By pressing any key, the test terminates.

10-4-11-8. Error message

- **Bad command**

Shows that an invalid command is received.

- **Bad address mark**

Shows that the occurrence of an address mark read error.

- **Record not found**

Shows that the specified record is not found.

- **DMA boundary error**

Shows that the DMA error across 64Kb boundary.

- **Bad track**

Shows that a bad track is found.

- **Bad ECC on disk read**

Shows that the occurrence of an ECC error during data read.

- **Data corrected**

A error occurred but shows that the error was corrected by ECC.

- **Seek error**

Shows that the occurrence of an error during seek.

- **Bad controller**

Shows that the occurrence of any abnormality in the controller.

- **Time out error**

Shows that an interrupt responses from the controller was not received in the prescribed time.

- **Compare error**

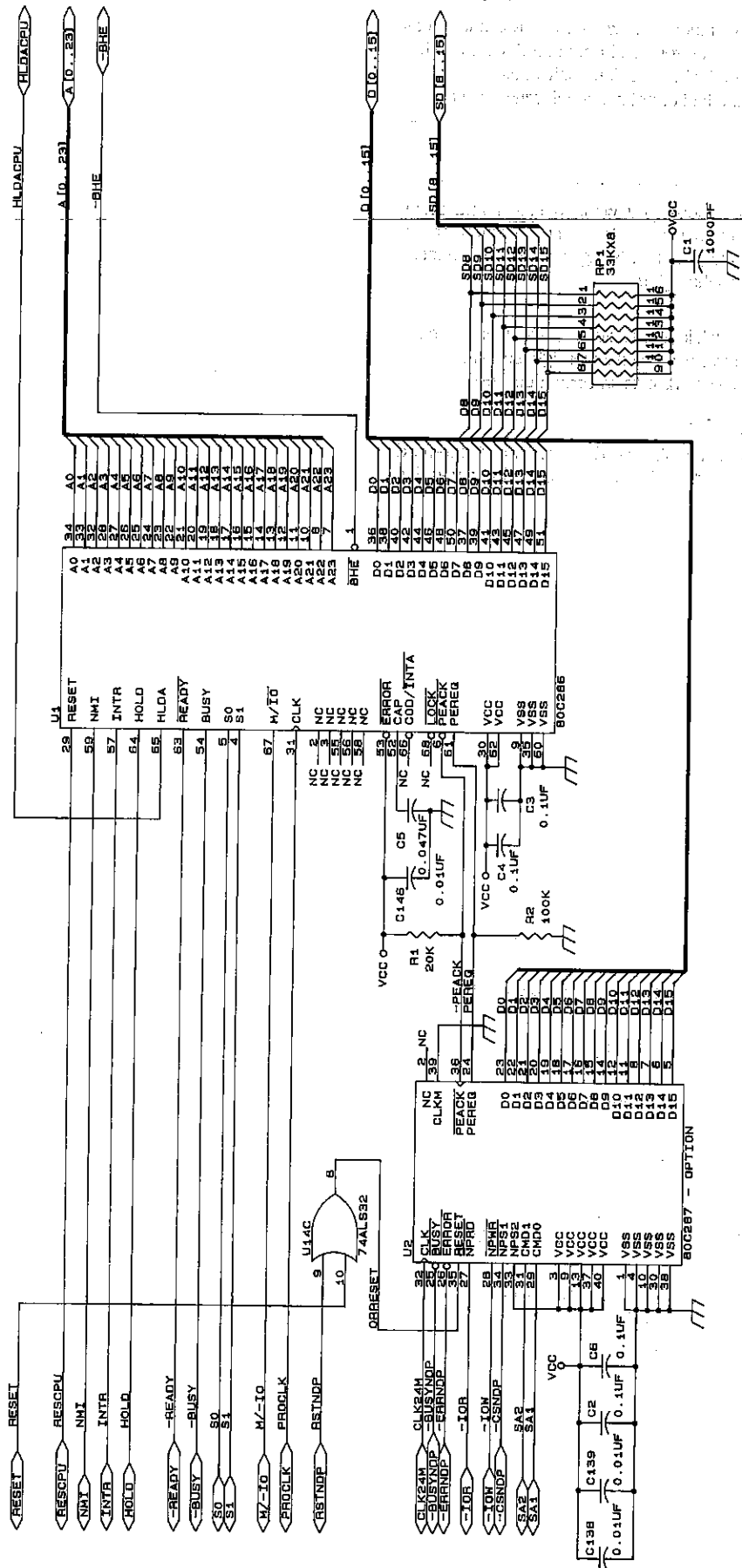
Shows that an unmatched of the write data with the read data.

- **Others error**

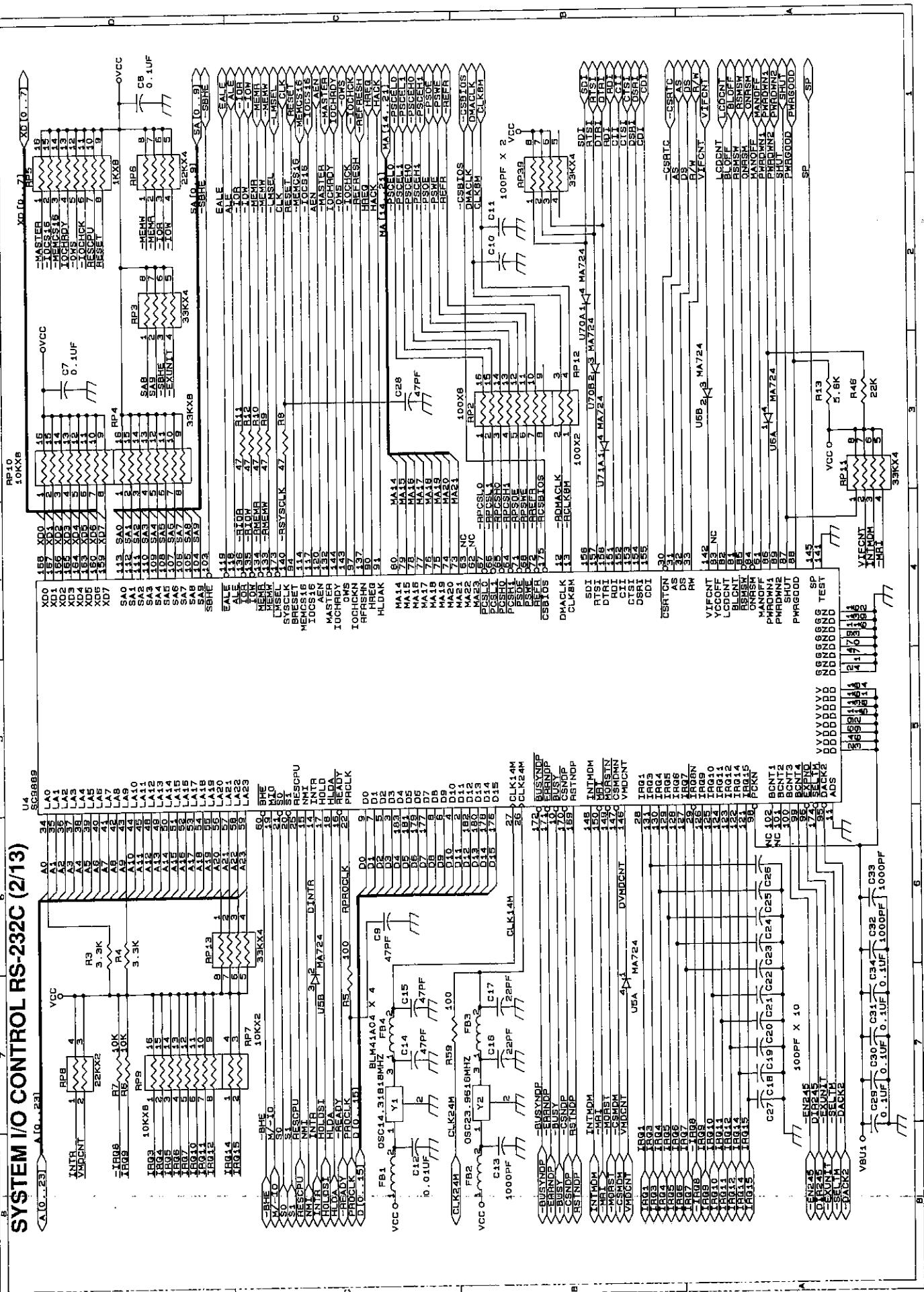
Shows that the occurrence of other errors not described above.

CHAPTER 11. CIRCUIT DIAGRAM AND PWB LAYOUT

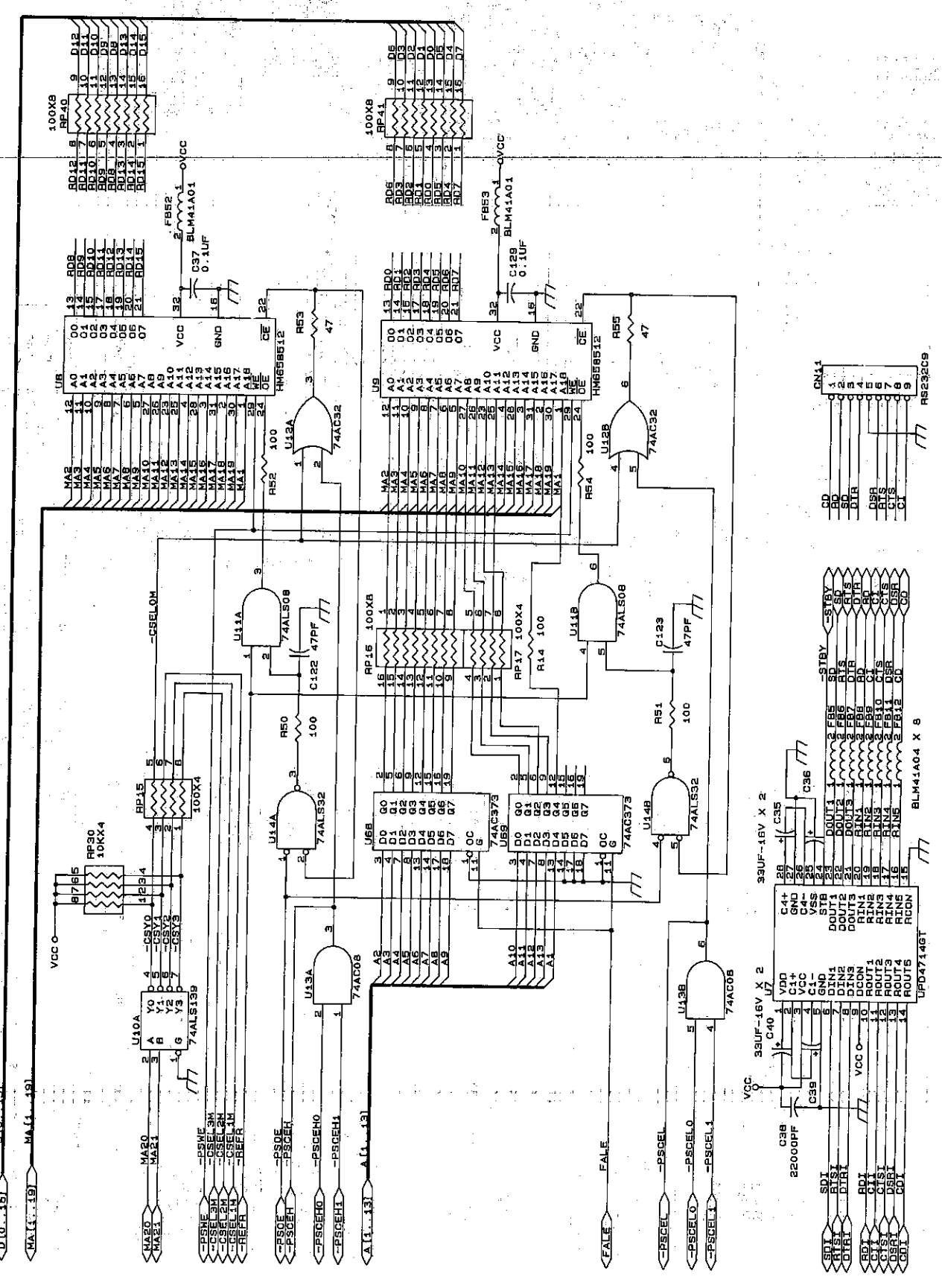
CPU & CO-PROCESSOR (1/13)



SYSTEM I/O CONTROL RS-232C (2/13)

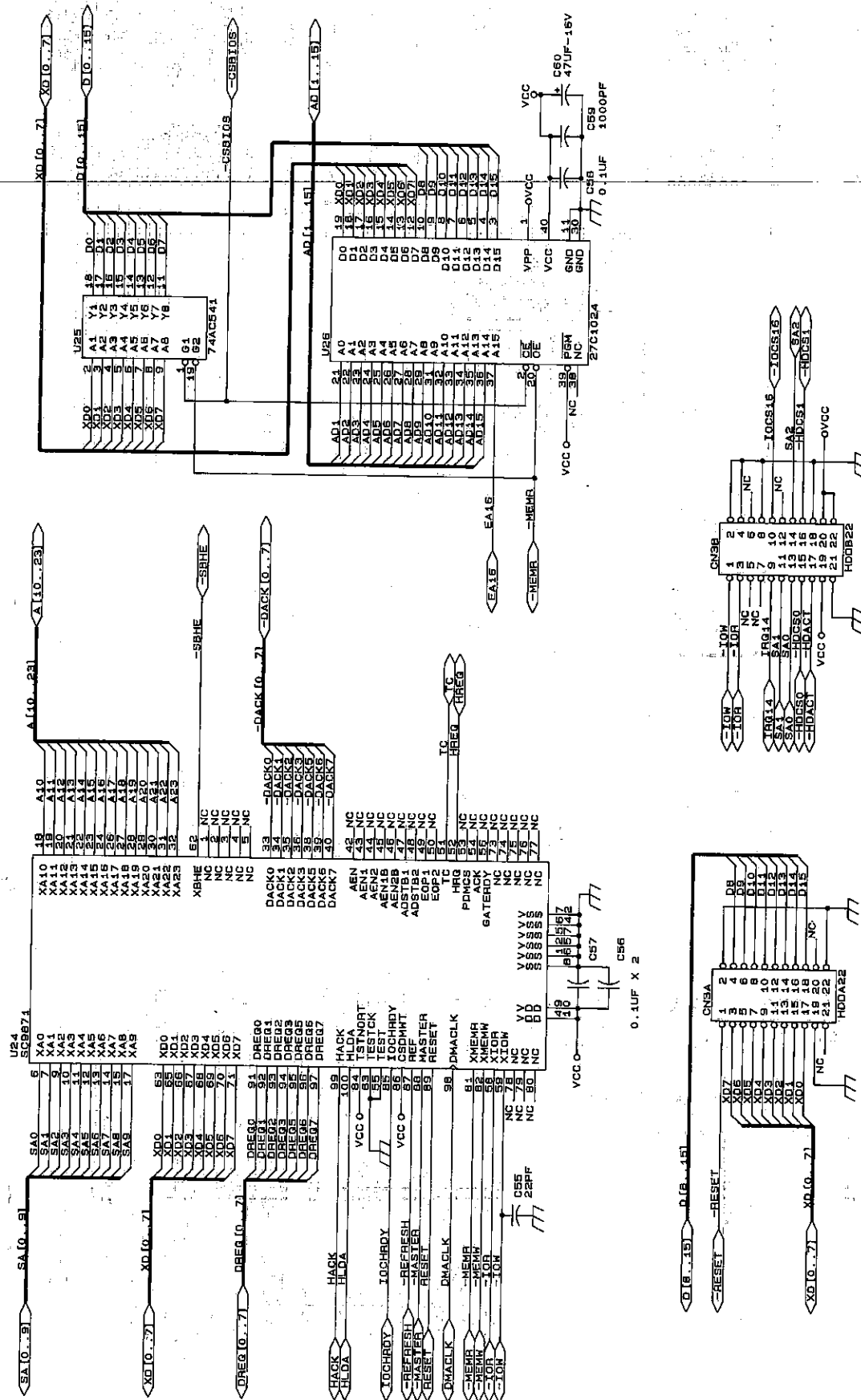


STANDARD MEMORY AND RS-232C DRIVER (3/13)



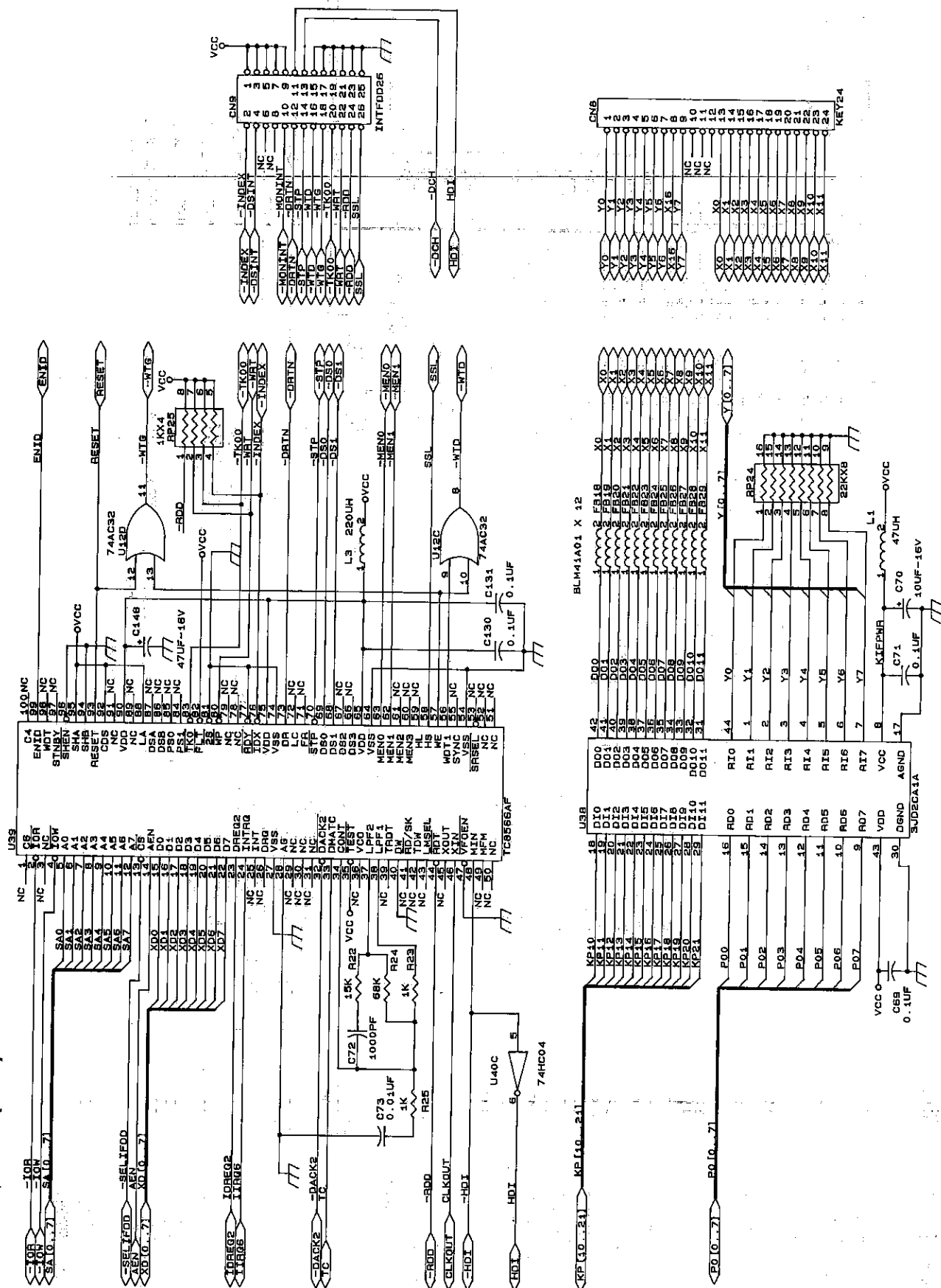


DMA CONTROLLER & BIOS ROM (5/13)





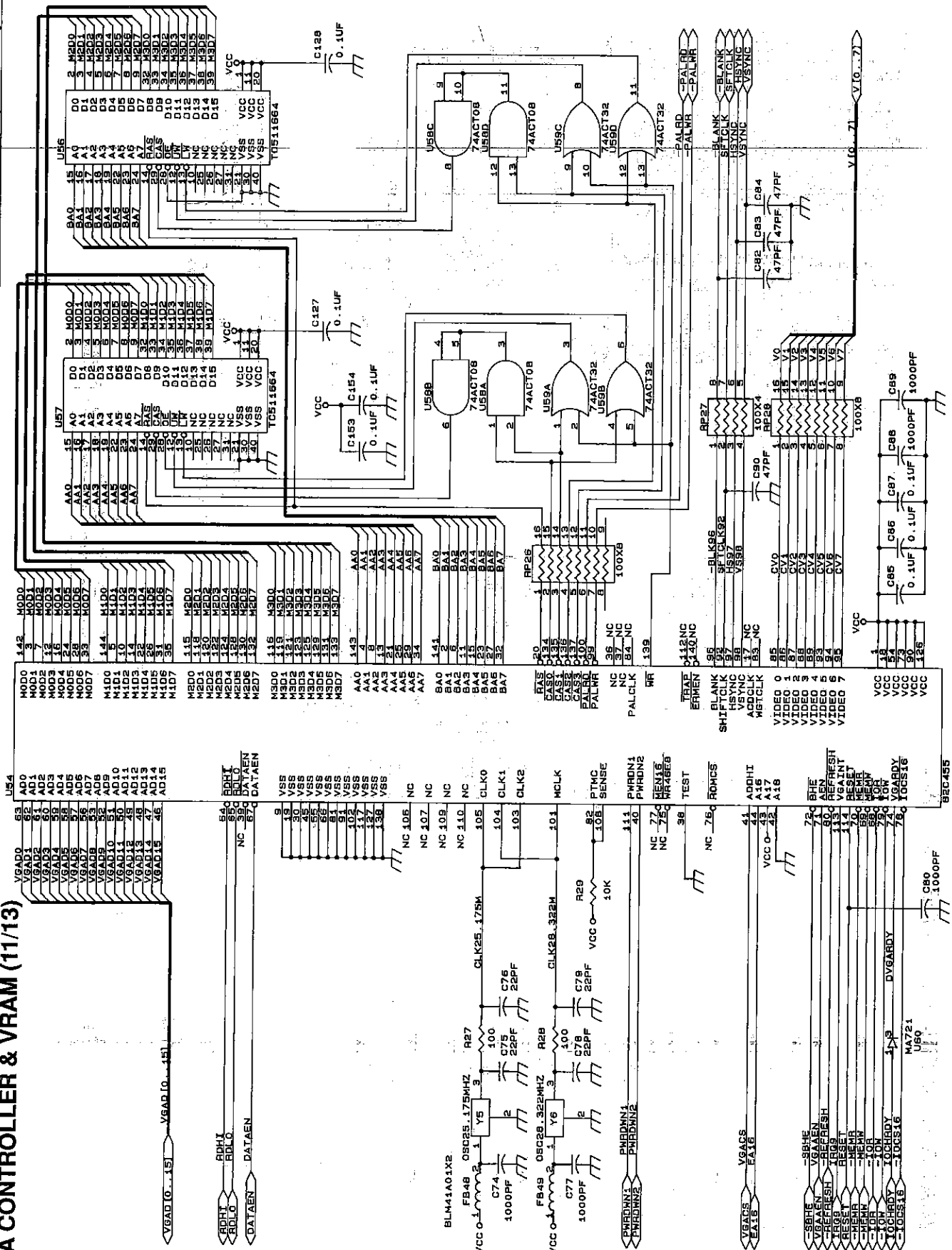
FDC & KEY I/F (7/13)





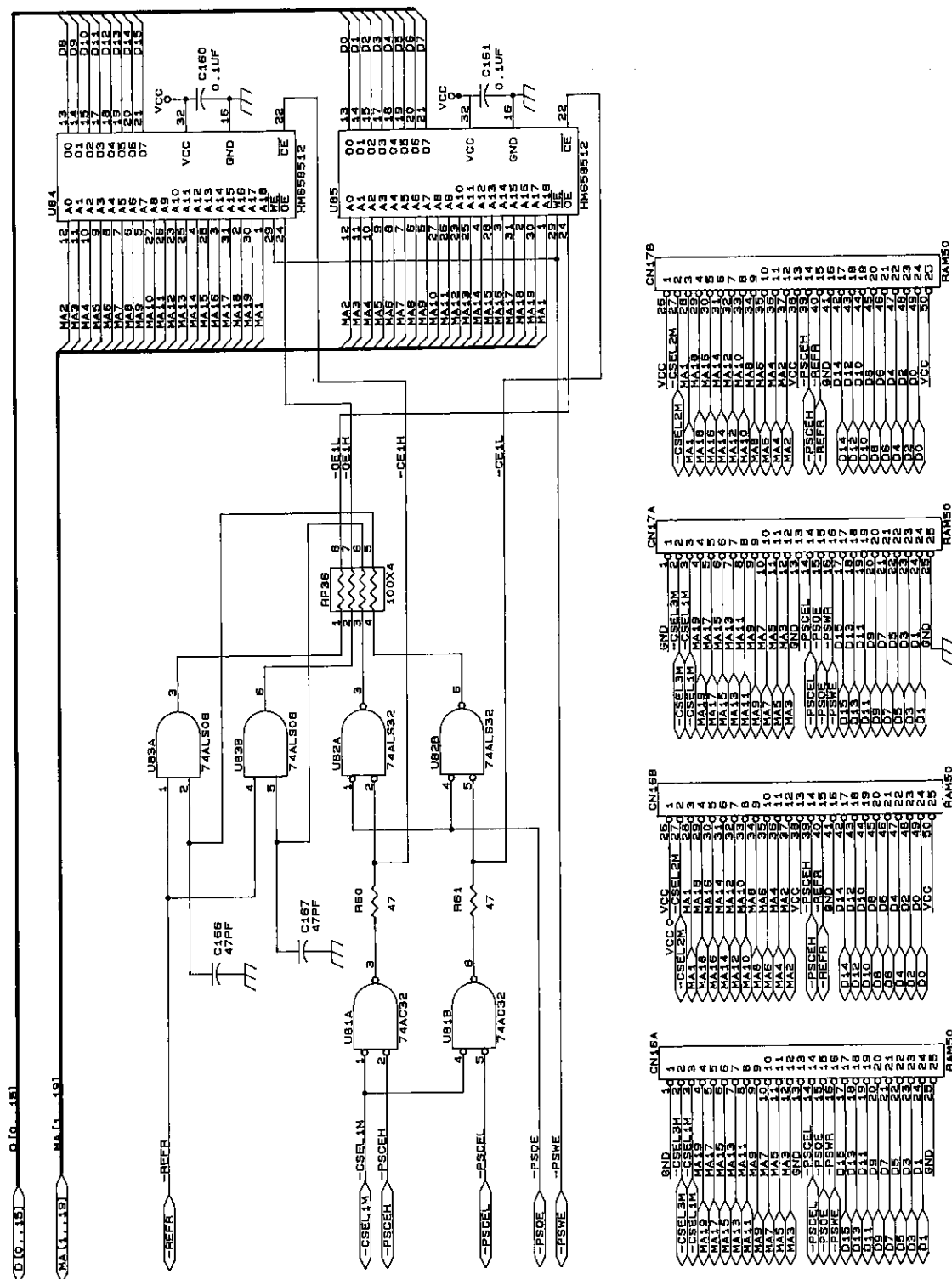


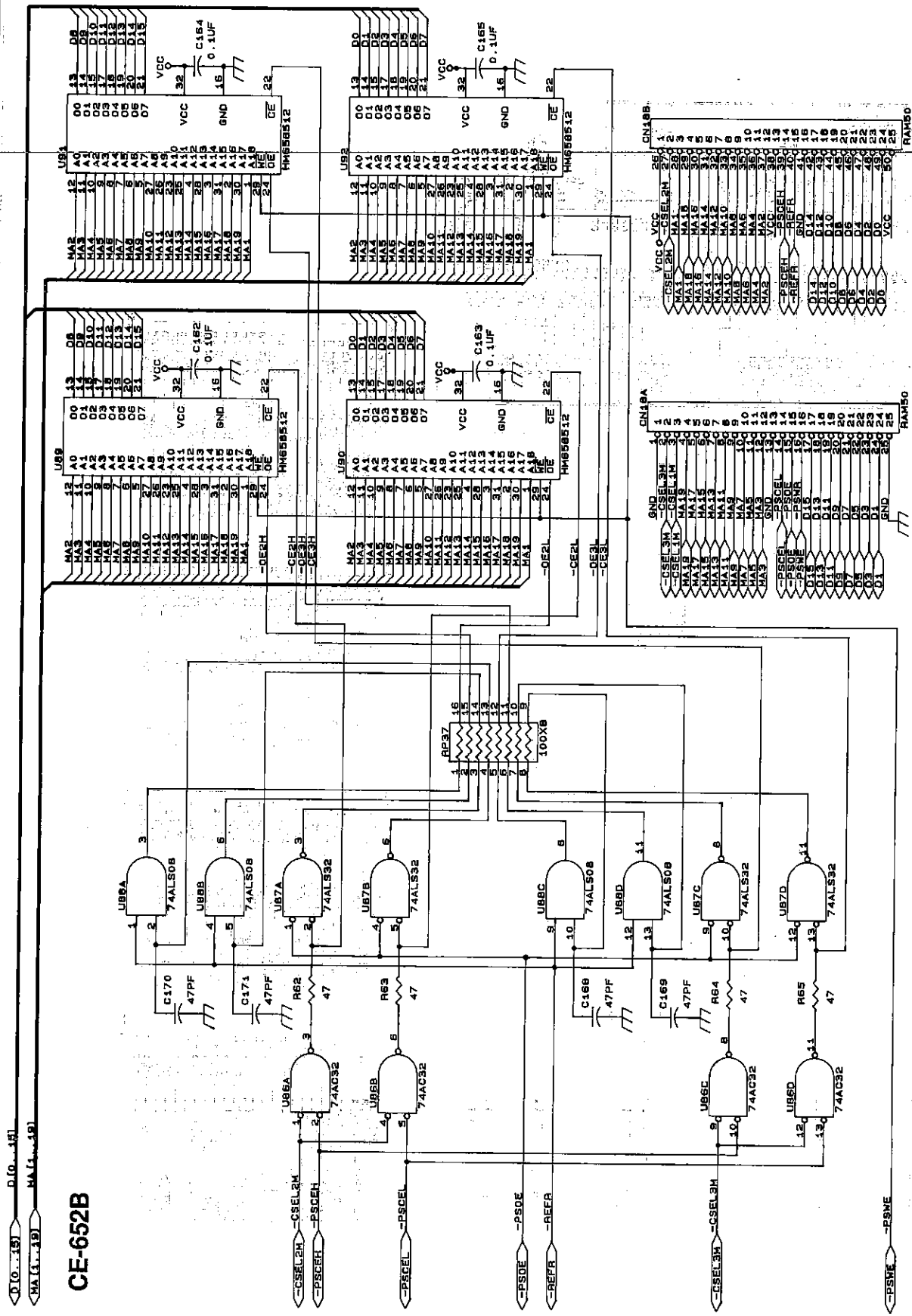
VGA CONTROLLER & VRAM (11/13)





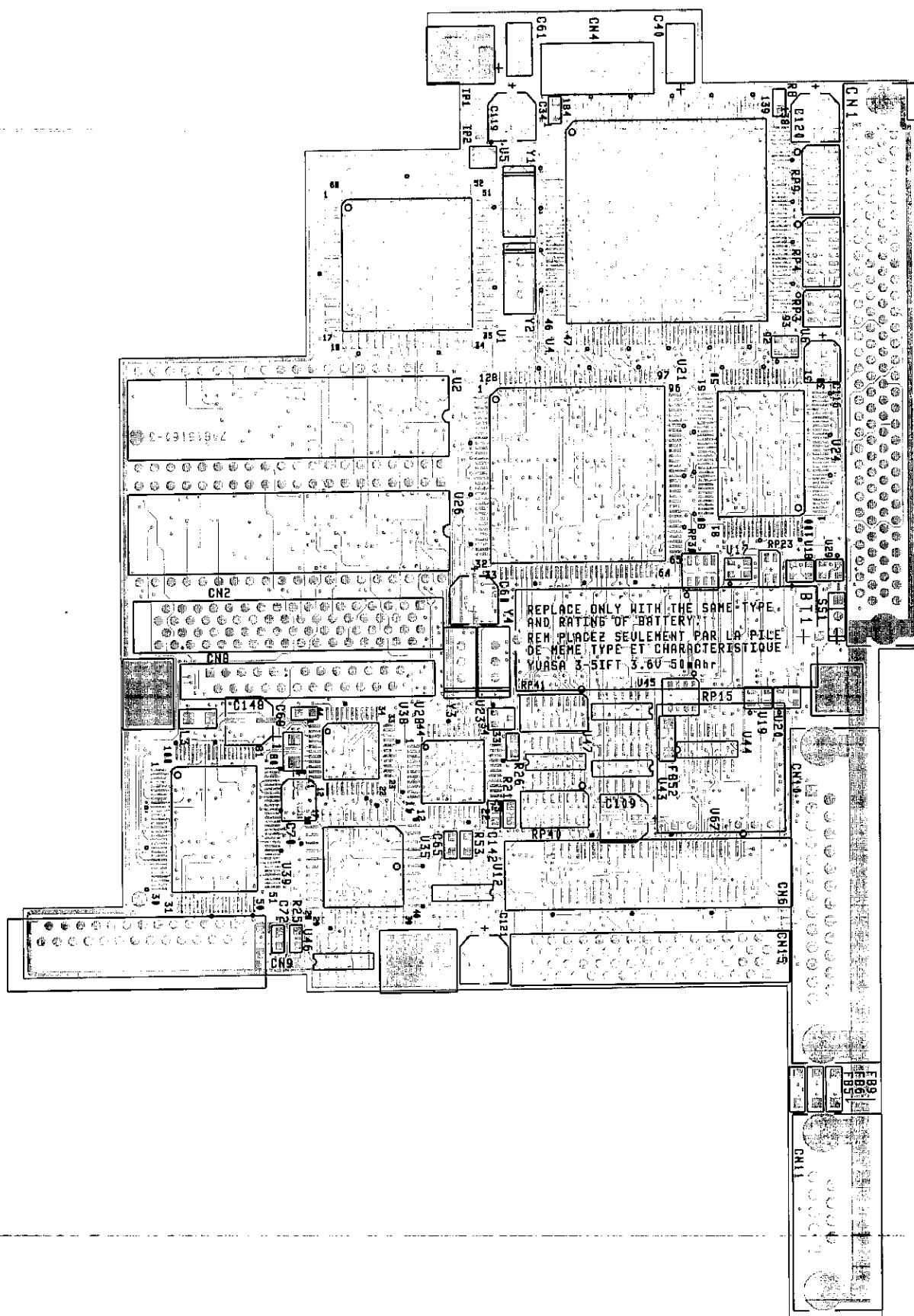






PWB LAYOUT

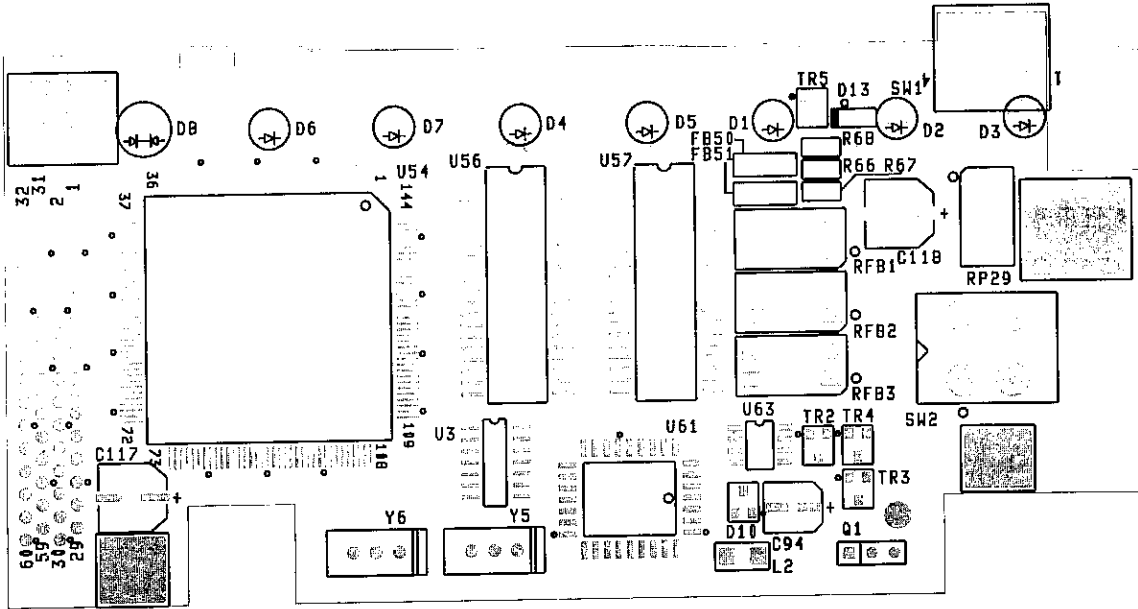
MAIN BOARD (PRIMARY SIDE)



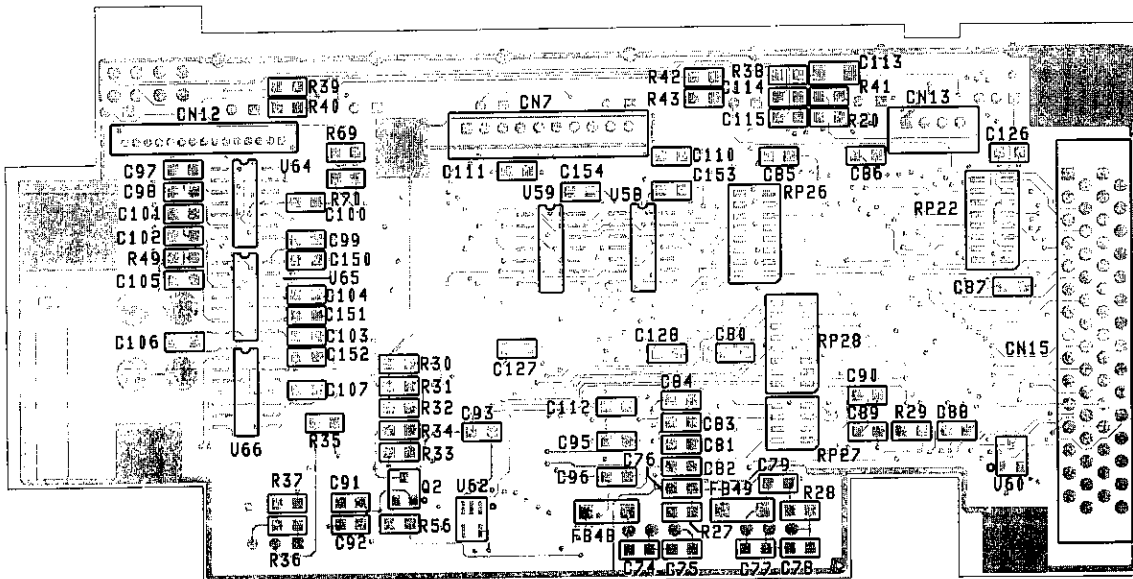


CRT BOARD

PRIMARY SIDE



SECONDARY SIDE



SHARP

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