SERVICE MANUAL FOR

9223

BY: Meg.chen

Technical Maintenance Department/GTK MTC

Nov.2009/R00

MiTAC

9223 N/B Maintenance

Contents

9223 N/B Maintenance

Contents

9223 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

The 9223 motherboard is Intel Montevina SFF Platform with Mobile Penryn ULV on Intel's advance 45 nm process technology with copper interconnect. The processor provides a high-performance low-power mobile processor based on the Intel Mobile processor architecture.

9223 platform implements Intel Cantiga GS40 SFF / ICH9-M SFF core logic. The Intel Cantiga GS chipset-based Memory Controller Hub and the Intel I/O Controller Hub 9 Mobile SFF(ICH9-M).

The GMCH component provide the host interface controller, system memory interface (SDRAM) ,Direct Media interface ,Integrated Graphics engine. The ICH9-M integrate a number of I/O device controller and interface for legacy and high-speed device.

9223 N/B Maintenance

1.2 System Overview

Basic Function		Spec	Remark
CPU			CPU 10W
	Type	Mobile Penryn Montevina ULV CPU SU2700 Mobile Penryn Montevina Celeron CPU C723	Montevina SFF SKU FSB 800
	TDP	10W TDP chassis design	Chipset NB low 7-8W,high 10-12.5W, SB 2.0-2.5W
Display		-13.3 1366x768 LED w/z driver -Max Brightness :TBD EDID Support	
Chipset		Intel Cantiga GS40 + ICH9M-enhanced SFF	
Memory			
	Type	DDRII 667/800 1GB/2GB	
	Slot	2 SO-DIMM	
	Max Size	4GB	

9223 N/B Maintenance

Continue to the previous page

Graphic		UMA	
Audio			
	Interface	Azalia	ALC 272
	Speaker	1.5W speaker x2	with Speaker Box
	Int. Mic	1 mic array	
	Volume	S/W volume control by K/B	
	Quality	TBD	
	Buzzer	Not Support	
Express Card			
	Slot Type	Express Card Type I 34 mm x1	PCI-E & USB interface support
	Function	Hot plug V	
Card Reader		3 in 1 (Realtek)	USB interface
	Slot Type	SD/MS/MS Pro/MMC	3 in 1 type

9223 N/B Maintenance

Continue to the previous page

Communication		Spec		Remark
LAN				
	Conn. I/F	RJ45 Jack		RTL8111DL
	Slot Type	On board LAN solution		
	Spec	10/100/1000 LAN (PCI-E)		
	Function	Boot on LAN	V	
		Wake on LAN in S3	V	
		Wake on LAN in S4	X	
		Alert on LAN	X	

9223 N/B Maintenance

Continue to the previous page

Wireless LAN			
	Slot Type	Mini PCI-E x2	
	Antenna	MIMO	1.3G (EU first) + MIMO + BT for antenna (US 2nd priority) 2.All Antenna on top
	Module Spec	1.802.11 b/g/n , AW-NE771 2.3G , EM770	MIMO
	Others	Radio wave enable by Fn+F1 key or killer Switch	
	Power on status	Remain the same status of last power off	

9223 N/B Maintenance

Continue to the previous page

Bluetooth			BTO if possible
	Slot Type	8 pin	Test criteria: 1Mbps @10m
	Antenna	Antenna on panel top	
	Module Spec	AW-BT252	
	Others		
	Power on status		
Webcam			
	Slot Type		
	Module Spec	AuzreWave, AM-1B013	
	Interface	USB/UVC function	

9223 N/B Maintenance

Continue to the previous page

Storage Device		Spec	Remark
HDD		SATA I/F,2.5'' height HDD	160/250/320 GB
ODD		9.5mm height ODD	SATA interface
	Type	Super Multi/DVD-Dual/DVD COMBO	Digital support only
	Structure		
I/O Interface		Spec	Remark
Video output		D-sub x 1	Vista
USB		Port x3 (USB2.0)	
Audio Jack		HP Out	**Black**
		Mic in	**Black**
LAN		RJ45	
User Interface		Spec	Remark
Button /Switch			One touch solution
	Power button	Push button type	
	ECO	Push button type	

9223 N/B Maintenance

Continue to the previous page

Status LED			
	WLAN	Blue	
	AC/BATT	Blue/Red	
	Charge	Blue	
	HDD/ODD	Blue	
	Caps Lock	Blue	
	Num Lock	Blue	
	PWR button	Blue	
	ECO button	Blue	
Input Device		Spec	Remark
Keyboard			
	Pitch/Stroke	19mm Pitch/1.7mm Stroke	

Continue to the previous page

Dimension	300mm			
Function Key		OS	Beep	
Radio on/off	Fn+F1 (WLAN)	Windows	TBD	
Radio on/off	X		TBD	
Sound down	Fn+F3	Windows	TBD	
Sound up	Fn+F4	Windows	TBD	
Display Change	Fn+F5	Dos/Windows	TBD	Behaviour: LCD→LCD+CRT→CRT→LCD
Brightness down	Fn+F6 16 levels	Dos/Windows	TBD	Switch to battery model still keep original brightness level
Brightness up	Fn+F7 16 levels	Dos/Windows	TBD	
T/P on/off	X		TBD	
Mute on/off	Fn+F10	Windows	TBD	Mute system master volume
Panel on/off	Fn+F11	Dos/Windows	TBD	Backlight Off
Suspend	Fn+F12	Windows	TBD	

9223 N/B Maintenance

Continue to the previous page

Pointing Device		Synaptics: TM391	Under plastic
	Function	Glide pad with 2 buttons	
	Pin	12 Pin	
Power		Spec	Remark
Battery			Gauge IC 20Z90
	Type	Li-ion type	
	Capacity	2250mAh	
	Cells No.	6 cells	
	Battery Life	Target: 4.5 hours with backlight min. with 6 cell battery	ECO mode
	Power off Charge	Target:2 hrs to 90%(6 cells)	
	Power on Charge	Target: TBD	Idle mode
	S3 Suspend Time	Target: TBD	
	RTC Battery	Not chargeable	5 years battery life

9223 N/B Maintenance

Continue to the previous page

AC Adapter		65W 3 pin DC	
	Input	AC 100-240V	
	Vendor	Delta	
Leakage Current		Battery remain 20% after 30 Days w/z 100% battery capacity (6 cell)	TBD

9223 N/B Maintenance

1.3 Function Description

1.3.1 CPU

• The Penryn Processor SU2700 on 45-nanometer process technology (also referred to as CPU and processor in this document) with the following new features:

• 800-MTs Source-Synchronous Front Side Bus (FSB)

• Intel® Trusted Execution Technology (Intel® TxT)

• SSE4.1 instructions

• New Deep Power Down Technology (also called C6 state) low power state which further reduces power consumption when the processor is idle

• Enlarged 2-MB L2 cache memory

1.3.2 CORE LOGIC

9223 N/B Maintenance

❖ Cantiga

- The Cantiga chipset Graphics Memory Controller Hub (also referred to as the (G)MCH in the document) and ICH9M I/O controller hub with the following new features.
- Gen 5.0 Integrated Graphics Engine
- 400-MHz core render clock at 1.05-V core voltage
- Support for DDR2 at 800 and 667 MTs

❖ ICH9-M

- The ICH9M I/O controller hub (also referred to as ICH9M in the document) is a follow-on product to Intel ICH8M with the following enhancements.
- 12 USB ports
- 4 SATA ports
- Support for Intel® Active Management Technology (Intel® AMT) 4.0
- Support for Integrated Trusted Port module 1.2
- CPU Deep Power Down Technology (also called C6 state) state support

1.3.3 Memory

Support DDR2 667/800 MHz SO-DIMM expandable to 4GB (2 DDR2-SODIMM slots)

Slot1	Slot2	Total
1GB	0GB	1GB
2GB	0GB	2GB
1GB	1GB	2GB
2GB	2GB	4GB

1.3.4 I/O PORTS

- CRT Port
  - Standard VGA compatible port
  - DDC1 and DDC2B compliant

PIN	SIGNAL	DESCRIPTION
1	CRT_RED	Red analog video output
2	CRT_GREEN	Green analog video output
3	CRT_BLUE	Blue analog video output
4	Monitor Sense	NC
5	GND	Monitor Sense
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	NC
12	CRT_DDDA	Data from DDC monitor
13	CRT_HSYNC	Horizontal Sync control
14	CRT_VSYNC	Vertical Sync control
15	CRT_DDCK	Clock to DDC monitor

❖ RJ-45

- RTL8111DL Integrated 10/100/1000 transveiver
- Supports PCI ExpressTM 1.1
- Auto-Negotiation with Next Page capability

9223 N/B Maintenance

• The Fast Ethernet MAC Controller features an IEEE802.3 and IEEE802.3x compliant MAC with external LAN physical layer chip supporting full duplex control.

• Support Wake-up On-LAN function from S3.

Pin	Signal Name	Direction	Description
1	PJTX+	Out	Transmit Data Ring
2	PJTX-	Out	Transmit Data Tip
3	PJRX+	IN	Receive Data Ring
4	PJRX-	IN	Receive Data Tip.
5	MDO2+ / RJ45_PJ4	-	Internal termination resistor
6	MDO2- / RJ45_PJ4	-	Internal termination resistor
7	MDO3 + / RJ45_PJ7	-	Internal termination resistor
8	MDO3 - / RJ45_PJ7	-	Internal termination resistor

❖ USB Ports

• Four industry standard USB 2.0 ports (Backward compatible to USB 1.1)

- Support maximum transfer rate up to 480Mbits/s

Pin	Signal Name	Direction	Description
1	VCC	Power	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	Ground	Ground

❖ Card Reader Port

- Support SD, MMC, Memory Stick, Memory Stick Duo (adapter), Memory Stick Pro.
- 3 in1 combo connector

1.3.5 DISPLAY

- 13.3” WXGA(1366x768 pixels) display size for notebook PC
- LED Backlight with LED controller IC
- Glare Surface
- Bezel less structure

1.3.6 READ ONLY MEMORY (SPI Serial Flash)

- Fully compatible with industry standard software including Windows Vista.
- Fully supports APM V1.2 and latest ACPI specification
- 1Mx8 (8Mbit) SPI Serial Flash BIOS
- Phoenix BIOS core (EFI)

1.3.7 POWER MANAGEMENT FEATURES

- Local standby mode (Individual devices such as HDD, graphics controller, LCD etc..)

- CPU Idle mode (Including ACPI modes C0, C1, C2, C3,C4 and C6)
- Suspend mode (S3 & S4 ACPI modes)
- Fully APM-base legacy power.
- Fully ACPI V1.0b, 2.0 and 3.0, compliant.
- Hibernate for Vista.
- Thermal management.

1.3.8 KEYBOARD CONTROLLER

- Winbond W83L951D.

1.3.9 LEDs INDIACTOR

- WiFi & AC/BAT & Charger & CDROM +HDD & Cap lock & Num lock.

1.3.10 TOUCH PAD MODULE

- Synaptics TM61P-391

1.4 Electrical Characteristic

1.4.1 Power Consumption Of Suspend Mode

- Suspend To RAM < 50mA
- Suspend To Disk / Soft-Off /Mechanical Off < 1mA

Power		Spec	Remark
Battery			Gauge IC 20Z90
	Type	Li-ion type	
	Capacity	2250mAh (P) (S)	
	Cells No.	6 cells	
	Battery Life	Target: 4.5 hours with backlight min. w/z 6 cell battery	ECO mode

9223 N/B Maintenance

	Power off Charge	Target:2 hrs to 90%(6 cells)	
	Power on Charge	Target: TBD	Idle mode
	S3 Suspend Time	Target: TBD	
	RTC Battery	Not chargeable	5 years battery life
AC Adapter		65W 3 pin DC	
	Input	AC 100-240V	
	Vendor	Delta	
Power Consumption		Battery remain 20% after 30 Days w/z 100% battery capacity (6 cell)	TBD

1.5 Reference Documents

Documents	Revision
Montevina Platform Design Guide for Penryn Processor, Cantiga Chipset and ICH9M I/O Controller Hub	2.1
Penryn Processor for Montevina Platform	2.2
Cantiga Chipset External Design Specification (EDS)	2.4
Intel® I/O Controller Hub 9 (ICH9) Family External Design Specification (EDS) – Volume 1	2.3
Realtek ALC272	0.9
Realtek RTS5159 USB 2.0 Card Reader Controller	0.93
PC2001 System Design Guide	0.7
PCI Local Bus Specification	2.2
SILEGO SLG8SP552	0.1

9223 N/B Maintenance

- Appendix B Function Key Definition

Function Key		
Radio on/off	Fn+F1 (WLAN)	w/o bibi sound
Radio on/off	Fn+F1 (Bluetooth)	TBD
Sound down	Fn+F3	w/o bibi sound
Sound up	Fn+F4	w/o bibi sound
Display Change	Fn+F5	W/o bibi sound
Brightness down	Fn+F6 8 levels	w/o bibi sound Could control it in DOS mode
Brightness up	Fn+F7 8 levels	
Mute on/off	Fn+F10	Mute system master volume
Panel on/off	Fn+F11	Disable backlight
		w/o bibi sound
Suspend	Fn+F12	w/o bibi sound
Power low		w/z bibi sound

9223 N/B Maintenance

2. System View and Disassembly

2.1 System View

2.1.2 Left-side View

❶ Power Connector
❷ VGA Port
❸ USB Port
❹ RJ-45 Connector
❺ Card Reader
❻ Express card slot

2.1.2 Right-side View

❶ Super Multi Drive
❷ Audio output Connector
❸ Microphone Connector
❹ USB Port
❺ Kensington Lock

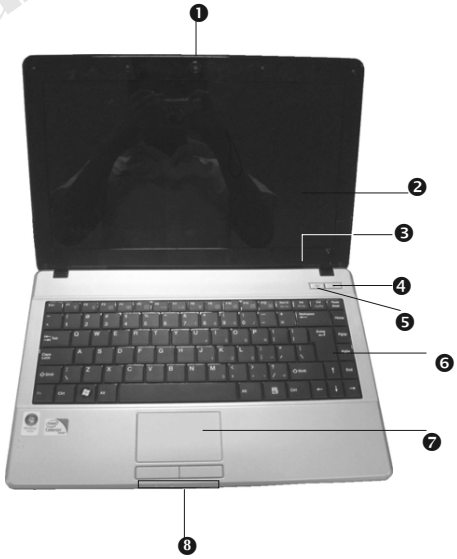
9223 N/B Maintenance

2.1.3 Bottom View

❶ Battery Pack

❷ Stereo Speaker

2.1.4 Top-open View



❶ Camera

❷ LCD Screen

❸ Microphone

❹ Power Button

❺ ECO Button

❻ Keyboard

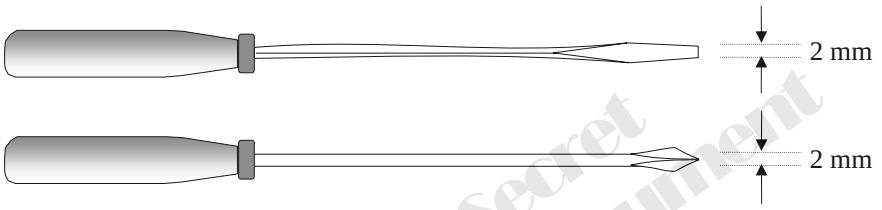
❼ Touch Pad

❽ Indicators

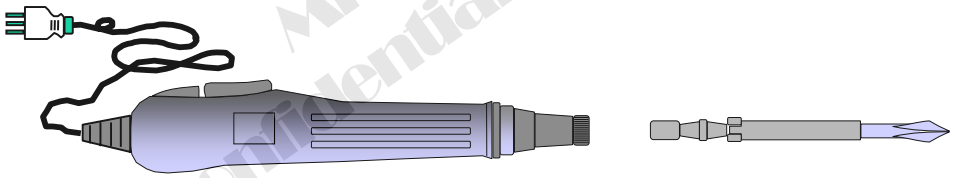
9223 N/B Maintenance

2.2 Tools Introduction

1. Screw driver with bit size for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

#0

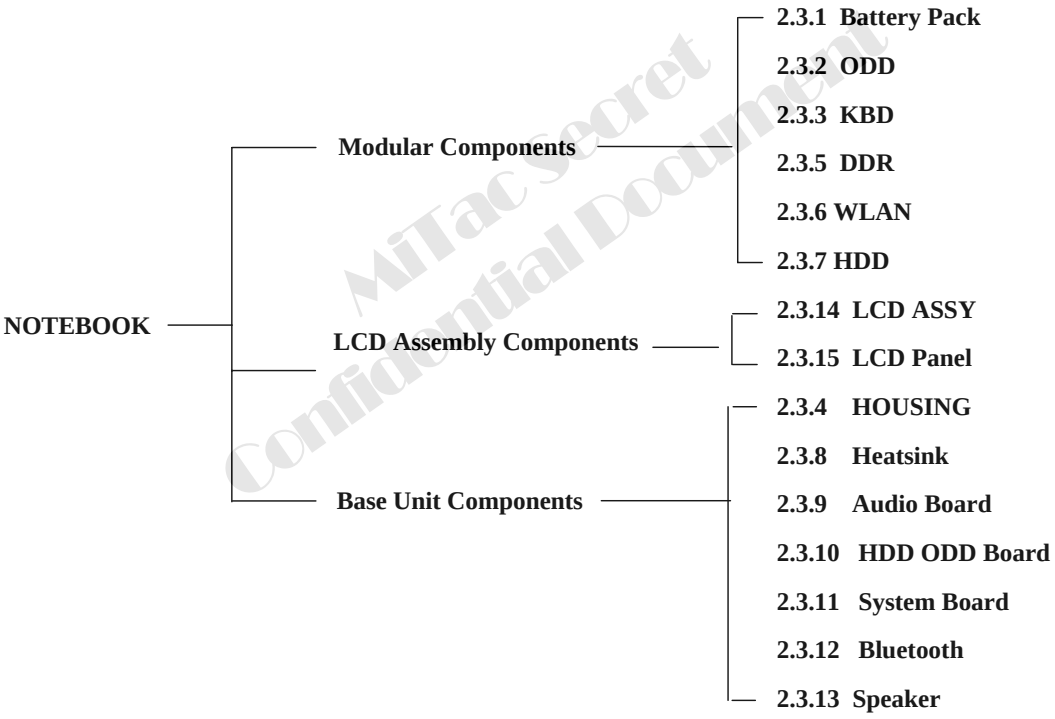
Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto Screwdriver	2.0-2.5 kg/cm2	#0

9223 N/B Maintenance

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



9223 N/B Maintenance

2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide two release levers outwards to the “unlock” ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” ( ) position.

9223 N/B Maintenance

2.3.2 ODD

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove one screw fastening the CD-ROM module to free the ODD (Figure 2-2)

Figure 2-2 Remove the ODD

Reassembly

1. Replace the ODD module, then secure with one screw.
2. Reassemble the battery pack. (See section 2.3.1 Reassembly)

9223 N/B Maintenance

2.3.3 KBD

Disassembly

1. Remove the battery pack. (See section 2.3.1 Disassembly)

2. Loosen the six latches locking the keyboard. (Figure 2-3)
3. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard (Figure 2-4)

Figure 2-3 Loosen the six latches

Figure 2-4 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with six latches.
2. Replace the battery pack. (See section 2.3.1 Reassembly)

9223 N/B Maintenance

2.3.4 Housing

Disassembly

1. Remove the battery pack, ODD. (See section 2.3.1~2.3.2 Disassembly)
2. Remove sixteen screws and two Dummy card to free the housing. (Figure 2-5~2-6)

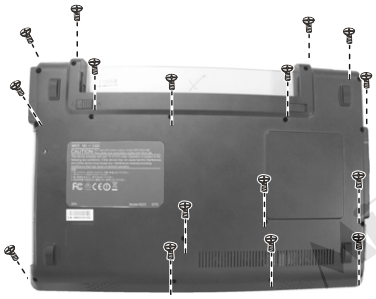


Figure 2-5 Remove the eighteen screws

Figure 2-6 Remove the two dummy card

Reassembly

1. Replace the housing and secure with sixteen screws and dummy card.
2. Replace the battery pack, ODD. (See section 2.3.1~2.3.2 Reassembly)

9223 N/B Maintenance

2.3.5 DDR

Disassembly

1. Remove the battery pack, ODD, Housing. (See section 2.3.1~2.3.2, 2.3.4 Disassembly)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-7)

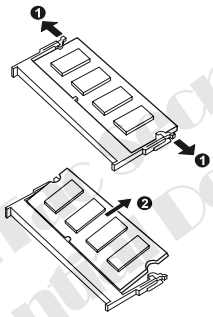


Figure 2-7 Remove the SO-DIMM

Reassembly

1. To install the DDR2, match the DDR2's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR2 into position.
3. Replace the battery pack, ODD, Housing. (See section 2.3.1~2.3.2, 2.3.4 Disassembly)

2.3.6 Wlan

Disassembly

1. Remove the battery pack, ODD, Housing. (Refer to section 2.3.1~2.3.2, 2.3.4 Disassembly)
2. Disconnect the two antennae first, then remove two screws to free the wlan. (Figure 2-8)

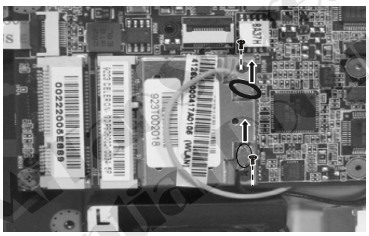


Figure 2-8 Free the Wlan

Reassembly

1. Replace the wlan and secure with two screws.
2. Reconnect two antennae into wlan.
3. Replace the battery pack, ODD, Housing. (Refer to section 2.3.1~2.3.2, 2.3.4 Reassembly)

2.3.7 HDD

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.6 Disassembly)
2. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-9)

Figure 2-9 Remove HDD

Reassembly

1. Slide the HDD module into the compartment and secure with one screw.
2. Replace the battery pack. ODD, Housing. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.6 Reassembly)

2.3.8 Heatsink

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.7 Disassembly)
2. Remove five screws that secure with heatsink and disconnect the cable from system board. (Figure 2-10)

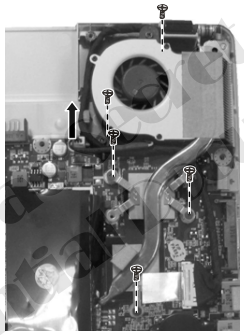


Figure 2-10 Remove heatsink

Reassembly

1. Replace the heatsink and secure with five screws.
2. Reconnect the cable from system board.
3. Replace the battery pack., ODD, Housing, WLAN, HDD. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.7 Reassembly)

2.3.9 Audio BD

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.8 Disassembly)
2. Disconnect the three cables from audio board then remove one screw that secure with audio Board. (Figure 2-11)

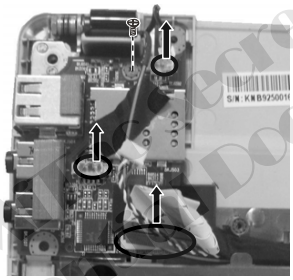


Figure 2-11 Remove audio board

Reassembly

1. Replace the audio board and secure with one screw.
2. Reconnect the three cables to system board.
3. Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.8 Reassembly)

2.3.10 HDD ODD Board

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.9 Disassembly)
2. Disconnect the cable from system board then pick up the HDD ODD board. (Figure 2-12)

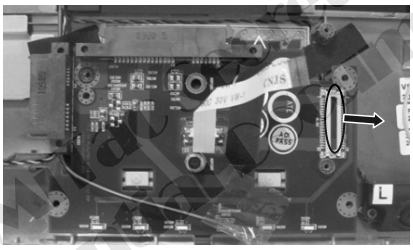


Figure 2-12 Remove HDD ODD board

Reassembly

1. Replace the HDD ODD board and reconnect the cable to system board.
2. Replace the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.9 Reassembly)

9223 N/B Maintenance

2.3.11 System Board

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.10 Disassembly)
2. Disconnect the three cables and remove threes screws from system board. (Figure 2-13)
3. Disconnect the cable from the back of the system board. (Figure 2-14)

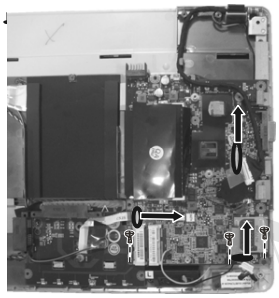


Figure 2-13 Remove three screws and three cables

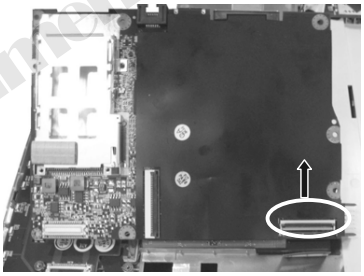


Figure 2-14 Remove System board

Reassembly

1.Reconnect the cable from the back of the system board.
2.Replace the system board and secure with three screws and reconnect the cable from system board.
3.Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.10 Reassembly)

2.3.12 Bluetooth

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.11 Disassembly)
2. Remove one screw to free the Bluetooth board. (Figure 2-15)

Figure 2-15 Remove Bluetooth board

Reassembly

1.To install the Bluetooth and secure with one screw .
2. Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.11 Reassembly)

2.3.13 Speaker

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.12 Disassembly)
2. Remove four screws to free the speaker. (Figure 2-16)

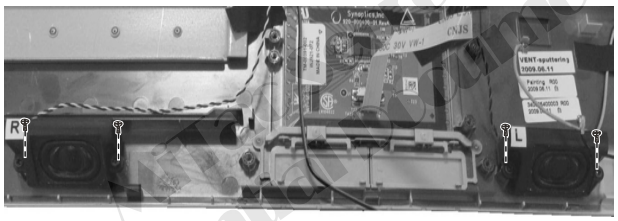


Figure 2-16 Remove speaker

Reassembly

1.To install the speaker and secure with four screws .
2. Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.12 Reassembly)

2.3.14 LCD ASSY

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth, Speaker. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.13 Disassembly)
2. Remove two screws to free the LCD ASSY. (Figure 2-17)

Figure 2-17 Remove two screws

Reassembly

1. Replace the LCD assembly and secure with two screws.
2. Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth, Speaker. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.13 Reassembly)

2.3.15 LCD Panel

Disassembly

1. Remove the battery pack, ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth, Speaker, lcd assy. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.14 Disassembly)
2. Remove two screws fastening the LCD cover. (Figure 2-18)
3. Remove two caps, Then remove two screws fastening the LCD cover. (Figure 2-19)
4. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
5. Carefully lift up the panel from the LCD housing.

Figure 2-18 Remove two screws

Figure 2-19 Remove hinges

6. Remove four screws fastening the LCD panel. (Figure 2-20)
7. Disconnect the cable to free the LCD panel. (Figure 2-21)

Figure 2-20 Remove four screws

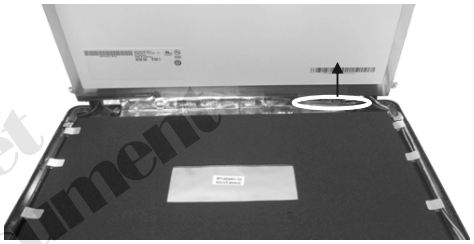


Figure 2-21 Remove cable

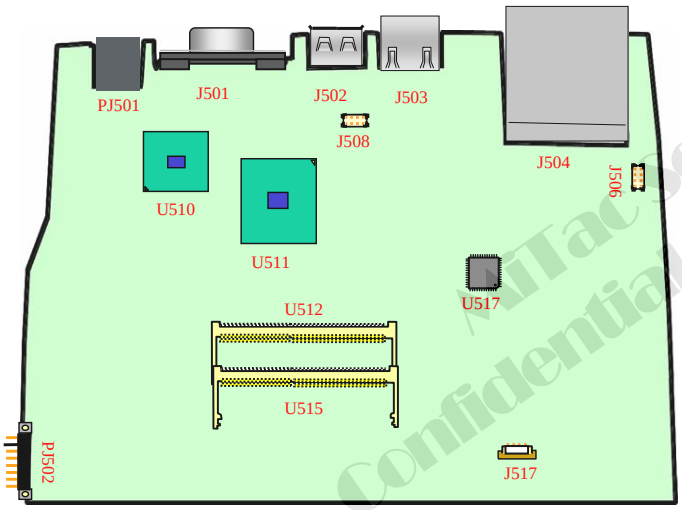
Reassembly

1. Replace the cable to the LCD, then replace LCD panel into the LCD housing and secure with four screws .
2. Replace the LCD cover and secure with four screws, then replace the two caps.
3. Replace the battery pack., ODD, Housing, WLAN, HDD, Heatsink, Audio board, HDD ODD board, System board, Bluetooth, Speaker, LCD assy. (Refer to section 2.3.1~2.3.2, 2.3.4~2.3.13 Reassembly)

9223 N/B Maintenance

3. Definition & Location of Major Components

3.1 Mother Board (Side A)

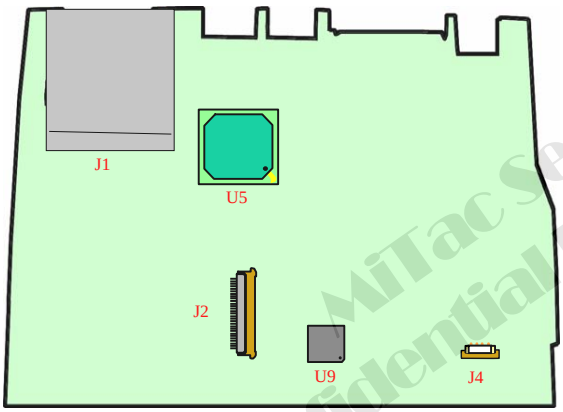


- **PJ501 : Power Connector**
- **J501 : VGA Connector**
- **J502 : USB Connector**
- **J503 : RJ45 Connector**
- **J504 : Card Reader Connector**
- **PJ502 : Battery Connector**
- **U510 : CPU**
- **U511 : Cantiga-GS40 North Bridge**
- **J508 : LCD Connector**
- **J506 : Bluetooth Connector**
- **J517 : Touch Pad Connector**
- **J512,J515 : DDR2 SO-DIMM Socket**
- **U517 : System Bios**

9223 N/B Maintenance

3. Definition & Location of Major Components

3.1 Mother Board (Side B)



- **J1 : Express Card Socket**
- **U5 : ICH9M South Bridge**
- **U9 : Keyboard Controller**
- **J4 : MB to Audio board**
- **J2 : Keyboard Connector**

4. Pin Descriptions of Major Components

4.1 Cantiga North Bridge -1

Host Interface Signals

Signal Name	Type	Description
H_A#[35:3]	I/O AGTL+ 2X	Host Address Bus: HA#[35:3] connects to the processor address bus. During processor cycles the HA#[35:3] are inputs. The (G)MCH drives HA#[35:3] during snoop cycles on behalf of PCI Express/Internal Graphics or ICH. HA#[35:3] are transferred at 2x rate. Note that the address is inverted on the processor bus.
H_ADS#	I/O AGTL+	Host Address Strobe: The system bus owner asserts H_ADS# to indicate the first of two cycles of a request phase. The (G)MCH can also assert this signal for snoop cycles and interrupt messages.
H_ADSTB#[1:0]	I/O AGTL+ 2X	Host Address Strobe: HA#[31:3] connects to the processor address bus. During processor cycles, the source synchronous strobes are used to transfer HA#[35:3] and HREQ#[4:0] at the 2x transfer rate. Strobe / Address Bits HADSTB#0 / HA#[15:3], HREQ#[4:0] HADSTB#1 / HA#[35:16]
H_AVREF H_DVREF	I A	Host Reference Voltage: Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface
H_BNR#	I/O AGTL+	Host Block Next Request: Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
H_BPRI#	O AGTL+	Host Bus Priority Request: The (G)MCH is the only Priority Agent on the system bus. It asserts this signal to get the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the H_LOCK# signal was asserted.

4.1 Cantiga North Bridge -2

H_BREQ#	I/O AGTL+	Host Bus Request: The (G)MCH pulls the processor bus H_BREQ# signal low during H_CPURST#. The signal is ampled by the processor on the active-to-inactive transition of H_CPURST#. H_BREQ# should be tri-stated after the hold tir requirement has been satisfied.
H_CPURST#	O AGTL+	Host CPU Reset: The H_CPURST# pin is an output from the (G)MCH. The (G)MCH asserts H_CPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. H_CPURST# allows the processor to begin execution in a known state.

Host Interface Signals(continued)

Signal Name	Type	Description
H_CPUSLP#	O LVCMOS	Host CPU Sleep: When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. (This is a CMOS type buffer with Vtt - NOT 3.3 volts.)
H_D#[63:0]	I/O AGTL+ 4X	Host Data: These signals are connected to the processor data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the processor bus depending on the HDINV#[3:0] signals.
H_DBSY#	I/O AGTL+	Host Data Bus Busy: Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
H_DEFER#	O AGTL+	Host Defer: Signals that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

4.1 Cantiga North Bridge -3

<table>
<tr><td>H_DINV#[3:0]</td><td>I/O
AGTL+</td><td>Host Dynamic Bus Inversion: Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8.
<table>
<tr><th>H_DINV#</th><th>Data Bits</th></tr>
<tr><td>H_DINV#3</td><td>H_D#[63:48]</td></tr>
<tr><td>H_DINV#2</td><td>H_D#[47:32]</td></tr>
<tr><td>H_DINV#1</td><td>H_D#[31:16]</td></tr>
<tr><td>H_DINV#0</td><td>H_D#[15:0]</td></tr>
</table></td></tr>
<tr><td>H_DPWR#</td><td>I/O
AGTL+</td><td>Host Data Power: Used by (G)MCH to indicate that a data return cycle is pending within 2 H_CLK cycles or more. Processor uses this signal during a read-cycle to activate the data input buffers in preparation for H_DRDY# and the related data.</td></tr>
<tr><td>H_DRDY#</td><td>I/O
AGTL+</td><td>Host Data Ready: Asserted for each cycle that data is transferred.</td></tr>
<tr><td>H_DSTBP#[3:0]
H_DSTBN#[3:0]</td><td>I/O
AGTL+ 4X</td><td>Host Differential Host Data Strobes: The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV#[3:0] at the 4x transfer rate.
<table>
<tr><th>Strobe</th><th>Data Bits</th></tr>
<tr><td>H_DSTBP#3, H_DSTBN#3</td><td>H_D#[63:48], H_DINV#[3]</td></tr>
<tr><td>H_DSTBP#2, H_DSTBN#2</td><td>H_D#[47:32], H_DINV#[2]</td></tr>
<tr><td>H_DSTBP#1, H_DSTBN#1</td><td>H_D#[31:16], H_DINV#[1]</td></tr>
<tr><td>H_DSTBP#0, H_DSTBN#9</td><td>H_D#[15:0], H_DINV#[0]</td></tr>
</table></td></tr>
</table>

4.1 Cantiga North Bridge -4

Host Interface Signals(continued)

Signal Name	Type	Description
H_HIT#	I/O AGTL+	Host Hit: Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with H_HITM# by the target to extend the snoop window.
H_HITM#	I/O AGTL+	Host Hit Modified: Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with H_HIT# to extend the snoop window.
H_LOCK#	I AGTL+	Host Lock: All processor bus cycles sampled with the assertion of H_LOCK# and H_ADS#, until the negation of H_LOCK# must be atomic.
H_RCOMP	I/O A	Host RCOMP: Used to calibrate the Host AGTL+ I/O buffers.
H_REQ#[4:0]	I/O AGTL+ 2X	Host Request Command: Defines the attributes of the request. H_REQ#[4:0] are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
H_RS#[2:0]	O AGTL+	Host Response Status: Indicates the type of response according to the following the table:
H_SWING	I A	Host Voltage Swing: These signals provide reference voltages used by the H_RCOMP circuits.
H_TRDY#	O AGTL+	Host Target Ready: Indicates that the target of the processor transaction can enter the data transfer phase.

HRS[2:0]#	Response type
000	Idle state
001	Retry response
010	Deferred response
011	Reserved (not driven by (G)MCH)
100	Hard Failure (not driven by (G)MCH)
101	No data response
110	Implicit Write back
111	Normal data response

9223 N/B Maintenance

4.1 Cantiga North Bridge -5

Host Interface Signals(continued)

Signal Name	Type	Description
THERMTRIP#	O AGTL+	Connects between the Processor, (G)MCH and the ICH. Assertion of THERMTRIP# (Thermal Trip) indicates the (G)MCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the (G)MCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the (G)MCH core junction temperature. To protect the (G)MCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the (G)MCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.

Memory Channel A Interface

Signal Name	Type	Description
SA_BS[2:0]	O SSTL-1.8/1.5	Bank Select: These signals define which banks are selected within each SDRAM rank.
SA_WE#	O SSTL-1.8/1.5	Write Enable Control Signal: Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM commands.
SA_RAS#	O SSTL-1.8/1.5	RAS Control Signal: Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_CAS#	O SSTL-1.8/1.5	CAS Control Signal: Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SDRAM commands.
SA_DM[7:0]	O SSTL-1.8/1.5 2x	Data Mask: These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane.
SA_DQS[7:0]	I/O SSTL-1.8/1.5 2x	Data Strobes: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions.

4.1 Cantiga North Bridge -6

SA_DQS#[7:0]	I/O SSTL-1.8/1.5 2x	Data Strobe Complements: These are the complementary strobe signals.
SA_DQ[63:0]	I/O SSTL-1.8/1.5 2x	Data Bus: Channel A data signal interface to the SDRAM data bus
SA_MA[14:0]	O SSTL-1.8/1.5	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.

Memory Channel A Interface(continued)

Signal Name	Type	Description
SA_CK[1:0]	O SSTL-1.8/1.5	SDRAM Differential Clock: Channel A SDRAM Differential Clock signal-pair. The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SA_CK#[1:0]	O SSTL-1.8/1.5	SDRAM Inverted Differential Clock: Channel A SDRAM Differential Clock signal-pair complement.
SA_CKE[1:0]	O SSTL-1.8/1.5	Clock Enable: (1 per Rank) used to: • Initialize the SDRAMs during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR
SA_CS#[1:0]	O SSTL-1.8/1.5	Chip Select: (1 per Rank): Used to select particular SA_CS#[1:0] SDRAM components during the active state. There is one Chip Select for each SDRAM rank
SA_ODT[1:0]	O SSTL-1.8/1.5	On Die Termination: Active Termination Control

9223 N/B Maintenance

4.1 Cantiga North Bridge -7

Memory Channel B Interface

Signal Name	Type	Description
SB_BS[2:0]	O SSTL-1.8/1.5	Bank Select: These signals define which banks are selected within each SDRAM rank.
SB_WE#	O SSTL-1.8/1.5	Write Enable Control Signal: Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM commands.
SB_RAS#	O SSTL-1.8/1.5	RAS Control Signal: Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_CAS#	O SSTL-1.8/1.5	CAS Control Signal: Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SDRAM commands.
SB_DM[7:0]	O SSTL-1.8/1.5 2x	Data Mask: These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane.
SB_DQS#[7:0]	I/O SSTL-1.8/1.5 2x	Data Strobe Complements: These are the complementary strobe signals.
SB_DQS[7:0]	I/O SSTL-1.8/1.5 2x	Data Strobes: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions.
SB_MA[14:0]	O SSTL-1.8/1.5	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.

4.1 Cantiga North Bridge -8

Memory Channel B Interface(continued)

Signal Name	Type	Description
SB_DQ[63:0]	I/O SSTL-1.8/1.5 2x	Data Bus: Channel B data signal interface to the SDRAM data bus.
SB_CK[1:0]	O SSTL-1.8/1.5	SDRAM Differential Clock: Channel B SDRAM Differential Clock signal-pair. The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM.
SB_CK#[1:0]	O SSTL-1.8/1.5	SDRAM Inverted Differential Clock: Channel B SDRAM Differential Clock signal-pair complement.
SB_CKE[1:0]	O SSTL-1.8/1.5	Clock Enable: (1 per Rank): Used to initialize the SDRAMs during power-up, power-down SDRAM ranks, place all SDRAM ranks into and out of self-refresh during STR.
SB_CS#[1:0]	O SSTL-1.8/1.5	Chip Select: (1 per Rank): Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
SB_ODT[1:0]	O SSTL-1.8/1.5	On Die Termination: Active Termination Control

Memory Reference and Compensation

Signal Name	Type	Description
SM_RCOMP	I A	System Memory Impedance Compensation: Refer Montevina Platform Design Guide for implementation
SM_RCOMP#	I A	System Memory Impedance Compensation: Refer Montevina Platform Design Guide for implementation
SM_RCOMP_V0	I A	System Memory pull up impedance compensation
SM_RCOMP_V0	I A	System Memory pull down impedance compensation
SM_VREF	I A	System Memory Reference Voltage for all data and data strobe signals.
SM_REXT	IO A	Constant circuit reference for clocks.

9223 N/B Maintenance

4.1 Cantiga North Bridge -9

PCI Express Based Graphics Interface Signals

Signal Name	Type	Description
PEG_COMPI	I A	PEG_COMPI PCI Express Graphics Input Current Compensation
PEG_COMPO	I A	PCI Express Graphics Output Current and Resistance Compensation
PEG_RX[15:0] PEG_RX#[15:0]	I PCI Express	PCI Express Graphics Receive Differential Pair
PEG_TX[15:0] PEG_TX#[15:0]	O PCI Express	PCI Express Graphics Transmit Differential Pair

DMI – (G)MCH to ICH Serial Interface

Signal Name	Type	Description
DMI_RXN[3:0] DMI_RXP[3:0]	I PCI Express	DMI input from ICH: Direct Media Interface receive differential pair
DMI_TXN[3:0] DMI_TXP[3:0]	O PCI Express	DMI output to ICH: Direct Media Interface transmit differential pair

CRT DAC Signals

Signal Name	Type	Description
CRT_RED	O A	RED Analog Video Output: This signal is a CRT analog video output from the internal color palette DAC.
CRT_GREEN	O A	GREEN Analog Video Output: This signal is a CRT analog video output from the internal color palette DAC.
CRT_BLUE	O A	BLUE Analog Video Output: This signal is a CRT analog video output from the internal color palette DAC.
CRT_TVO_IREF	O A	Resistor Set and TV Reference Current: Set point resistor for the internal color palette DAC and TV reference current.

9223 N/B Maintenance

4.1 Cantiga North Bridge -10

CRT DAC Signals(continued)

Signal Name	Type	Description
CRT_VSYNC	O HVCMOS	CRT Vertical Synchronization: This signal is used as the vertical sync (polarity is programmable).
CRT_HSYNC	O HVCMOS	CRT Horizontal Synchronization: This signal is used as the horizontal sync (polarity is programmable) or “sync interval”.
CRT_IRTN	O A	Resistor Set: Set point resistor for the internal color palette DAC.

Analog TV-out Signals

Signal Name	Type	Description
TV_DCONSEL[1	O COD	TV D-connector Select: Selects appropriate full-voltage discernment signals for TV-out D-connector.
TVA_DAC	O A	TVDAC Channel A Output: Can map to any one of the following: • Composite Video, Blank, and Sync (CVBS) • Component Pb
TVB_DAC	O A	TVDAC Channel B Output: Can map to any one of the following: • Svideo - Y • Component Y
TVC_DAC	O A	TVDAC Channel C Output: Can map to any one of the following: • Svideo - C • Component Pr
TV_RTN	O A	Current Return for TV DAC Channel A/B/C: Connect to ground on board

9223 N/B Maintenance

4.1 Cantiga North Bridge -11

LVDS Signals

Signal Name	Type	Description
LDVS Channel A		
LVDSA_CLK	O LVDS	LVDS Channel A differential clock output – positive
LVDSA_CLK#	O LVDS	LVDS Channel A differential clock output – negative
LVDSA_DATA#	O LVDS	LVDS Channel A differential data output – negative
LVDSA_DATA[	O LVDS	LVDS Channel A differential data output – positive
LDVS Channel B		
LVDSB_CLK	O LVDS	LVDS Channel B differential clock output – positive
LVDSB_CLK#	O LVDS	LVDS Channel B differential clock output – negative
LVDSB_DATA#	O LVDS	LVDS Channel B differential data output – negative
LVDSB_DATA[	O LVDS	LVDS Channel B differential data output – positive
Panel Power and Backlight Control		
L_BKLT_CTRL	O HVCMOS	Panel Backlight Brightness Control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
L_BKLT_EN	O HVCMOS	LVDS Backlight Enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
L_VDD_EN	O HVCMOS	LVDS Panel Power Enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.

9223 N/B Maintenance

4.1 Cantiga North Bridge -12

LVDS Reference Signals		
LVDS_IBG	I/O Ref	LVDS Reference Current
LVDS_VBG	O A	Leave as NC
LVDS_VREFH	I Ref	Must be connected to ground.
LVDS_VREFL	I Ref	Must be connected to ground.

Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
CRT_DDC_CLK	I/O COD	CRT DDC clock monitor control support
CRT_DDC_DAT	I/O COD	CRT DDC Data monitor control support
L_CTRL_CLK	I/O COD	Control signal (clock) for External SSC clock chip control – optional
L_CTRL_DATA	I/O COD	Control signal (data) for External SSC clock chip control – optional
L_DDC_CLK	I/O COD	EDID support for flat panel display
L_DDC_DATA	I/O COD	EDID support for flat panel display
SDVO_CTRL_CL	I/O COD	HDMI port B Control Clock (This pin is shared with SDVO)
SDVO_CTRL_D	I/O COD	HDMI port B Control Data (This pin is shared with SDVO)
DDPC_CTRLCL	I/O COD	HDMI port C Control Clock
DDPC_CTRLDA	I/O COD	HDMI port C Control Data

9223 N/B Maintenance

4.1 Cantiga North Bridge -13

IntelR High Definition Audio (IntelR HD Audio) Signals

Signals	Type	Description
HDA_SDO	I CMOS	Intel HD Audio Serial Data Input to (G)MCH Audio HW: Driven by Intel HD Audio Controller.
HDA_SDI	I/O CMOS	Point to Point ICH Intel HD Audio Serial response output
HDA_RST#	I CMOS	Global Intel HD Audio link reset
HDA_BCLK	I CMOS	Global Intel HD Audio 24.00-MHz clk
HDA_SYNC	I CMOS	Global 48-KHz Frame Sync and Inbound Tag Signal: SYNC is sourced from the Intel HD Audio controller and input to (G)MCH Audio HW.

IntelR Management Engine Interface (IntelR MEI) Signals

Signal Name	Type	Description
CL_CLK	I/O GTL	Controller Link Bi Directional Clock
CL_DATA	I/O GTL	Controller Link Bi Directional Data
CL_RST#	I GTL	Controller Link Reset
CL_VREF	I A	External reference voltage for Controller Link input buffers
CL_PWROK	I GTL	Intel Management Engine/Controller Link Power OK

9223 N/B Maintenance

4.1 Cantiga North Bridge -14

PLL Signals

Signal Name	Type	Description
DPLL_REF_CLK	I Diff Clk	Display PLLA Differential Clock In: 96 MHz Display PLL Differential Clock In, no SSC support –
DPLL_REF_CLK	I Diff Clk	Display PLLA Differential Clock In Complement: Display PLL Differential Clock In Complement - no SSC support.
DPLL_REF_SSC	I Diff Clk	Display PLLB Differential Clock In: 100 MHz Optional Display PLL Differential Clock In for SSC support NOTE: Differential Clock input for optional SSC support for LVDS display.
DPLL_REF_SSC	I Diff Clk	Display PLLB Differential Clock In Complement: Optional Display PLL Differential Clock In Complement for SSC support. NOTE: Differential Clock input for optional SSC support for LVDS display.
HPLL_CLK	I Diff Clk	Differential Host Clock In: Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low-voltage differential signal and runs at 1/4 the FSB data rate.

PLL Signals(continued)

Signal Name	Type	Description
HPLL_CLK#	I Diff Clk	Differential Host Clock Input Complement:
PEG_CLK	I Diff Clk	Differential PCI Express based Graphics / DMI Clock In: These pins receive a differential 100-MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
PEG_CLK#	I Diff Clk	Differential PCI Express based Graphics / DMI Clock In Complement

9223 N/B Maintenance

4.1 Cantiga North Bridge -15

Reset and Miscellaneous Signals

Signal Name	Type	Description
CLKREQ#	O COD	External Clock Request: (G)MCH drives CLKREQ# to control the PCI Express differential clock input to itself.
GFX_VID[4:0]	O HVCMOS	Voltage ID to support Graphics Render Standby Mode
GFX_VR_EN	O HVCMOS	VR Enable Signal to support Graphics Render Standby Mode
ICH_SYNC#	O HVCMOS	ICH Synchronization: Asserted to synchronize with ICH on faults. ICH_SYNC# must be connected to ICH's MCH_SYNC# signal.
PM_SYNC#	I HVCMOS	Power Management Sync: Used to indicate a Cx state transition between ICH and (G)MCH.
DPRSLPVR	I HVCMOS	Deeper Sleep - Voltage Regulator: Deeper Sleep Voltage signal from ICH
PM_DPRSTP#	I LVCMOS	Deeper Sleep State: Deeper Sleep State signal coming from the ICH.
PM_EXT_TS#[1	I HVCMOS	External Thermal Sensor Input: If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling.
SM_PWROK	I CMOS	DDR3 Power Good Monitor: Connected to VSS in DDR2. Driven by platform logic for DDR3.
SM_DRAMRST	O SSTL-1.5	DDR3 DRAM Reset: Reset signal from MCH to DRAM devices. One for all channels or SO-DIMMs. Used only in DDR3 mode.
PWROK	I HVCMOS	Power OK: Indication to the (G)MCH that core power is stable. This input buffer is 3.3-V tolerant.
RSTIN#	I HVCMOS	Reset In: When asserted this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PLTRST# output of the ICH. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.

4.1 Cantiga North Bridge -16

Reset and Miscellaneous Signals(continued)

Signal Name	Type	Description
TSATN#	O AGTL+	Thermal Sensor Aux Trip Notification: Output from the (G)MCH to the EC indicating the Aux2 trip point (SW programmable) has been crossed.
JTAG_TDI	I CMOS	Intel Management Engine JTAG Test Data Input
JTAG_TDO	I/O CMOS	Intel Management Engine JTAG Test Data Output
JTAG_TCK	I CMOS	Intel Management Engine JTAG Test Clock
JTAG_TMS	I CMOS	Intel Management Engine JTAG Test Mode Select
NC	NC	No Connects: This signals should be left as no connects.

Power and Ground (Sheet 1 of 3)

Voltage	Ball Name	Description
Host		
1.05	VTT	Host Interface I/O Voltage
1.05	VTTLF	These balls are internally connected to power and require decoupling capacitors.
1.05	VCC_AXF	Host Interface I/O and HSIO voltage
System Memory		
1.5/1.8	VCC_SM	I/O Voltage
1.5/1.8	VCC_SM/NC	I/O Voltage - May be left NC on DDR2 Motherboards
1.5/1.8	VCC_SM_LF	These balls are internally connected to power and require a decoupling capacitor.
1.5/1.8	VCC_SM_CK	Clock I/O Voltage
1.05	VCCA_SM	I/O Logic and DLL voltage

9223 N/B Maintenance

4.1 Cantiga North Bridge -17

Power and Ground (Sheet 2 of 3)

Voltage	Ball Name	Description
1.05	VCCA_SM_CK	Clock logic voltage
PCI Express* Based Graphics / DMI		
1.05	VCC_PEG	Analog, I/O Logic, and Term Voltage for PCI Express Based Graphics
1.5	VCCA_PEG_BG	Band Gap Voltage for PCI Express Based Graphics
Ground	VSSA_PEG_BG	Band Gap Ground for PCI Express Based Graphics
1.05	VCC_DMI	TX Analog and Termination Voltage for DMI
PLL		
1.05	VCCA_HPLL	Host PLL Analog Supply
1.05	VCCD_HPLL	Host PLL Digital Supply
1.05	VCCA_MPLL	MPLL Analog circuits
1.05	VCCA_DPLLA	Display A PLL power supply
1.05	VCCA_DPLLB	Display B PLL power supply
1.05	VCCA_PEG_PLL	Analog PLL Voltage for PCI Express Based Graphics
1.05	VCCD_PEG_PLL	Digital PLL Voltage for PCI Express Based Graphics
High Voltage		
3.3	VCC_HV	HV buffer power supply
CRT		
3.3	VCCA_CRT_DAC	Analog power supply
1.5	VCCD_QDAC	Quiet digital power supply (same as VCCD_QDAC for TV)
LVDS		
1.8	VCCD_LVDS	Digital power supply
1.8	VCC_TX_LVDS	I/O power supply
1.8	VCCA_LVDS	Analog power supply
Ground	VSSA_LVDS	Analog ground
TV		
1.5	VCCD_TVDAC	TV DAC power supply
3.3	VCCA_TV_DAC	TVDAC IO Voltage
1.5	VCCD_QDAC	Quiet Digital TV DAC Power Supply (Shared with CRTDAC)
3.3	VCCA_DAC_BG	TV DAC Band Gap Power
Ground	VSSA_DAC_BG	TV DAC Band Gap Ground
Intel HD Audio		
1.5	VCC_HDA	Intel HD Audio Power supply
Intel Management Engine		
1.05	VCC	Intel Management Engine voltage is tied to VCC

4.1 Cantiga North Bridge -18

Power and Ground (Sheet 3 of 3)

Voltage	Ball Name	Description
Core		
1.05	VCC	Core chipset voltage supply
1.05 (Nominal)	VCC_AXG	Graphics voltage supply
1.05	VCC_AXG_SENSE	GFX Voltage Supply Sense Signal
Ground	VSS_AXG_SENSE	VSS Sense Signal
Ground	VSS	Ground
Ground	VSS_SCB	Sacrificial Corner Balls for improved package reliability

4.2 ICH9M South Bridge -1

Direct Media Interface Signals

Name	Type	Description
DMI0TXP, DMI0TXN	O	Direct Media Interface Differential Transmit Pair 0
DMI0RXP, DMI0RXN	I	Direct Media Interface Differential Receive Pair 0
DMI1TXP, DMI1TXN	O	Direct Media Interface Differential Transmit Pair 1
DMI1RXP, DMI1RXN	I	Direct Media Interface Differential Receive Pair 1
DMI2TXP, DMI2TXN	O	Direct Media Interface Differential Transmit Pair 2
DMI2RXP, DMI2RXN	I	Direct Media Interface Differential Receive Pair 2
DMI3TXP, DMI3TXN	O	Direct Media Interface Differential Transmit Pair 3
DMI3RXP, DMI3RXN	I	Direct Media Interface Differential Receive Pair 3
DMI_ZCOMP	I	Impedance Compensation Input: Determines DMI input impedance.
DMI_IRCOMP	O	Impedance/Current Compensation Output: Determines DMI output impedance and bias current.

4.2 ICH9M South Bridge -2

PCI Express

Name	Type	Description
PETp1, PETn1	O	PCI Express* Differential Transmit Pair 1
PERp1, PERn1	I	PCI Express Differential Receive Pair 1
PETp2, PETn2	O	PCI Express Differential Transmit Pair 2
PERp2, PERn2	I	PCI Express Differential Receive Pair 2
PETp3, PETn3	O	PCI Express Differential Transmit Pair 3
PERp3, PERn3	I	PCI Express Differential Receive Pair 3
PETp4, PETn4	O	PCI Express Differential Transmit Pair 4
PERp4, PERn4	I	PCI Express Differential Receive Pair 4
PETp5, PETn5	O	PCI Express Differential Transmit Pair 5
PERp5, PERn5	I	PCI Express Differential Receive Pair 5
PETp6/GLAN_TXp, PETn6/GLAN_TXn	O	PCI Express Differential Transmit Pair 6: The differential pair will function as the Gigabit LAN Connect Interface transmit pair when the integrated Gigabit LAN controller is enabled.
PERp6/GLAN_RXp, PERn6/GLAN_RXn	I	PCI Express Differential Receive Pair 6: The differential pair will function as the Gigabit LAN Connect Interface receive pair when the integrated Gigabit LAN controller is enabled.

LAN Connect Interface

Name	Type	Description
GLAN_CLK	I	Gigabit LAN Input Clock: Clock driven by the Platform LAN Connect device. The frequency will vary depending on link speed. NOTE: The clock is shared between the LAN Connect Interface and the Gigabit LAN Connect Interface.
LAN_RXD[2:0]	I	Received Data: The Platform LAN Connect device uses these sig to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	Transmit Data: The integrated LAN controller uses these signals to transfer data and control information to the Platform LAN Connect component.
LAN_RSTSYNC	O	LAN Reset/Sync: This is the reset/sync signal from the LAN Connect Interface to the physical device. The Platform LAN Connect device's Reset and Sync signals are multiplexed onto this pin. NOTE: The signal is shared between LAN Connect Interface and Gigabit LAN Connect Interface.

4.2 ICH9M South Bridge -3

Gigabit LAN Connect Interface

Name	Type	Description
GLAN_CLK	I	Gigabit LAN Input Clock: Clock driven by the Platform LAN Connect device. The frequency will vary depending on link speed. NOTE: The clock is shared between the LAN Connect Interface and the Gigabit LAN Connect Interface.
GLAN_TXp/PET6p; GLAN_TXn/PET6n	O	Gigabit LAN Differential Transmit Pair. Can be instead used as PCI Express port 6 differential transmit pair.
GLAN_RXp/PER6p; GLAN_RXn/PER6n	I	Gigabit LAN Differential Receive Pair. Can be instead used as PCI Express port 6 differential receive pair.
GLAN_COMPO	O	Impedance Compensation Output pad: Determines Gigabit LAN Connect Interface output impedance and bias current.
GLAN_COMPI	I	Impedance Compensation Input pad: Determines Gigabit LAN Connect Interface input impedance.
LAN_RSTSYNC	O	LAN Reset/Sync: This is the reset/sync signal from the Gigabit LAN interface to the physical device. The Platform LAN Connect device's Reset and Sync signals are multiplexed onto this pin. NOTE: The signal is shared between LAN Connect Interface and Gigabit LAN Connect Interface.

4.2 ICH9M South Bridge -4

Gigabit LAN Connect Interface(continued)

Name	Type	Description
GLAN_CLK	I	Gigabit LAN Input Clock: Clock driven by the Platform LAN Connect device. The frequency will vary depending on link speed. NOTE: The clock is shared between the LAN Connect Interface and the Gigabit LAN Connect Interface.
GLAN_TXp/PET6p; GLAN_TXn/PET6n	O	Gigabit LAN Differential Transmit Pair. Can be instead used as PCI Express port 6 differential transmit pair.
GLAN_RXp/PER6p; GLAN_RXn/PER6n	I	Gigabit LAN Differential Receive Pair. Can be instead used as PCI Express port 6 differential receive pair.
GLAN_COMPO	O	Impedance Compensation Output pad: Determines Gigabit LAN Connect Interface output impedance and bias current.
GLAN_COMPI	I	Impedance Compensation Input pad: Determines Gigabit LAN Connect Interface input impedance.
LAN_RSTSYNC	O	LAN Reset/Sync: This is the reset/sync signal from the Gigabit LAN interface to the physical device. The Platform LAN Connect device's Reset and Sync signals are multiplexed onto this pin. NOTE: The signal is shared between LAN Connect Interface and Gigabit LAN Connect Interface.

Firmware Hub Interface

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	Firmware Hub Signals. These signals are multiplexed with the LPC address signals.
FWH4 / LFRAME#	O	Firmware Hub Signals. This signal is multiplexed with the LPC LFRAME# signal.
INIT3_3V# (Desktop Only)	O	Initialization 3.3 V: This is the identical 3.3 V copy of INIT# intended for Firmware Hub.

4.2 ICH9M South Bridge -5

PCI Interface (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	PCI Address/Data: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] R contain data. The Intel ICH9 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	Bus Command and Byte Enables: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. C/BE[3:0]# Command Type 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH9 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.

4.2 ICH9M South Bridge -6

DEVSEL#	I/O	Device Select: The ICH9 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH9 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH9 address or an address destined for DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH9-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH9 until driven by a target device.
FRAME#	I/O	Cycle Frame: The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH9 when the ICH9 is the target, and FRAME# is an output from the ICH9 when the ICH9 is the initiator. FRAME# remains tri-stated by the ICH9 until driven by an initiator.

4.2 ICH9M South Bridge -7

PCI Interface Signals (Sheet 2 of 3)

Name	Type	Description
IRDY#	I/O	Initiator Ready: IRDY# indicates the ICH9's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH9 has valid data present on AD[31:0]. During a read, it indicates the ICH9 is prepared to latch data. IRDY# is an input to the ICH9 when the ICH9 is the target and an output from the ICH9 when the ICH9 is an initiator. IRDY# remains tri-stated by the ICH9 until driven by an initiator.
TRDY#	I/O	Target Ready: TRDY# indicates the ICH9's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH9, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH9, as a target is prepared to latch data. TRDY# is an input to the ICH9 when the ICH9 is the initiator and an output from the ICH9 when the ICH9 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH9 until driven by a target.
STOP#	I/O	Stop: STOP# indicates that the ICH9, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH9, as an initiator, to stop the current transaction. STOP# is an output when the ICH9 is a target and an input when the ICH9 is an initiator.

4.2 ICH9M South Bridge -8

PAR	I/O	Calculated/Checked Parity: PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH9 counts the number of ones within the 36 bits plus PAR and the sum is always even. The ICH9 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH9 generates PAR for address and data phases and only ensures PAR to be valid one PCI clock after the corresponding address or data phase. The ICH9 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH9 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH9 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH9 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH9 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH9 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PERR#	I/O	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error. The ICH9 drives PERR# when it detects a parity error. The ICH9 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ0# REQ1#/ GPIO50 REQ2#/ GPIO52 REQ3#/ GPIO54	I	PCI Requests: The ICH9 supports up to 4 masters on the PCI bus REQ[3:1]# pins can instead be used as GPIO.

4.2 ICH9M South Bridge -9

PCI Interface Signals (Sheet 3 of 3)

Name	Type	Description
GNT0# GNT1#/ GPIO51 GNT2#/ GPIO53 GNT3#/ GPIO55	O	PCI Grants: The ICH9 supports up to 4 masters on the PCI bus. GNT[3:1]# pins can instead be used as GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. NOTE: GNT[3:0]# are sampled as a functional strap. See Section 2.24.1 for details.
PCICLK	I	PCI Clock: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. Note: (Mobile Only) This clock does not stop based on STP_PCI# signal. PCI Clock only stops based on SLP_S3#.
PCIRST#	O	PCI Reset: This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	PCI Lock: This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH9 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus in desktop configurations. Note: In mobile configuration, devices on the PCI bus (other than the ICH9) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH9 has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	PCI Power Management Event: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH9 may drive PME# active due to an internal wake event. The ICH9 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

4.2 ICH9M South Bridge -10

Serial ATA Interface Signals (Sheet 1 of 4)

Name	Type	Description
SATA0TXP SATA0TXN	O	Serial ATA 0 Differential Transmit Pairs: These are outbound high-speed differential signals to Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA0RXP SATA0RXN	I	Serial ATA 0 Differential Receive Pair: These are inbound high-speed differential signals from Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA1TXP SATA1TXN	O	Serial ATA 1 Differential Transmit Pair: These are outbound high-speed differential signals to Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1.

Serial ATA Interface Signals (Sheet 2 of 4)

Name	Type	Description
SATA1RXP SATA1RXN	I	Serial ATA 1 Differential Receive Pair: These are inbound high-speed differential signals from Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1
SATA2TXP SATA2TXN (ICH9R, ICH9DH, ICH9DO Only)	O	Serial ATA 2 Differential Transmit Pair: These are outbound high-speed differential signals to Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1. NOTE: This port is not functional in the Desktop ICH9 Base component.
SATA2RXP SATA2RXN (ICH9R, ICH9DH, ICH9DO Only)	I	Serial ATA 2 Differential Receive Pair: These are inbound high-speed differential signals from Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1. NOTE: This port is not functional in the Desktop ICH9 Base component.

4.2 ICH9M South Bridge -11

SATA3TXP SATA3TXN (ICH9R, ICH9DH, ICH9DO Only)	O	Serial ATA 3 Differential Transmit Pair: These are outbound high-speed differential signals to Port 3. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1. NOTE: This port is not functional in the Desktop ICH9 Base component.
SATA3RXP SATA3RXN (ICH9R, ICH9DH, ICH9DO Only)	I	Serial ATA 3 Differential Receive Pair: These are inbound hig speed differential signals from Port 3. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1. NOTE: This port is not functional in the Desktop ICH9 Base component.
SATA4TXP SATA4TXN	O	Serial ATA 4 Differential Transmit Pair: These are outbound high-speed differential signals to Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2.
SATA4RXP SATA4RXN	I	Serial ATA 4 Differential Receive Pair: These are inbound high-speed differential signals from Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2
SATA5TXP SATA5TXN	O	Serial ATA 5 Differential Transmit Pair: These are outbound high-speed differential signals to Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2.
SATA5RXP SATA5RXN	I	Serial ATA 5 Differential Receive Pair: These are inbound high-speed differential signals from Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2.
SATARBIAS	O	Serial ATA Resistor Bias: This is an analog connection point for an external resistor to ground.
SATARBIAS#	I	Serial ATA Resistor Bias Complement: This is an analog connection point for an external resistor to ground.

4.2 ICH9M South Bridge -12

Serial ATA Interface Signals (Sheet 3 of 4)

Name	Type	Description
SATA0GP / GPIO21	I	Serial ATA 0 General Purpose: This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP / GPIO19	I	Serial ATA 1 General Purpose: Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP / GPIO36 (ICH9R, ICH9DH, ICH9DO Only)	I	Serial ATA 2 General Purpose: Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36. NOTE: This signal can also be used as GPIO36 for Desktop components. This signal can only be used as GPIO36 in the Desktop ICH9 Base component.
SATA3GP / GPIO37 (ICH9R, ICH9DH, ICH9DO Only)	I	Serial ATA 3 General Purpose: Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37. NOTE: This signal can also be used as GPIO37 for Desktop components. This signal can only be used as GPIO37 in the Desktop ICH9 Base component.

4.2 ICH9M South Bridge -13

SATA4GP / GPIO36 (Mobile Only)	I	Serial ATA 4 General Purpose: Same function as SATA0GP, except for SATA Port 4. Note: This signal can also be used as GPIO36 for Mobile components.
SATA5GP / GPIO37 (Mobile Only)	I	Serial ATA 5 General Purpose: Same function as SATA0GP, except for SATA Port 5. Note: This signal can also be used as GPIO37 for Mobile components.
SATALED#	OD O	Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for details.
SATACLKREQ#/ GPIO35	OD O	Serial ATA Clock Request: This signal is an open-drain output pin when configured as SATACLKREQ#. It is used to connect to the system clock chip. When active, request for SATA Clock running is asserted. When tri-stated, it tells the Clock Chip that SATA Clock can be stopped. An external pull-up resistor is required.

Serial ATA Interface Signals (Sheet 4 of 4)

Name	Type	Description
SCLOCK/GPIO22	OD O	SGPIO Reference Clock: The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. If SGPIO interface is not used, this signal can be used as a GPIO.
SLOAD/GPIO38	OD O	SGPIO Load: The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as a GPIO.
SDATAOUT0/ GPIO39 SDATAOUT1/ GPIO48	OD O	SGPIO Dataout: Driven by the controller to indicate the drive status in the following sequence: drive 0, 1, 2, 3, 4, 5, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPIO.

9223 N/B Maintenance

4.2 ICH9M South Bridge -14

LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	LPC Multiplexed Command, Address, Data: For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH4	O	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0#, LDRQ1# / GPIO23	I	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

Interrupt Signals

Name	Type	Description
SERIRQ	I/OD	Serial Interrupt Request: This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/OD	PCI Interrupt Requests: In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 5.8.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.

9223 N/B Maintenance

4.2 ICH9M South Bridge -15

USB Interface Signals

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	Universal Serial Bus Port [1:0] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller #1. NOTE: No external resistors are required on these signals. The R Intel ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	Universal Serial Bus Port [3:2] Differential: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller #1. NOTE: No external resistors are required on these signals. The ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	Universal Serial Bus Port [5:4] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller #1. NOTE: No external resistors are required on these signals. The ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.

4.2 ICH9M South Bridge -16

USBP6P, USBP6N, USBP7P, USBP7N	I/O	Universal Serial Bus Port [7:6] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller #2. NOTE: No external resistors are required on these signals. The ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.
USBP8P, USBP8N, USBP9P, USBP9N	I/O	Universal Serial Bus Port [9:8] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 8 and 9. These ports can be routed to UHCI controller #5 or the EHCI controller #2. NOTE: No external resistors are required on these signals. The ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.

4.2 ICH9M South Bridge -17

USB Interface Signals

Name	Type	Description
USBP10P, USBP10N, USBP11P, USBP11N	I/O	Universal Serial Bus Port [11:10] Differential: These differential pairs are used to transmit Data/Address/Command signals for ports 10 and 11. These ports can be routed to UHCI controller #6 or the EHCI controller #2. These ports can be optionally routed to EHCI Controller #1 when bit 0 RCBA 35F0h is set. NOTE: No external resistors are required on these signals. The ICH9 integrates 15 k pull-downs and provides an output driver impedance of 45 which requires no external series resistor.
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO29 OC6# / GPIO30 OC7# / GPIO31 OC8# / GPIO44 OC9# / GPIO45 OC10# / GPIO46 OC11# / GPIO47	I	Overcurrent Indicators: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[11:0]# may optionally be used as GPIOs. NOTE: OC[11:0]# are not 5 V tolerant.
USBRBIAS	O	USB Resistor Bias: Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	USB Resistor Bias Complement: Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

4.2 ICH9M South Bridge -18

Power Management Interface Signals (Sheet 1 of 3)

Name	Type	Description
PLTRST#	O	Platform Reset: The Intel®ICH9 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, TPM, etc.). The ICH9 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH9 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH9 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). NOTE: PLTRST# is in the VccSus3_3 well.
THRM#	I	Thermal Alarm: Active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	Thermal Trip: When low, this signal indicates that a thermal trip from the processor occurred, and the ICH9 will immediately transition to a S5 state. The ICH9 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S3#	O	S3 Sleep Control: SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	S4 Sleep Control: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. NOTE: This pin must be used to control the DRAM power in order to use the ICH9's DRAM power-cycling feature. Refer to Chapter 5.13.11.2 for details. NOTE: In a system with Intel AMT or ASF support, this signal should be used to control the DRAM power. In M1 state (where the host platform is in S3–S5 states and the manageability sub-system is running) the signal is forced high along with SLP_M# in order to properly maintain power to the DIMM used for manageability sub-system.

4.2 ICH9M South Bridge -19

SLP_S5#	O	S5 Sleep Control: SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
SLP_M#	O	Manageability Sleep State Control: This signal is used to control power planes to the Intel®AMT or ASF sub-system. If no Intel AMT or ASF Management Engine firmware is present, SLP_M# will have the same timings as SLP_S3#.
S4_STATE# / GPIO26	O	S4 State Indication: This signal asserts low when the host platform is in S4 or S5 state. In platforms where the management engine is forcing the SLP_S4# high along with SLP_M#, this signal can be used by other devices on the board to know when the host platform is below the S3 state.

Power Management Interface Signals (Sheet 2 of 3)

Name	Type	Description
PWROK	I	Power OK: When asserted, PWROK is an indication to the ICH9 that all power rails have been stable for 99 ms and that PCICLK has been stable for 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH9 asserts PLTRST#. NOTE: 1. PWROK must deassert for a minimum of three RTC clock periods in order for the ICH9 to fully reset the power and properly generate the PLTRST# output. 2. PWROK must not glitch, even if RSMRST# is low.
CLPWROK	I	Controller Link Power OK: When asserted, indicates that power to the Controller Link subsystem (MCH, ICH, etc.) is stable and tells the ICH to deassert CL_RST# to the MCH. NOTES: 1. CLPWROK must not assert before RSMRST# deasserts. 2. CLPWROK must not assert after PWROK asserts.

4.2 ICH9M South Bridge -20

PWRBTN#	I	Power Button: The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RI#	I	Ring Indicate: This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	System Reset: This pin forces an internal reset after being debounced. The ICH9 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	Resume Well Reset: This signal is used for resetting the resume power plane logic. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable.
LAN_RST#	I	LAN Reset: When asserted, the internal LAN controller is in reset. This signal must be asserted until the LAN power wells (VccLAN3_3 and VccLAN1_05) and VccCL3_3 power well are valid. When deasserted, this signal is an indication that the LAN power wells are stable. NOTES: 1. LAN_RST# must not deassert before RSMRST# deasserts 2. LAN_RST# must not deassert after PWROK asserts. 3. LAN_RST# must not deassert until 1ms after the LAN power wells (VccLAN3_3 and VccLAN1_05 and VccCL3_3 power well are valid. 4. If integrated LAN is not used LAN_RST# can be tied to Vss.
WAKE#	I	PCI Express* Wake Event: Sideband wake signal on PCI Express asserted by components requesting wake up.
MCH_SYNC#	I	MCH SYNC: This input is internally ANDed with the PWROK input. Connect to the ICH_SYNC# output of (G)MCH.

4.2 ICH9M South Bridge -21

Power Management Interface Signals (Sheet 3 of 3)

Name	Type	Description
SUS_STAT# / LPCPD#	O	Suspend Status: This signal is asserted by the ICH9 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC interface.
SUSCLK	O	Suspend Clock: This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
VRMPWRGD	I	VRM Power Good: This signal should be connected to the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input. This signal is in the suspend well.
CK_PWRGD	O	Clock Generator Power Good: indicates to the clock generator when the main power well is valid. This signal is asserted high when both SLP_S3# and VRMPWRGD are high.
PMSYNC# (Mobile Only) / GPIO0	O	Power Management Sync: When asserted, it signals the MCH to deassert CPUSLP# pin when exiting out of C5 or C6. Signal may also be used as a GPIO.
CLKRUN# (Mobile Only)/ GPIO32 (Desktop Only)	I/O	PCI Clock Run: Used to support PCI CLKRUN protocol. Connects to peripherals that need to request clock restart or prevention of clock stopping.

4.2 ICH9M South Bridge -22

STP_PCI# / GPIO15 (Desktop Only)	O	Stop PCI Clock: This signal is an output to the external clock generator for it to turn off the PCI clock. It is used to support PCI CLKRUN# protocol on mobile platforms. In Sx, this pin is also used to communicate the host clock frequency select for Management Engine operation in order to support Moff/Sx to R M1/Sx transitions in a mobile Intel AMT or ASF enabled system. This signal is used as a GPIO in desktop platforms.
STP_CPU# / GPIO25 (Desktop Only)	O	Stop CPU Clock: This signal is an output to the external clock generator for it to turn off the processor clock. It is used to support the C3 state on mobile platforms. In Sx, this pin is also used to communicate the host clock frequency select for Management Engine operation in order to support Moff/Sx to R M1/Sx transitions in a mobile Intel AMT or ASF enabled system. This signal is used as a GPIO in desktop platforms.
BATLOW# (Mobile Only) / TP0 (Desktop Only)	I	Battery Low: This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S3–S5 state. This signal can also be enabled to cause an SMI# when asserted.
DPRSLPVR (Mobile Only) / GPIO16	O	Deeper Sleep - Voltage Regulator: This signal is used to lower the voltage of the VRM during the C4 state. When the signal is high, the voltage regulator outputs the lower “Deeper Sleep” voltage. When low (default), the voltage regulator outputs the higher “Normal” voltage.
DPRSTP# (Mobile Only) / TP1 (Desktop Only)	O	Deeper Stop: This is a copy of the DPRSLPVR and it is active low.

4.2 ICH9M South Bridge -23

Processor Interface Signals (Sheet 1 of 2)

Name	Type	Description
A20M#	O	Mask A20: A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
FERR#	I	Numeric Coprocessor Error: This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH9 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is asserted, the ICH9 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. NOTE: FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	Ignore Numeric Error: This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH9 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Config Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.

4.2 ICH9M South Bridge -24

INIT#	O	Initialization: INIT# is asserted by the ICH9 for 16 PCI clocks to reset the processor. ICH9 can be configured to support processor Built In Self Test (BIST).
INTR	O	CPU Interrupt: INTR is asserted by the ICH9 to signal to the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.
NMI	O	Non-Maskable Interrupt: NMI is used to force a non-Maskable interrupt to the processor. The ICH9 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	System Management Interrupt: SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH9 in response to one of many enabled hardware or software events.
STPCLK#	O	Stop Clock Request: STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH9 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.

4.2 ICH9M South Bridge -25

Processor Interface Signals (Sheet 2 of 2)

Name	Type	Description
RCIN#	I	Keyboard Controller Reset CPU: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH9's other sources of INIT#. When the ICH9 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. NOTE: The ICH9 will ignore RCIN# assertion during transitions to the S1, S3, S4, and S5 states.
A20GATE	I	A20 Gate: A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD	O	CPU Power Good: This signal should be connected to the processor's PWRGOOD input to indicate when the processor power is valid. This is an output signal that represents a logical AND of the ICH9's PWROK and VRMPWRGD signals.
DPSLP# (Mobile Only) / TP2 (Desktop Only)	O	Deeper Sleep: DPSLP# is asserted by the ICH9 to the processor. When the signal is low, the processor enters the deep sleep state by gating off the processor Core Clock inside the processor. When the signal is high (default), the processor is not in the deep sleep state.

SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	SMBus Data: External pull-up resistor is required.
SMBCLK	I/OD	SMBus Clock: External pull-up resistor is required.
SMBALERT# / GPIO11	I	SMBus Alert: This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPIO.

4.2 ICH9M South Bridge -26

System Management Interface Signals (Sheet 1 of 2)

Name	Type	Description
INTRUDER#	I	Intruder Detect: This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPIO if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	System Management Link: SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT# / CLGPIO4 (Digital Office Only) / GPIO60	O OD	SMLink Alert: Output of the integrated LAN controller and input to either the integrated ASF, Intel®AMT or an external management controller in order for the LAN's SMLINK slave to be serviced. External pull-up resistor is required. This signal can instead be used as a GPIO or CLGPIO (Digital Office Only).
MEM_LED / GPIO24	O OD	Memory LED: Provides DRAM-powered LED control. Allows for the blinking of an LED to indicate memory activity in all power states. This functionality is configured and controlled by the Intel® Management Engine. This signal can instead be used as GPIO24.
SUS_PWR_ACK (Mobile Only)/ CLGPIO1 (Digital Office Only) / GPIO10	O	SUS_PWR_ACK: This signal is asserted by the Intel®Management Engine to indicate when the ICH suspend well may be powered down. External 10 k pull-up resistor to VccSus3_3 is required. This functionality is configured and controlled by the Management Engine. This signal can instead be used as GPIO10 in platforms that do not support Intel® AMT or ASF. This signal is used as GPIO10 or CLGPIO1 (Digital Office Only) in desktop systems.
AC_PRESENT (Mobile Only)/ CLGPIO2 (Digital Office Only) / GPIO14	I	AC_PRESENT: This signal is used to indicate to the Intel® Management Engine that the platform is connected to an AC powe source. This functionality is configured and controlled by the Management Engine. This signal can instead be used as GPIO14 in platforms that do not support Intel®AMT or ASF. This signal is used as GPIO14 or CLGPIO2 (Digital Office Only) in desktop systems.

4.2 ICH9M South Bridge -27

System Management Interface Signals (Sheet 2 of 2)

Name	Type	Description
WOL_EN / GPIO9	O	Wake On LAN Power Enable. In an Intel® AMT or ASF enabled system, this output signal is driven high by the ICH to control the LAN subsystem power (VccLAN3_3, VccCL3_3, LAN PHY Power, and SPI device) to support Wake on LAN (WOL) when the Intel®Management Engine is powered off. This functionality is configured and controlled by the Management Engine prior to entering the powered off state. NOTES: 1. This signal should be OR'd with the SLP_M# signal on the motherboard to determine when to power the LAN subsystem 2. In order to support WOL out of a G3 state, the WOL_EN pin needs to be pulled high by an external resistor until the Management Engine is initialized. If ASF or AMT are disabled on a board that is configured for WOL_EN support, BIOS must utilize GPIO9 to control power to the LAN subsystem when entering S3–S5. In platforms that do not support Intel AMT or ASF, this signal is used as GPIO9.
CLGPIO1 (Digital Office Only) / SUS_PWR_ACK (Mobile Only)/ GPIO10	I	Controller Link General Purpose I/O 1. This signal is not used by the Intel® Management Engine in desktop systems. This signal is used as GPIO10 in desktop systems. This signal is used as SUS_PWR_ACK in mobile systems.
CLGPIO2 (Digital Office Only) / AC_PRESENT (Mobile Only) / GPIO14	I/O	Controller Link General Purpose I/O 2. This signal is not used by the Intel® Management Engine in desktop systems. This signal is used as GPIO14 in desktop systems. This signal is used as AC_PRESENT in mobile systems.

4.2 ICH9M South Bridge -28

CLGPIO4 (Digital Office Only) / LINKALERT# / GPIO60	I/O	Controller Link General Purpose I/O 4. This signal is not used by the Intel®Management Engine in mobile and desktop systems. This signal may be used as GPIO60 or LINKALERT#.
CLGPIO5 (Digital Office Only) / GPIO57	I	Controller Link General Purpose I/O 5. This signal is not used by the Intel®Management Engine in desktop systems. In mobile systems, this signal is asserted to indicate Physical Presence to the integrated TPM module. This signal is used as GPIO57 in desktop systems.
CLGPIO6 (Digital Office Only) / SPI_CS1# / GPIO58	I/O	Controller Link General Purpose I/O 6. This signal is not used by the Intel®Management Engine in mobile and desktop systems. This signal may be used as a GPIO58 or SPI_CS1#, configured via a soft strap.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	Crystal Input 1: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	Crystal Input 2: This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

4.2 ICH9M South Bridge -29

Other Clocks

Name	Type	Description
CLK14	I	Oscillator Clock: Used for 8254 timers. Runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	48 MHz Clock: Used to run the USB controller. Runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	100 MHz Differential Clock: These signals are used to run the SATA controller at 100 MHz. This clock is permitted to stop during S3/S4/S5 states.
DMI_CLKP, DMI_CLKN	I	100 MHz Differential Clock: These signals are used to run the Direct Media Interface. Runs at 100 MHz.

Miscellaneous Signals (Sheet 1 of 3)

Name	Type	Description
INTVRMEN	I	Internal Voltage Regulator Enable: This signal enables the internal VccSus1_05, VccSus1_5 and VccCL1_5 regulators. This signal must be pulled-up to VccRTC.
LAN100_SLP	I	Internal Voltage Regulator Enable: When connected to VccRTC this signal enables the internal voltage regulators powering VccLAN1_05 and VccCL1_05. This signal must be pulled-up to VccRTC.
SPKR	O	Speaker: The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. NOTE: SPKR is sampled as a functional strap. See Section 2.24.1 for more details. There is a weak integrated pull-down resistor on SPKR pin.

4.2 ICH9M South Bridge -30

Miscellaneous Signals (Sheet 2 of 3)

Name	Type	Description
RTCRST#	I	RTC Reset: When asserted, this signal resets register bits in the RTC well. NOTES: 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
SRTCRST#	I	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed. NOTES: 1. The SRTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCRST# pin must rise before the RSMRST#pin.
TP0 (Desktop Only) / BATLOW# (Mobile Only)	I	Test Point 0: This signal must have an external pull-up to VccSus3_3.
TP1 (Desktop Only) / DPRSTP# (Mobile Only)	O	Test Point 1: Route signal to a test point.
TP2 (Desktop Only) / DPSLP# (Mobile Only)	O	Test Point 2: Route signal to a test point.
TP3	I/O	Test Point 3: Route signal to a test point.

4.2 ICH9M South Bridge -31

TP4 (Desktop Only) / CL_DATA1 (Mobile Only)	I/O	Test Point 4: Route signal to a test point.
TP5 (Desktop Only) / CL_CLK1 (Mobile Only)	I/O	Test Point 5: Route signal to a test point.
TP6 (Desktop Only) / CL_VREF1 (Mobile Only)	I	Test Point 6: Route signal to a test point.
TP7 (Desktop Only) / CL_RST1# (Mobile Only)	O	Test Point 7: Route signal to a test point.

Miscellaneous Signals (Sheet 3 of 3)

Name	Type	Description
TP[10:8] (Mobile Only) / PWM[2:0] (Desktop Only)	OD O	Test Point [10:8]: Route signal to a test point.
TP11 (Mobile Only) / SST (Desktop Only)	I/O	Test Point 11: Route signal to a test point.
TP12 (Mobile Only) / PECI (Desktop Only)	I/O	Test Point 12: Route signal to a test point.

4.2 ICH9M South Bridge -32

Intel®High Definition Audio Link Signals (Sheet 1 of 2)

Name	Type	Description
HDA_RST#	O	Intel®High Definition Audio Reset: Master hardware reset to external codec(s).
HDA_SYNC	O	Intel High Definition Audio Sync: 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for more details. There is a weak integrated pull-down resistor on this pin.
HDA_BIT_CLK	O	Intel High Definition Audio Bit Clock Output: 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Intel(R)ICH9). This signal has a weak internal pull-down resistor.
HDA_SDOUT	O	Intel High Definition Audio Serial Data Out: Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for more details. There is a weak integrated pull-down resistor on this pin.

4.2 ICH9M South Bridge -33

Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS0#	O	SPI Chip Select 0: Used as the SPI bus request signal. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for more details.
SPI_CS1# / CLGPIO6 (Digital Office Only)/ GPIO58	O	SPI Chip Select 1: Used as the SPI bus request signal. Signal can also be used as a CLGPIO6 (Digital Office Only) or GPIO58. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for more details. There is a weak integrated pull-up resistor on this pin.
SPI_MISO	I	SPI Master IN Slave OUT: Data input pin for ICH9.
SPI_MOSI	O	SPI Master OUT Slave IN: Data output pin for ICH9. NOTE: This signal is sampled as a functional strap. See Section 2.24.1 for more details. There is a weak integrated pull-down resistor on this pin.
SPI_CLK	O	SPI Clock: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

4.2 ICH9M South Bridge -34

Controller Link Signals

Signal Name	Type	Description
CL_CLK0	I/O	Controller Link Clock 0: bi-directional clock that connects to the (G)MCH.
CL_DATA0	I/O	Controller Link Data 0: bi-directional data that connects to the (G)MCH.
CL_VREF0	I	Controller Link Reference Voltage 0: External reference voltage for Controller Link 0.
CL_RST0#	O	Controller Link Reset 0: North Controller Link reset that connects to the (G)MCH.
CL_RST1# (Mobile Only) / TP7 (Desktop Only)	O	Controller Link Reset 1: South Controller Link reset that connects to a Wireless LAN Device supporting Intel® Active Management Technology.
CL_CLK1 (Mobile Only) / TP5 (Desktop Only)	I/O	Controller Link Clock 1: bi-directional clock that connects to a Wireless LAN Device supporting Intel®Active Management Technology.
CL_DATA1 (Mobile Only) / TP4 (Desktop Only)	I/O	Controller Link Data 1: bi-directional data that connects to a Wireless LAN Device supporting Intel®Active Management Technology.
CL_VREF1 (Mobile Only) / TP6 (Desktop Only)	I	Controller Link Reference Voltage 1: External reference voltage for Controller Link 1.

4.2 ICH9M South Bridge -35

Intel®Quiet System Technology Signals

Signal Name	Type	Description
PWM[2:0] (Desktop Only) / TP[10:8] (Mobile Only)	OD O	Fan Pulse Width Modulation Outputs: Pulse Width Modulated duty cycle output signal that is used for Intel® Quiet System Technology. When controlling a 3-wire fan, this signal controls a power transistor that, in turn, controls power to the fan. When controlling a 4-wire fan, this signal is connected to the “Control” signal on the fan. The polarity of this signal is programmable. The output default is low. These signals are 5 V tolerant.
TACH0 / (Desktop Only) GPIO17 TACH1 / (Desktop Only) GPIO1 TACH2 / (Desktop Only) GPIO6 TACH3 / (Desktop Only) GPIO7	I	Fan Tachometer Inputs: Tachometer pulse input signal that is used to measure fan speed. This signal is connected to the “Sense” signal on the fan. Can instead be used as a GPIO.
SST (Desktop Only) / TP11 (Mobile Only)	I/O	Simple Serial Transport: Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors.
PECI (Desktop Only) / TP12 (Mobile Only)	I/O	Platform Environment Control Interface: Single-wire, serial bus. Connect to corresponding pin of the processor for accessing processor digital thermometer.

9223 N/B Maintenance

4.2 ICH9M South Bridge -36

General Purpose I/O Signals (Sheet 1 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO60	I/O	3.3 V	Suspend	Native	Multiplexed with LINKALERT#, or can be used as CLGPIO4 (Digital Office Only). (Note 11).
GPIO59	I/O	3.3 V	Suspend	Native	Multiplexed with OC[0]#. (Note 11).
GPIO58	I/O	3.3 V	Suspend (Note 6)	GPI	Multiplexed with SPI_CS1# or can be used as CLGPIO6 (Digital Office Only) (Note 8 and 10).
GPIO57	I/O	3.3 V	Suspend	GPI	Unmultiplexed. Can be used as CLGPIO5 (Digital Office Only).

General Purpose I/O Signals (Sheet 2 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO56	I/O	3.3 V	Suspend	GPI	Unmultiplexed
GPIO55	I/O	3.3 V	Core	Native	Multiplexed with GNT3# (Note 8).
GPIO54	I/O	5.0 V	Core	Native	Multiplexed with REQ3#. (Note 11).
GPIO53	I/O	3.3 V	Core	Native	Multiplexed with GNT2# (Note 8).
GPIO52	I/O	5.0 V	Core	Native	Multiplexed with REQ2#. (Note 11).
GPIO51	I/O	3.3 V	Core	Native	Multiplexed with GNT1# (Note 8).
GPIO50	I/O	5.0 V	Core	Native	Multiplexed with REQ1#. (Note 11).
GPIO49	I/O	3.3V	Core	GPO	Unmultiplexed (Note 8).
GPIO48	I/O	3.3 V	Core	GPI	Multiplexed with SDATAOUT1.
GPIO[47:44]	I/O	3.3V	Suspend	Native	Multiplexed with OC[11:8]#. (Note 11).
GPIO[43:40]	I/O	3.3 V	Suspend	Native	Multiplexed with OC[4:1]#. (Note 11).
GPIO39	I/O	3.3 V	Core	GPI	Multiplexed with SDATAOUT0.
GPIO38	I/O	3.3 V	Core	GPI	Multiplexed with SLOAD.
GPIO37	I/O	3.3 V	Core	GPI	Desktop: Multiplexed with SATA3GP. Mobile: Multiplexed with SATA5GP.
GPIO36	I/O	3.3 V	Core	GPI	Desktop: Multiplexed with SATA2GP. Mobile: Multiplexed with SATA4GP.
GPIO35	I/O	3.3 V	Core	GPO	Multiplexed with SATACLKREQ#.

4.2 ICH9M South Bridge -37

GPIO34	I/O	3.3 V	Core	GPO	Mobile: Multiplexed with HDA_DOCK_RST#. Desktop: UnMultiplexed.
GPIO33	I/O	3.3 V	Core	GPO	Mobile: Multiplexed with HDA_DOCK_EN#. Desktop: UnMultiplexed.
GPIO32 (Desktop Only)	I/O	3.3 V	Core	GPO	Mobile: This GPIO is not implemented and is used instead as CLKRUN#. Desktop: UnMultiplexed.
GPIO31	I/O	3.3 V	Suspend	Native	Multiplexed with OC7#. (Note 11).
GPIO30	I/O	3.3 V	Suspend	Native	Multiplexed with OC6#. (Note 11).
GPIO29	I/O	3.3 V	Suspend	Native	Multiplexed with OC5#. (Note 11).
GPIO28	I/O	3.3 V	Suspend	GPO	Unmultiplexed.
GPIO27	I/O	3.3 V	Suspend	GPO	Unmultiplexed
GPIO26	I/O	3.3 V	Suspend	Native	Multiplexed with S4_STATE#. (Note 9)
GPIO25 (Desktop Only)	I/O	3.3 V	Suspend	Native	Mobile: This GPIO is not implemented and is used instead as STP_CPU#. Desktop: Default as STP_CPU# (Note 4).
GPIO24	I/O	3.3 V	Suspend	GPO	Can be used as MEM_LED. GPIO24 configuration register bits are not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Native	Multiplexed with LDRQ1#. (Note 11).

4.2 ICH9M South Bridge -38

General Purpose I/O Signals (Sheet 3 of 3)

Name	Type	Tolerance	Power Well	Default	Description
GPIO22	I/O	3.3 V	Core	GPI	Multiplexed with SCLOCK.
GPIO21	I/O	3.3 V	Core	GPI	Multiplexed with SATA0GP.
GPIO20	I/O	3.3 V	Core	GPO	Unmultiplexed. (Note 8)
GPIO19	I/O	3.3 V	Core	GPI	Multiplexed with SATA1GP.
GPIO18	I/O	3.3 V	Core	GPO	Unmultiplexed.
GPIO17	I/O	3.3 V	Core	GPI	Desktop: Multiplexed with TACH0. Mobile: Unmultiplexed
GPIO16	I/O	3.3 V	Core	Native (Mobile) / GPO (Desktop)	Mobile: Natively used as DPRSLPVR. Desktop: UnMultiplexed.
GPIO15 (Desktop Only)	I/O	3.3 V	Suspend	Native	Mobile: GPIO is not implemented and is used instead as STP_PCI#. Desktop: Default as STP_PCI#. (Note 4).
GPIO14	I/O	3.3 V	Suspend	GPI	Mobile: Can be used as AC_PRESENT Desktop: Unmultiplexed. Can be used as CLGPIO2 (Digital Office Only).
GPIO13	I/O	3.3 V	Suspend	GPI	Unmultiplexed.
GPIO12	I/O	3.3 V	Suspend	GPO	Unmultiplexed.
GPIO11	I/O	3.3 V	Suspend	Native	Multiplexed with SMBALERT#. (Note 11).
GPIO10	I/O	3.3 V	Suspend	GPI	Mobile: Can be used as SUS_PWR_ACK. Desktop: Unmultiplexed. Can be used as CLGPIO1 (Digital Office Only).
GPIO9	I/O	3.3 V	Suspend	Native	Can be used as WOL_EN.
GPIO8	I/O	3.3 V	Suspend	GPI	Unmultiplexed.
GPIO[7:6]	I/O	3.3 V	Core	GPI	Desktop: Multiplexed with TACH[3:2]. Mobile: Unmultiplexed
GPIO[5:2]	I/OD	5 V	Core	GPI	Multiplexed with PIRQ[H:E]# (Note 6).
GPIO1	I/O	3.3 V	Core	GPI	Desktop: Multiplexed with TACH1. Mobile: Unmultiplexed
GPIO0	I/O	3.3 V	Core	GPI	Mobile: Multiplexed with PMSYNC#. Desktop: Unmultiplexed

4.2 ICH9M South Bridge -39

Power and Ground Signals (Sheet 1 of 3)

Name	Description
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged in desktop configurations or the main battery is removed or completely drained and AC power is not available in mobile configurations.
Vcc1_05	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for Logic and I/O. This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for Logic and I/O. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccCL1_05	1.05V supply for Controller Link. This plane must be on in S0 and other times Controller Link is used. This voltage is generated internally. This pin can be left as No Connect unless decoupling is required.
VccCL1_5	1.5V supply for Controller Link. This plane must be on in S0 and other times Controller Link is used. This voltage is generated internally. This pin can be left as No Connect unless decoupling is required.
VccCL3_3	3.3V supply for Controller Link. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0 and other times Controller Link is used. NOTE: VccCL3_3 must always be powered when VccLAN3_3 is powered.
VccDMI	Power supply for DMI. 1.05V, 1.25V or 1.5V depending on (G)MCH's DMI voltage.
VccDMIPLL	1.5 V supply for core well logic. This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.

4.2 ICH9M South Bridge -40

Power and Ground Signals (Sheet 2 of 3)

Name	Description
VccGLAN1_5	1.5V supply for integrated Gigabit LAN I/O buffers. This power can be turned off if the integrated Gigabit LAN is not used. If the integrated Gigabit LAN is used, the power is off in S3, S4, S5.
VccGLAN3_3	3.3V supply for integrated Gigabit LAN logic and I/O. This power can be turned off if the integrated Gigabit LAN is not used. If the integrated Gigabit LAN is used, the power is off in S3, S4, S5.
VccGLANPLL	1.5V supply for core well logic. This signal is used for the integrated Gigabit LAN PLL. This power is shut off in S3, S4, S5 and G3 states.
VccHDA	Core supply for Intel®High Definition Audio. This pin can be either 1.5 or 3.3 V. This power may be shut off in S3, S4, S5 or G3 states. NOTE: VccSusHDA and VccHDA can be connected to either 1.5 V or 3.3 V supplies, but both pins must be connected to supplies that are the same nominal value.
VccLAN1_05	1.05 V supply for LAN controller logic. This is a separate power plane that ma or may not be powered in S3–S5 states. This voltage is generated internally. These pins can be left as No Connect unless decoupling is required.

4.2 ICH9M South Bridge -41

VccLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0 NOTE: VccLAN3_3 must always be powered when VccCL3_3 or Vcc3_3 is powered.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. Note: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Intel® ICH9-based platform can be done by using a jumper on RTCRST# or GPI.
VccSATAPLL	1.5 V supply for core well logic. This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. Must be powered even if SATA is not used.
VccSus1_05	1.05 V supply for suspend well logic. This power is not expected to be shut off unless the system is unplugged in desktop configurations or the main battery is removed or completely drained and AC power is not available in mobile configurations. This voltage is generated internally. These pins can be left as No Connects unless decoupling is required.
VccSus1_5	1.5V supply for the suspend well I/O. This power is not expected to be shut off unless the system is unplugged in desktop configurations. This voltage is generated internally. These pins can be left as No Connects unless decoupling is required.
VccSus3_3	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged in desktop configurations or the main battery is removed or completely drained and AC power is not available in mobile configurations.

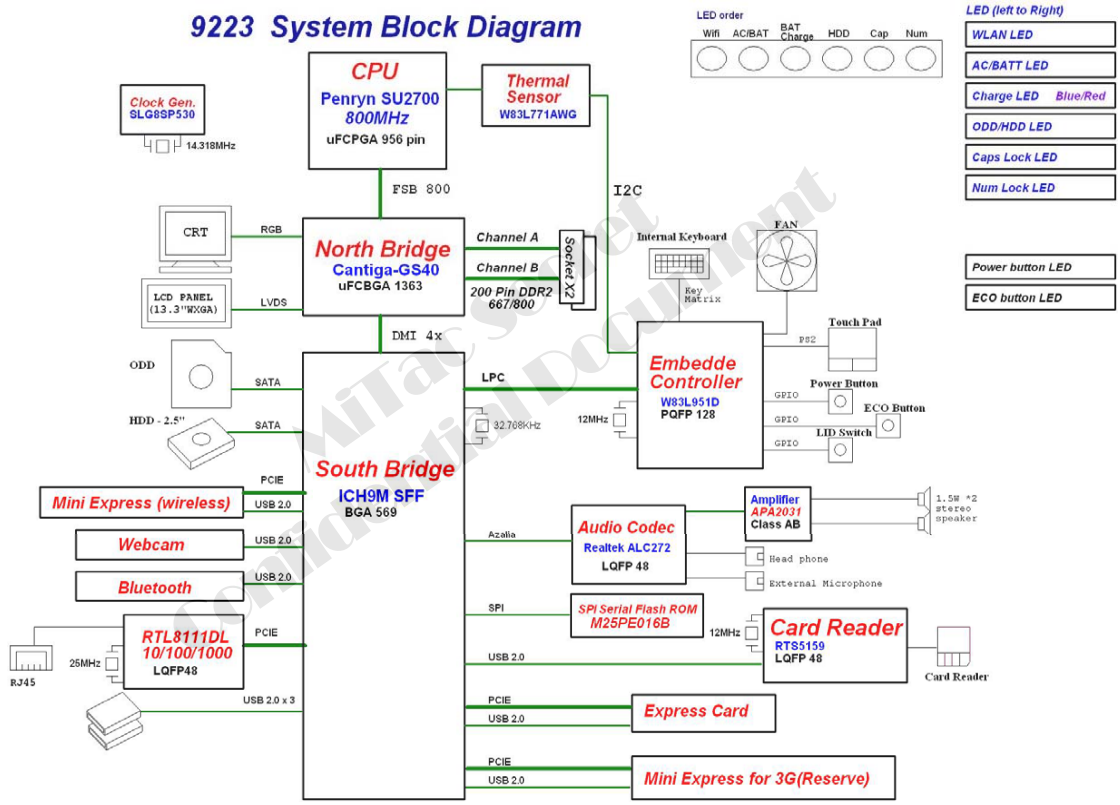
4.2 ICH9M South Bridge -42

Power and Ground Signals (Sheet 3 of 3)

Name	Description
VccSusHDA	Suspend supply for Intel®High Definition Audio. This pin can be either 1.5 or 3.3 V. This power is not expected to be shut off unless the system is unplugged in desktop configurations or the main battery is removed or completely drained and AC power is not available in mobile configurations. NOTE: VccSusHDA and VccHDA can be connected to either 1.5 V or 3.3 V supplies, but both pins must be connected to supplies that are the same nominal value.
VccUSBPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This powe may be shut off in S3, S4, S5 or G3 states. Must be powered even if USB not used.
Vss	Grounds.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals listed in Table 2-12.

9223 N/B Maintenance

5. System Block Diagram



9223 N/B Maintenance

6. Trouble Shooting

- 6.1 No Power
- 6.2 No Display
- 6.3 Graphics Controller Failure LCD No Display
- 6.4 External Monitor No Display
- 6.5 Keyboard (K/B) or Touch-Pad (T/P) Failure
- 6.6 Hard Disk Drive Failure
- 6.7 Bluetooth Failure
- 6.8 USB Port Failure
- 6.9 Audio Failure
- 6.10 LAN Failure
- 6.11 Card Reader Slot Failure
- 6.12 Mini Express (Wireless) Socket Failure
- 6.13 Express Card Socket Failure

9223 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display.

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

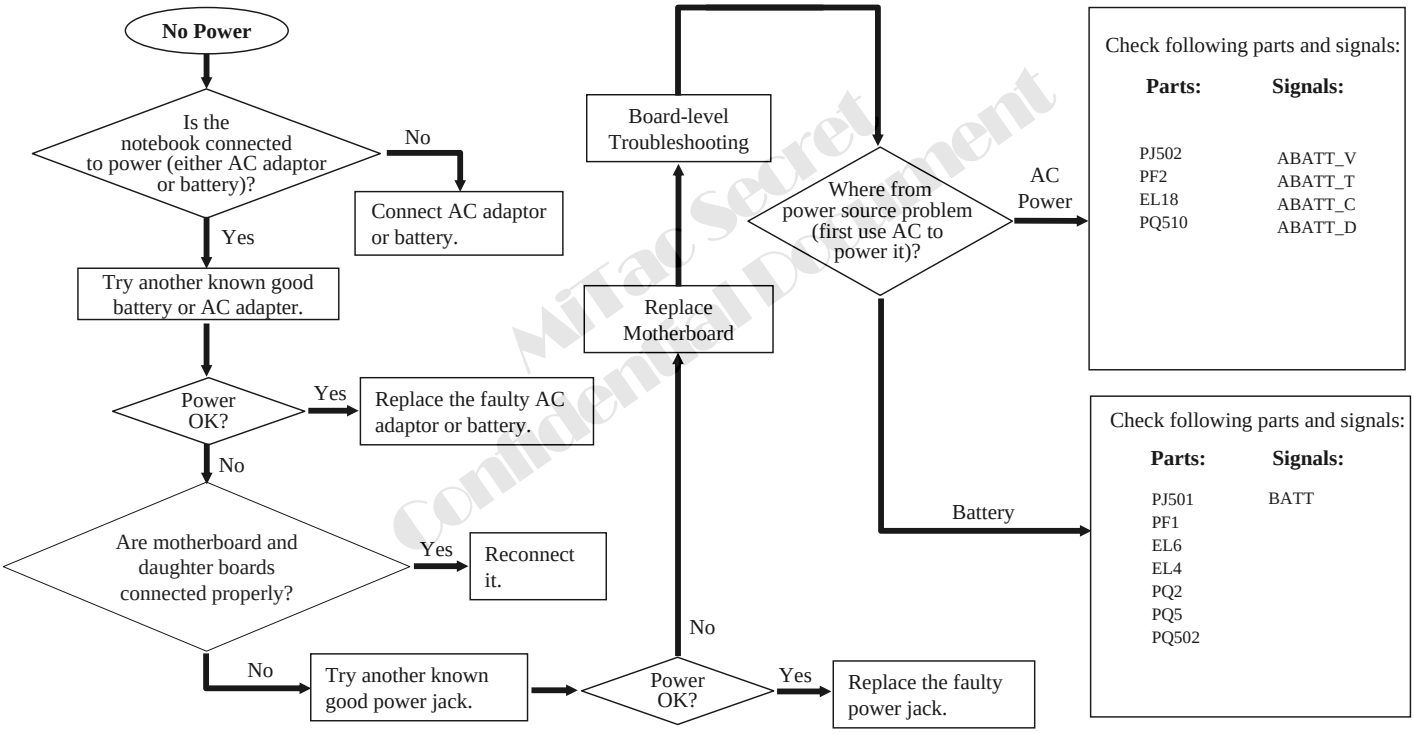
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification.

9223 N/B Maintenance

6.1 No Power

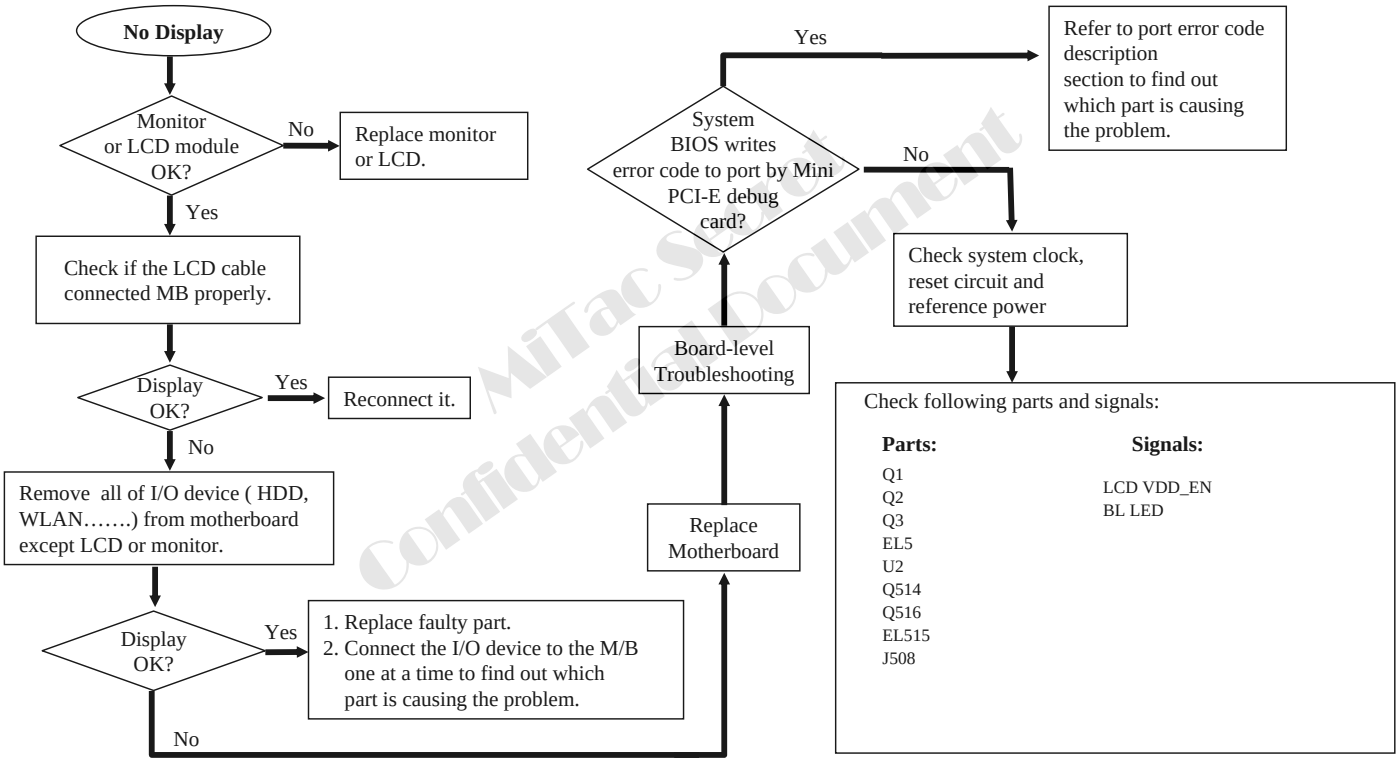
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



9223 N/B Maintenance

6.2 No Display

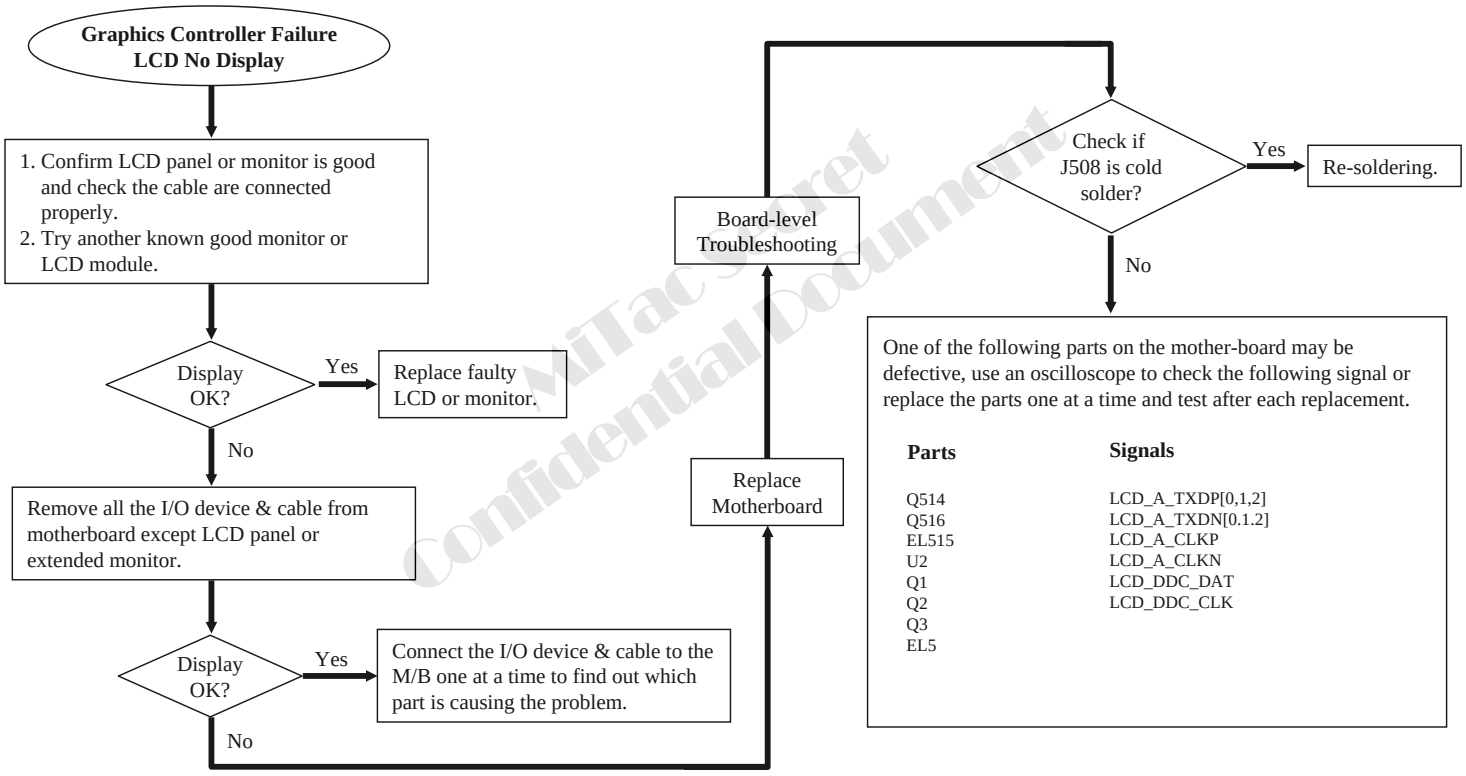
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



9223 N/B Maintenance

6.3 Graphics Controller Failure LCD No Display

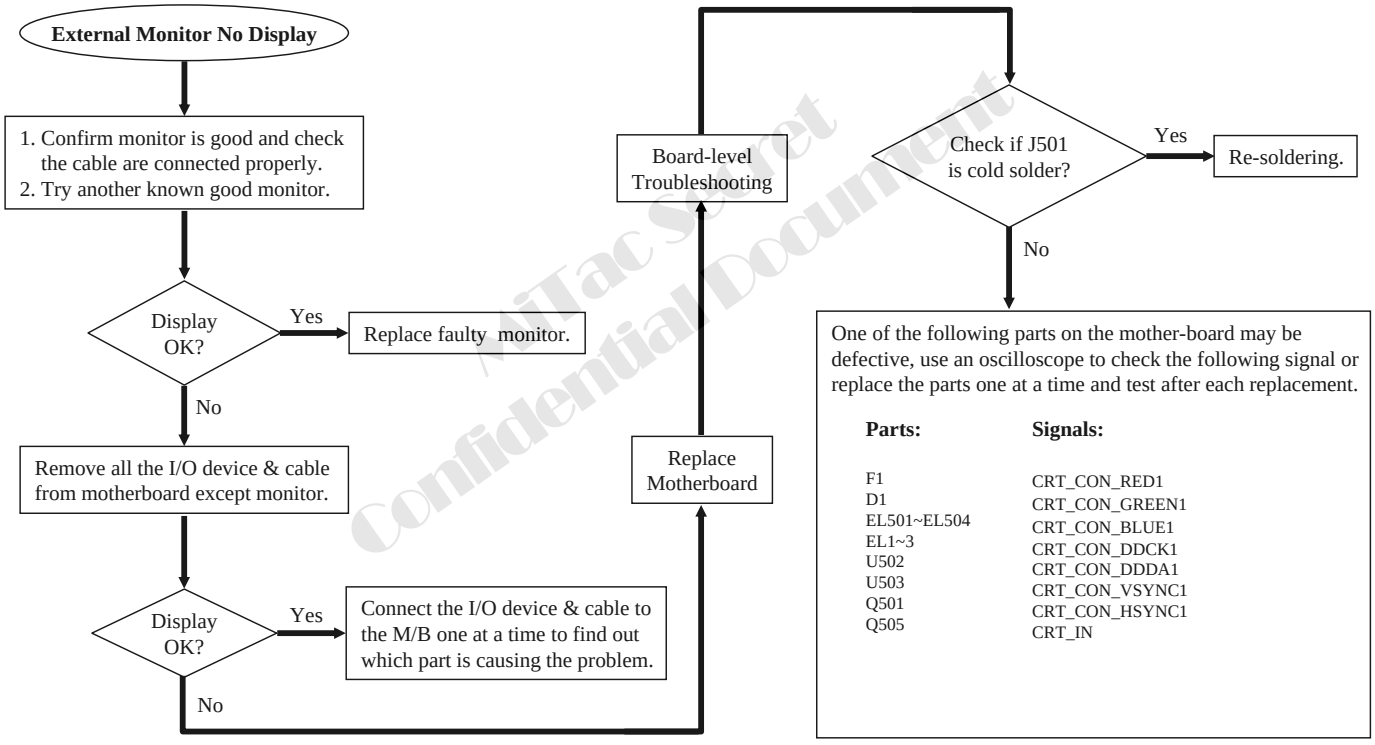
There is no display or picture abnormal on LCD although power-on-self-test is passed.



9223 N/B Maintenance

6.4 External Monitor No Display

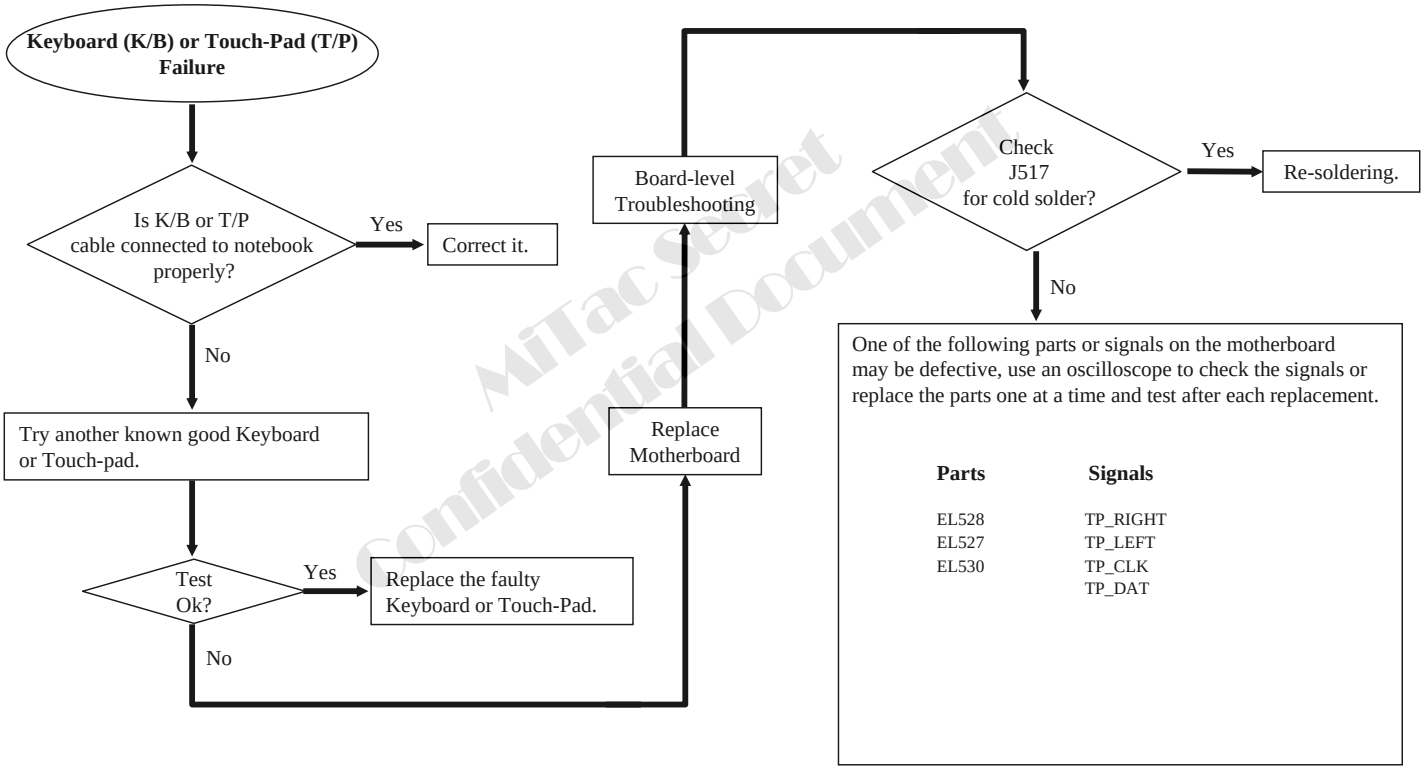
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



9223 N/B Maintenance

6.5 Keyboard (K/B) or Touch-Pad (T/P) Failure

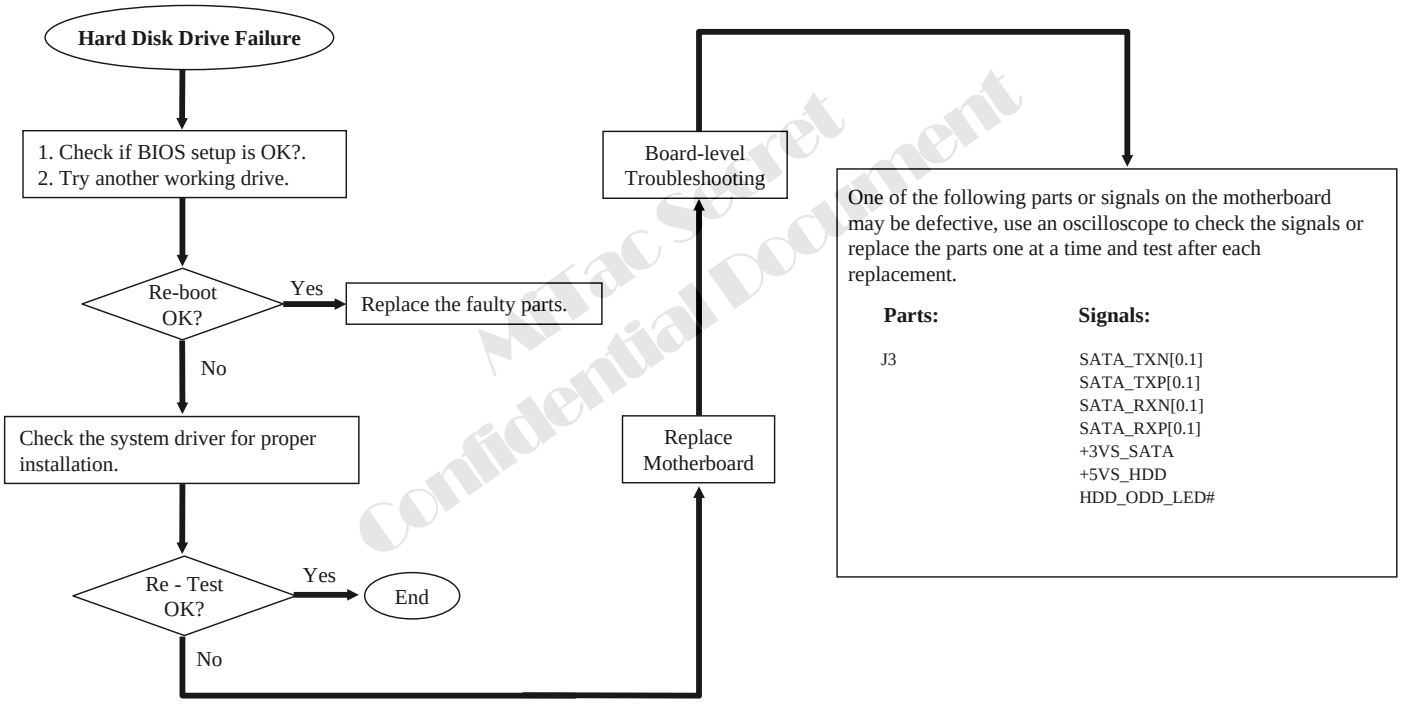
Error message of keyboard or touch-pad test error is shown or any key does not work.



9223 N/B Maintenance

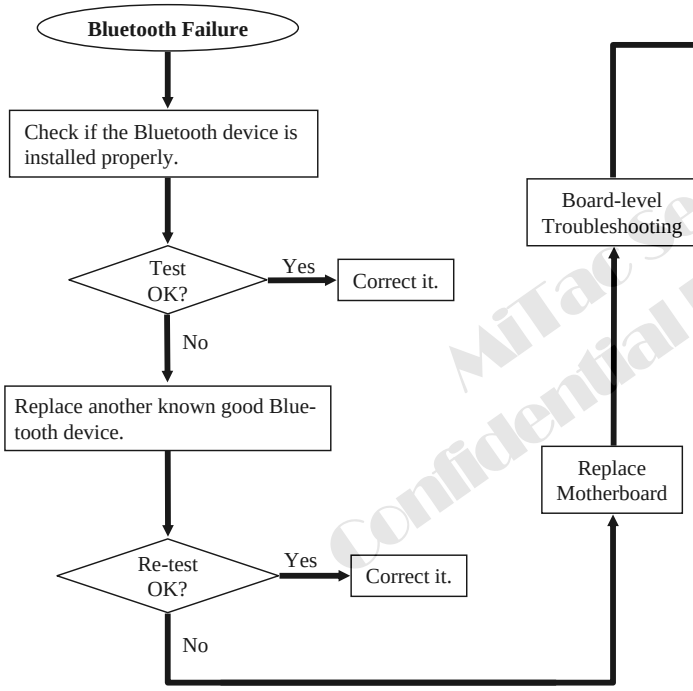
6.6 Hard Disk Drive Failure

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



6.7 Bluetooth Failure

An error occurs when a Bluetooth device is installed.

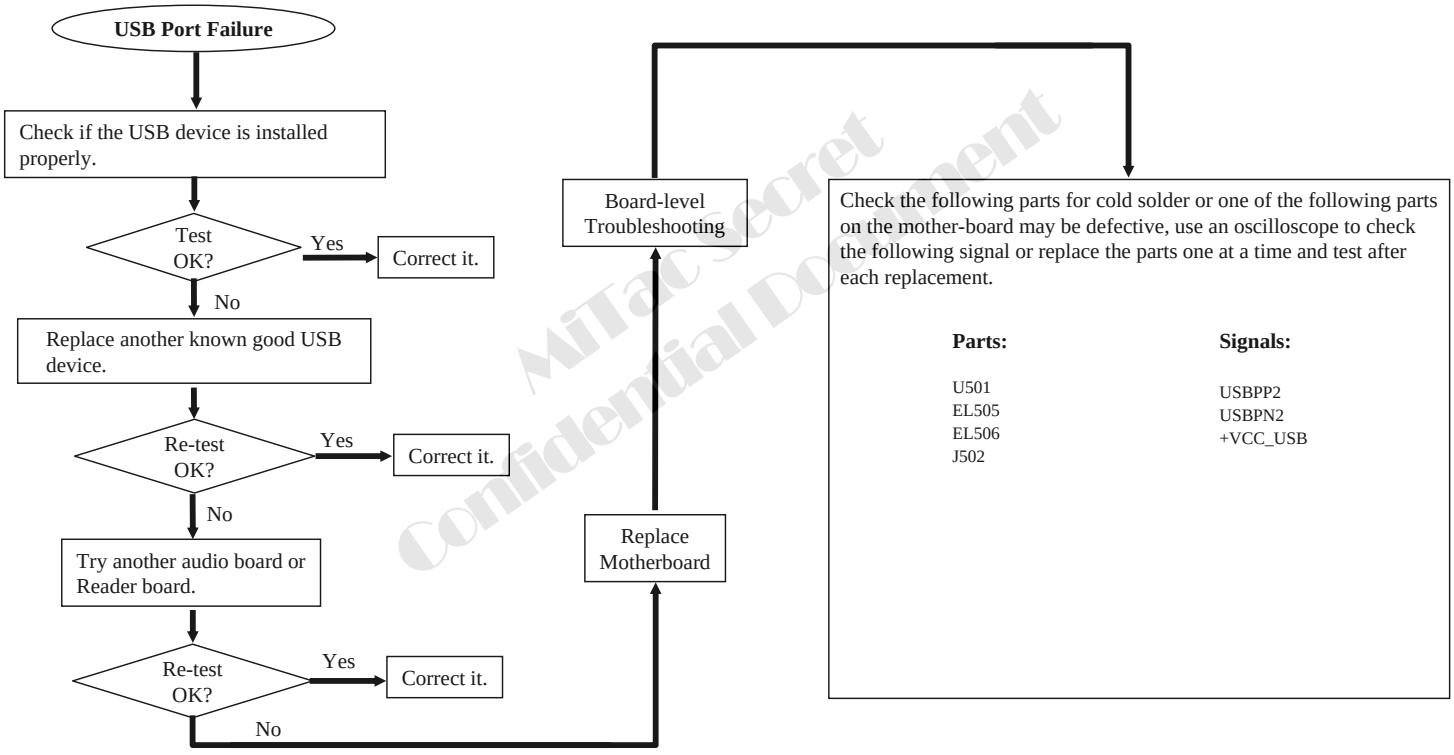


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
J506	BT_ON#
EL533	WLAN_BT_DAT
Q502	WLAN_BT_CLK
	USBPP11
	USBPN11

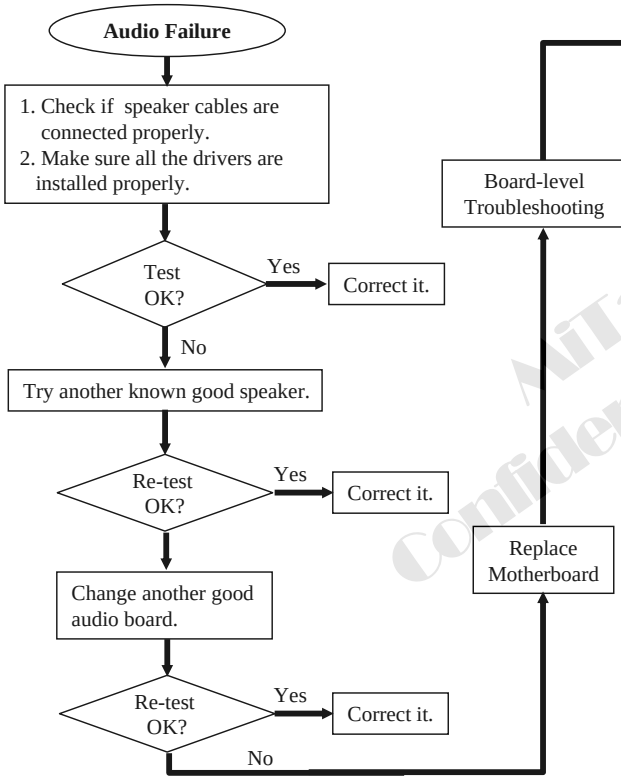
6.8 USB Port Failure

An error occurs when a USB I/O device is installed.



6.9 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

If no sound cause of line out, check the following parts & signals:

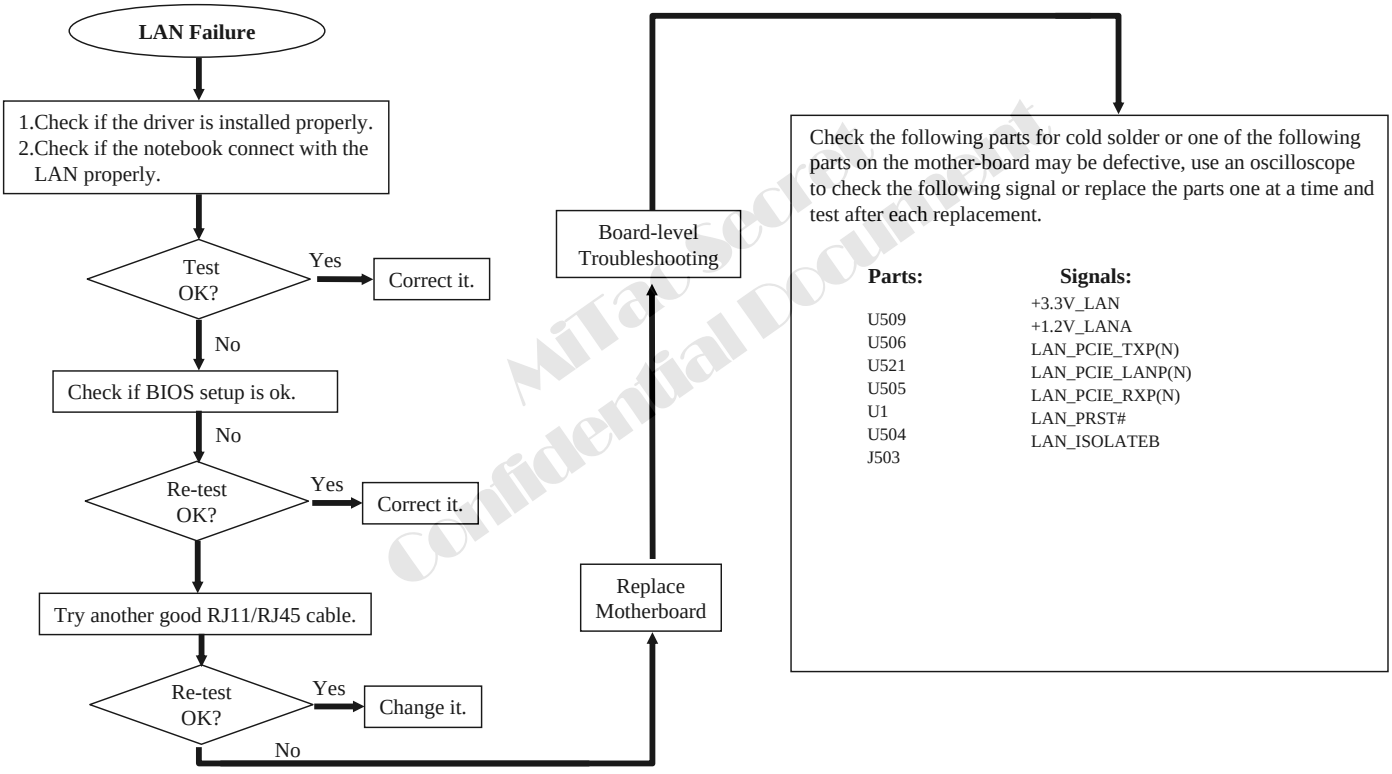
Parts:
J4

Signals:

AUDIO_PWR_ON
HP_MUTE#
SB_SPK_OFF#
SB_SPKR
+UIM PWR
UIM_RST
UIM_CLK
+UIM_VPP
UIM_DATA

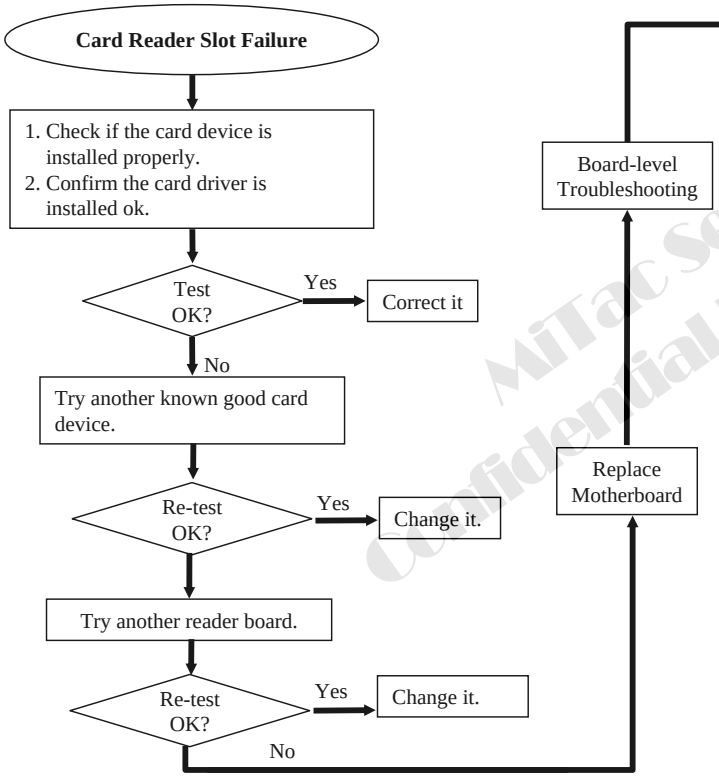
6.10 LAN Failure

An error occurs when a LAN device is installed.



6.11 Card Reader Slot Failure

An error occurs when a card device is installed.

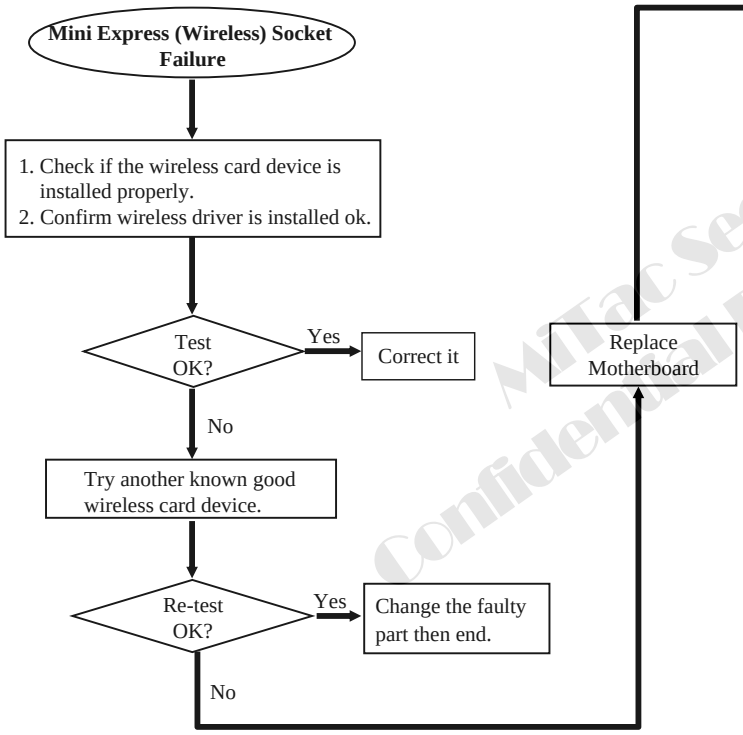


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U507	SD_CD#
J504	SD_D0_MS_D0
	SD_DATA1.2.3
	SD_CMD
	SD_CLK
	MS_CD#
	MS_CLK
	MS_DATA1.2.3

6.12 Mini Express (Wireless) Socket Failure

An error occurs when a wireless card device is installed.



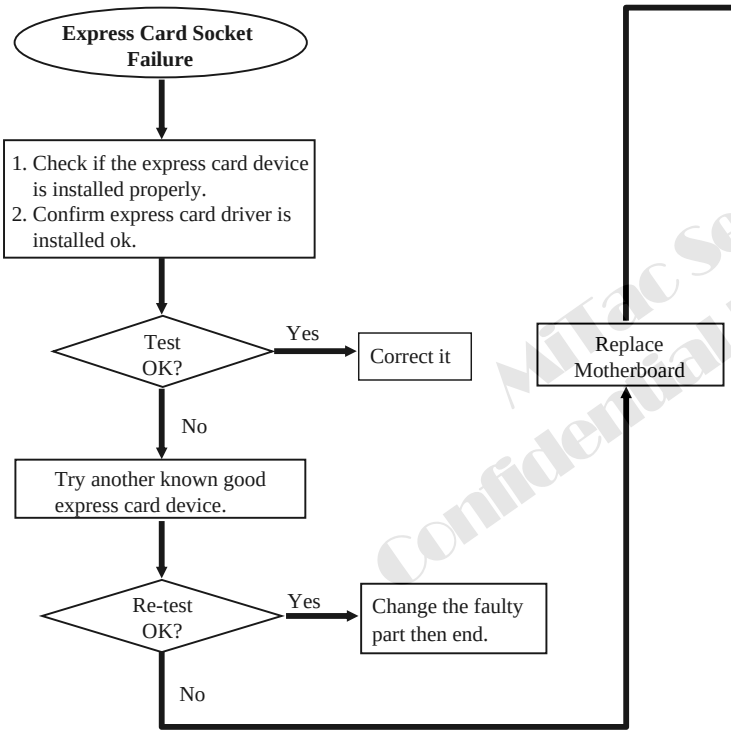
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**
J514	CLK_PCIE_SP(N)
U518	MINI_PCIE_RXP(N)
	MINI_PCIE_TXP(N)
	WLAN_BT_CLK
	WLAN_BT_DAT
	SMBCLK
	SMBDATA

6.13 Express Card Socket Failure

An error occurs when a express card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals
J1	+1.5VS_CARD
U514	+3V_CARD
	+3VS_CARD
	CLK_PCIE_CARDP(N)
	NEWCARD_PCIE_RXP(N)
	NEWCARD_PCIE_TXP(N)
	SMBCLK
	SMBDATA
	PCIE_WAKE#
	CPERST#
	CLKREQ_NEWCARD#