SERVICE MANUAL FOR

8666

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MiTAC

8666 N/B Maintenance

Contents

Contents

Contents

8666 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8666 portable notebook computer system

1.1.2 System Overview

The MiTAC 8666 model is designed for Intel Mobile Pentium-M Processor Banias 1.3G ~ 1.5GHz or Dothan 1.3G ~ 2.1GHz with 400MHz, and Dothan 1.6G ~ 2.1GHz with 533MHz FSB with Micro-FCPGA package.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as Wireless Lan indicator, Power indicator, Battery status indicator, ODD, HDD, Num Lock, Caps Lock, Scroll Lock, It also equipped with LAN, 56K Fax MODEM, 4 USB ports, S-Video and audio line out, external microphone function.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC3200 DDR400 SDRAM.

The VIA PN800 Mobile North Bridge integrates a high performance CPU interface for Intel Pentium 4 / Pentium-M

processor, a full featured AGP port controller, Integrated Graphics with 2D/ 3D/ Video Controllers, a advanced high-performance DDR400 SDRAM controller, and high bandwidth Ultra V-Link host controller connecting with VIA VT8235CE South Bridge.

The VIA VT8235CE integrates Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Inter-operable with VIA Host-to-V-Link Host Controller.

The VIA VT6103L is a Fast Ethernet 10 / 100 1-port PHY / Transceiver with MII interface, and meet all applicable IEEE 802.3, 10Base-T and 100Base-Tx standards.

The ENE CB1410 CardBus controller functions as a single slot PCI to Cardbus bridge. The CB1410 compliant with PCI Local Bus Specification Rev2.2, PC99 System Design Guide, and PC Card Standard 8.0.

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	Mobile Pentium-M Processor 1.3G ~ 1.9GHz
Core logic	VIA PN800 + VIA VT8235CE chipset
VGA Control	North Bridge Integrated
System BIOS	SST49LF040
Memory	DDR RAM : DDR333 Nanya NT512D64S8HBAFM-6K DDR400 Micron, MT8VDDT3264HD
Video Memory	Share memory
Clock Generator	ICS 950902
LVDS	VIA VT1634AL
TV	VIA VT1623M
LAN PHY	VIA VT6103L
PCMCIA	ENE CB1410
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212
Modem	AC97 Link: MDC (Mobile Daughter Card)

1.2.1 Intel Banias Processors in Micro-FCPGA Package

Intel Banias Processors with 593 pins Micro-FCBGA package.

It has the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Clock Generator

The **ICS950902** is a single chip clock solution for desktop designs using the VIA P4X/P4M/KT/KN266/333 style chipsets with PC133 or DDR memory. The **ICS950902** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the

output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

❖ **Recommended Application:**

VIA P4X/P4M/KT/KN266/333 style chipsets.

❖ **Output Features:**

- 1 - Pair of differential CPU clocks @ 3.3V (CK408)/ 1 - Pair of differential open drain CPU clocks (K7)
- 1 - Pair of differential push pull CPU_CS clocks @ 2.5V
- 3 - AGP @ 3.3V
- 7 - PCI @ 3.3V (1 - Free running)
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V (Default 48MHz I2C select only)
- 2 - REF @ 3.3V, 14.318MHz
- 12 - SDRAM (6 pair - DDR) selectable

❖ **Features/Benefits:**

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- DDR output buffer supports up to 200MHz.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

1.2.3 PN800 Mobile North Bridge

❖ **Defines Highly Integrated Solutions for Full Featured Value PC Mobile Designs**

- High Performance UMA North Bridge: Integrated Pentium 4 North Bridge with 800 MHz FSB support and UniChrome Pro 3D / 2D Graphics & Video Controllers in a single chip
- Advanced 64-bit memory controller supporting DDR400 / 333 / 266 SDRAM
- Combines with VIA VT8235-CE / VT8237 South Bridge for integrated 10/100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237)
- 1.5V Core and Pentium 4 AGTL+ I/O
- 37.5 x 37.5mm HSBGA (Ball Grid Array with Heat Spreader) package with 829 balls and 1mm ball pitch
- Pin compatible with PM800, PM880, PN880, PT800A and PT880 Pentium 4 North Bridges

❖ **High Performance CPU Interface**

- Supports Intel 800 / 533 / 400 MHz FSB Pentium 4 and Pentium M processors
- Supports Intel Hyper-Threading Technology
- Supports DBI (Dynamic Bus Inversion) and Data, Address, Response Parity
- Twelve outstanding transactions (twelve level In-Order Queue (IOQ))

- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions

❖ **Full Featured Accelerated Graphics Port (AGP) Controller**

- AGP v3.0 compliant 8x / 4x transfer modes with Fast Write support
- 1.5V AGP I/O interface
- Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
- Supports Side Band Addressing (SBA) mode
- Supports Flush / Fence commands
- Supports DBI (Dynamic Bus Inversion)
- Asynchronous AGP and CPU interface
- Thirty-two level request queue for read and write
- One-hundred-twenty-eight level (quadwords) of read data FIFO
- Sixty-four level (quadwords) of write data FIFO
- Graphics Address Relocation Table (GART)
- One level TLB structure

8666 N/B Maintenance

- Sixteen entry fully associative page table
- LRU replacement scheme

❖ **Advanced High-Performance DDR400 SDRAM Controller**

- Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface
- Supports mixed 64 / 128 / 256 / 512 / 1024Mb DDR SDRAMs in x8 and x16 configurations
- Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
- Supports 4 unbuffered double-sided DIMMs and up to 8 GBytes of physical memory
- Two sets of memory data, address and control signals each of which drives up to 2 DIMMs
- Programmable timing / drive for memory address, data and control signals independently for each signal set
- DRAM interface pseudo-synchronous with host CPU for optimal memory performance
- Concurrent CPU, AGP / integrated graphics controller and V-Link access for minimum memory access latency
- Bank interleave and up to 16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks

while accessing the current bank)

- CPU Read-Around-Write capability for non-stalled operation
- Speculative DRAM read before snoop result to reduce PCI master memory read latency
- Supports Burst Read and Write operations with burst length of 4 or 8
- Twelve cache lines (96 quadwords) of integrated CPU-to-DRAM write buffers and twelve separate cache lines of CPU-to-DRAM read prefetch buffers
- Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
- Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing

❖ **High Bandwidth 1 GB / Sec 16-Bit "Ultra V-Link" Host Controller**

- Supports 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth
- Full duplex transfers with separate command / strobe for 4x and 8x modes
- Request / Data split transaction
- Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to eliminate data wait-states and throttle transfer latency to avoid data overflow

8666 N/B Maintenance

- Highly efficient V-Link arbitration with minimum overhead

❖ **Advanced System Power Management Support**

- ACPI 2.0 and PCI Bus Power Management 1.1 compliant
- Supports Suspend-to-DRAM (STR) and DRAM self-refresh
- Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
- Supports SMI, SMM, and STPCLK mechanisms
- Supports Enhanced Intel Speedstep™ Technology
- Low-leakage I/O pads

❖ **Integrated Graphics with 2D / 3D / Video Controllers**

- Optimized Unified Memory Architecture (UMA)
- Supports 16 / 32 / 64 MB Frame Buffer sizes
- 200 MHz Graphics Engine Clock
- Two independent 128-bit data paths between North Bridge and graphics core to improve video performance, one for frame buffer access and one for texture / command access

- PCI v2.2 compliant (for control and configuration)
- AGP v3.0 compliant (for control and data transfer)

❖ **2D Acceleration**

- 128-bit 2D graphics engine
- Hardware 2D rotation
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit BLock Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32bpp) with 256-level blending effect
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

❖ 3D Acceleration

• 3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipes
- Dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 8K Texture Cache

• Capability

- Supports ROP2
- Supports various texture formats including 16/32bpp ARGB, 8bpp Palletized (ARGB), YUV 422/420 and compressed texture (DXTC)
- Texture sizes up to 2048x2048
- Microsoft DirectX texture compression
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear, and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping

- Hardware back-face culling
- Specular lighting

- **Performance**
  - Two textures per pass
  - Triangle rate up to 4.5 million triangles per second
  - Pixel rate up to 200 million pixels per second for 2 textures each
  - Texel bilinear fill rate up to 400 million texels per second
  - High quality dithering

❖ **Video Acceleration**

- **High Quality Video Processor**
  - RGB555, RGB565, RGB8888 and YUV422 video playback formats
  - High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
  - Independent graphics and video gamma tables
  - 2 sets of Color and Chroma Key support
  - Color enhancement for contrast, hue, saturation and brightness
  - YUV-to-RGB color space conversion
  - Display rotation in clockwise and counter-clockwise directions

- Bob, Weave, Median-filter and Adaptive de-interlacing modes
- 3:2 / 2:2 pull-down detection
- De-blocking mode support
- Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and deblocking to one pass process
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

- **Video Overlay**
  - Simultaneous graphics and TV video playback overlay
  - Supports video window overlays
  - Supports both YUV and RGB format Chroma Key
  - Supports 16 operations for Color and Chroma Key
  - Hardware sub-picture blending

- **MPEG Video Playback**
  - MPEG-2 hardware VLD (Various Length Decode), iDCT, and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution
  - MPEG-4 ASP (Advanced Simple Profile) Level 5 with GMC (Global Motion Compensation) L0/L1 and ¼ pixel MC support for high video quality and performance
  - High quality DVD and streaming video playback

- DVD playback auto-flipping
- DVD sub-picture playback overlay

- **Video Capture Capability**
  - 8-bit capture port following ITU-R BT656, VIP 1.1 and VIP 2.0 standards supporting 16 / 32-bit RGB and YUV422 video capture formats
  - Video capture and playback tear free auto flipping
  - Multiplexed on Digital Video Port 0 (DVP0 selectable as Capture-In or TV-Out)
  - External Hsync / Vsync support

❖ **Advanced Graphics Power Management Support**

- Built-in reference voltage generator and monitor sense circuits
- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
- External I/O signal controls enabling of graphics accelerator into standby / suspend-off state
- Dynamic clock gating for inactive functions to achieve maximum power savings
- I2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

8666 N/B Maintenance

- **Extensive Display Support for External Video Output**
  - **CRT Display Interface**
  - **Digital Video Port with Support for TV Out or Video Capture In**
  - **Digital Video Port with Support for TV Out or External DVI Transmitter**
  - **24-Bit / Dual-12-Bit FPD Interface to External LVDS Transmitter**
  - **Two Display Engines**
    - Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths, and refresh rates (supports different images on different displays simultaneously)
    - CRT, FPD, DVI monitor and TV refresh rates are independently programmable for optimum image quality
    - Improved display flexibility with simultaneous FPD / CRT, FPD / TV, FPD / DVI and other combined operations
  - **CRT Display**
    - CRT display interface with 24-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
    - Supports CRT resolutions up to 1920 x 1440
  - **TV-Out Interface**
    - 12-bit interface to external TV encoder for ATSC, NTSC or PAL TV display
    - Selectable to use either Digital Video Port 0 (DVP0) or Digital Video Port 1 (GDVP1)

- Supports 3.3V signaling on DVP0 and 1.5V signaling on GDVP1

- **12-Bit DVI Transmitter Interface**
  - Option of AGP-multiplexed digital video port 1 (GDVP1) when that port is not being used for TV out
  - Supports external DVI transmitter for a driving a DVI monitor
  - Double-data-rate data transfer with clock rates up to 165 MHz
  - Built-in digital phase adjuster to fine-tune signal timing between clock and data bus
- **24-Bit Flat Panel Display (FPD) Interface**
  - Multiplexed with external AGP port pins
  - Supports 18/24-bit FPD interface with external LVDS transmitter chip using single or double-data rate data transfer
  - Supports panel resolutions up to 1600x1200
- **Dual 12-Bit Flat Panel Display (FPD) Interface**
  - Alternate operating mode of FPD interface with external LVDS transmitters
  - Single or separate sets of clock and sync signals
  - Supports panel resolutions up to 1600x1200

❖ **Full Software Support**

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Microsoft DirectX Texture Compression (DXTC / S3TC)

- Supports OpenGL
- Drivers for major operating systems and APIs: Windows 9x/ME, Windows 2000, Windows XP, Direct3DDirectDraw, DirectShow, and OpenGL ICD for Windows 9x/ME and XP
- Windows NT 4.0 Standard VGA driver

❖ **DuoView+™ Dual Image Capability**

- WinXP, WinME and Win98 multi-monitor, extended desktop support
- Independent resolution, refresh rate and color depth for secondary desktop

1.2.4 VT8235CE Highly Integrated South Bridge

The VT8235 Version CE South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 Version CE includes standard intelligent peripheral controllers:

a) IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHYceiver.

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 Version CE also supports

the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235 Version CE includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

i) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of onboard peripherals for Windows family compliance.

The VT8235 Version CE also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 Version CE supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

1.2.5 CardBus: CB1410

Features:

3.3V operation with 5V tolerant

LFBGA 144-ball package

- **Compliant with**
  - PCI Local Bus Specification, Revision 2.2
  - PCI Bus Power Management Interface Specification, Revision 1.1
  - PCI Mobile Design Guide, Version 1.1
  - Advanced Configuration and Power Interface Specification, Revision 1.0
  - PC 99 System Design Guide
  - PC Card Standard 8.0

8666 N/B Maintenance

- **Interrupt Configuration**
  - Supports parallel PCI interrupts
  - Supports parallel IRQ and parallel PCI interrupts
  - Supports serialized IRQ and parallel PCI interrupts
  - Supports serialized IRQ and PCI interrupts
- **Power Management Control Logic**
  - Supports CLKRUN# protocol
  - Supports SUSPEND#
  - Supports PCI PME# from D3, D2, D1 and D0
  - Supports PCI PME# from D3Cold
  - Supports D3STATE# (CB1410 only)
- **Power Switch Interface**
  - CB1410 supports parallel 4 wire power switch interface.
- **Misc Control Logic**
  - Supports serial EEPROM interface
  - Supports socket activity LED
  - Supports 5 GPIOs and GPE#
  - Supports SPKROUT, CAUDIO and RIOUT#
  - Supports PCI LOCK#

1.2.6 AC'97 Audio System: Advance Logic, Inc, ALC65

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems,including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bitvolume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/

Direct Sound 3D/ I3DL2/ A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation,10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate
- Compliant with AC'97 2.3 specifications

  - 14.318MHz- 24.576MHz PLL to save crystal
  - 12.288MHz BITCLK input can be consumed
  - Integrated PCBEEP generator to save buzzer
  - Interrupt capability

- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP,PHONE-IN
- Two software selectable MIC inputs applications (software selectable)
- Boost preamplifier for MIC input 50mW/20 amplifier
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features
- Stereo MIC record for AEC/BF application
- Supports Power Off CD function
- Adjustable VREFOUT control Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification

- Power support: Digital: 3.3V; Analog: 3.3V/5V

1.2.7 MDC: PCTEL Modem Daughter Card PCT2303W (ASKEY V1456VQL-P1)

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chip set is fully programmable to meet world-wide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer

threshold. The PCT2303W chip set has been designed to meet stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

Features:

Virtual com port with a DTE throughout up to 460.8Kbps.

G3 Fax compatible

Auto dial and auto answer

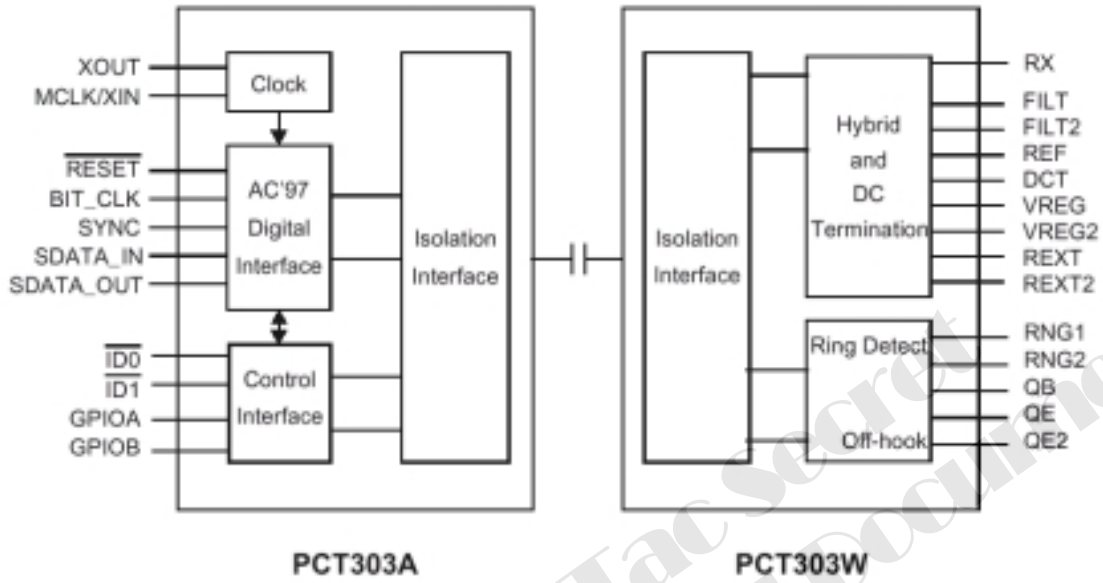
Ring detection

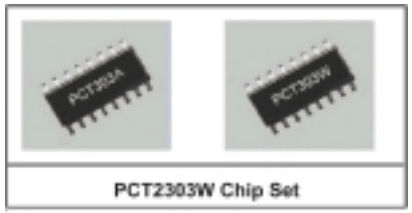
- **Codec/DAA Features**
  - AC97 2.1 compliant
  - 86dB dynamic range TX/RX paths
  - 2-4-wire hybrid
  - Integrated ring detector
  - High voltage isolation of 4000V
  - Support for “Caller ID”
  - Compliant with FCC Part68, CTR21, Net4 and JATE

- Low power standby
- Low profile SOIC package 16 pins 10x3x1.55mm
- Low power consumption
- 10mA @ 3.3V operation
- 1mA @ 3.3V power down
- Integrated modem codec

❖ **Standard Features**

- **Data**
  - ITU-T V.90 (56Kbps), V.34 (4.8Kbps TO 33.6 Kbps), V.32 bis (4.8Kbps to 14.4Kbps), V.22 bis (1.2 bps to 2.4 Kbps), V.21 and Bell 103 and 212A(300 to 1200 bps) modulation protocol
  - Data Compression ITU-T V.42bis MNP Class 5
  - Error Correction ITU-T V.42 LAPM MNP 2-4
- **Fax**
  - ITU-T V. 17, V.29, V.27ter, V.21, Channel 2, Group 3, EIA Class I





1.2.8 System Flash Memory (BIOS)

- **Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets**
- **Flexible Erase Capability**
  - Uniform 4 KByte Sectors
  - Uniform 16 KByte overlay blocks for SST49LF002A
  - Uniform 64 KByte overlay blocks for SST49LF004A
  - Top boot block protection
  - 16 KByte for SST49LF002A

- 64 KByte for SST49LF004A
- Chip-Erase for PP Mode

- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
- **Firmware Hub Hardware Interface Mode**
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block
  - Block Locking Register for all blocks
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection

1.2.9 Memory System

1.2.9.1 64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

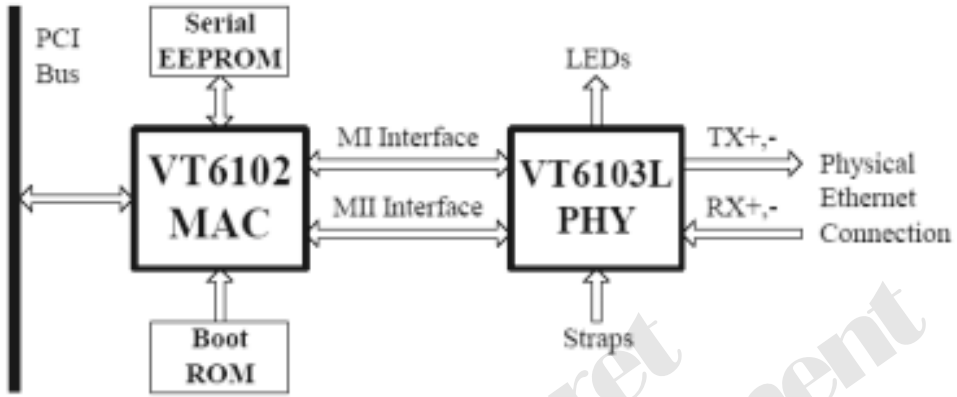
- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation

- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.10 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHY Receiver is a Low-power, Physical-layer Device (PHY)

The VT6103L is a Physical Layer device for Ethernet 10Base-T and 100Base-TX using category 5 Unshielded and Type 1 Shielded cables. This VLSI device is designed for easy implementation of 10 / 100 Mb/s Fast Ethernet LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

8666 N/B Maintenance



❖ **Product Features**

- Single Chip 100Base-TX / 10Base-T Physical Layer Solution
- Dual Speed – 100 / 10 Mbps
- Half and Full Duplex
- MII Interface to Ethernet Controller
- MII Interface to Configuration & Status
- Auto Power Saving Mode
- Auto Negotiation: 10 / 100, Full / Half Duplex
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Sta

- On Chip Wave Shaping – No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs
  - Link Status
  - Duplex status
  - Speed Status
  - Collision
- 48 Pin LQFP Package

1.2.11 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters

8666 N/B Maintenance

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB.
- Support 4 Timer (8 bit) signal with 3 prescalers
- Support 2 PWM channels, 2 D-A and 8 A-D converters
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Wireless LAN On/Off	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	CRT/LCD switch	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness Down	Decreases the LCD brightness.
Fn + F7	Brightness Up	Increases the LCD brightness.
Fn + F10	Mute system sound	
Fn + F11	LCD backlight On/Off	
Fn + F12	Suspend to RAM	Force the computer into Suspend to DRAM mode.

1.3.2 Power On/Off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode. Windows power management control panel set power button behavior.

You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None

2. Standby

3. Off

4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

1.3.4.1 Three LED Indicators

There are 2 sets of 3 LED indicators on panel housing and above keyboard separately.

From left to right that indicate WIRELESS LAN, POWER, BATTERY STATUS

-- WIRELESS LAN:

This LED lights green when operated in wireless LAN mode, otherwise it turns off.

-- POWER:

This LED lights green when the notebook was powered by AC power line or Battery, Flashes when entered suspend to RAM state. The LED is off when the notebook is in power off state.

-- BATTERY STATUS:

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes and beeps . When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged

1.3.4.2 Five LED Indicators:

System has 5 status LED indicators at front side which to display system activity. From left to right that indicate CD-ROM, HARD DISK, NUM LOCK, CAPS LOCK, SCROLL LOCK.

1.3.5 Battery Status

1.3.5.1 Battery Warning

-- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.

-- Battery Warning: Capacity below 10%, Battery Capacity LED flashes , and system beeps.

-- System will Suspend to HDD after 2 Minutes to protect users data.

1.3.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 11.5 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power On/Off Management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

CR2032 3V 220mAh lithium battery

When AC in or system main battery inside, CMOS battery will consume no power.

AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.

1.3.8 I/O Port

- One Power Supply Jack
- One External CRT Connector For CRT Display
- Supports four USB port for all USB devices
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN

- Headphone Out Jack
- Microphone Input Jack

1.3.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Power Management

The 8666 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full on Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.4.1.3 Standby Mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

-- CPU: Stop grant

-- LCD: backlight off

-- HDD: spin down

1.4.1.4 Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM

  -- CPU: off

  -- Intel 855GME: Partial off

  -- VGA: Suspend

  -- PCMCIA: Suspend

  -- Audio: off

  -- SDRAM: self refresh

- Suspend to HDD

  -- All devices are stopped clock and power-down

  -- System status is saved in HDD

-- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4.2.1 HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: VIA VT8235CE GPIO Definitions

Pin Name	MUX Function	GPIO Function	Power Plane
GPI0	B/CB#	GPI	VBAT
GPO0	WIRELESS_PD#	GPO	VSUS33
GPI1	SCI#	GPI	VSUS33
GPO1	SUSA#	GPO	VSUS33
GPI2	EXTSMI#	GPI	VSUS33
GPO2	SUSB#	GPO	VSUS33
GPI3	WAKE_UP#	GPI	VSUS33
GPO3	SUSST#	GPO	VSUS33
GPI4	LIDSW#	GPI4	VSUS33
GPO4	SPK_OFF	GPO	VSUS33
GPI5	CARD_RI#	GPI	VSUS33
GPO5	CPU_STP#	GPO	
GPI6	AGPBUSY#	GPI	
GPO6	PCI_STP#	GPO	
GPI7	PCI_REQ5#	GPI	
GPO7	PCI_GNT5#	GPO	
GPIO12	PCI_INTE#	GPIO	
GPIO13	KBD_US/JP#	GPIO	
GPIO14	CRT_IN#	GPIO	
GPIO15	ENABKL_SB	GPIO	
GPI16	X	GPI	VBAT
GPI17	X	GPI	
GPI18	SB_THRM#	GPI	
GPIO20	X	GPIO	
GPIO21	X	GPIO	
GPIO22	MINIPCI_ACT#	GPIO	
GPIO23	HDPSLP#	GPIO	
GPIO26	SMBDATA2	GPIO	VSUS33
GPIO27	SMBCLK2	GPIO	VSUS33
GPIO28	X	GPIO	
GPIO29	DPRSLPVR	GPIO	

1.6 Appendix 2: W83L950D KBC Pins Definitions (1)

Port	Pin	Function	Implement
P0	0-7	Scan matrix	KO[0..7]
P1	0-7		KO[8..15]
P3	0-7		KI[0..7]
P2	0	LPC enable	H8_THRM#
	1	GPIO x1	H8_WAKE_UP#
	2	SMBUS1 or UART	BATT_G#
	3		BATT_R#
	4	GPIO x4	EXTSMI#
	5		CAP#
	6		NUM#
	7		SCROLL#
P4	0	Xcin/cout or PWM 2,3	H8_ENABKL
	1		CHARGING
	2	GPIO x2 (INT1)	LEARING
	3		H8_SUSB
	4	KBRST	H8_HRCIN#
	5	A20	A20GATE
	6	GPIO x2	H8_SCI
	7		H8_PWRON
P5	0	GPIO x1	SW_VDD3
	1	GPIO x3 (INT20,30,40)	H8_LIDSW#
	2		BATT_DEAD#
	3		H8_ADEN#
	4	GPIO x2	BATT_LED#
	5		KBC_PWRON_VDD3S
	6	D/A, PWM 2,3	BLADJ
	7		H8_I_CTR

1.6 Appendix 2: W83L950D KBC Pins Definitions (2)

Continue to previous page

Port	Pin	Function	Implement
P6	0	A/D (INT5-12)	PWRBTN#
	1		KBC_RI#
	2		AC_ POWER#
	3		BATT_V
	4		BATT_T
	5		H8_I_LIMIT
	6		H8_PROCHOT#
	7		+BC_CPUCORE
P7	0	PS/2 port x3	T_DATA
	1		H8_RSMRST
	2		ICH_PWRBTN
	3		T_CLK
	4		H8_PWRON_SUSB#
	5		SUSC#
	6	SMBUS	BAT_DATA
	7		BAT_CLK
P8	0	LPC interface	PCICLK_KBC
	1		SERIRQ
	2		LAD3
	3		LAD2
	4		LAD1
	5		LAD0
	6		KBC_PCIRST#
	7		LFRAME#

1.7 Appendix 3: 8666 External Specifications (1)

Model	8666
CPU Intel	- Intel Pentium-M/Celeron-M Processor - FSB 533 /400MHz
Chip Set	- VIA PN800+VT 8235CE
L2 Cache	- 512K(Celeron-M)/1M(Pentium-M,Banias) / 2M (Pentium-M,Dothan)
System BIOS	- 512KB Flash EPROM - include System BIOS, VGA BIOS - Plug&Play capability -ACPI
Memory	- 0MB memory on board - 2 memory SO-DIMM slots for memory expansion - 200pin DDR333/400 SDRAM SO-DIMM Memory Module - Expandable to 2048MB (P) - 1.25-inch height memory module supported
Video Controller	- SMA (Share Memory Architecture)
Optical Drive	- Combo, DVD+RW, DVD-RW, DVD-Dual (12.7mm)/Super multi Detected as 2nd Master (by ODD F/W) - Cable select pull low, recognize as secondary master
FDD	- External USB I/F Option
HDD	- 2.5" 30GB / 40GB / 60GB / 80GB HDD(9.5mm) 4200rpm or 5400rpm - Ultra DMA 100/133(P)
Display	- 14.1"/15" XGA TFT - Resolution: 1024x768
Keyboard	- 19mm key pitch / 3mm stroke - Hot key spec: Fn+F1 : Wireless LAN ON/OFF , Fn+F3/F4 : Volume down/up, Fn+F5 : LCD/CRT output change Fn+F6/F7: Brightness up/down, Fn+F11: Display ON/OFF, Fn+F10: System Mute, Fn+F12: sleep button
Pointing Device	- TouchPad (No scroll button)
PC Card Slot	- TypeII x 1 - PCMCIA Standard Rev.2.1 , CardBus support , w/o ZV port
Audio System	- Built-in Sound system - AC97 I/F - 16-bit Sampling and Playback - 16-bit stereo - Full duplex supported - 3D sound supported - AC-3 support - Built-in stereo speaker, Built-in microphone - Sound Volume control by Hot-Key (Fn + F3 : Volume down, Fn

1.7 Appendix 3: 8666 External Specifications (2)

Continue to previous page

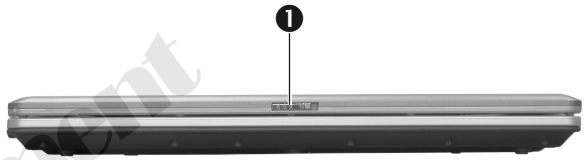
I/O Port	- USB(2.0) x 4 - Mic-in x 1(Mono) - SPDIF-out x 1 (Stereo) - S-Video (PAL/NTSC) x 1 - RJ-45 LAN Jack x 1 (with cap) RJ-11Modem Jack x 1 (with cap) - VGA port x 1 - DC-in x 1
Communication	- 56Kbps(V.90) Fax Modem(MDC) and 10/100Base-TX LAN - Wireless LAN (Mini PCI Interface IEEE802.11b, g)
Indicator	- 5 LEDs at parm rest: ODD/HDD/Number Lock/Caps Lock/Scroll Lock - 3 LEDs on LCD cover: WLAN/Power/Battery status - 3 LEDs on LCD cover: WLAN/Power/Battery status
Battery	- Li-ion Battery 2200mAh(6-cell) - Battery Life: 3 hrs (Mobile Mark, 256MB Memory, P-M 1.5GHz CPU, Backlight: Mid.) - Standard -Power-ON charge available - RTC backup battery(Lithium)
Power Supply	- 60W/65W Universal AC Adapter(100-240V)
Safety Lock	- Kensington Lock x 1
Dimension	- W277 x D329 x H26~33.3mm
Weight	- 2.6kg
OS	- Windows XP Pro (With SP2)
Accessories	- TBD
Windows Logo	- Support PC2001 Specification - Need to get the Log files for Windows XP Pro, WHQL Certified

2. System View and Disassembly

2.1 System View

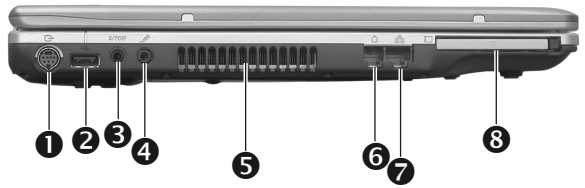
2.1.1 Front View

❶ Top Cover Latch



2.1.2 Left-side View

❶ S-Video
❷ USB Port *1
❸ Line Out Connector
❹ MIC In Connector
❺ Ventilation Openings
❻ RJ-11 Connector
❼ RJ-45 Connector
❽ PCMCIA Card Socket



2.1.3 Right-side View

❶ CD/DVD-ROM Drive
❷ USB Port *1
❸ Power Connector

2.1.4 Rear View

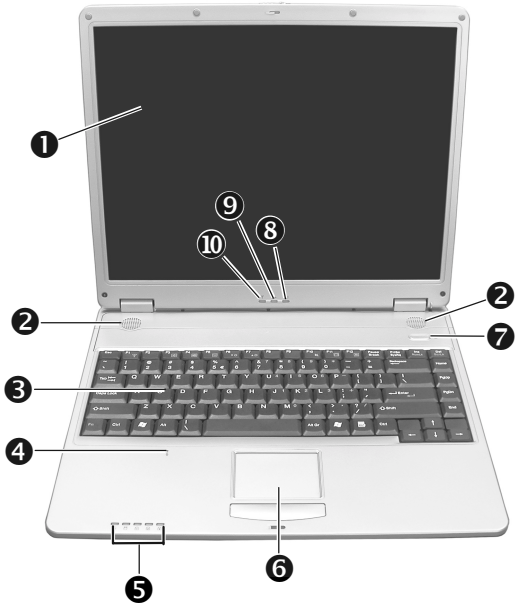
❶ Lock
❷ USB Ports *2
❸ VGA Port

2.1.5 Bottom View

❶ Hard Disk Drive
❷ CPU
❸ Battery Park

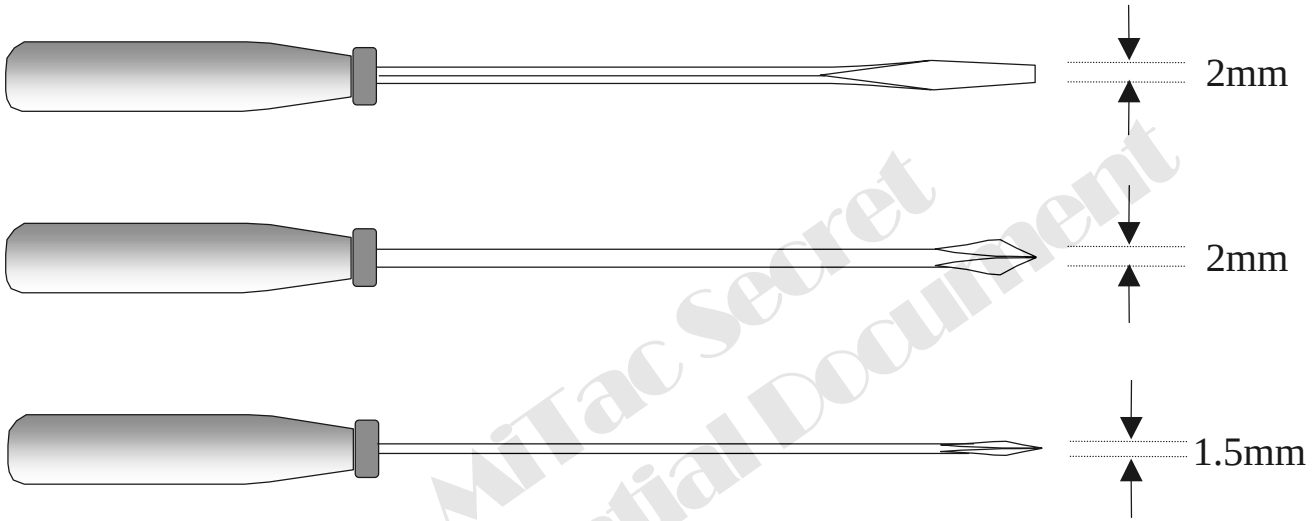
2.1.6 Top-open View

❶ LCD Screen
❷ Stereo Speaker Set
❸ Keyboard
❹ Internal MIC In
❺ Device LED Indicators
❻ Touch Pad
❼ Power Button
❽ Battery Indicator
❾ Power Indicator
❿ Wireless Indicator

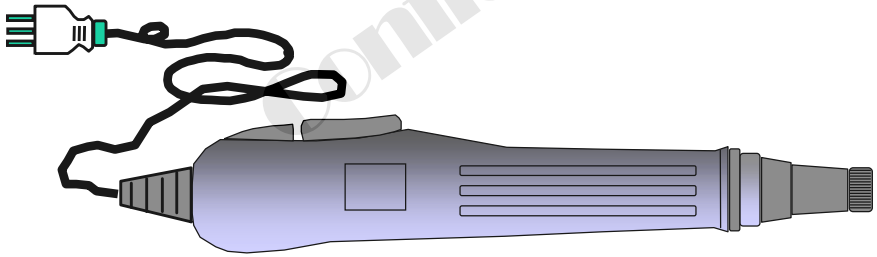


2.2 Tools Introduction

1. Minus screw driver with bit size 2mm and 1.5mm for notebook assembly & disassembly. .



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

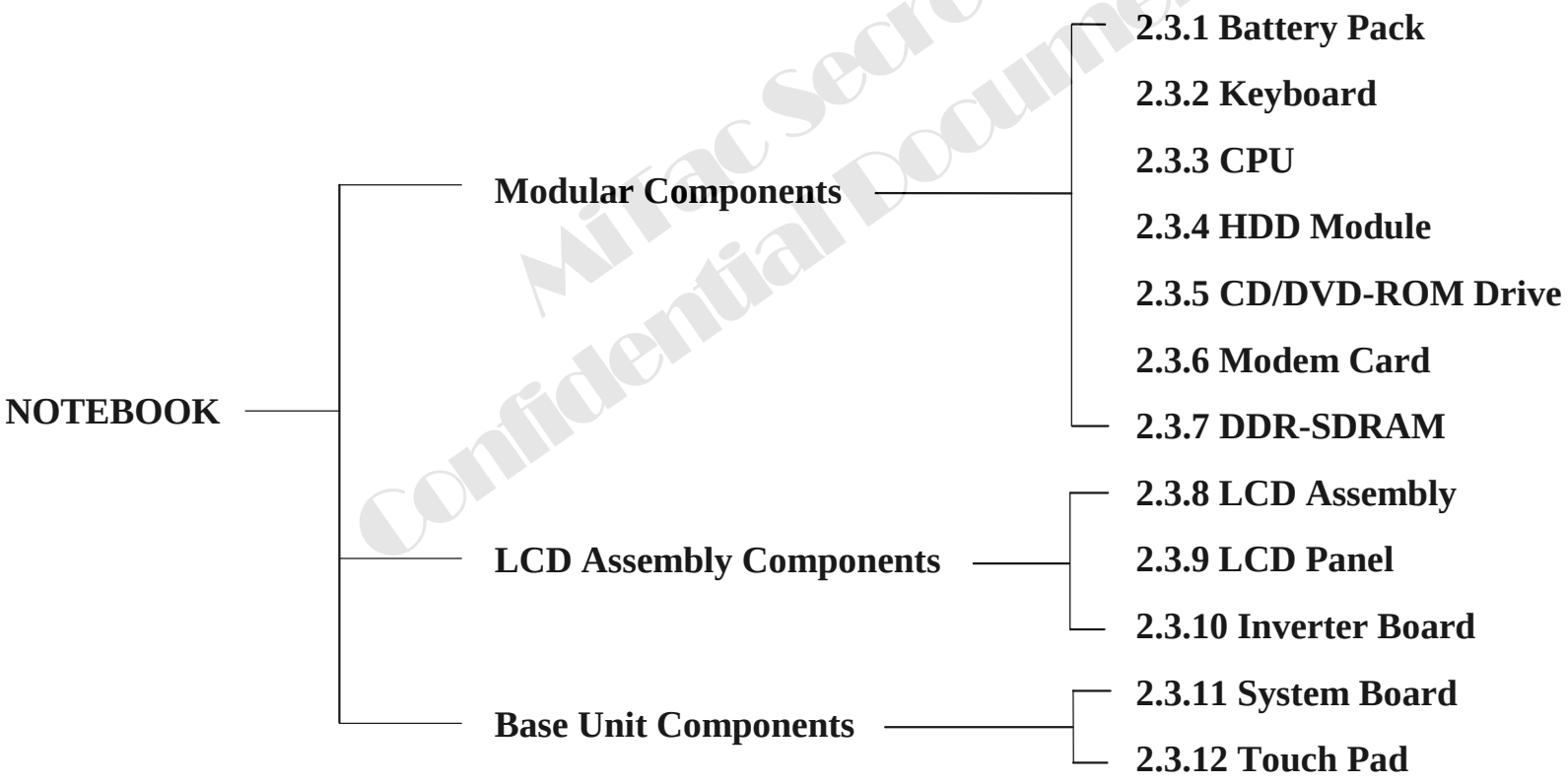
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)
3. Lift the keyboard cover up. (Figure 2-3)

Figure 2-2 Push the keyboard cover

Figure 2-3 Lift the keyboard cover

4. Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board, then separate the keyboard. (Figure 2-5)

Figure 2-4 Lift the keyboard

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard cover.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Figure 2-6)
3. Remove the four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-7)

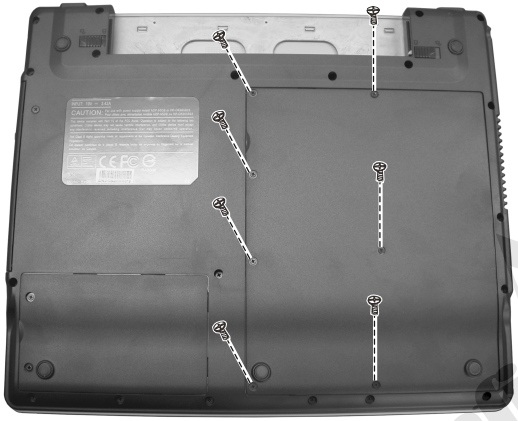


Figure 2-6 Remove the seven screws

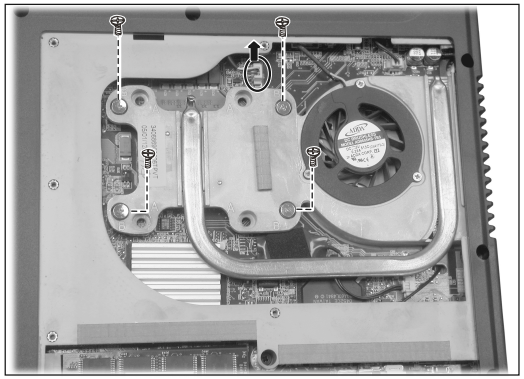


Figure 2-7 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screw driver, upraise the CPU socket to unlock the CPU. (Figure 2-8)

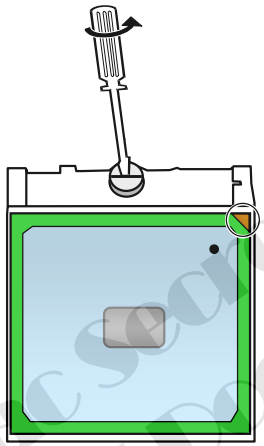


Figure 2-8 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the CPU cover and secure with seven screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-9)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-10)

Figure 2-9 Remove the HDD compartment cover

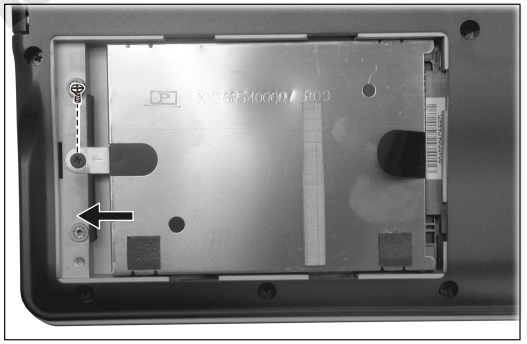


Figure 2-10 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-11)

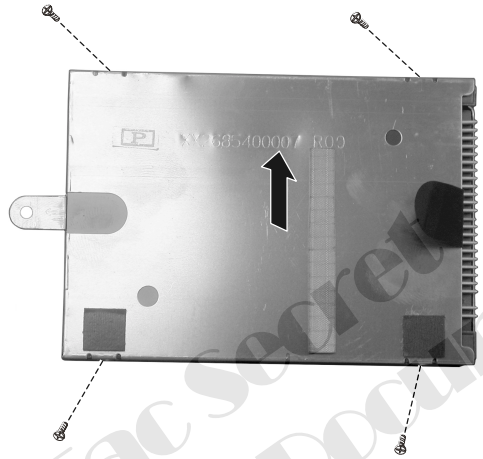


Figure 2-11 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the one screw fastening the CD/DVD-ROM drive. (Figure 2-12)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-12)

Figure 2-12 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.6 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)
3. Remove the two screws fastening the modem card. (Figure 2-13)
4. Lift up the modem card and disconnect the cord. (Figure 2-14)

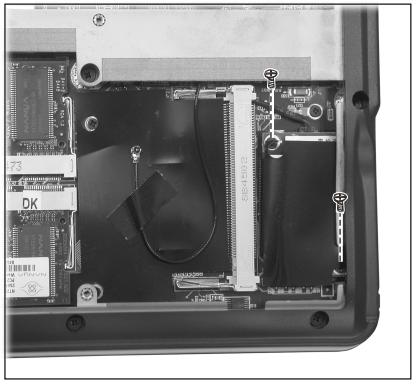


Figure 2-13 Remove the two screws

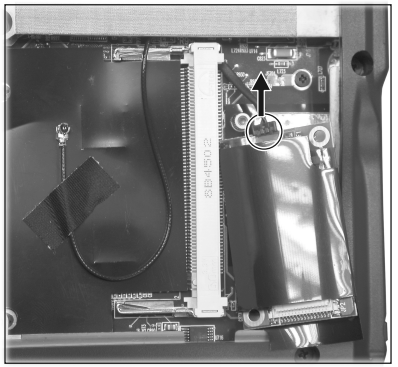


Figure 2-14 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.3.3 Reassembly)
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.7 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)

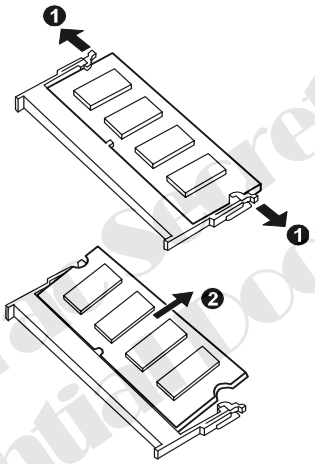


Figure 2-15 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-15)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.3.3 Reassembly)
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.3.1 and 2.3.2 Disassembly)
2. Separate the antenna from the system board. (Figure 2-16)
3. Remove the two hinge covers, then carefully pull the antenna wires out. (Figure 2-17)

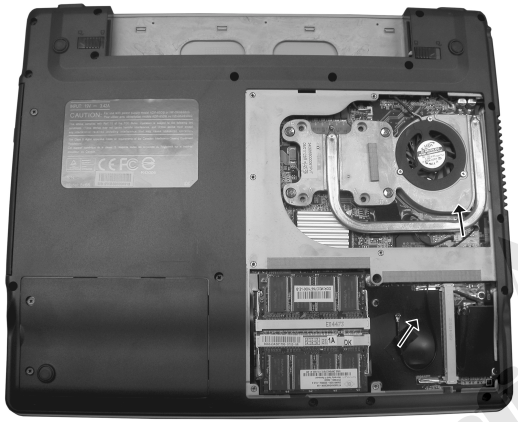


Figure 2-16 Separate the antenna

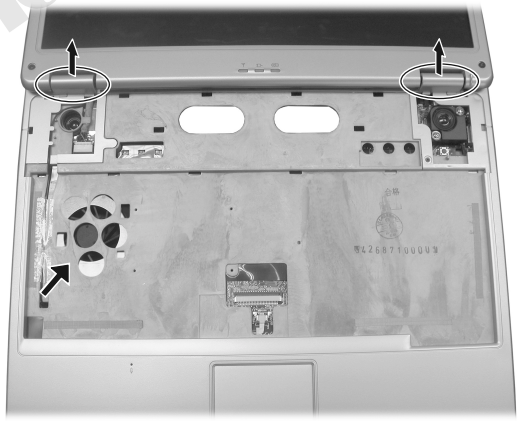


Figure 2-17 Remove the two hinge covers

4. Disconnect the two cables from the system board. (Figure 2-18)
5. Remove the four screws, then free the LCD assembly. (Figure 2-19)

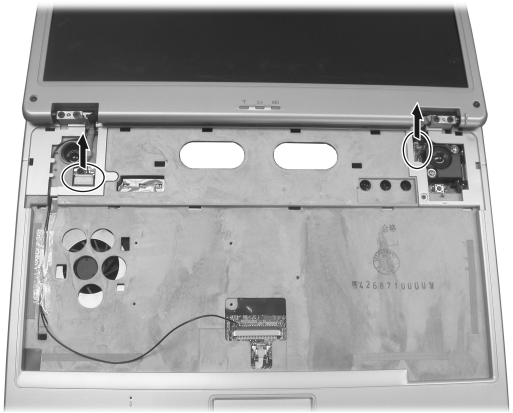


Figure 2-18 Disconnect the two cables

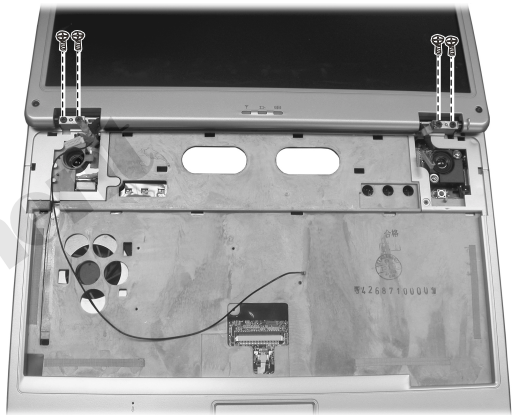


Figure 2-19 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna wires back into Mini PCI compartment.
3. Reconnect the two cables to the system board.
4. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.9 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.8 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-20)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the eight screws and disconnect the cable. (Figure 2-21)

Figure 2-20 Remove LCD cover

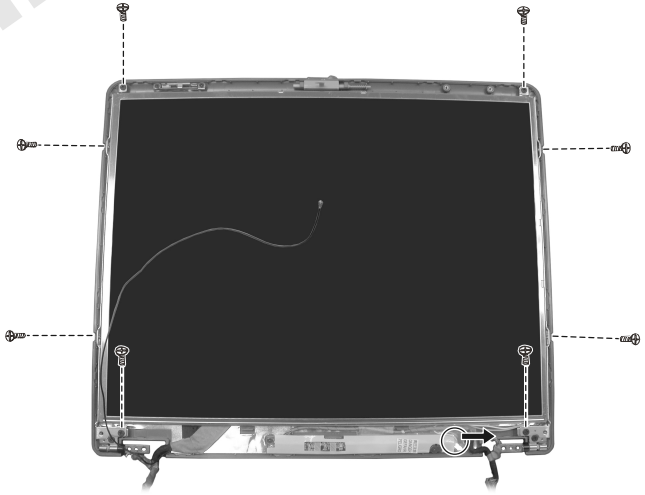


Figure 2-21 Remove the eight screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-22)
6. Disconnect the cable to free the LCD panel. (Figure 2-23)

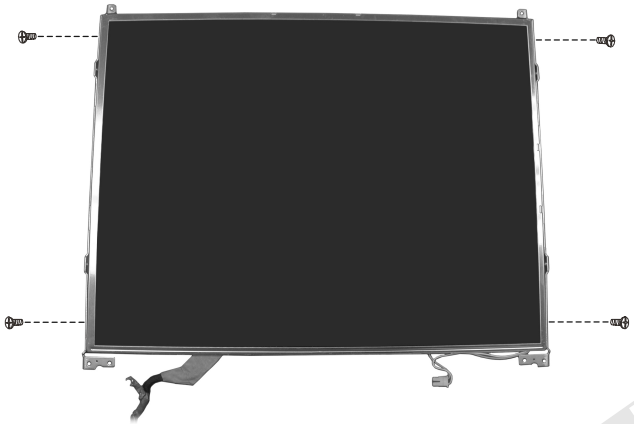


Figure 2-22 Remove the four screws

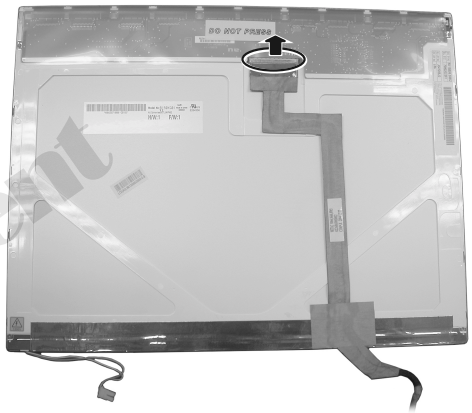


Figure 2-23 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing and secure with eight screws.
4. Reconnect one cable to inverter board.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, keyboard and battery pack. (See sections 2.3.8, 2.3.2 and 2.3.1 Reassembly)

2.3.10 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.8 Disassembly)
2. Remove the LCD cover. (Refer to the steps 1-3 of section 2.3.9 Disassembly)
3. Remove the two screws fastening the inverter board and disconnect the cable, then free the inverter board. (Figure 2-24)

Figure 2-24 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover. (Refer to section 2.3.9 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.3.8 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.3.2 and 2.3.1 Reassembly)

2.3.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, modem card, DDR and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Disconnect the touch pad's cable from the system board. (Figure 2-25)
3. Remove the three screws fastening the housing. (Figure 2-26)

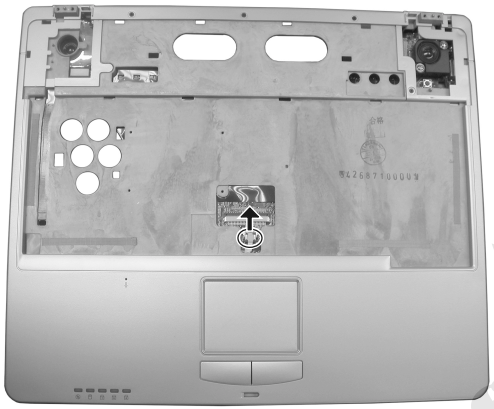


Figure 2-25 Disconnect the one cable

Figure 2-26 Remove the three screws

4. Disconnect the left speaker's cable, then remove the twenty-one screws and free the housing. (Figure 2-27)
5. Disconnect the right speaker's cable, then remove the five screws fastening the system board.And lift the system board. (Figure 2-28)

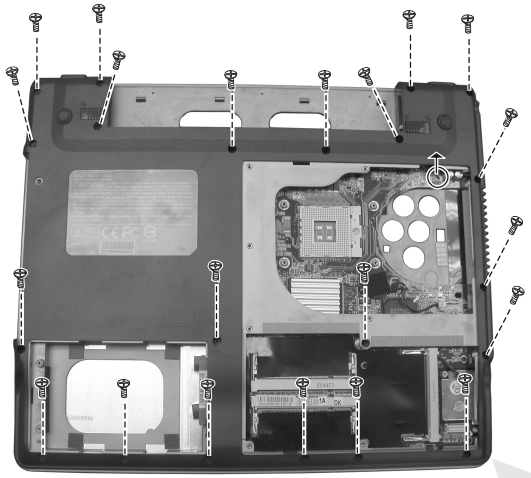


Figure 2-27 Free the housing

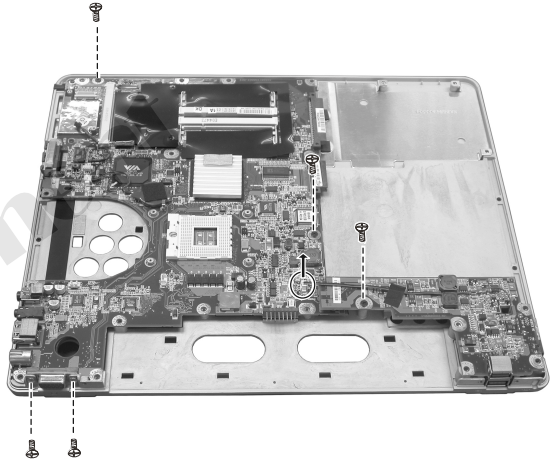


Figure 2-28 Lift the system board

6. Separate the daughter board from the system board and free the system board. (Figure 2-29)

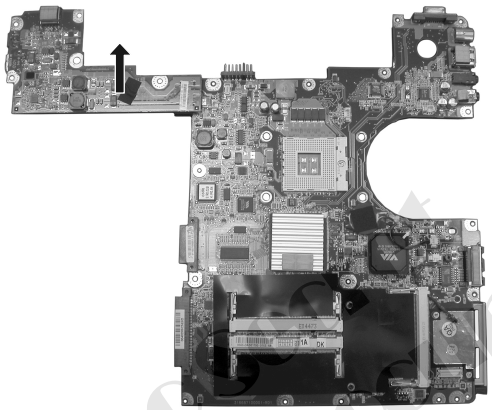


Figure 2-29 Free the system board

Reassembly

1. Replace the daughter board into the system board.
2. Replace the system board back into the top cover and secure with five screws.
3. Reconnect the right speaker's cable into the system board.
4. Replace the housing and secure with twenty-four screws.
5. Reconnect the left speaker's cable into the system board.
6. Turn over the base unit, then reconnect the touch pad's cable.
7. Replace the LCD assembly, DDR, modem card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.3.12 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, modem card, DDR, LCD assembly and the system board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7, 2.3.8 and 2.3.11 Disassembly)
2. Remove the four screws and lift the shielding, then free the touch pad. (Figure 2-30)

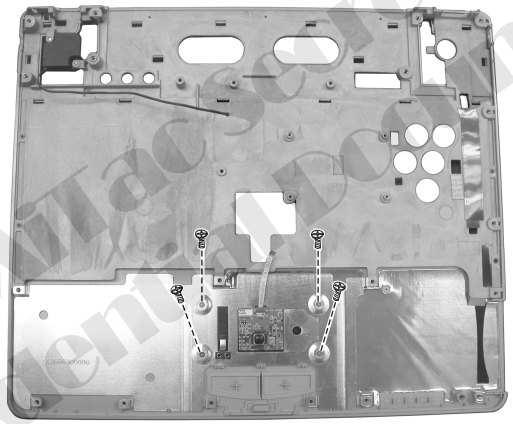


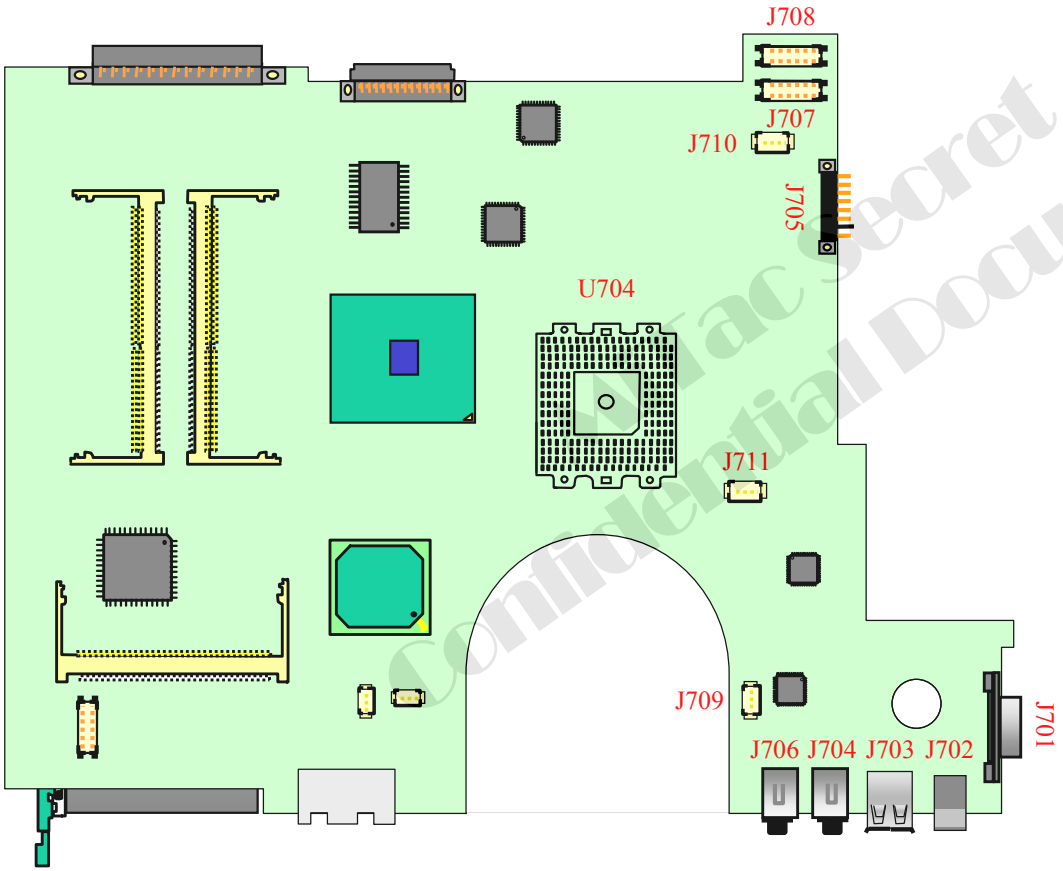
Figure 2-30 Free the touch pad

Reassembly

1. Replace the touch pad, then fit the shielding and secure with four screws.
2. Replace the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, modem card, DDR, LCD assembly and the system board. (See sections previous section reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 1

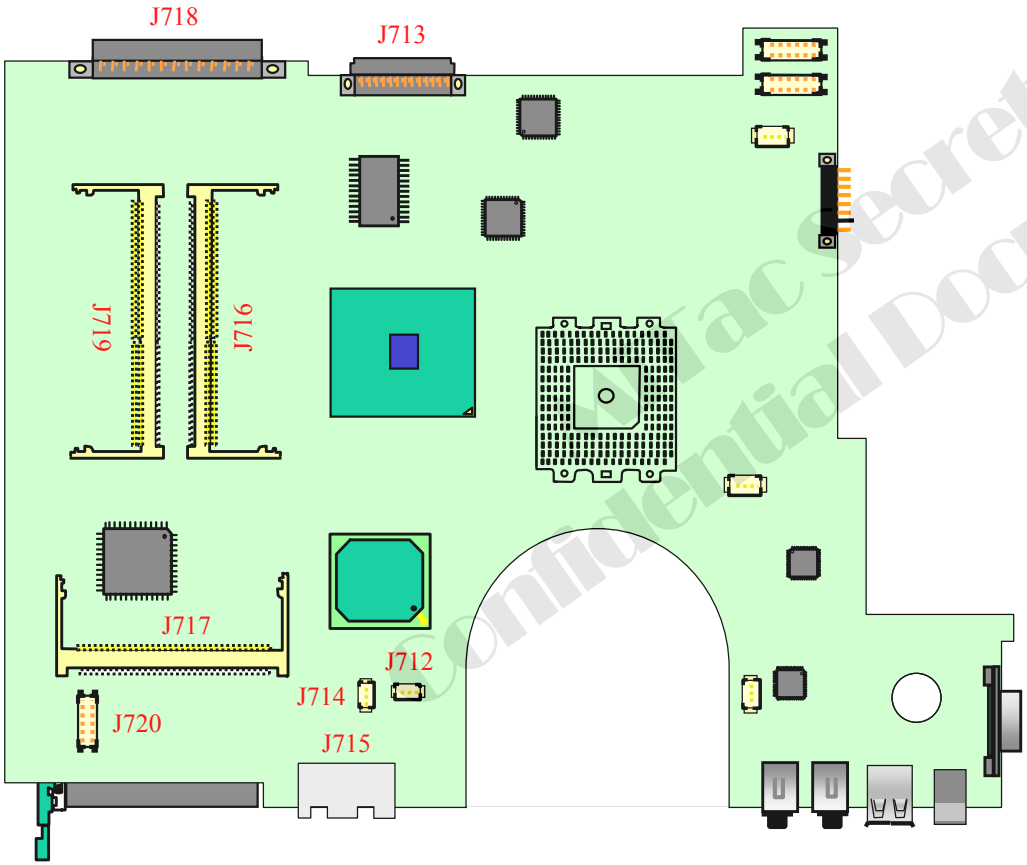


- U704 : CPU (AMD Mobile K8) Socket
- J701 : External VGA Connector
- J702 : S-Video Port
- J703 : USB Port
- J704 : Line Out Jack
- J705 : Battery Connector
- J706 : MIC In Jack
- J707,J708 : Daughter Board Connector
- J709 : Internal Left Speak Connector
- J710 : Internal Right Speak Connector
- J711 : CPU Fan Connector

------ To next page ------

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 2



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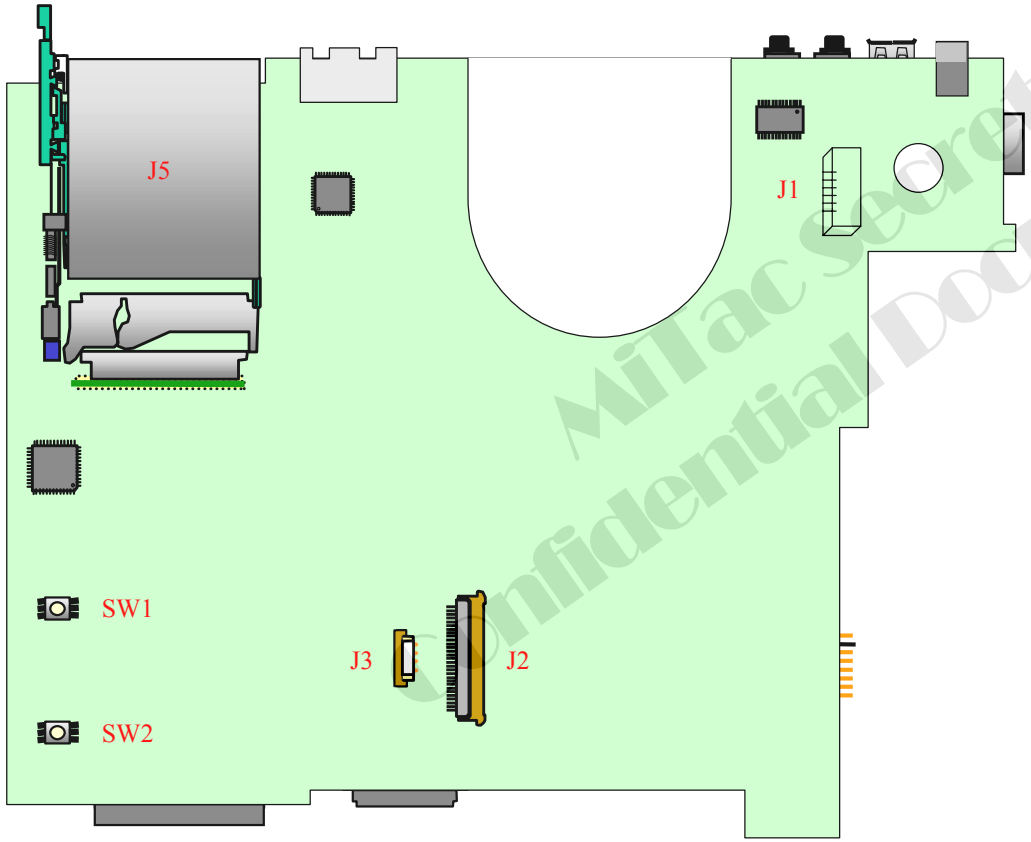
- J712 : RTC Battery Connector
- J713 : Secondary IDE Connector
- J714 : MDC Jump Wire Connector
- J715 : RJ11 & RJ45 Connector
- J716,J719 : Extend DDR SDRAM Socket
- J717 : Mini-PCI Socket
- J718 : Primary EIDE Connector
- J720 : MDC Board Connector

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side B)

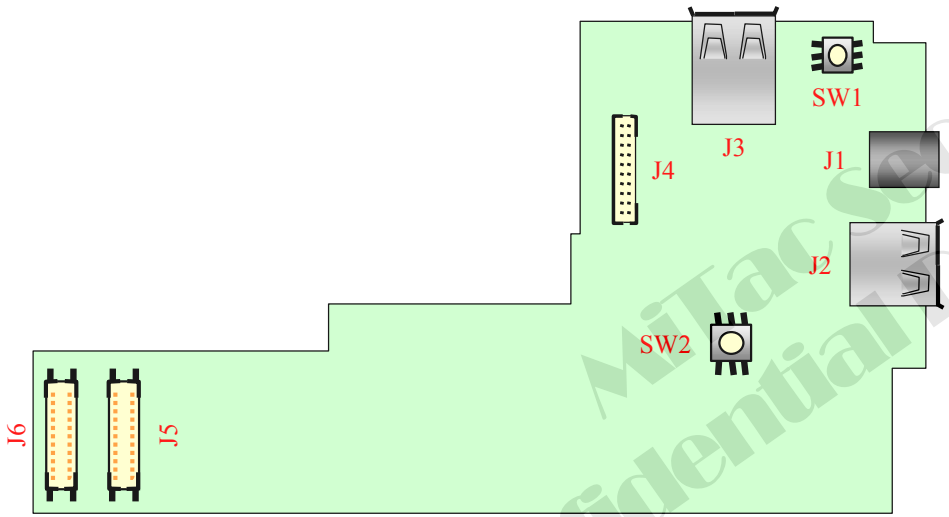


- J1 : LCD Connector
- J2 : Internal Keyboard Connector
- J3 : Touch-Pad Connector
- J5 : PCMCIA Card Socket

- SW1 : Touch-Pad Left Button
- SW2 : Touch-Pad Right Button

3. Definition & Location of Connectors / Switches

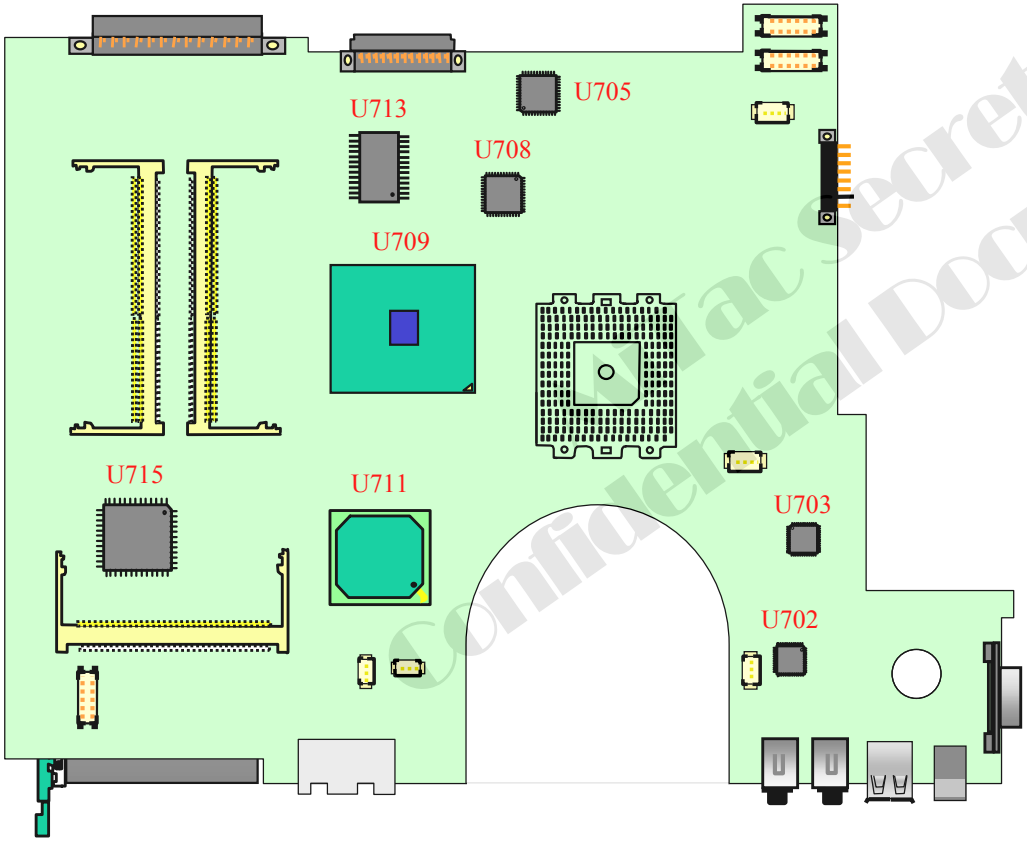
3.2 Daughter Board (Side A)



- J1 : Power Jack
- J2/J3 : USB Port
- J4 : LCD Inverter Board Connector
- J5/J6 : Daughter Board Connector
- SW1 : Cover Switch
- SW2 : Power Button

4. Definition & Location of Major Components

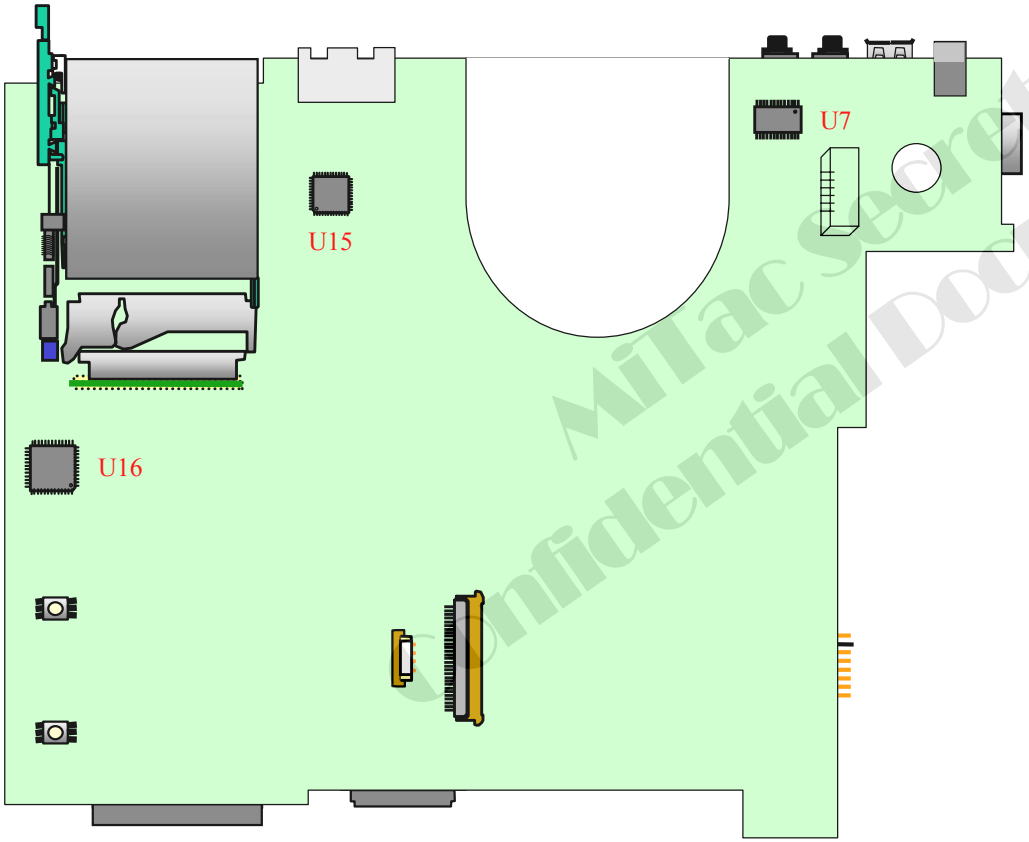
4.1 Mother Board (Side A)



- U702 : ALC655 Audio Codec
- U703 : VT1634AL LVDS Transmitter
- U705 : KBC (W83L950D)
- U708 : TV Encoder (VT1623M)
- U709 : NB VIA_PN800
- U711 : SB VT8235CE
- U713 : ICS950902 Clock Generator
- U715 : ENE CB1410 CardBus

4. Definition & Location of Major Components

4.1 Mother Board (Side B)



- U7 : TPA0212_GND Amplifier
- U15 : VT6103L LAN Controller
- U16 : System BIOS

5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor CPU - 1

CPU Pin Description

`Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

CPU Pin Description Continue

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Pentium M Processor CPU - 2

CPU Pin Description Continue

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

CPU Pin Description Continue

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Pentium M Processor CPU - 3

CPU Pin Description Continue

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

CPU Pin Description Continue

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Pentium M Processor CPU - 4

CPU Pin Description Continue

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

CPU Pin Description Continue

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 PN800 North Bridge - 1

CPU Interface

Signal Name	Pin #	I/O	Signal Description
HA[35:3]#	(see pin lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the North Bridge during cache snooping operations. Address signals up through HA[35]# allow future support of a 64 Gbyte memory space (the current design supports up to HA[33]# for support of 16 GB)..
HADSTB [1:0]#	C26, A22	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HASTB1# is the strobe for HA[31:17]# and HASTB0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see pin lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDBI[3:0]#	A5, J3, B13, A6	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTBP [3:0]# **HDSTBN [3:0]#**	D1, H3, E13, F8 E1, H2, D13, D8	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTBP3# / HDSTBN3# are the strobes for HD[63:48]# & HDBI3#; HDSTBP2# / HDSTBN2# are the strobes for HD[47:32]# & HDBI2#; HDSTBP1# / HDSTBN1# are the strobes for HD[31:16]# & HDBI1#; and HDSTBP0# / HDSTBN0# are the strobes for HD[15:0]# & HDBI0#.
ADS#	A19	IO	**Address Strob**e. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	B19	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	C19	IO	**Data Read**y. Asserted for each cycle that data is transferred.
HIT#	C17	IO	**Hi**t. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	F16	I	**Hit Modifie**d. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.

CPU Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
HLOCK#	F18	I	**Host Loc**k. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	F19, E19, D20, C20, D19	IO	**Request Comman**d. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G18	IO	**Host Target Read**y. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	B17, D18, B18	IO	**Response Signal**s. Indicates the type of response per the table below: **RS[2:0]# Response type RS[2:0]# Response type** 000 Idle State 100 Hard Failure 001 Retry Response 101 Normal Without Data 010 Defer Response 110 Implicit Writeback 011 Reserved 111 Normal With Data
DPWR#	G15	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
BREQ0#	E18	O	**Bus Request 0.** Bus request output to CPU.
BPRI#	C16	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PN800 drives this signal to gain control of the processor bus.
BNR#	C18	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	E17	IO	**Defe**r. The PN800 uses a dynamic deferring policy to optimize system performance. The PN800 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	K6	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock pin description group).

5.2 PN800 North Bridge - 2

DDR SDRAM Interface – "A" Data

Signal Name	Pin #	I/O	Signal Description
MDA[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMA[7:0]	AT16, AP20, AP24, AN32, AD35, V34, L33, D36	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSA[7:0]#	AR16, AN20, AT24, AT33, AD34, U34, L31, D35	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSA[3:0]#	AP25, AP29, AR25, AT25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEA[3:0]	L34, R35, M35, T33	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

DDR SDRAM Interface – "B" Data

Signal Name	Pin #	I/O	Signal Description
MDB[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMB[7:0]	AN18, AP22, AR28, AG32, Y33, N35, H36, A34	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSB[7:0]#	AP18, AR22, AT28, AG33, Y34, N34, H34, A33	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSB[3:0]#	AP28, AR29, AT29, AT30	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEB[3:0]	J35, K31, J33, K32	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

5.2 PN800 North Bridge - 3

AGP 8x / 4x Bus Interface

Signal Name	Pin #	I/O	Signal Description
GADSTB1F (GADSTB1 for 4x), **GADSTB1S** (GADSTB1# for 4x)	AG3 AG1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTB1F ("First" strobe) and GADSTB1# as GADSTB1S ("Second" strobe). GADSTB1 and GADSTB1# provide timing for 4x transfer mode.
GFRAME (GFRAME# for 4x)	AL4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GDEVSEL (GDEVSEL# for 4x)	AK1	IO	**Device Select (PCI transactions only).** Driven by the North Bridge when a PCI initiator is attempting to access main memory. Input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GIRDY (GIRDY# for 4x)	AL5	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AK3	IO	**Target Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when target is ready for data transfer.
AGP8XDET#	AB1	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode. Readable in Device 0 Function 0 Rx84[3].

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GADSTB assertion for AGP-style transfers and with GFRAME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE#[3:0] for 4x mode)	AK5, AK2, AL3, AN4	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AN3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE# **GDBIL**	AF4 AG4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Not**e: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F (GADSTB0 for 4x), **GADSTB0S** (GADSTB0# for 4x)	AT3 AR3	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTB0F ("First" strobe) and GADSTB0# as GADSTB0S ("Second" strobe). GADSTB0 and GADSTB0# provide timing for 4x mode.

5.2 PN800 North Bridge - 4

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GSBA[7:0]# (GSBA[7:0] for 4x)	AE1, AE4, AE3, AE2, AD2, AC3, AC4, AC1	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF (GSBSTB for 4x), **GSBSTBS** (GSBSTB# for 4x)	AD3 AD1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AE6, AE5, AD6	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting GPIPE# or start a PCI transaction by asserting GFRAME#. GST[2:0] are always outputs from the target (North Bridge) and inputs to the master (graphics controller).

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GWBF (GWBF# for 4x)	AB2	I	**Write Buffer Full.**
GRBF (GRBF# for 4x)	AE7	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GREQ (GREQ# for 4x)	AD4	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AD5	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AN1	IO	**System Error.**
GSTOP (GSTOP# for 4x)	AM3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).
Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).
Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)
Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the GSBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only GSBA (GPIPE# isn't used in 8x mode).
Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

5.2 PN800 North Bridge - 5

CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR	R1	AO	**Analog Red.** Analog red output to the CRT monitor.
AG	R2	AO	**Analog Green.** Analog green output to the CRT monitor.
AB	R3	AO	**Analog Blue.** Analog blue output to the CRT monitor.
HSYNC	U4	O	**Horizontal Sync.** Output to CRT.
VSYNC	U3	O	**Vertical Sync.** Output to CRT.
RSET	V7	AI	**Reference Resistor.** Tie to GNDDAC through an external 82 Ω 1%%resistor to control the RAMDAC full-scale current value. See Design Guide for details.

I/O pads for the pins in the above table are powered by VCC33GFX (i.e., 3.3V I/O).

Digital Power / Ground

Signal Name	Pin #	I/O	Signal Description
VTT	(see pin lists	P	**Power** for **CPU I/O Interface Logic (15 Pins).** Typical 1.65V (CPU dependent)
VCC25MEM	(see pin lists	P	**Power** for **Memory I/O Interface Logic (25 Pins).** 2.5V ±5%.
VCC15VL	AD16-17	P	**Power** for **V-Link I/O Interface Logic (2 Pins).** 1.5V ±5%
VCC15AGP	(see pin lists	P	**Power** for **AGP Bus I/O Interface Logic (6 Pins).** 1.5V ±5%
VCC33GFX	V13, W13, Y13	P	**Power for Graphics Display I/O Logic (3 Pins).** 3.3V ±5%
VCC15	(see pin lists	P	**Power** for **Internal Logic (51 Pins).** 1.5V ±5%
VSUS15	AT14	P	**Suspend Power (1 Pin).** 1.5V ±5%
GND	(see pin lists	P	**Digital Ground (161 Pins).** Connect to main ground plane.

Ultra V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD15, **VD14,** **VD13,** **VD12,** **VD11,** **VD10,** **VD9,** **VD8,** **VD7,** **VD6,** **VD5**, **VD4**, **VD3**, **VD2**, **VD1**, **VD0**	AP13 AN13 AR6 AT6 AM12 AP12 AN6 AM7 AP11 AM11 AP7 AR7 AR11 AN10 AR8 AP8	IO	**V-Link Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD pins but are on the indicated pins of the South Bridge chip). Check the strap pin table for details.
VPAR	AT7	IO	**V-Link Parity.**
VBE#	AN7	IO	**V-Link Byte Enable.**
UPCMD	AN12	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	AM10	I	**V-Link Strobe from Client to Host.**
UPSTB–	AM9	I	**V-Link Complement Strobe from Client to Host.**
DNCMD	AP10	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	AN9	O	**V-Link Strobe from Host to Client.**
DNSTB–	AP9	O	**V-Link Complement Strobe from Host to Client.**

Note: I/O pads for the pins in the above table are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

5.2 PN800 North Bridge - 6

Dedicated Digital Video Port 0 (DVP0)

Signal Name	Pin #	I/O	Signal Description
TVD11 / DVP0D11 / CAPD11, **TVD10** / DVP0D10 / CAPD10 / strap, **TVD9** / DVP0D9 / CAPD9 / strap, **TVD8** / DVP0D8 / CAPD8 / strap, **TVD7** / DVP0D7 / CAPD7 / strap, **TVD6** / DVP0D6 / CAPD6 / strap, **TVD5** / DVP0D5 / CAPD5 / strap, **TVD4** / DVP0D4 / CAPD4 / strap, **TVD3** / DVP0D3 / CAPD3 / strap, **TVD2** / DVP0D2 / CAPD2 / strap, **TVD1** / DVP0D1 / CAPD1 / strap, **TVD0** / DVP0D0 / CAPD0 / strap	AA6 AB6 AB5 Y7 Y6 Y5 AA4 Y2 Y3 AA5 W2 W1	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVHS / DVP0HS / CAPHS	W4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS / CAPVS	V1	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	W3	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKIN / DVP0DET / CAPBCLK	V2	I	**TV Encoder 0 Clock In.** Feedback from TV encoder. Internally pulled down.
TVCLK / DVP0CLK / CAPACLK	Y4	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

SMB / I2C Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
SBPLCLK	GIRDY	AL5	IO	**I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT	GC#BE1	AL3	IO	**I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK	GREQ	AD4	IO	**I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT	GGNT	AD5	IO	**I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK2 **SPCLK1** / CAPD12 **SPDAT2,** **SPDAT1** / CAPD13	n/a n/a n/a n/a	T3 V3 T4 V4	IO	**Serial Port (SMB/I2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDATn pins are the data signals used for serial data transfer. SPxxx1 is typically used for DVI monitor communications and SPxxx2 is typically used for DDC for CRT monitor communications. These pins are programmed via "Sequencer" graphics registers (port 3C5) in the "Extended" VGA register space (see the UniChrome-II Graphics Registers document for additional details). The SPxxx1 registers are programmed via 3C5.31 ("IIC Serial Port Control 1") and the SPxxx2 registers are programmed via 3C5.26 ("IIC Serial Port Control 0"). In both registers, the clock out state is programmed via bit-5 and the data out state via bit-4, clock in status may be read in bit-3 and data in status in bit-2, and the port may be enabled via bit-0.

I/O pads for SPCLK[2:1] / SPDAT[2:1] above are powered by VCC33GFX (i.e., 3.3V I/O).
All other pins in the above table are powered by VCC15AGP (i.e., 1.5V I/O)

5.2 PN800 North Bridge - 7

CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP)

Signal Name	Pin #	I/O	Signal Description
		I	**Video Capture Data.** To configure DVP0 as a video capture port, pin DVP0D6 must be strapped low. Pin Function: 8-Bit Mode / 16-Bit Mode
CAPD15 / GPO0	V5		CAPBD7 / CAPAD15
CAPD14 / GPOUT	W5		CAPBD6 / CAPAD14
CAPD13 / SPDAT1	V4		CAPBD5 / CAPAD13
CAPD12 / SPCLK1,	V3		CAPBD4 / CAPAD12
CAPD11 / DVP0D11 / TVD11,	AA6		CAPBD3 / CAPAD11
CAPD10 / DVP0D10 / TVD10 / strap,	AB6		CAPBD2 / CAPAD10
CAPD9 / DVP0D9 / TVD9 / strap,	AB5		CAPBD1 / CAPAD9
CAPD8 / DVP0D8 / TVD8 / strap,	Y7		CAPBD0 / CAPAD8
CAPD7 / DVP0D7 / TVD7 / strap,	Y6		CAPAD7 / CAPAD7
CAPD6 / DVP0D6 / TVD6 / strap,	Y5		CAPAD6 / CAPAD6
CAPD5 / DVP0D5 / TVD5 / strap,	AA4		CAPAD5 / CAPAD5
CAPD4 / DVP0D4 / TVD4 / strap,	Y2		CAPAD4 / CAPAD4
CAPD3 / DVP0D3 / TVD3 / strap,	Y3		CAPAD3 / CAPAD3
CAPD2 / DVP0D2 / TVD2 / strap,	AA5		CAPAD2 / CAPAD2
CAPD1 / DVP0D1 / TVD1 / strap,	W2		CAPAD1 / CAPAD1
CAPD0 / DVP0D0 / TVD0 / strap	W1		CAPAD0 / CAPAD0
CAPHS / DVP0HS / TVHS	W4	I	**Video Capture Horizontal Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPVS / DVP0VS / TVVS	V1	I	**Video Capture Vertical Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.

CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP) (Continued)

Signal Name	Pin #	I/O	Signal Description
CAPAFLD / BISTIN	V6	I	**Video Capture "A"-Channel TV Field Indicator.** For capture port "A" (16-bit and 8-bit mode).
CAPBCLK / DVP0DET / TVCLKIN	V2	I	**Video Capture Clock B.** Port "B" (8-bit mode) input clock from external video decoder. Internally pulled down. Not used in 16-bit mode.
CAPACLK / DVP0CLK / TVCLK	Y4	I	**Video Capture Clock A.** Port "A" (16-bit and 8-bit mode) input clock from external video decoder. Internally pulled down.

Note: I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O)

DDR SDRAM Interface – Address

Signal Name	Pin #	I/O	Signal Description
MAA[13:0], MAB[13:0]	(see pin lists)	O	**Memory Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (MAA) and EA (MAB).
BAA[1:0], BAB[1:0]	AT35, AT31, AF36, AJ36	O	**Bank Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (BA) and EA (BB).
SRASA#, SCASA#, SWEA#, SRASB#, SCASB#, SWEB#	AP26, AN25, AR26, AL29, AN28, AN31	O	**Row Address, Column Address and Write Enable Command Indicators A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 Rx E8 (ScmdA) and EA (ScmdB).

Note: I/O pads for all SDRAM pins are powered by VCC25MEM. MD / DQS input voltage levels are referenced to MEMVREF.

5.2 PN800 North Bridge - 8

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

Signal Name	AGP Name	Pin #	I/O	Signal Description
GTVD11 / GDVP1D11,	GC#BE3	AK5	O	**Data.**
GTVD10 / GDVP1D10,	GD26	AH5		
GTVD9 / GDVP1D9,	GD24	AG5		
GTVD8 / GDVP1D8,	GD30	AG6		
GTVD7 / GDVP1D7,	GD28	AH4		
GTVD6 / GDVP1D6,	GD29	AF3		
GTVD5 / GDVP1D5,	GSBA4#	AE2		
GTVD4 / GDVP1D4,	GD27	AG2		
GTVD3 / GDVP1D3,	GSBA5#	AE3		
GTVD2 / GDVP1D2,	GSBSTBS	AD1		
GTVD1 / GDVP1D1,	GSBSTBF	AD3		
GTVD0 / GDVP1D0	GSBA2#	AC3		
GTVHS / GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.** Internally pulled down.
GTVVS / GDVP1VS	GSBA0#	AC1	O	**Vertical Sync.** Internally pulled down.
GTVDE / GDVP1DE	GSBA1#	AC4	O	**Display Enable.** Internally pulled down.
GTVCLKIN / FPDET	GADSTB1S	AG1	I	**Clock In.** Input from TV encoder. Internally pulled down.
GTVCLK / GDVP1CLK	GSBA6#	AE4	O	**Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK# / GDVP1CLK#	GSBA7#	AE1	O	**Clock Out Complement.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.
I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).
Note: If the FPD port is enabled and TV-out capability is required at the same time, the dedicated TV-out port (DVP0) must be used because pin AG1 will be dedicated to the FPDET function.

AGP-Multiplexed Digital Video Port 1 (GDVP1) – DVI Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
GDVP1D11 / GTVD11,	GC#BE3	AK5	O	**Data.**
GDVP1D10 / GTVD10,	GD26	AH5		
GDVP1D9 / GTVD9,	GD24	AG5		
GDVP1D8 / GTVD8,	GD30	AG6		
GDVP1D7 / GTVD7,	GD28	AH4		
GDVP1D6 / GTVD6,	GD29	AF3		
GDVP1D5 / GTVD5,	GSBA4#	AE2		
GDVP1D4 / GTVD4,	GD27	AG2		
GDVP1D3 / GTVD3,	GSBA5#	AE3		
GDVP1D2 / GTVD2,	GSBSTBS	AD1		
GDVP1D1 / GTVD1,	GSBSTBF	AD3		
GDVP1D0 / GTVD0,	GSBA2#	AC3		
GDVP1HS / GTVHS	GSBA3#	AD2	O	**Horizontal Sync.**
GDVP1VS / GTVVS	GSBA0#	AC1	O	**Vertical Sync.**
GDVP1DE / GTVDE	GSBA1#	AC4	O	**Data Enable.**
GDVP1DET	GD31	AF1	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK / GTVCLK	GSBA6#	AE4	O	**Clock.**
GDVP1CLK# / GTVCLK#	GSBA7#	AE1	O	**Clock Complement.**

5.2 PN800 North Bridge - 9

24-Bit / Dual 12-Bit Flat Panel Display Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD23 / **FPD0D11,**	GD11	AM4	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes.
FPD22 / **FPD0D10,**	GD13	AN2		Two FPD interface modes, 24-bit and dual 12-bit, are supported.
FPD21 / **FPD0D09,**	GD14	AL1		Strapping pin DVP0D4 is used to select the interface mode to theLVDS transmitter chip:
FPD20 / **FPD0D08,**	GD15	AP1		Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit
FPD19 / **FPD0D07,**	GC#BE2	AK2		In "24-bit" mode, only one set of control pins is required. However, in dual 12-bit mode, the
FPD18 / **FPD0D06,**	GD16	AJ3		PN800 provides two sets of control signals that are required for certain LVDS transmitter chips.
FPD17 / **FPD0D05,**	GD17	AJ1		In 24-bit mode, two operating modes are supported:
FPD16 / **FPD0D04,**	GD18	AJ4		3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge
FPD15 / **FPD0D03,**	GD23	AH3		transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1
FPD14 / **FPD0D02,**	GD20	AH1		Single data rate: each clock rising edge transmits a complete 24-bit pixel
FPD13 / **FPD0D01,**	GD22	AK4		In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1
FPD12 / **FPD0D00,**	GADSTB1F	AG3		Double data rate: each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPD11 / **FPD1D1**1,	GD1	AP2		
FPD10 / **FPD1D1**0,	GD0	AT2		
FPD09 / **FPD1D0**9,	GD3	AT5		
FPD08 / **FPD1D0**8,	GD4	AR4		
FPD07 / **FPD1D0**7,	GD5	AT1		
FPD06 / **FPD1D0**6,	GD6	AN5		
FPD05 / **FPD1D0**5,	GD7	AT4		

24-Bit / Dual 12-Bit Flat Panel Display Interface (Continued)

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD04 / **FPD1D0**4,	GADSTB0F	AT3	O	
FPD03 / **FPD1D0**3,	GC#BE0	AN4		
FPD02 / **FPD1D0**2,	GADSTB0S	AR3		
FPD01 / **FPD1D0**1,	GD10	AR1		
FPD00 / **FPD1D00**	GD12	AL2		
FPHS	GFRAME	AL4	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPVS	GDEVSEL	AK1	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPDE	GD19	AK6	O	**Flat Panel Data Enable.** 24-bit mode or port 0 in dual 12-bit mode
FPDET	GADSTB1S	AG1	I	**Flat Panel Detect.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK	GD21	AH2	O	**Flat Panel Clock.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK#	GWBF	AB2	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 in dual 12-bit mode. For double-data-rate data transfers.
FP1HS	GD9	AP3	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS	GPAR	AN3	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE	GSERR	AN1	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET / GTVCLKIN	GD8	AM1	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK	GD2	AP4	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK#	GSTOP	AM3	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. For double-data-rate data transfers.

5.2 PN800 North Bridge - 10

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description	Power Plane
HCLK+	M5	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 / 166 / 200 / 266 MHz). This clock is used by all PN800 logic that is in the host CPU domain.	**VTT**
HCLK–	M6	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
MCLKOA	B31	O	**Memory (SDRAM) Clock A.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
MCLKIA	A32	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKOA.	**VCC25MEM**
MCLKOB	A31	O	**Memory (SDRAM) Clock B.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
DISPCLKI	N3	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to GND if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	N4	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**
GCLK	N7	I	**AGP Clock.** Clock for AGP logic.	**VCC15AGP**
XIN	N5	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
RESET#	AM13	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the PN800 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VSUS15**
PWROK	AP14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VSUS15**
SUSST#	AN14	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test (Continued)

Signal Name	Pin #	I/O	Signal Description	Power Plane
AGPBUSY# / NMI	AL14	O	**AGP Interface Busy.** Connect to a South Bridge GPIO pin for monitoring the status of the internal AGP bus. See Design Guide for details. Pin function selectable with Device 0 Function 0 RxBE[7] (default = NMI).	**VCC25MEM**
GPOUT / CAPD14	W5	O	**General Purpose Output.** This pin reflects the state of SRD[0].	**VCC33GFX**
GPO0 / CAPD15	V5	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].	**VCC33GFX**
INTA#	U2	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TCLK	W6	I	**Test Clock.** This pin is used for testing and must be connected to GND through a 1K-4.7K ohm resistor for all board designs.	**VCC33GFX**
TESTIN#	C31	I	**Test In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
DFTIN#	D32	I	**DFT In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
BISTIN / CAPAFLD	V6	I	**BIST In.** This pin is used for testing and must be tied to GND with a 1K-4.7K ohm resistor on all board designs.	**VCC33GFX**

Flat Panel Power Control (Muxed with AGP)

Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD	ST1	AE5	IO	**Enable Panel VDD Power.**
ENAVEE	ST0	AD6	IO	**Enable Panel VEE Power.**
ENABLT	ST2	AE6	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

5.2 PN800 North Bridge - 11

Compensation

Signal Name	Pin #	I/O	Signal Description	Power Plane
HRCOMP	F15	AI	**Host CPU Compensation.** Connect 20.5 §Ù 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.	**VTT**
VLCOMPP	AM6	AI	**V-Link Compensation.** Connect a 360Ω 1% resistor to ground.	**VCC15VL**
AGPCOMPN	AB3	AI	**AGP N Compensation.** Connect a 60.4Ω1% resistor to VCC15AGP.	**VCC15AGP**
AGPCOMPP	AC6	AI	**AGP P Compensation.** Connect a 60.4Ω1% resistor to ground.	**VCC15AGP**

Reference Voltages

Signal Name	Pin #	I/O	Signal Description	Power Plane
GTLVREF	H17	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HDVREF[0:3]	H11, H14, K7, J7	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically using a resistive voltage divider. See Design Guide.	**VTT**
HAVREF[0:1]	H19, G22	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HCOMPVREF	G14	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF [0:5]	J29, R29, W29, AE29, AK22, AK17	P	**Memory Voltage Reference.** 0.5 VCC25MEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCC25MEM**
VLVREF	AL7	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**
AGPVREF[0:1]	AF7, AD7	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Analog Power / Ground

Signal Name	Pin #	I/O	Signal Description
VCCA33HCK1	M4	P	**Power for Host CPU Clock PLL 1** (3.3V ±5%). Host CPU Clock PLL 1 generates 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, and 200 MHz.
GNDAHCK1	M3	P	**Ground for Host CPU Clock PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA33HCK2	L1	P	**Power for Host CPU Clock PLL 2** (3.3V ±5%). Host CPU Clock PLL 2 generates 500 MHz for CPU / DRAM frequencies of multiples of 166 MHz.
GNDAHCK2	L2	P	**Ground for Host CPU Clock PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	D31	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	E31	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33GCK	M1	P	**Power for AGP Clock PLL** (3.3V ±5%)
GNDAGCK	M2	P	**Ground for AGP Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA15PLL1	P3	P	**Power for Graphics Controller PLL 1** (1.5V ±5%).
GNDAPLL1	P2	P	**Ground for Graphics Controller PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA15PLL2	P6	P	**Power for Graphics Controller PLL 2** (1.5V ±5%).
GNDAPLL2	N6	P	**Ground for Graphics Controller PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA15PLL3	N1	P	**Power for Graphics Controller PLL 3** (1.5V ±5%).
GNDAPLL3	N2	P	**Ground for Graphics Controller PLL 3.** Connect to main ground plane through a ferrite bead.
VCCA33DAC[1:2]	T5, P4	P	**Power for DAC.** (3.3V ±5%)
GNDADAC[1:3]	T6, P5, R4	P	**Ground for DAC.** Connect to main ground plane through a ferrite bead.

5.3 VT8235CE South Bridge - 1

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD[7:0]	(see pin list)	IO	**Data Bus.** These pins are also used to send strap information to the chipset north bridge. At power up, VD7 reflects the state of a strap on SDCS3#, VD[6:4] reflect the state of straps on pins SDA[2:0], and VD[3:0] reflect the state of straps on pins Strap_VD3-0. The specific interpretation of these straps is north bridge chip design dependent.
VPAR	F24	IO	**Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235CE (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.
VBE#	G24	IO	**Byte Enable.**
VCLK	L22	I	**V-Link Clock.**
UPCMD	K23	O	**Command from Client-to-Host.**
DNCMD	K25	I	**Command from Host-to-Client.**
UPSTB	J26	O	**Strobe from Client-to-Host.**
UPSTB#	J24	O	**Complement Strobe from Client-to-Host.**
DNSTB	K26	I	**Strobe from Host-to-Client.**
DNSTB#	H24	I	**Complement Strobe from Host-to-Client.**

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	U26	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).
FERR#	U24	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T24	OD	**Ignore Numeric Error.** This pin is connected to the CPU iPignore errorlr pin.
INIT#	R26	OD	**Initialization.** The VT8235 Version CE asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
INTR	T25	OD	**CPU Interrupt.** INTR is driven by the VT8235 Version CE to signal the CPU that an interrupt request is pending and needs service.
NMI	T26	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 Version CE generates an NMI when PCI bus SERR# is asserted.
SLP#	V26	OD	**Sleep.** Used to put the CPU to sleep.
SMI#	U25	OD	**System Management Interrupt.** SMI# is asserted by the VT8235 Version CE to the CPU in response to different Power-Management events.
STPCLK#	R24	OD	**Stop Clock.** STPCLK# is asserted by the VT8235 Version CE to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 §Ù pullup resistors to VCC_CMOS (see Design Guide).

5.3 VT8235CE South Bridge - 2

Advanced Programmable Interrupt Controller (APIC) Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	T23	O	**Internal APIC Data 1.** Function 0 Rx58[6] = 1
APICD0	R25	O	**Internal APIC Data 0.** Function 0 Rx58[6] = 1
APICCLK	U23	I	**APIC Clock.**

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VRDSLP / GPI29/ GPO29	AB9	OD	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selectsthe proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0.
GHI# / **GPI22/ GPO22**	R22	OD	**CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0.
DPSLP# / GPI23/ GPO23	P21	OD	**CPU Deep Sleep.** This pin performs the DPSLP# function if Device 17 Function 0RxE5[3]=0.
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ# / GPI6	AD10	I	**AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinlist)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME#assertion and data is driven or received in following cycles.
CBE[3:0]#	M3, L4, C1, E2	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byteenables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	H2	IO	**Device Select.** The VT8235 Version CE asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235 Version CE-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	J1	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	J2	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	H1	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	K4	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
SERR#	C2	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 Version CE can be programmed to generate an NMI to the CPU.
PERR#	C3	_	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle.
PAR	F4	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.

5.3 VT8235CE South Bridge - 3

PCI Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
INTA# **INTB#** **INTC#** **INTD#** **INTE#** / GPI12, / GPO12, **INTF#** / GPI13, / GPO13, **INTG#** / GPI14, / GPO14, **INTH#** / GPI15, / GPO15	A4 B4 B5 C4 D4 E4 A3 B3	I	**PCI Interrupt Reques**t. The INTA# through INTD# pins are typically connected to thePCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# NTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#
REQ5# / GPI7, **REQ4#,** **REQ3#,** **REQ2#,** **REQ1#,** **REQ0#**	R3 P3 D5 C5 B6 A5	I	**PCI Request.** These signals connect to the VT8235 Version CE from each PCI slot (oreach PCI master) to request the PCI bus. To use pin R3 as REQ5#, Function 0 RxE4 mustbe set to 1 otherwise this pin will function as General Purpose Input 7.
GNT5# / GPO7, **GNT4#,** **GNT3#,** **GNT2#,** **GNT1#,** **GNT0#**	R2 R4 E5 C6 D6 A6	O	**PCI Grant.** These signals are driven by the VT8235 Version CE to grant PCI access to aspecific PCI master. To use pin R2 as GNT5#, Function 0 RxE4 must be set to 1otherwise this pin will function as General Purpose Output 7.
PCIRST#	R1	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus.
PCICLK	R23	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AB7	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 Version CE drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 §Ù resistor if the function is not used. Refer to the ihPCI Mobile Design Guidelo and applicable VIA North Bridge Design Guide (KT400A, CLE266, or P4X400) for more details.

LAN Controller - Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	B11	I	***PD***	**MII Collision Detect.** From the external PHY.
MCRS	A11	I	***PD***	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	A7	O	***PD***	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	B7	IO	***PD***	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C9	I	***PD***	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	C7, A8, B8, C8	I	***PD***	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	D8	I	***PD***	**MII Receive Data Valid.**
MRXERR	D10	I	***PD***	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	C10	I	***PD***	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	A9, B9, B10, A10	O	***PD***	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	C11	O	***PD***	**MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY.
MIIVCC	D9, E9, E10, E11	**Power**		**MII Interface Power.** 3.3V ±5%.
MIIVCC25	D12, E12	**Power**		**MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	**Power**		**Power For Internal LAN RAM.** 2.5V ±5%.
RAMGND	E6	**Power**		**Ground For Internal LAN RAM.**

5.3 VT8235CE South Bridge - 4

Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	**D11**	**O**		Serial EEPROM Chip Select.
EECK	**C12**	**O**		Serial EEPROM Clock.
EEDO	**B12**	**I**		Serial EEPROM Data Output. **Connect to EEPROM Data Out pin.**
EEDI	**A12**	**O**		Serial EEPROM Data Input. **Connect to EEPROM Data In pin.**

Low Pin Count (LPC) Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	**AF6**	**IO**		LPC Frame.
LREQ#	**AE6**	**IO**		LPC DMA / Bus Master Request.
LAD[3-0]	**AD7, AE7, AF7, AD8**	**IO**	**PU**	LPC Address / Data.

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

System Management Bus (SMB) Interface (I 2 C Bus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AC4	IO	**SMB / I 2 C Channel 1 Clock.**
SMBCK2 / GPI27 / GPO27	AC3	IO	**SMB / I 2 C Channel 2 Clock.** Rx95[2] = 0
SMBDT1	AB2	IO	**SMB / I 2 C Channel 1 Data.**
SMBDT2 / GPI26 / GPO26	AD1	IO	**SMB / I 2 C Channel 2 Data.** Rx95[2] = 0
SMBALRT#	AB1	I	**SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	E20	IO	**USB 2.0 Port 0 Data +**
USBP0Œ	D20	IO	**USB 2.0 Port 0 Data Œ**
USBP1+	A20	IO	**USB 2.0 Port 1 Data +**
USBP1Œ	B20	IO	**USB 2.0 Port 1 Data Œ**
USBP2+	E18	IO	**USB 2.0 Port 2 Data +**
USBP2Œ	D18	IO	**USB 2.0 Port 2 Data Œ**
USBP3+	A18	IO	**USB 2.0 Port 3 Data +**
USBP3Œ	B18	IO	**USB 2.0 Port 3 Data Œ**
USBP4+	D16	IO	**USB 2.0 Port 4 Data +**
USBP4Œ	E16	IO	**USB 2.0 Port 4 Data Œ**
USBP5+	A16	IO	**USB 2.0 Port 5 Data +**
USBP5Œ	B16	IO	**USB 2.0 Port 5 Data Œ**
USBCLK	E23	I	**USB 2.0 Clock.** 48MHz clock input for the USB interface
USBOC0#	C26	I	**USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1#	D24	I	**USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low.
USBOC2#	B26	I	**USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low.
USBOC3#	C25	I	**USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low.
USBOC4#	B24	I	**USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low.
USBOC5#	A24	I	**USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low.
USBVCC	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V
USBGND	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Ground.**
VSUSUSB	C24	**Power**	**USB 2.0 Suspend Power.** 2.5V ±5%.
VCCUPLL	A23, B23	**Power**	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%.
GNDUPLL	C23, D23	**Power**	**USB 2.0 PLL Analog Ground.**

5.3 VT8235CE South Bridge - 5

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY /PDDMARDY /PDSTROBE	Y22	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Read**y. Output flow control. The device mayassert DDMARDY to pause output transfers **Primary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY /SDDMARDY /SDSTROBE	AF17	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Read**y. Output flow control. The devicemay assert DDMARDY to pause output transfers **Secondary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# /PHDMARDY /PHSTROBE	W26	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Read**y. Primary channel input flow contro**l.** Thehost may assert HDMARDY to pause input transfers **Primary Host Strob**e. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# /SHDMARDY /SHSTROBE	AF23	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Read**y. Input flow control. The host mayassert HDMARDY to pause input transfers **Host Strobe** B. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# /PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# /SSTOP	AE23	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	Y23	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	AD17	I	**Secondary Device DMA Request.** Secondary channel DMA request

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
PDDACK#	Y24	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	AD23	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	AD24	I	**Primary Channel Interrupt Request.**
IRQ15	AE26	I	**Secondary Channel Interrupt Request.**
PDCS1#	V22	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	V23	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1# / strap	AF25	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the EExx pins.
SDCS3# / strap	AF26	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VD[7].
PDA[2-0]	W24, V25, W23	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0] / strap	AE24, AC22, AF24	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4].
PDD[15-0]	(see pin list)	IO	**Primary Disk Data.**
SDD[15-0]	(see pin list)	IO	**Secondary Disk Data.**

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AD9	I	**Serial IRQ.** This pin has an internal pull-up resistor.

5.3 VT8235CE South Bridge - 6

AC97 Audio / Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	T3	O	**AC97 Reset.**
ACBTCK	T1	I	**AC97 Bit Clock.**
ACSYNC	T2	O	**AC97 Sync.**
ACSDO	U2	O	**AC97 Serial Data Out.**
ACSDIN0 (VSUS33)*f*	U3	I	**AC97 Serial Data In 0.**
ACSDIN1 (VSUS33)*f*	V2	I	**AC97 Serial Data In 1.**
ACSDIN2 / GPIO20 / PCS0#	U1	I	**AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1
ACSDIN3 / GPIO21 / PCS1# / SLPBTN#	V3	I	**AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1

Resets, Clocks, and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	**AC5**	**I**	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic **powered by VBAT.**
PWROK#	**AF1**	**O**	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	**R1**	**O**	**PCI Reset.** Active low reset signal for the PCI bus. The VT8235 Version CE will assert this pin during power-up or from the control register.
OSC	**AB8**	**I**	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	**AE4**	**I**	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	**AF3**	**O**	**RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	**AE9**	**I**	**Test.**
TPO	**AF9**	**O**	**Test Pin Output.** Output pin for test mode.
NC	**(see pin list)**	**–**	**No Connect.** Do not connect.

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK / IRQ1	**W1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. **Rx51[2]=0** Interrupt Request **1. Interrupt input 1.**
MSDT / IRQ12	**W2**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**2. Interrupt input 12.
KBCK / KA20G	**W3**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	**V1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / strap	**AF10**	**O**		**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC BIOS ROM.

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

Speaker

Signal Name	Pin #	I/O	PU	Signal Description
SPKR / strap	**AF8**	**O**		**Speaker.** Strap low to enable (high to disable) CPU frequency **strapping.**

5.3 VT8235CE South Bridge - 7

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 ***(VBAT)***	**AE2**	**I**	General Purpose Input 0. **Status on PMIO Rx20[0]**
GPI1 ***(VSUS33)***	**AC2**	**I**	General Purpose Input 1. **Status on PMIO Rx20[1]**
GPI2 / EXTSMI# ***(VSUS33)***	**AA1**	**I**	General Purpose Input 2. **Status on PMIO Rx20[4]**
GPI3 / RING# ***(VSUS33)***	**Y2**	**I**	General Purpose Input 3. **Status on PMIO Rx20[8]**
GPI4 / LID# ***(VSUS33)***	**AC1**	**I**	General Purpose Input 4. **Status on PMIO Rx20[11]**
GPI5 / BATLOW# ***(VSUS33)***	**V4**	**I**	General Purpose Input 5. **Status on PMIO Rx20[12]**
GPI6 / AGPBZ#	**AD10**	**I**	General Purpose Input 6. **Status on PMIO Rx20[5]**
GPI7 / REQ5#	**R3**	**I**	General Purpose Input 7. **RxE4[2] = 0**
GPI12 / GPO12 / INTE#	**D4**	**I**	General Purpose Input 12. **RxE4[4] = 0, 5B[1]=0**
GPI13 / GPO13 / INTF#	**E4**	**I**	General Purpose Input 13. **RxE4[4] = 0, 5B[1]=0**
GPI14 / GPO14 / INTG#	**A3**	**I**	General Purpose Input 14. **RxE4[4] = 0, 5B[1]=0**
GPI15 / GPO15 / INTH#	**B3**	**I**	General Purpose Input 15. **RxE4[4] = 0, 5B[1]=0**
GPI16 / INTRUDER# ***(VBAT)***	**AE1**	**I**	General Purpose Input 16. **Status on PMIO Rx20[6]**
GPI17 / CPUMISS	**Y1**	**I**	General Purpose Input 17. **Status on PMIO Rx20[5]**
GPI18 / THRM# / AOLGPI	**Y4**	**I**	General Purpose Input 18. **Rx8C[3] = 0**
GPI20 / GPO20 / ACSDIN2 / PCS0#	**U1**	**I**	**General Purpose Input 20.** RxE4[6]=1, E5[1]=0, **PMIO 4C[20] = 1**
GPI21 / GPO21 / ACSDIN3 / PCS1# / SLPBTN#	**V3**	**I**	**General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1
GPI22 / GPO22 / GHI#	**R22**	**I**	**General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1
GPI23 / GPO23 / DPSLP#	**P21**	**I**	**General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1

General Purpose Inputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPI26 / GPO26 / SMBDT2 ***(VSUS33)***	**AD1**	**I**	**General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0
GPI27 / GPO27 / SMBCK2 ***(VSUS33)***	**AC3**	**I**	**General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0
GPI28 / GPO28	**AC8**	**I**	**General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1
GPI29 / GPO29 / VRDSLP	**AB9**	**I**	**General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1

Note: Register references above are Device 17 Function 0 unless indicated otherwise.
Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0# / GPIO20 / ACSDIN2	**U1**	**O**	Programmable Chip Select 0. **RxE4[6]=1, E5[1]=1**
PCS1# / GPIO21 / ACSDIN3 / SLPBTN#	**V3**	**O**	Programmable Chip Select 1. **RxE4[6]=1, E5[2]=1**

5.3 VT8235CE South Bridge - 8

General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO0 ***(VSUS33)***	**AA3**	**O**	General Purpose Output 0.
GPO1 / SUSA# ***(VSUS33)***	**AA2**	**O**	General Purpose Output 1. **Rx94[2] = 1**
GPO2 / SUSB# ***(VSUS33)***	**AD3**	**O**	General Purpose Output 2. **Rx94[3] = 1**
GPO3 / SUSST1# ***(VSUS33)***	**Y3**	**O**	General Purpose Output 3. **Rx94[4] = 1**
GPO4 / SUSCLK ***(VSUS33)***	**AB3**	**O**	General Purpose Output 4. **Rx95[1] = 1**
GPO5 / CPUSTP#	**AC7**	**O**	General Purpose Output 5. **RxE4[0] = 1**
GPO6 / PCISTP#	**AD6**	**O**	General Purpose Output 6. **RxE4[1] = 1**
GPO7 / GNT5#	**R2**	**O**	General Purpose Output 7. **RxE4[2] = 0**
GPO12 / GPI12 / INTE#	**D4**	**O**	General Purpose Output 12. **RxE4[4]=1, 5B[1]=0**
GPO13 / GPI13 / INTF#	**E4**	**O**	General Purpose Output 13. **RxE4[4]=1, 5B[1]=0**
GPO14 / GPI14 / INTG#	**A3**	**O**	General Purpose Output 14. **RxE4[4]=1, 5B[1]=0**
GPO15 / GPI15 / INTH#	**B3**	**O**	General Purpose Output 15. **RxE4[4]=1, 5B[1]=0**
GPO20 / GPI20 / ACSDIN2 / PCS0#	**U1**	**OD**	General Purpose Output 20. **RxE4[6]=1, E5[1]=0**
GPO21 / GPI21 / ACSDIN3 / PCS1# /SLPBTN#	**V3**	**OD**	General Purpose Output 21. **RxE4[6]=1, E5[2]=0**
GPO22 / GPI22 / GHI#	**R22**	**OD**	General Purpose Output 22. **RxE5[3]=1, PMIO 4C[22]=1**
GPO23 / GPI23 / DPSLP#	**P21**	**OD**	General Purpose Output 23. **RxE5[3]=1, PMIO 4C[23]=1**
GPO26 / GPI26 / SMBDT2 ***(VSUS33f)***	**AD1**	**OD**	General Purpose Output 26. **Rx95[2] = 1, 95[3] = 1**
GPO27 / GPI27 / SMBCK2 ***(VSUS33f)***	**AC3**	**OD**	General Purpose Output 27. **Rx95[2] = 1, 95[3] = 1**

General Purpose Outputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPO28 / GPI28	**AC8**	**OD**	General Purpose Output 28. **RxE5[3] = 1, PMIO 4C[28]=1**
GPO29 / GPI29 / VRDSLP	**AB9**	**OD**	General Purpose Output 29. **RxE5[3] = 1, PMIO 4C[29]=1**

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: Default pin functions are underlined in the table above.

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	**AD2**	**I**	**Power Button.** Used by the Power Management subsystem to monitor an external **system on/off button or switch. Internal logic powered by VSUS33.**
SLPBTN# / GPIO21/ ACSDIN3 / PCS1#	**V3**	**I**	**Sleep Button.** Used by the Power Management subsystem to monitor an external sleepbutton or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1
RSMRST#	**AD4**	**I**	**Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.
EXTSMI# / GPI2	**AA1**	**IOD**	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only)
PME#	**W4**	**I**	**Power Management Event.** (10K PU to VSUS33 if not used)
SMBALRT#	**AB1**	**I**	**SMB Alert**. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used)

5.3 VT8235CE South Bridge - 9

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
LID# / GPI4	**AC1**	**I**	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used)
INTRUDER# / GPI16	**AE1**	**I**	**Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6]
THRM# / GPI18/ AOLGPI	**Y4**	**I**	**Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIORx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-4]).
RING# / GPI3	**Y2**	**I**	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used)
BATLOW# / GPI5	**V4**	**I**	**Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only)
CPUSTP# / GPO5	**AC7**	**O**	**CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO6	**AD6**	**O**	**PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1	**AA2**	**O**	**Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used)
SUSB# / GPO2	**AD3**	**O**	**Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used)
SUSC#	**AF2**	**O**	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used)

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
SUSST1# / GPO3	**Y3**	**O**	**Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33.
SUSCLK	**AB3**	**O**	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., KT400A, CLE266, or P4X400) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS / GPI17	**Y1**	**I**	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AOLGPI / GPI18/ THRM#	**Y4**	**I**	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pinmay be used as AOLGPI, GPI18 and THRM# all at the same time.

Strap Pins for VT8235 Version CE Configuration

Signal Name	Pin #	Function	Description	Note
Strap_AUTO	**AE10**	**Auto Reboot**	L: Enable Auto Reboot **H: Disable Auto Reboot (Default)**	
SPKR	**AF8**	**CPU Frequency Strapping**	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping (Default)	
KBCS#	**AF10**	**Internal Keyboard** Controller	L: Disable internal KBC H: Enable internal KBC (Default)	
SDCS1#	**AF25**	Eliminate External LAN EEPROM	L: Enable. Use external EEPROM (Default) H: Disable. Do not use external EEPROM	

5.3 VT8235CE South Bridge - 10

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VSUS33	AA4, AB4-6	P	**Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the ihsoft-offlÉD state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT#
VSUS25	T4, U4	P	**Suspend Power.** 2.5V ±5%.
VSUSUSB	C24	P	**USB Suspend Power.** 2.5V ±5%.
VBAT	AF4	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VLVREF	H22	P	**V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers.
VLCOMP	J22	AI	**V-Link Compensation.**
VCCVK	(see pin list)	P	**V-Link Compensation Circuit Voltage.** 2.5V ±5%
MIIVCC	D9, E9-11	P	**LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead.
MIIVCC25	D12. E12	P	**LAN MII Suspend Power.** 2.5V ±5%.
LANVCC	E7	P	**LAN Power.** 2.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
LANGND	E6	P	**LAN Ground.** Connect to GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0Œ, P1+, P1Œ, P2+, P2Œ, P3+, P3Œ, P4+, P4Œ, P5+, P5Œ). Connect to VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.
VCCUPLL	A23, B23	P	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead.
GNDUPLL	C23, D23	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	T22	P	**PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead.
PLLGND	U22	P	**PLL Analog Ground.** Connect to GND through a ferrite bead.

Power and Ground （Continued）

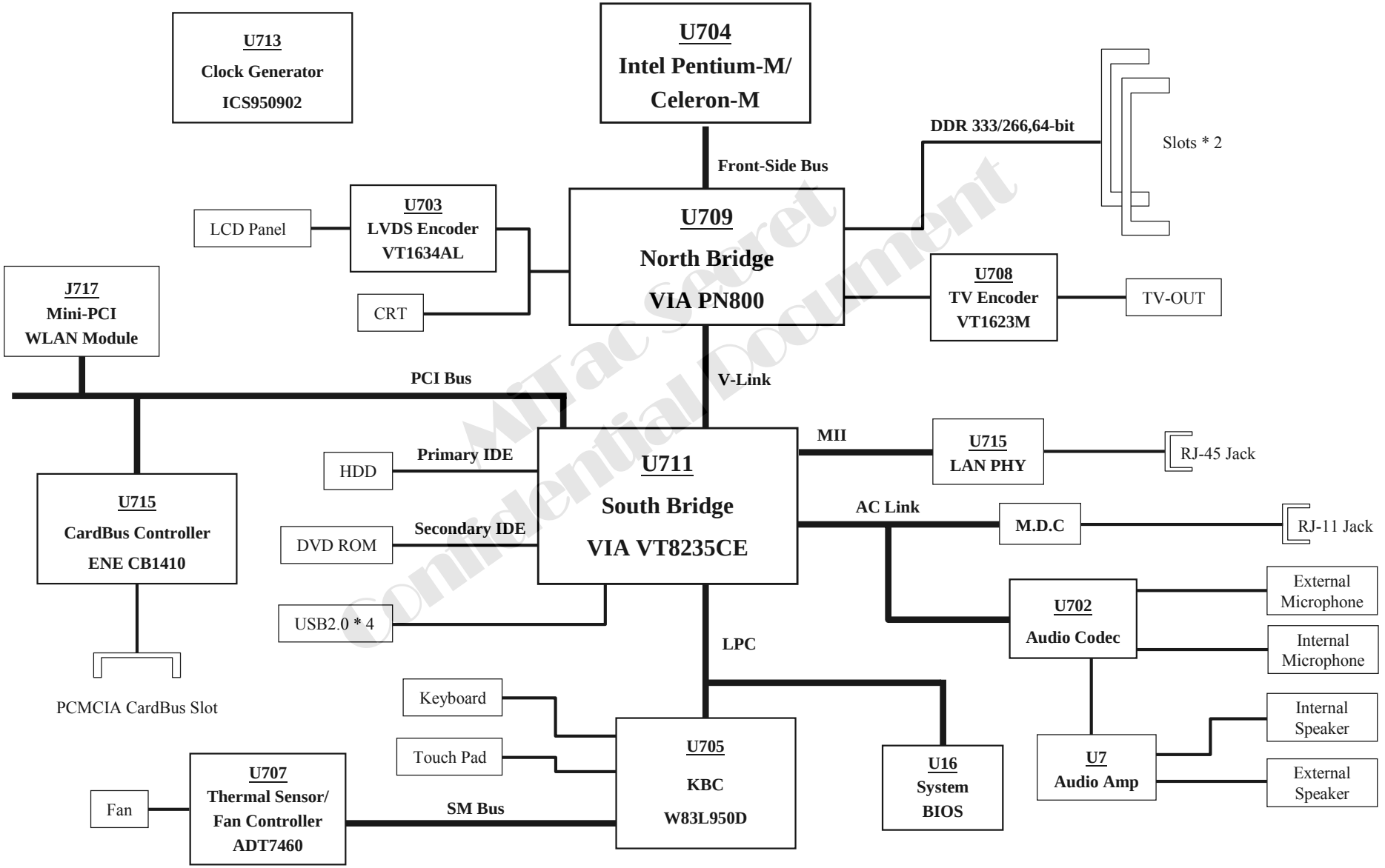
Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)	P	I/O Power. **3.3V ±5%**
VCC	(see pin list)	P	Core Power. **2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.**
GND	(see pin list)	P	**Ground.** Connect to primary motherboard ground plane.

Strap Pins for North Bridge Configuration

Signal Name	Pin #	Function	Description	Note
SDCS3#	AF26	NB Configuration	SDCS3# signal state is reflected on signal pinVD[7] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA2	AE24	NB Configuration	SDA2 signal state is reflected on signal pinVD[6] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA1	AC22	NB Configuration	SDA1 signal state is reflected on signal pinVD[5] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA0	AF24	NB Configuration	SDA0 signal states is reflected on signal pinsVD[4] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD3	AC6	NB Configuration	Strap_VD3 signal state is reflected on signal pinVD[3] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD2	AD5	NB Configuration	Strap_VD2 signal state is reflected on signal pinVD[2] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD1	AE5	NB Configuration	Strap_VD1 signal state is reflected on signal pin, VD[1] during power up for North Bridge configuration.	**Check the North Bridge DS for details**
Strap_VD0	AF5	NB Configuration	Strap_VD0 signal state is reflected on signalpin, VD[0] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**

Note: Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]
Internal Pulldowns are present on all LAN pins

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the Mini PCI debug board.

7.2 Error Codes (1)

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Signals that Reset occurred
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register configure through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter
1Ch	Initialize video
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test DMA controller
25h	Initialize 8237A controller
26h	Initialize INT vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign-on messages displayed

7.2 Error Codes (2)

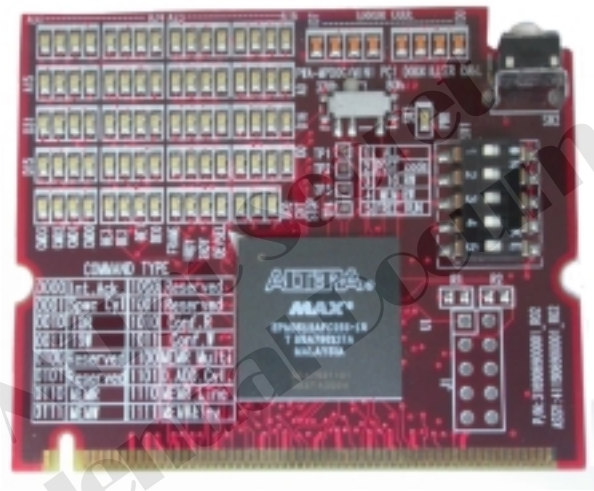
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	OEM initialization of keyboard controller
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update keyboard controller output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search for and initialize the mouse
3Eh	Update NUMLOCK status
3Fh	OEM initialization of COM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's initialization of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 No Display (*2)
- 8.3 LCD No Display or Picture Abnormal
- 8.4 External Monitor No Display or Color Abnormal
- 8.5 TV Test Error
- 8.6 Memory Test Error
- 8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.8 Hard Drive Test Error
- 8.9 CD-ROM Drive Test Error
- 8.10 USB Port Test Error
- 8.11 PC Card Socket Test Error
- 8.12 Mini-PCI Socket Test Error
- 8.13 Audio Test Error
- 8.14 LAN Test Error

8666 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

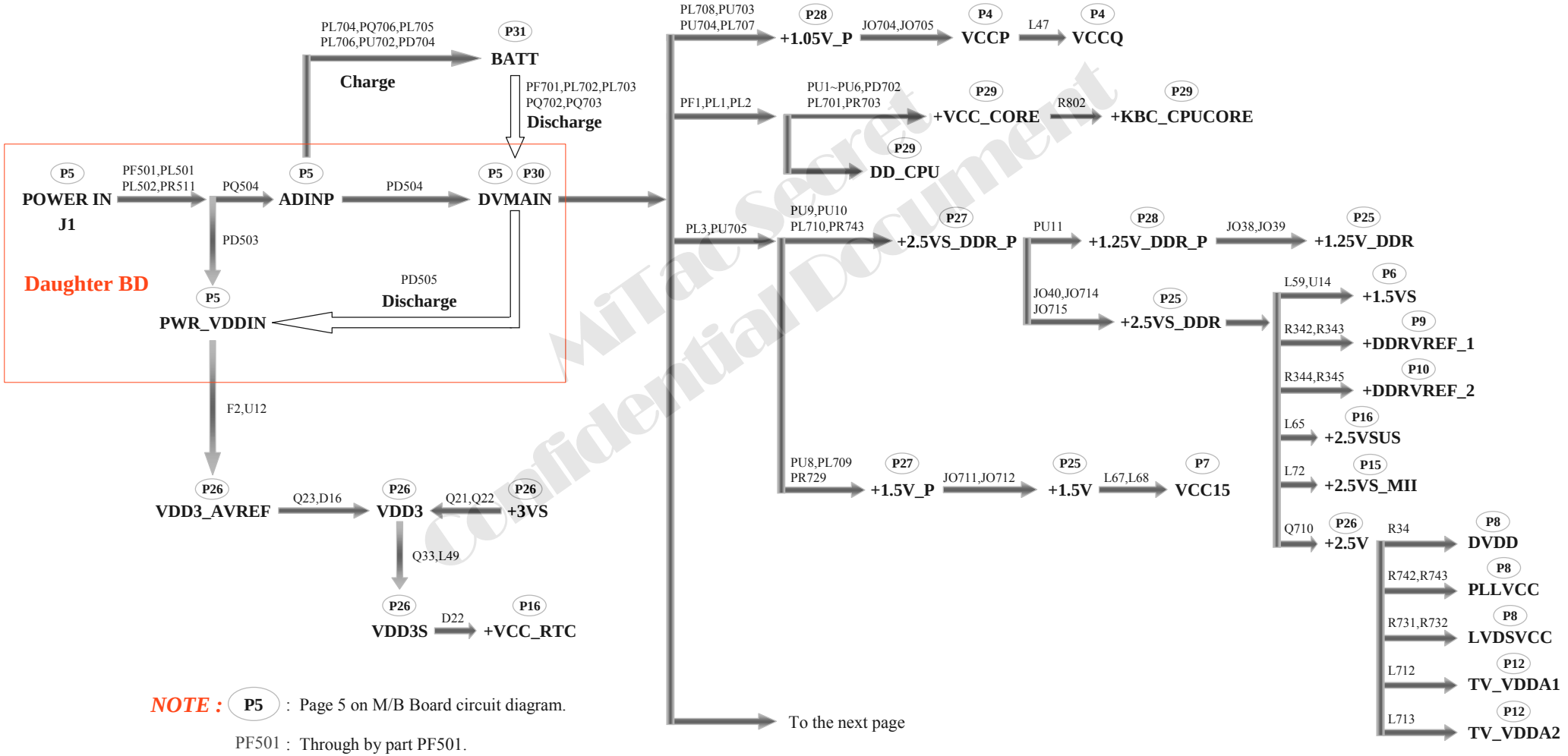
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8.1 No Power (1)

When power button is pressed ,nothing happens ,power indicator does not light up.

Main Voltage Map



NOTE : P5 : Page 5 on M/B Board circuit diagram.

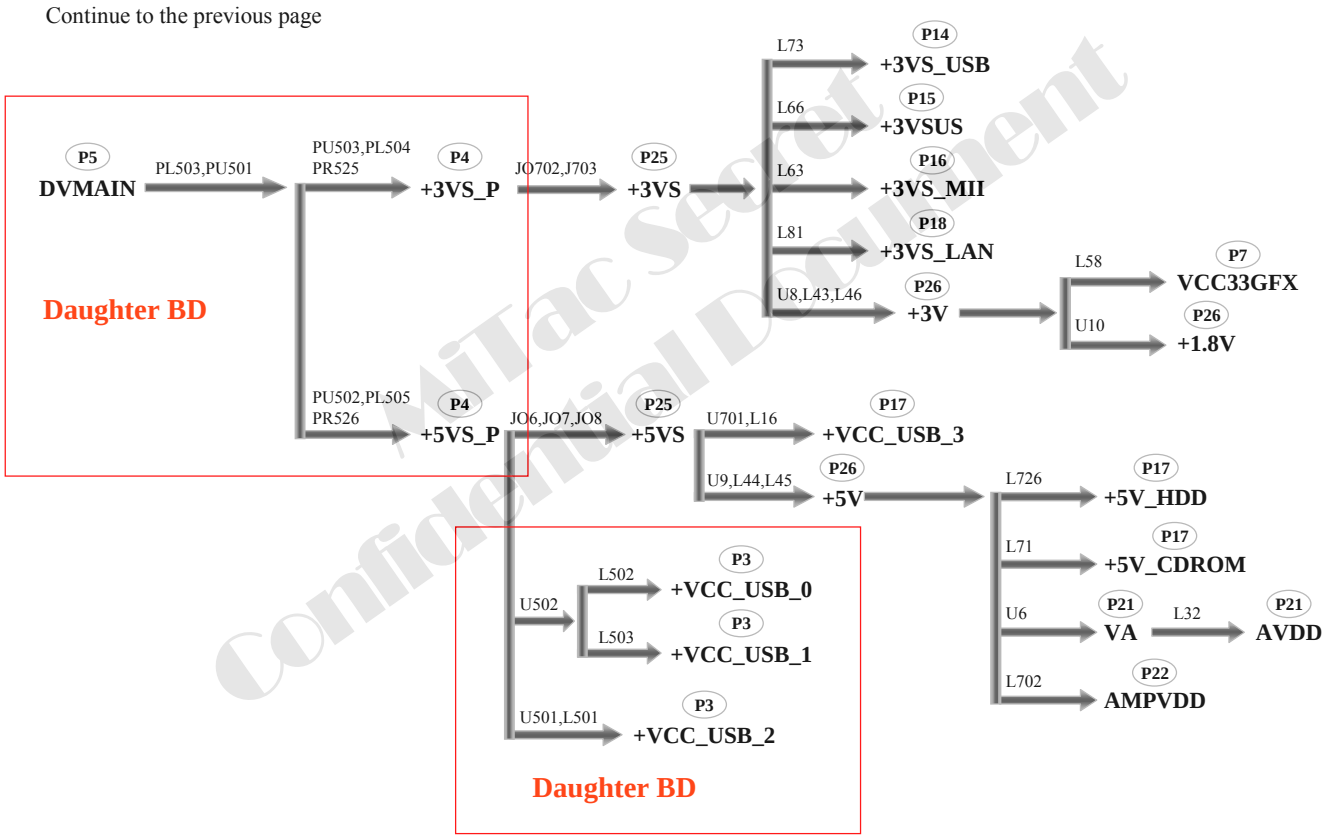
PF501 : Through by part PF501.

8666 N/B Maintenance

8.1 No Power (2)

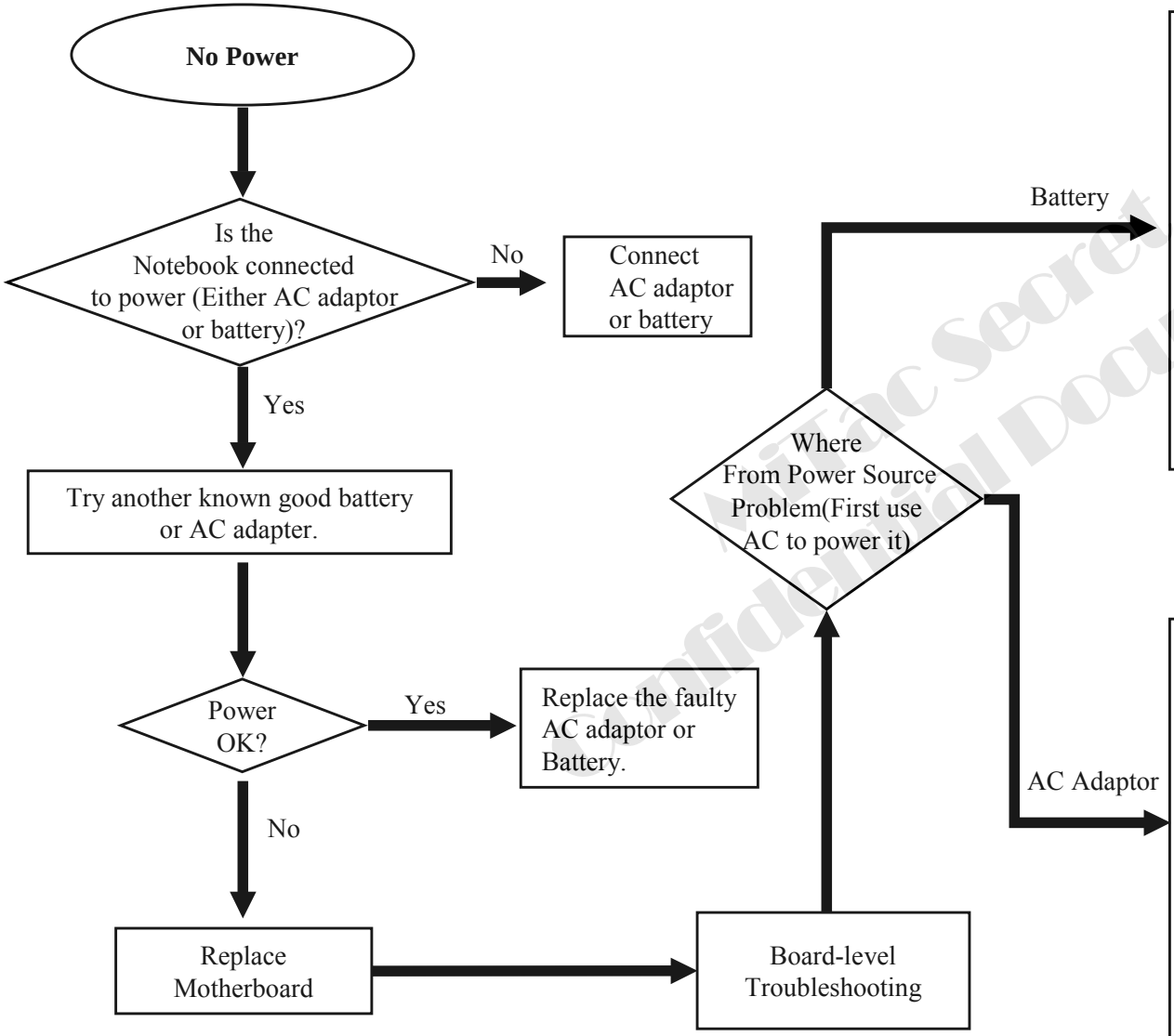
When power button is pressed ,nothing happens ,power indicator does not light up.

Main Voltage Map



8.1 No Power (3)

When power button is pressed ,nothing happens ,power indicator does not light up.



Check the following parts for cold solder or one of the following parts on the **Mother Board** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts			
J705	PQ702	PL704	PQ710
PF701	PQ703	PL705	PQ707
PL702	PQ704	PL706	PQ709
PL703	PU702	PU701	PD704
PQ701	PQ706	PQ705	PD706

Signal	
BATT	ADINP
BAT_T	ADEN#
BAT_V	CHARGING
D/VMAIN	I_CTR

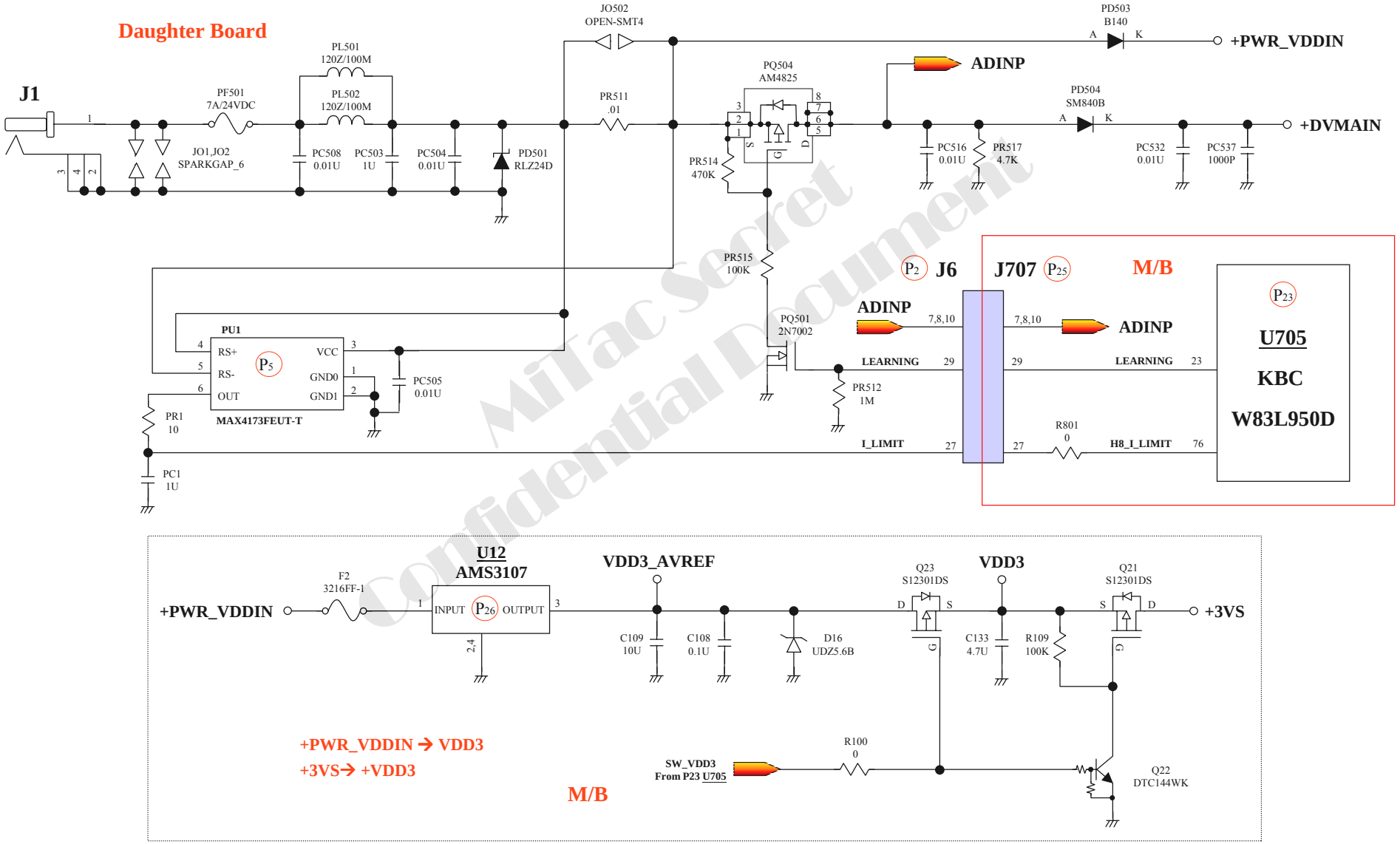
Check the following parts for cold solder or one of the following parts on the **Mother Board** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts			
J1	PR511	PD505	F2
PF501	PR514	PQ501	U12
PL501	PQ504	PU1	Q23
PL502	PD503	PR515	Q21
PD501	PD504	PR512	Q22

Signal	
D/VMAIN	I_LIMIT
PWR_VDDIN	VDD3
LEARNING	+3VS
VDD3_AVREF	

8.1 No Power (4)

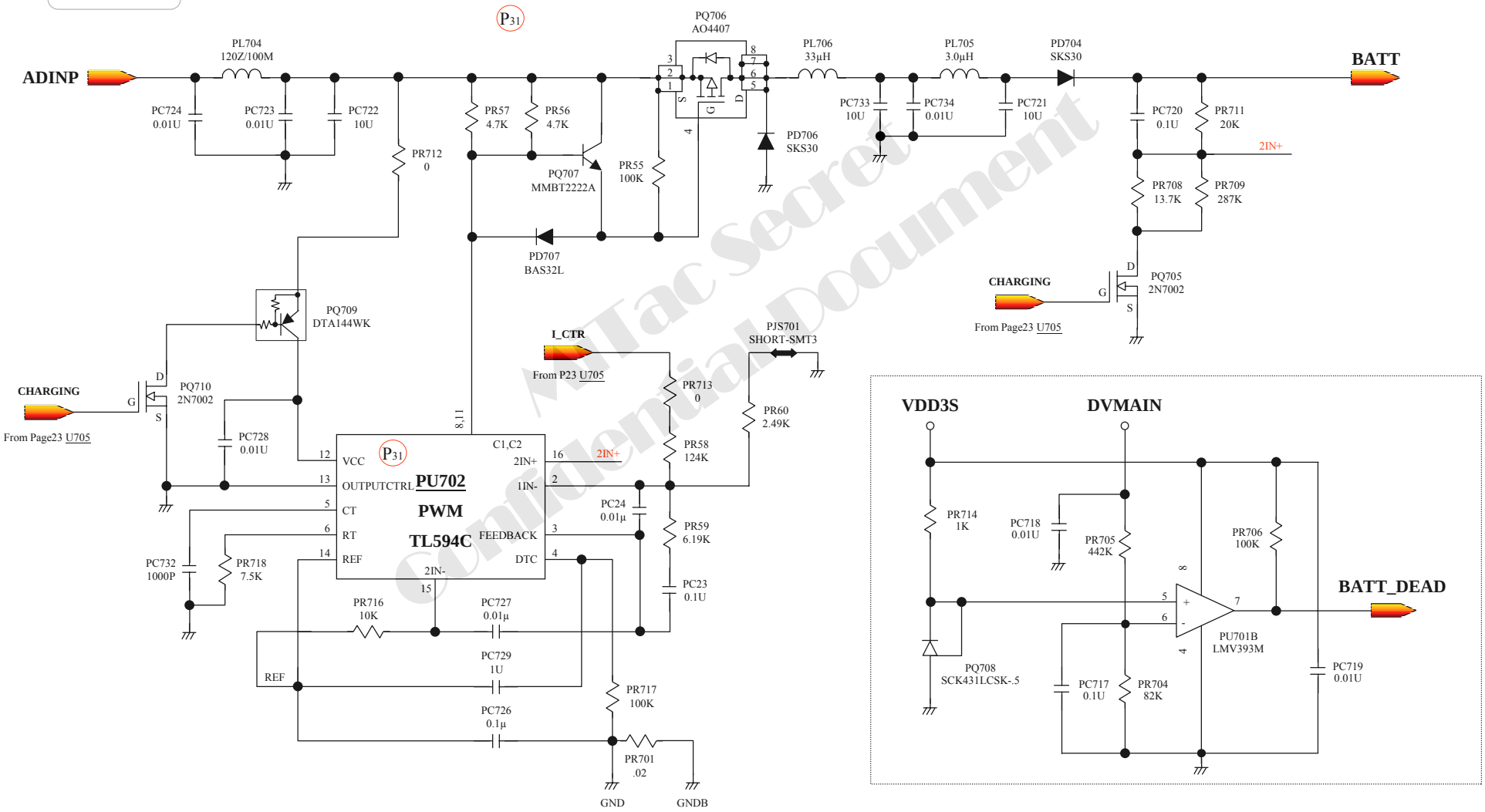
When power button is pressed ,nothing happens ,power indicator does not light up.



8.1 No Power (5)

When power button is pressed ,nothing happens ,power indicator does not light up.

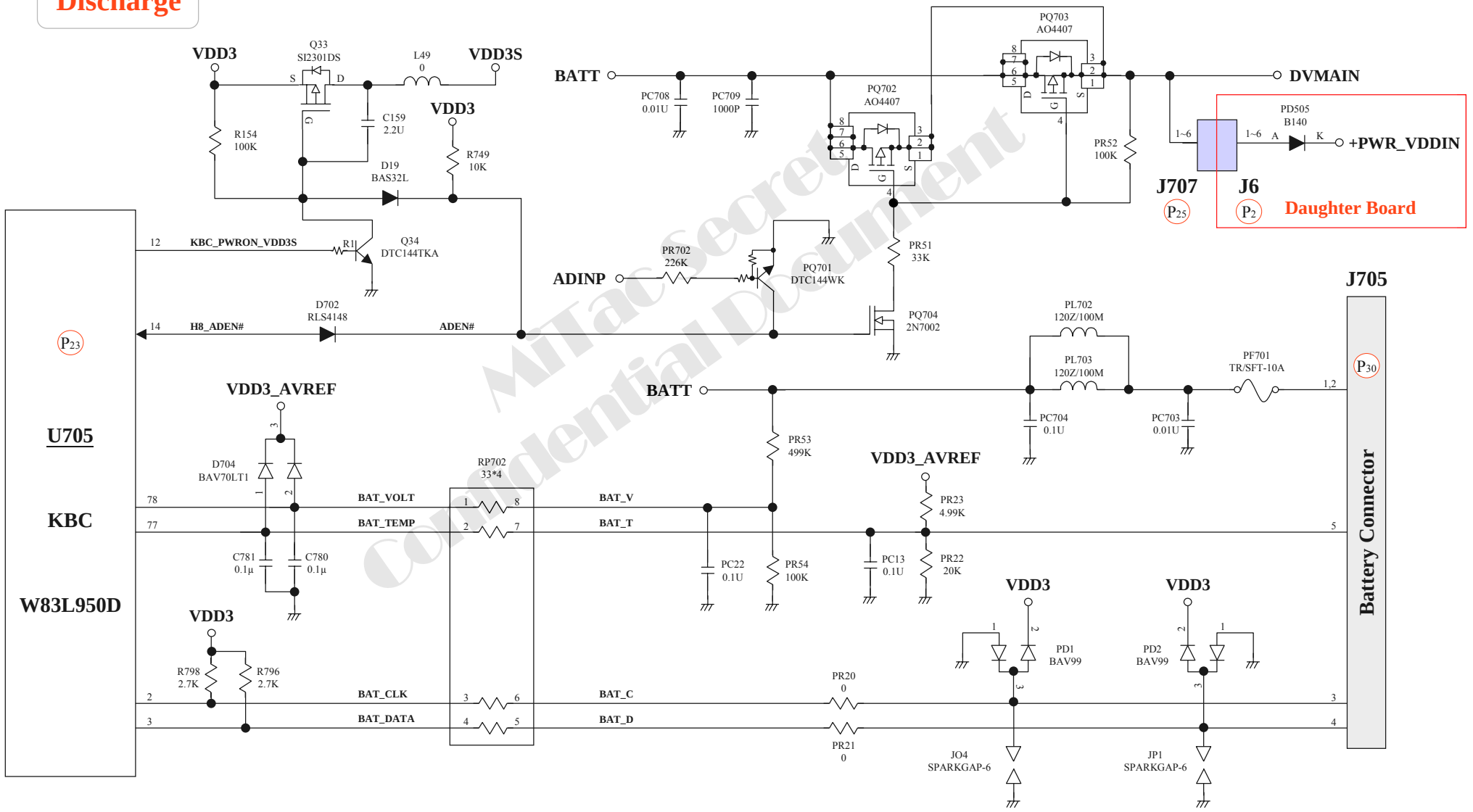
Charge



8.1 No Power (6)

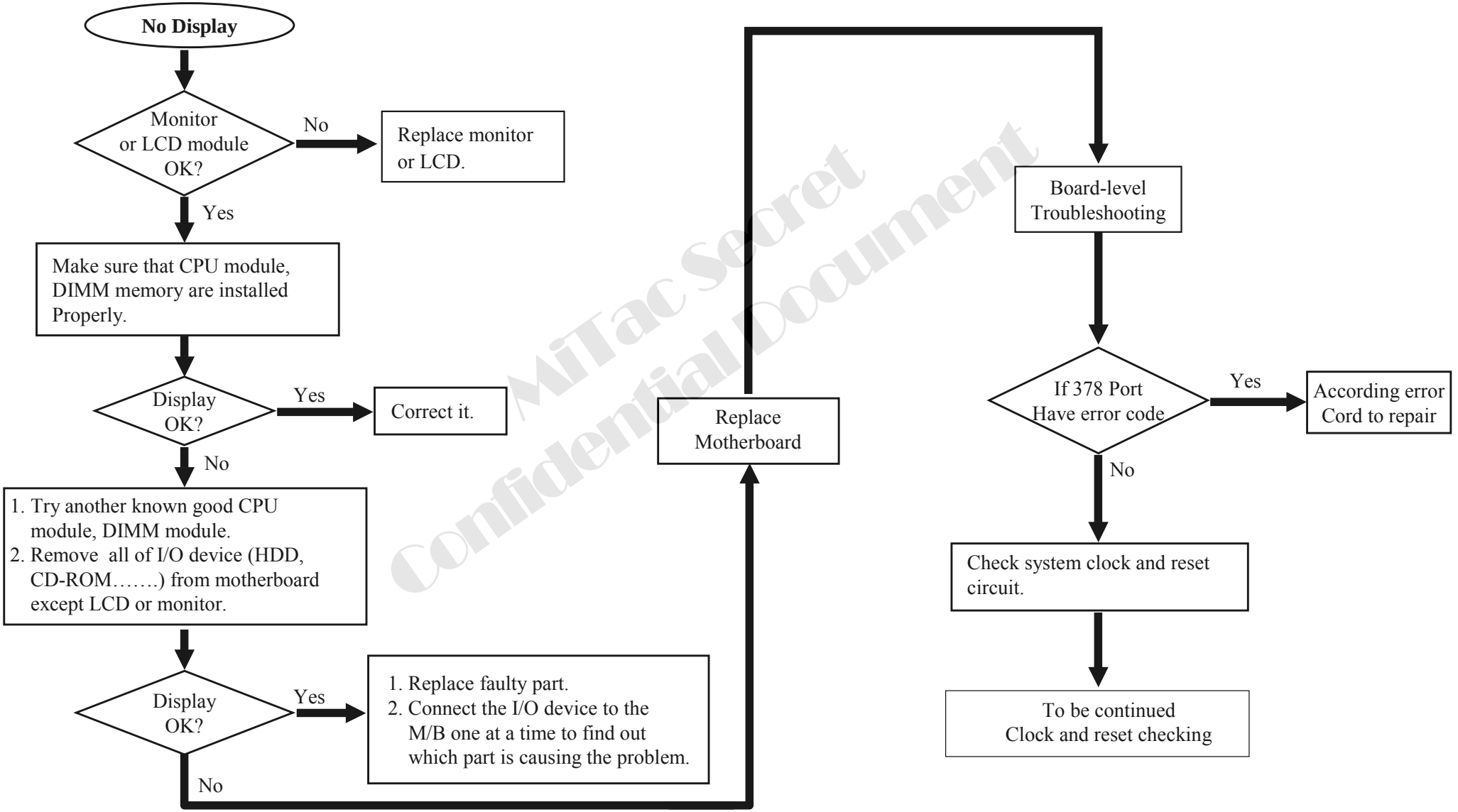
When power button is pressed ,nothing happens ,power indicator does not light up.

Discharge



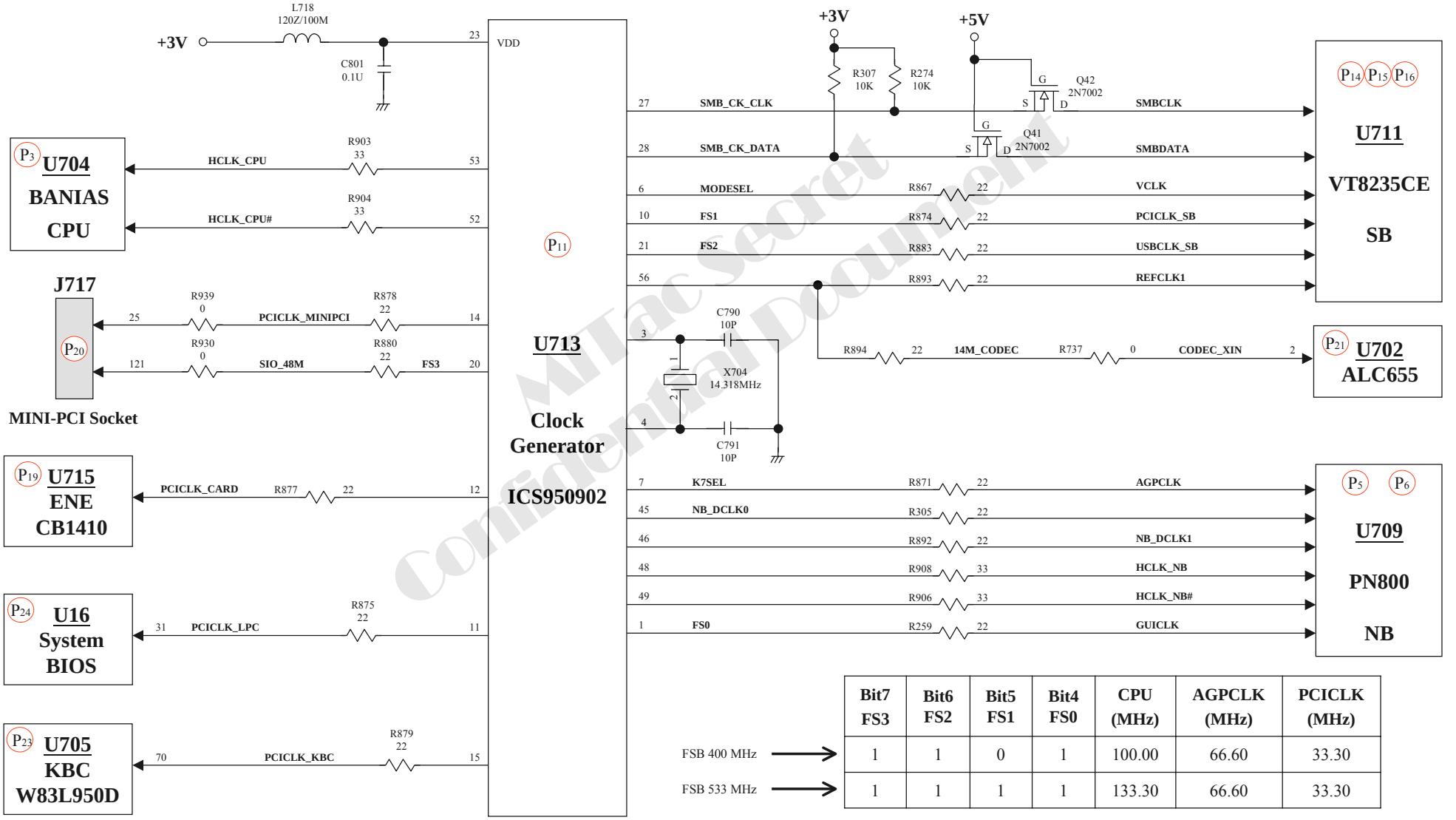
8.2 No Display (1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



8.2 No Display (2)

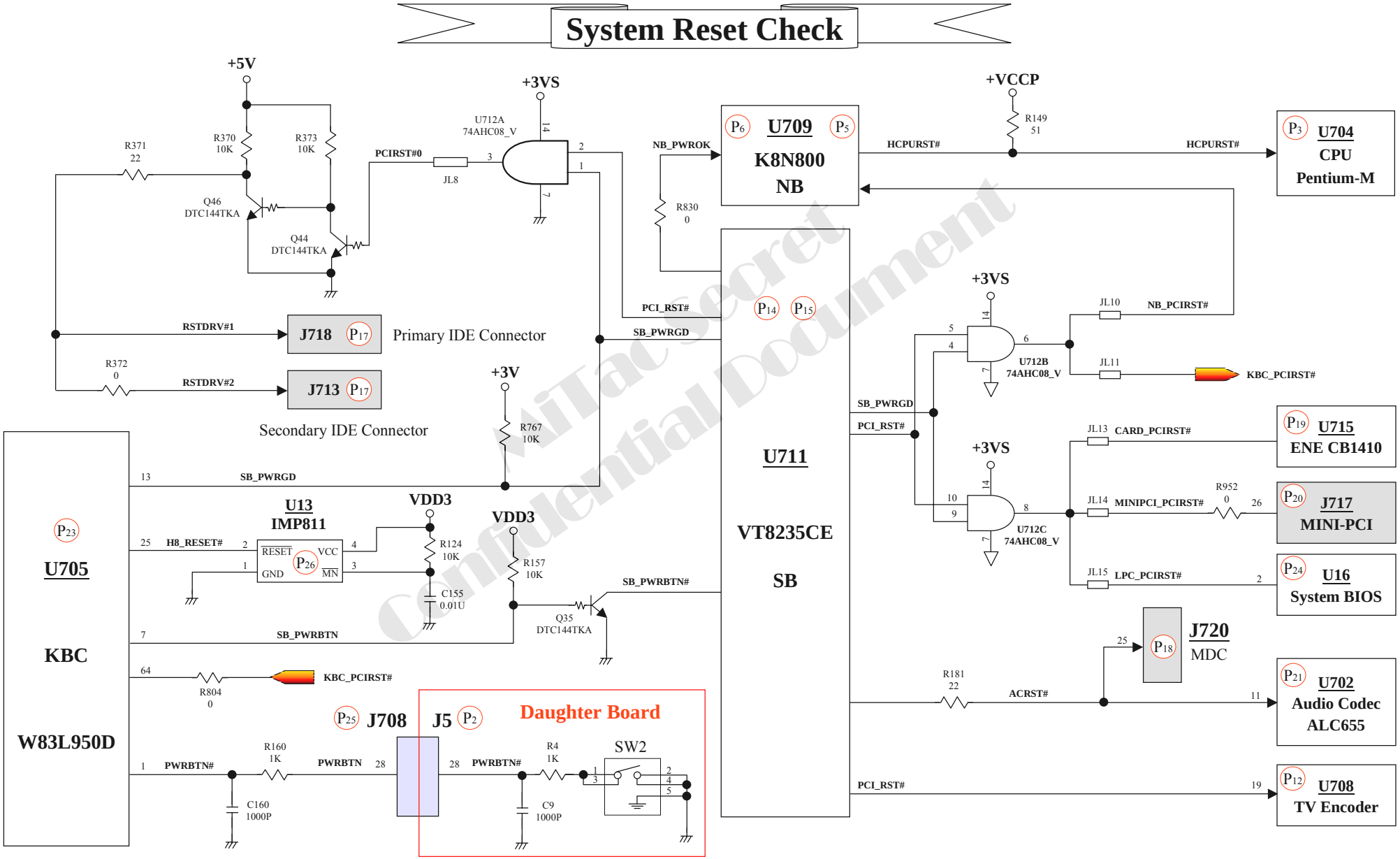
System Clock Check



	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU (MHz)	AGPCLK (MHz)	PCICLK (MHz)
FSB 400 MHz →	1	1	0	1	100.00	66.60	33.30
FSB 533 MHz →	1	1	1	1	133.30	66.60	33.30

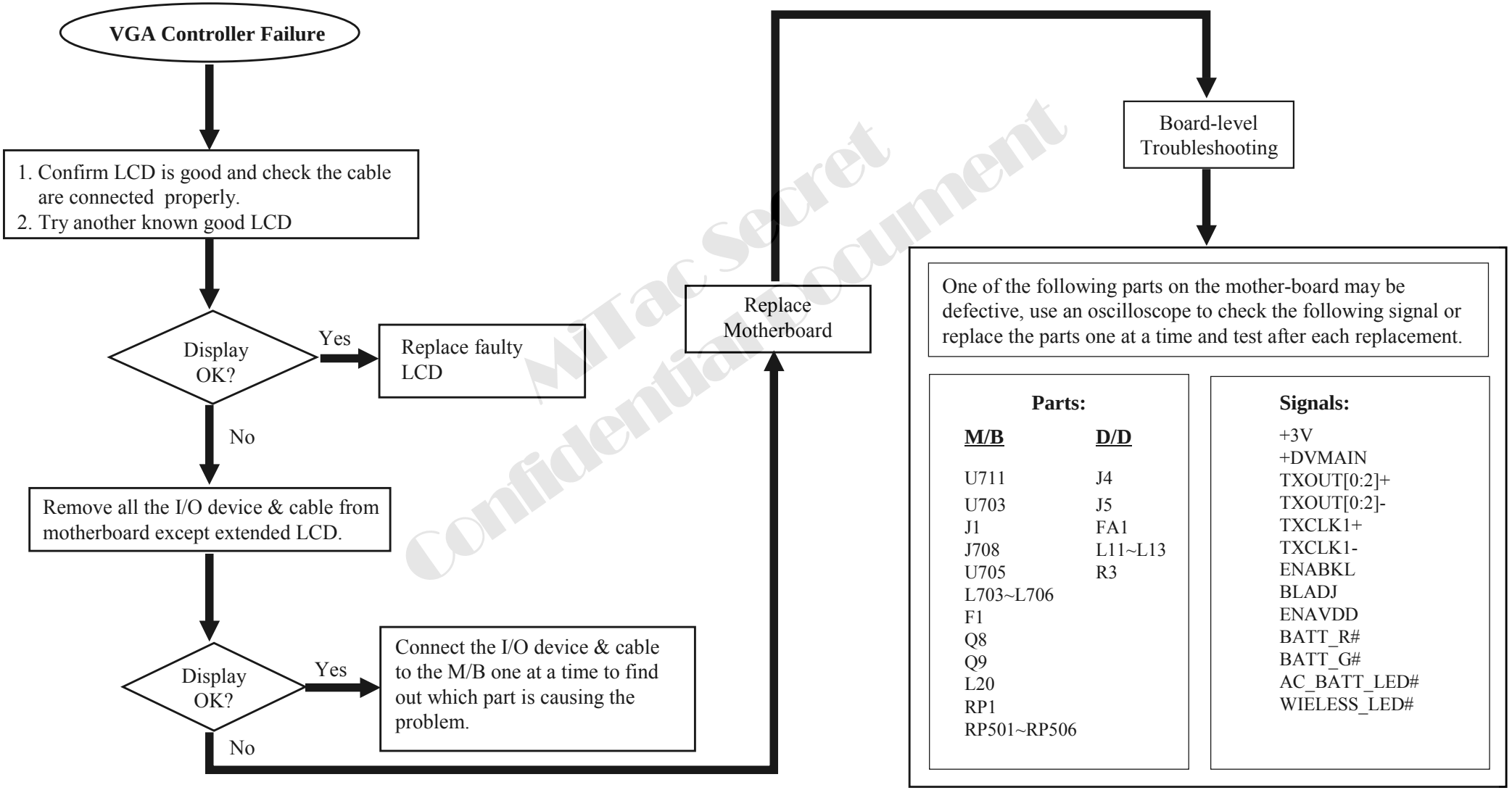
8666 N/B Maintenance

8.2 No Display (3)



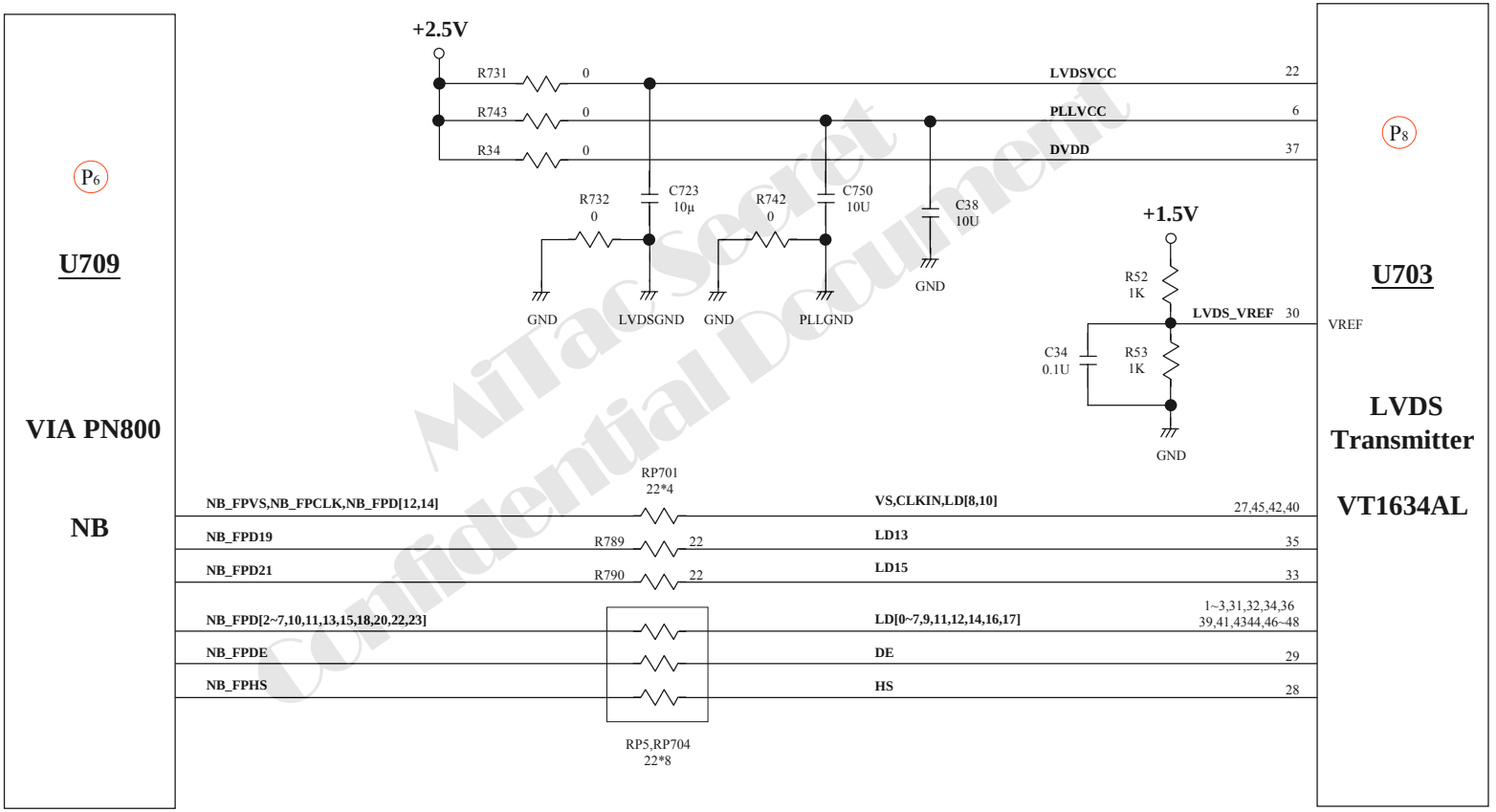
8.3 LCD No Display or Picture Abnormal (1)

There is no display or picture abnormal on LCD or monitor.



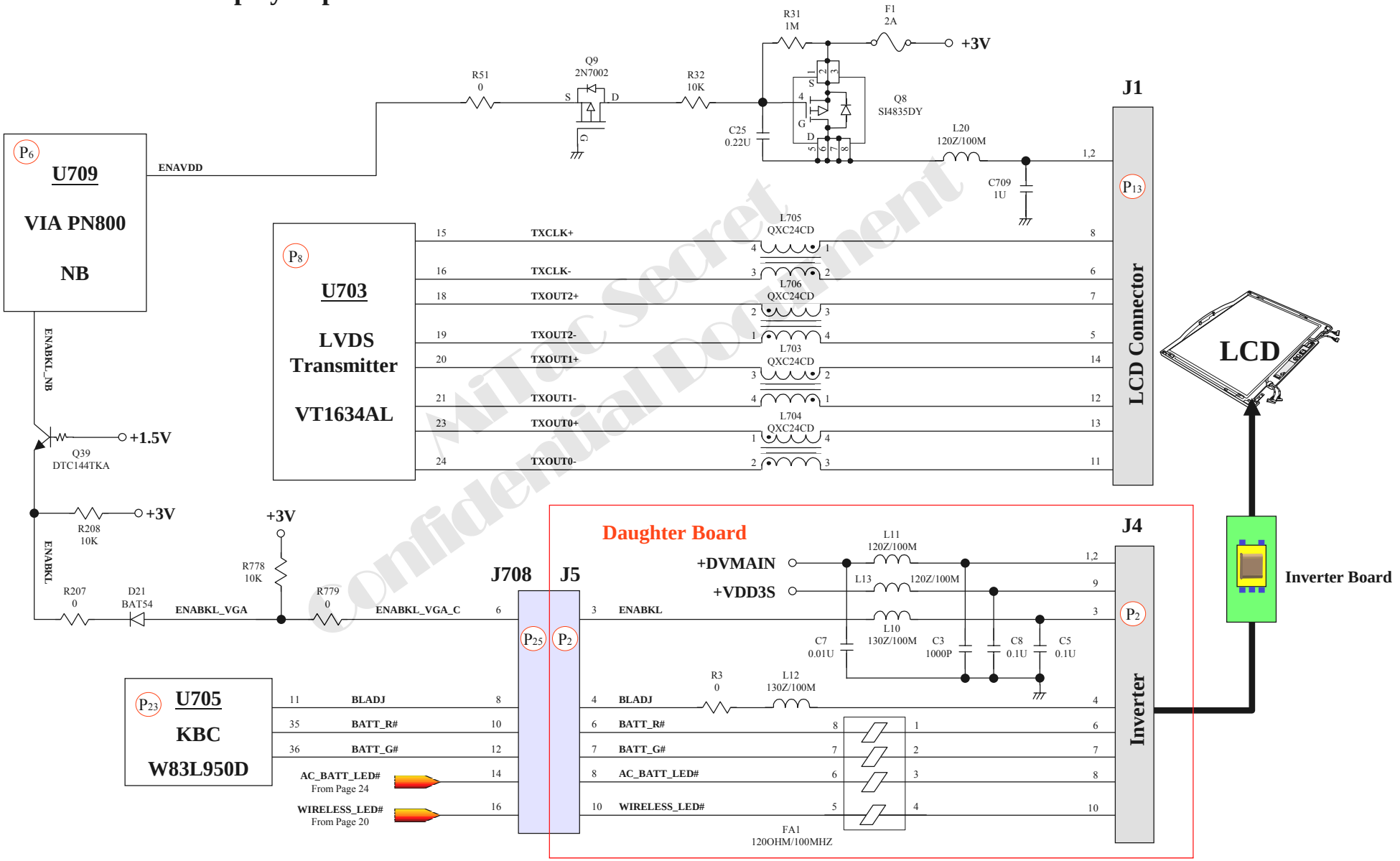
8.3 LCD No Display or Picture Abnormal (2)

There is no display or picture abnormal on LCD or monitor.



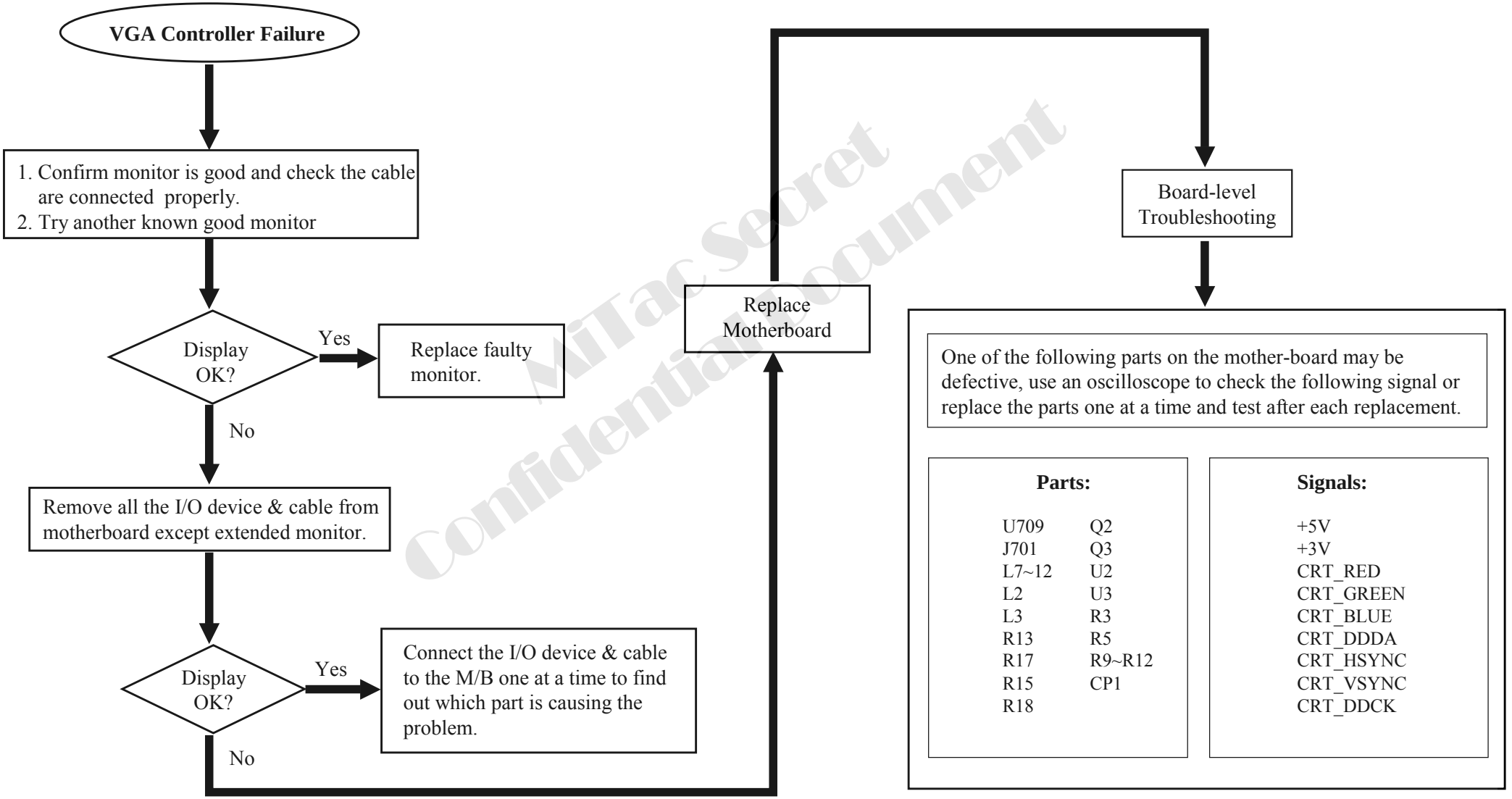
8.3 LCD No Display or Picture Abnormal (3)

There is no display or picture abnormal on LCD or monitor.



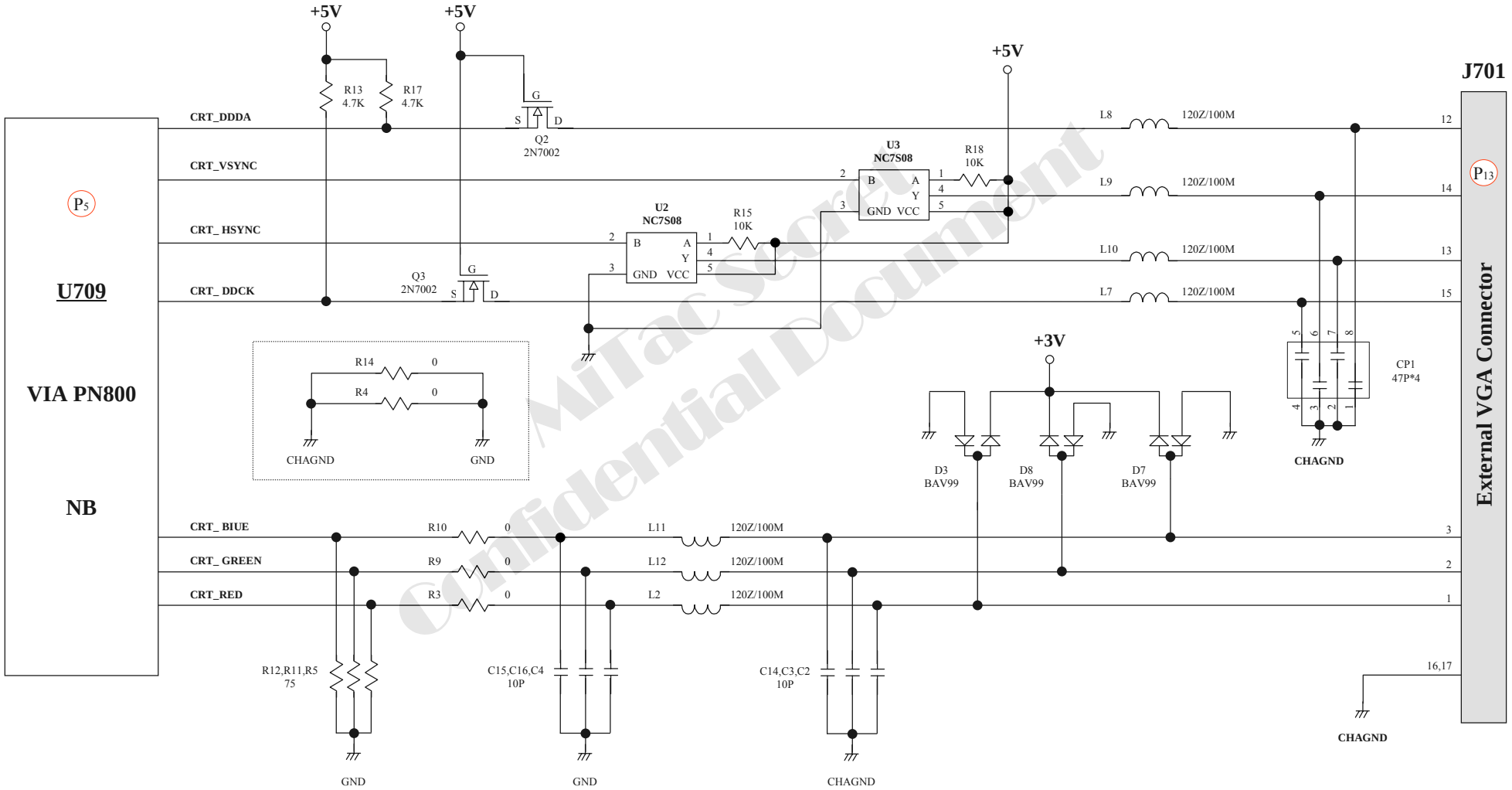
8.4 External Monitor No Display or Color Abnormal (1)

There is no display or picture abnormal on monitor.



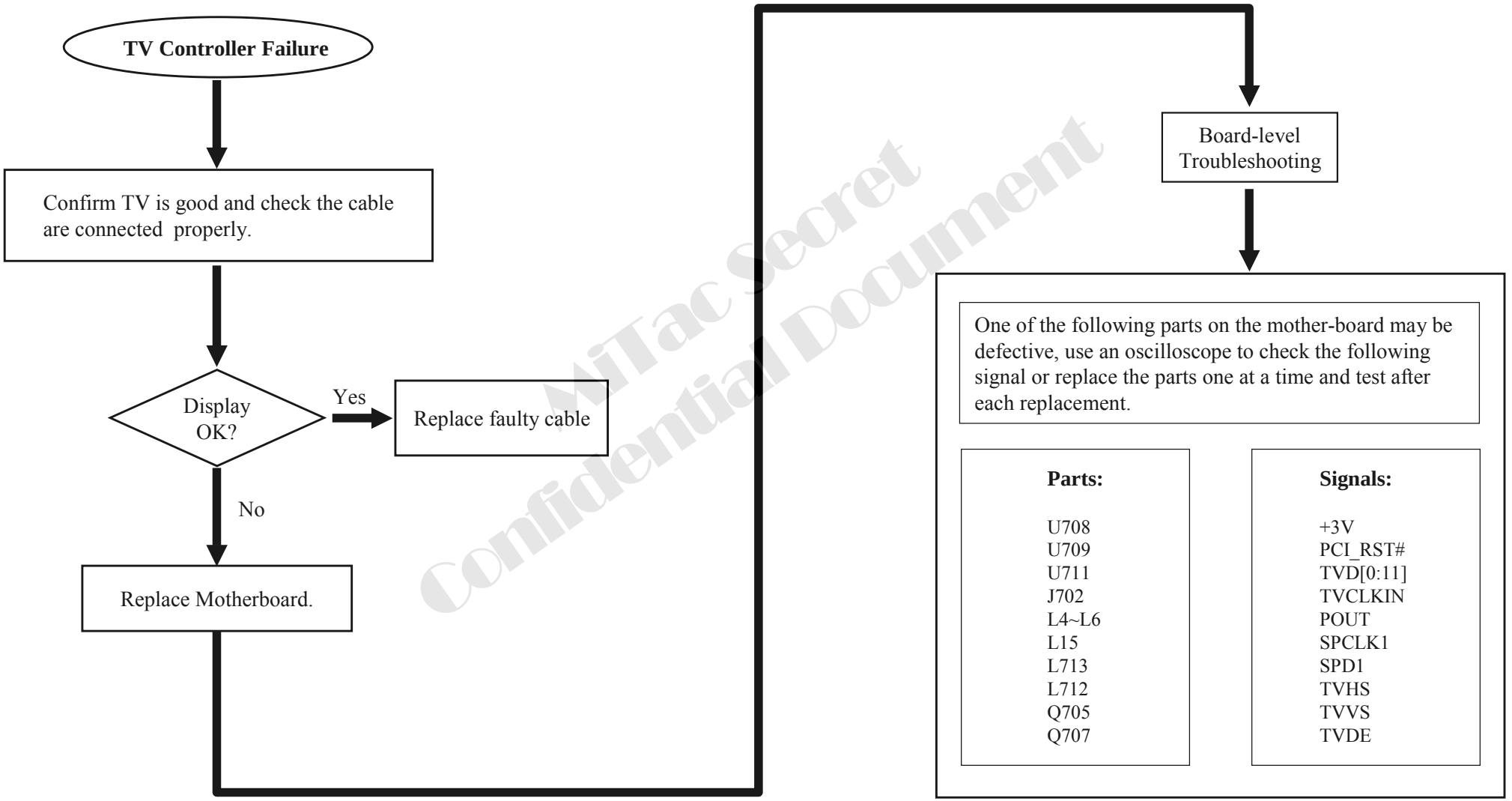
8.4 External Monitor No Display or Color Abnormal (2)

There is no display or picture abnormal on monitor.



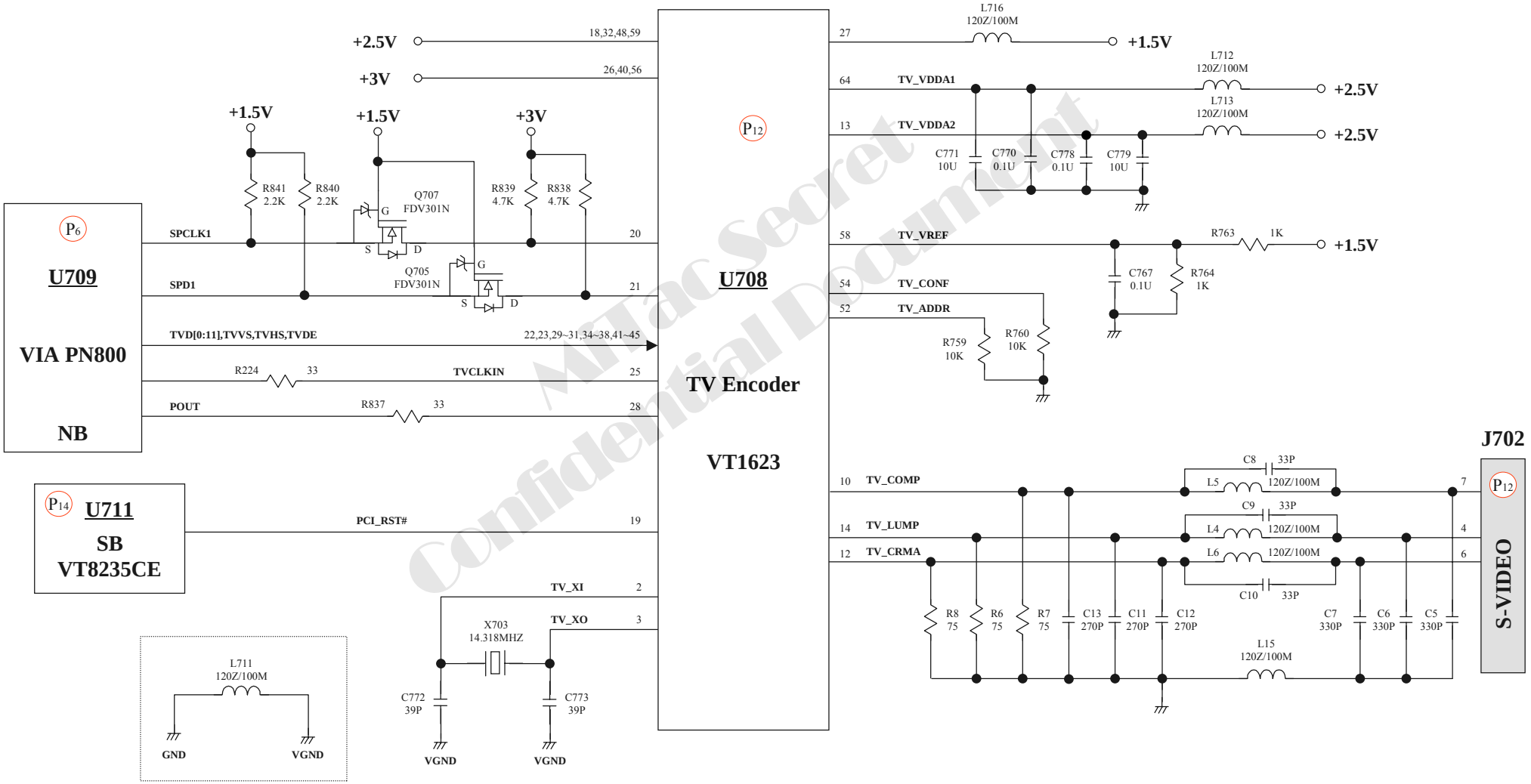
8.5 TV Test Error (1)

There is no display or picture abnormal on TV.



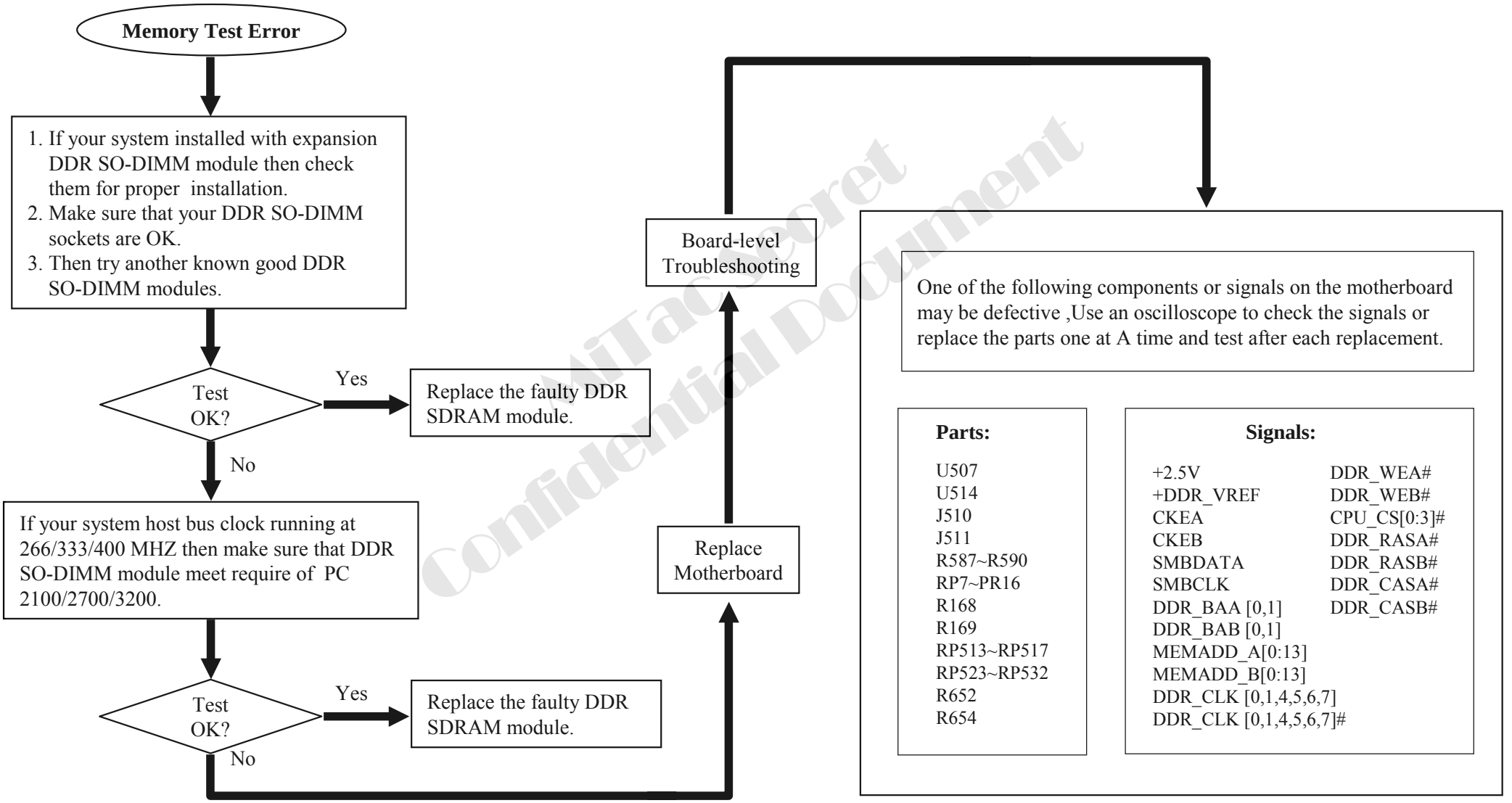
8.5 TV Test Error (2)

There is no display or picture abnormal on TV.



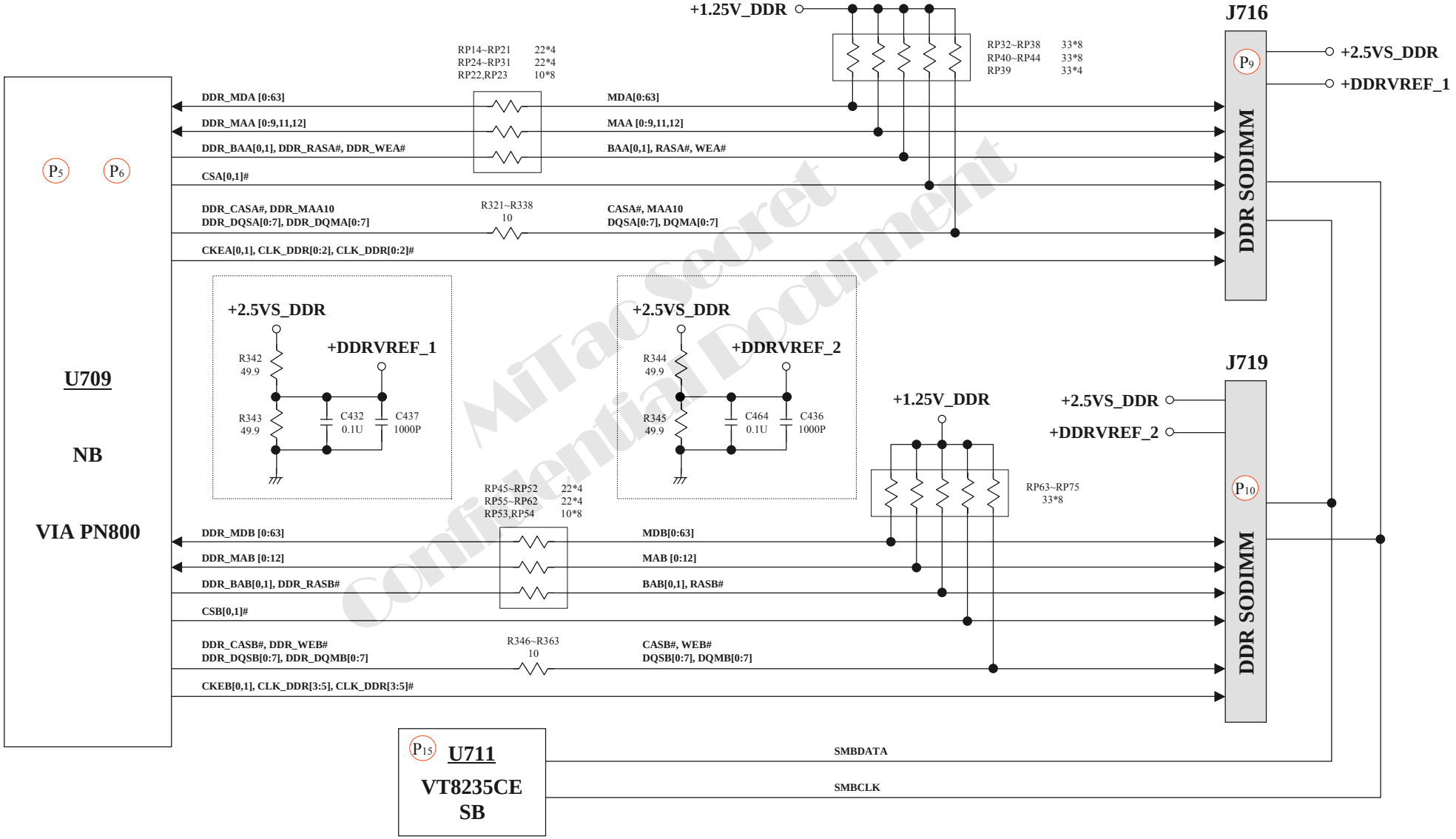
8.6 Memory Test Error (1)

Extend DDRAM is failure or system hangs up.



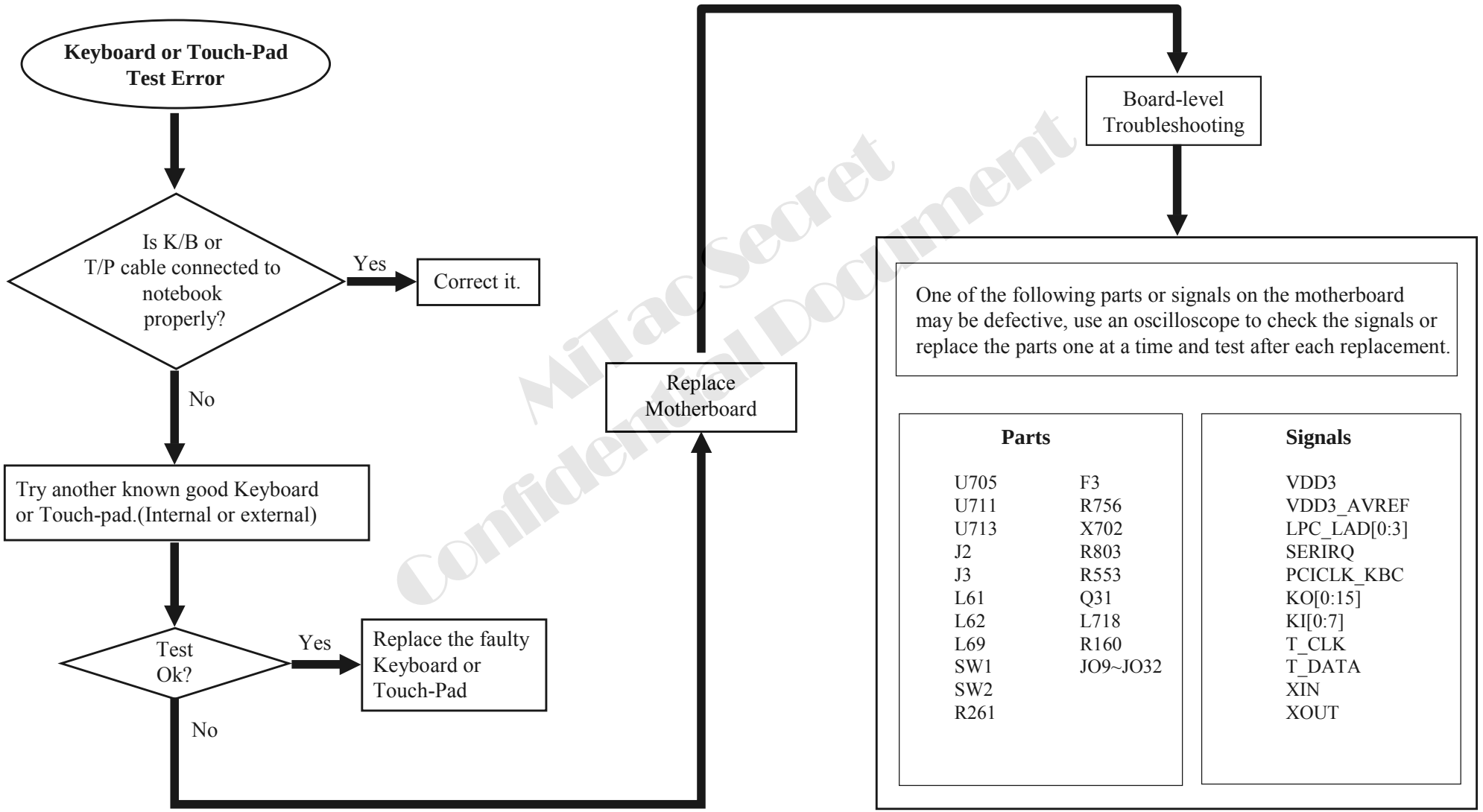
8.6 Memory Test Error (2)

Extend DDRAM is failure or system hangs up.



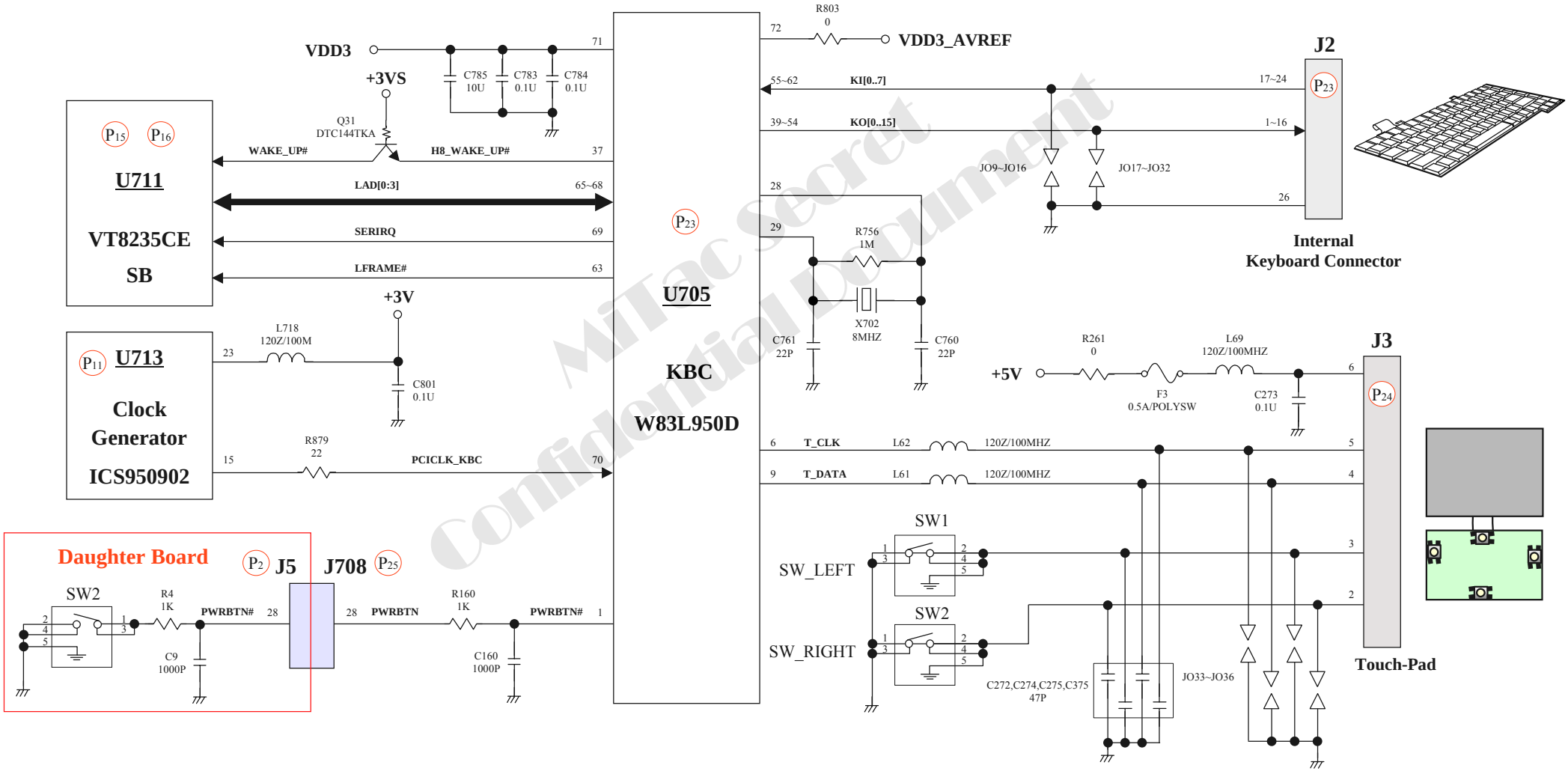
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

Error message of keyboard or touch-pad failure is shown or any key does not work.



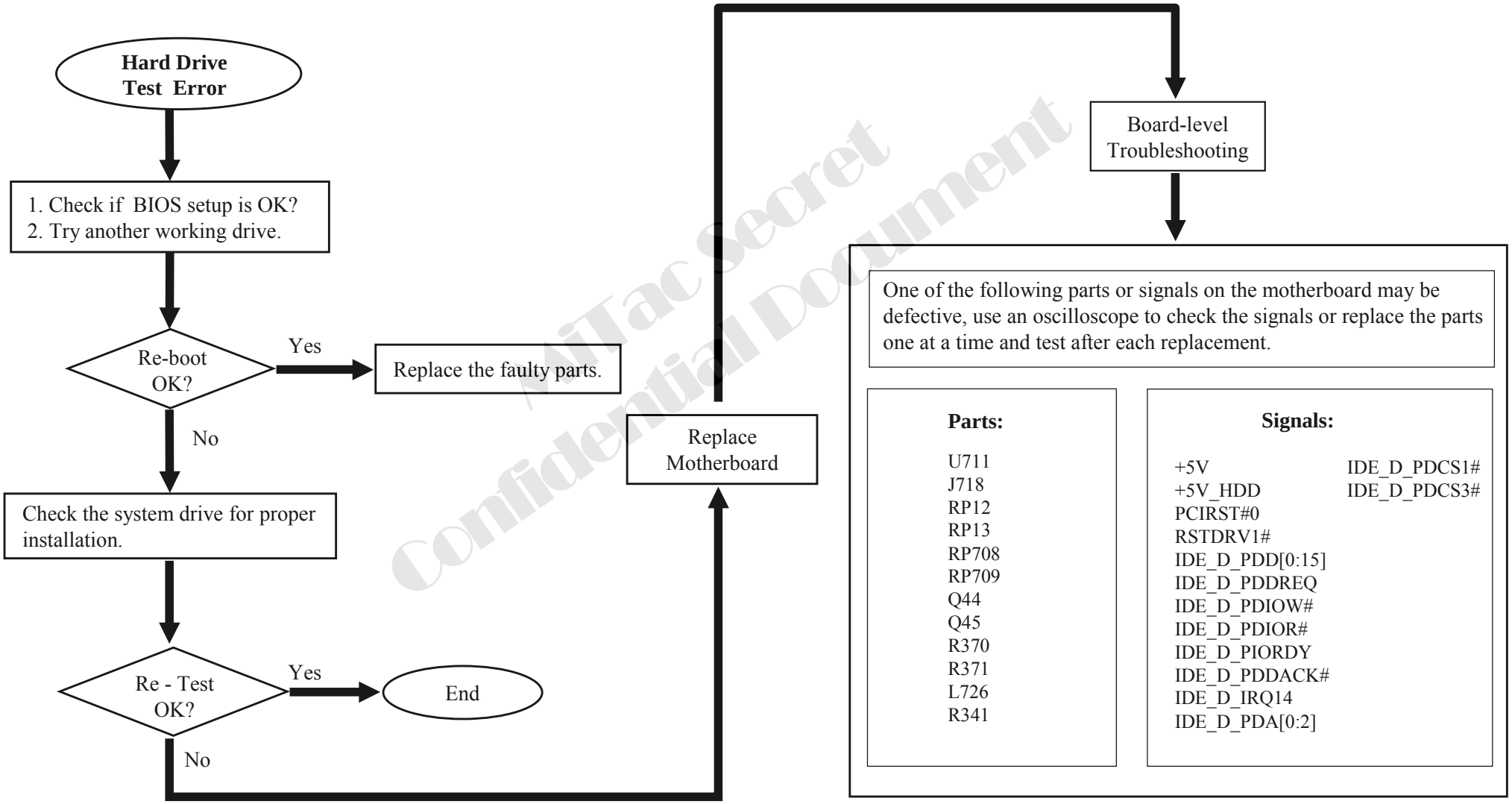
8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

Error message of keyboard or touch-pad failure is shown or any key does not work.



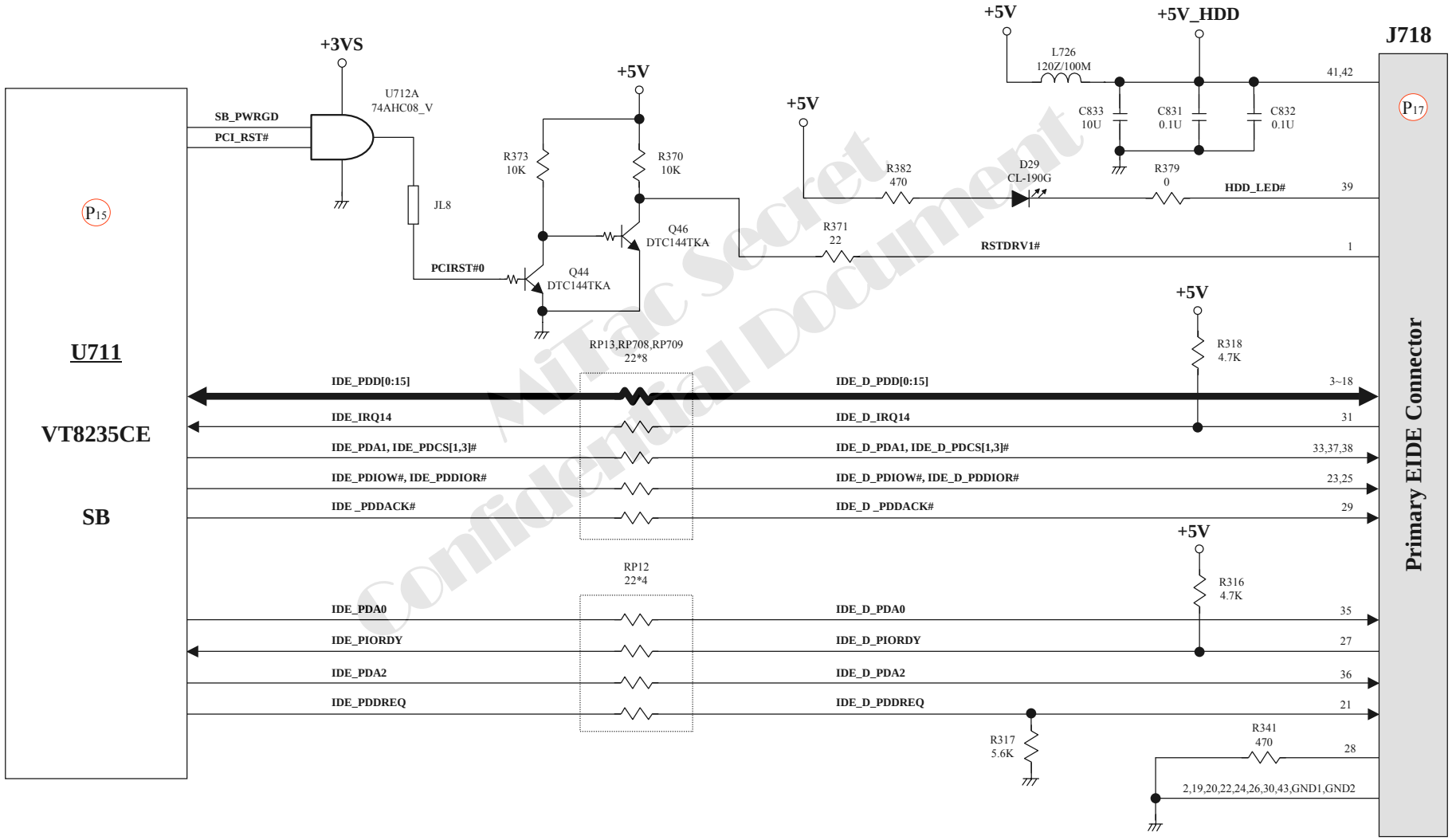
8.8 Hard Drive Test Error (1)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



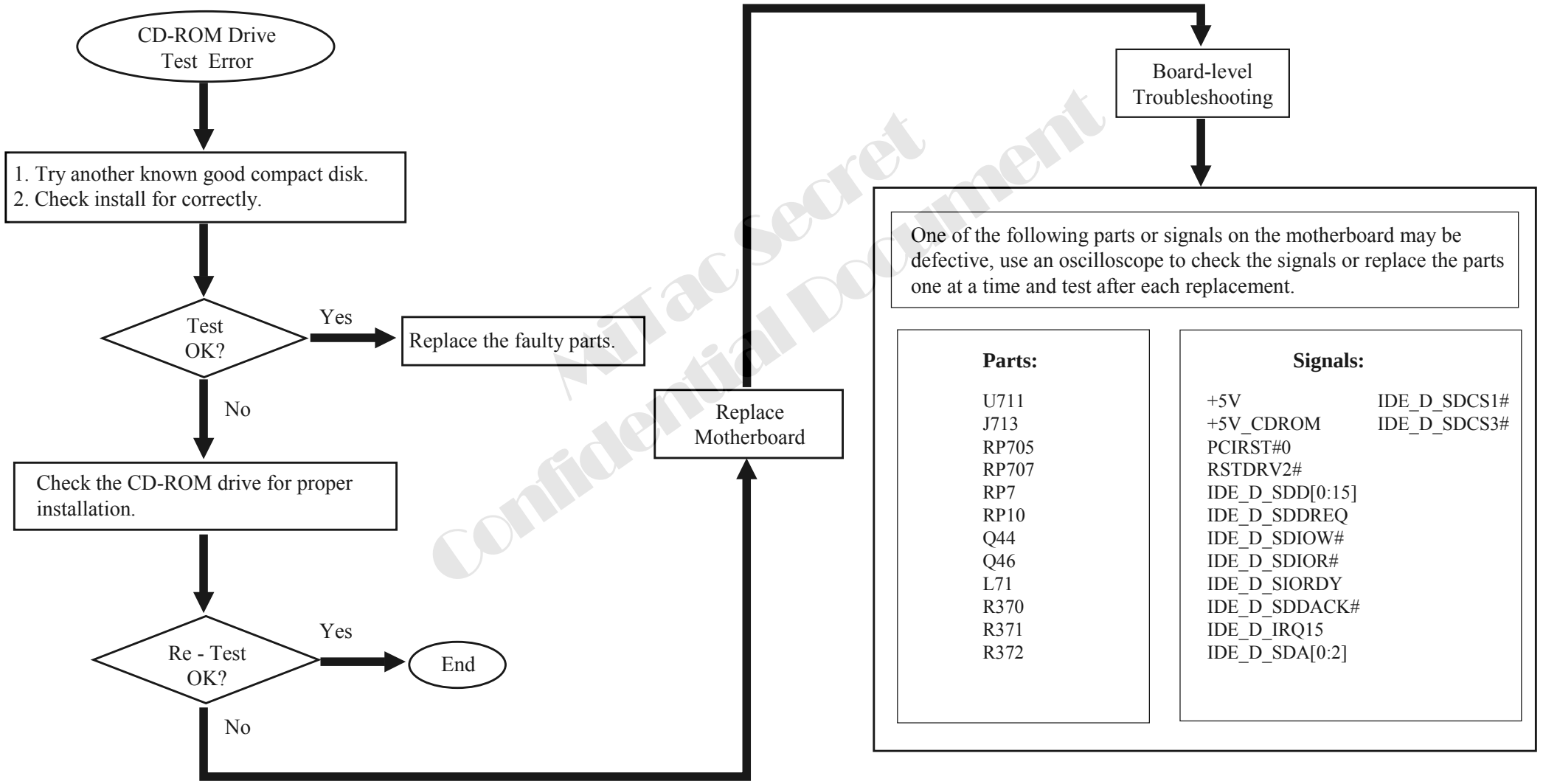
8.8 Hard Drive Test Error (2)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.



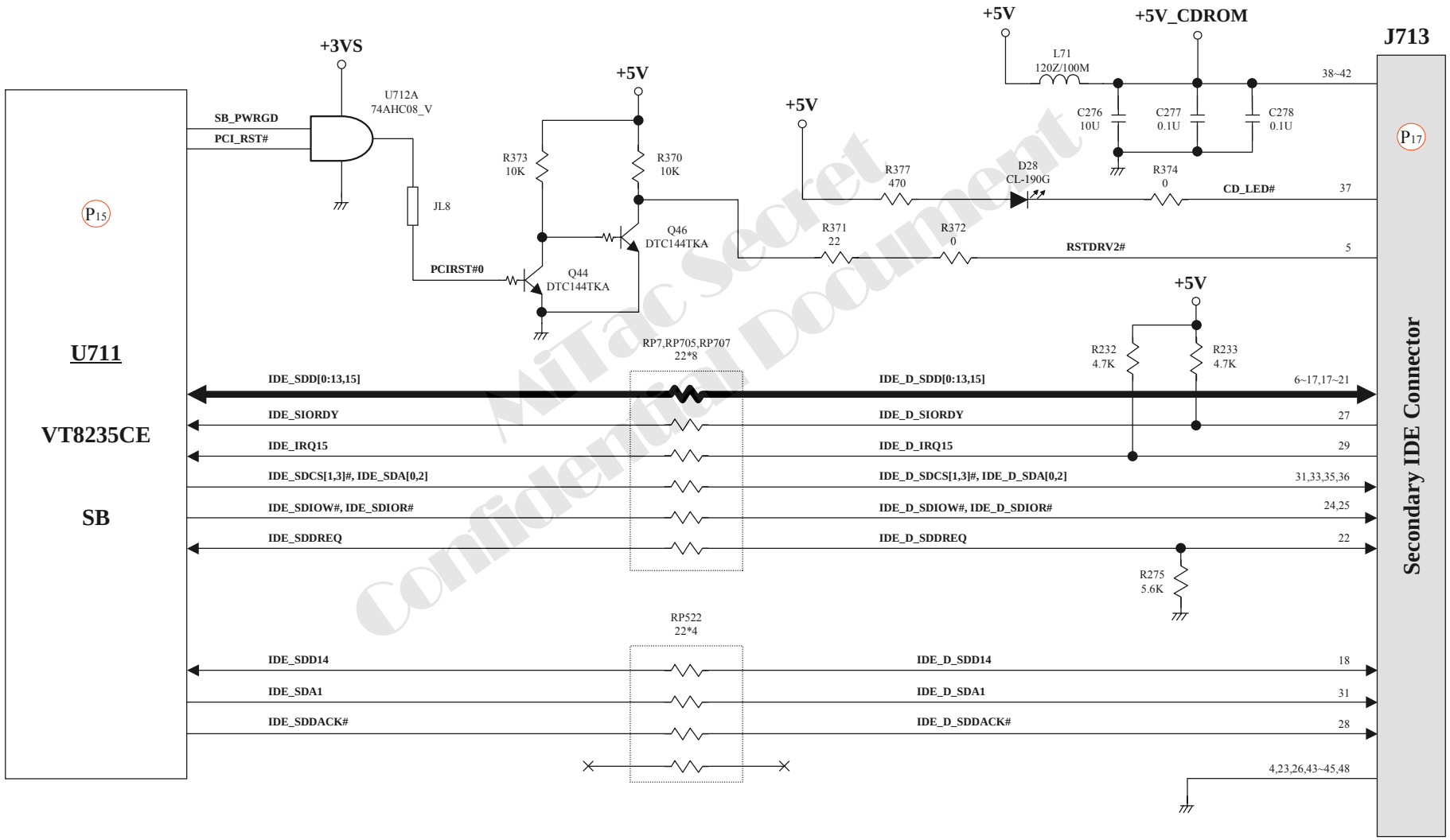
8.9 CD-ROM Drive Test Error (1)

An error message is shown when reading data from CD-ROM drive.



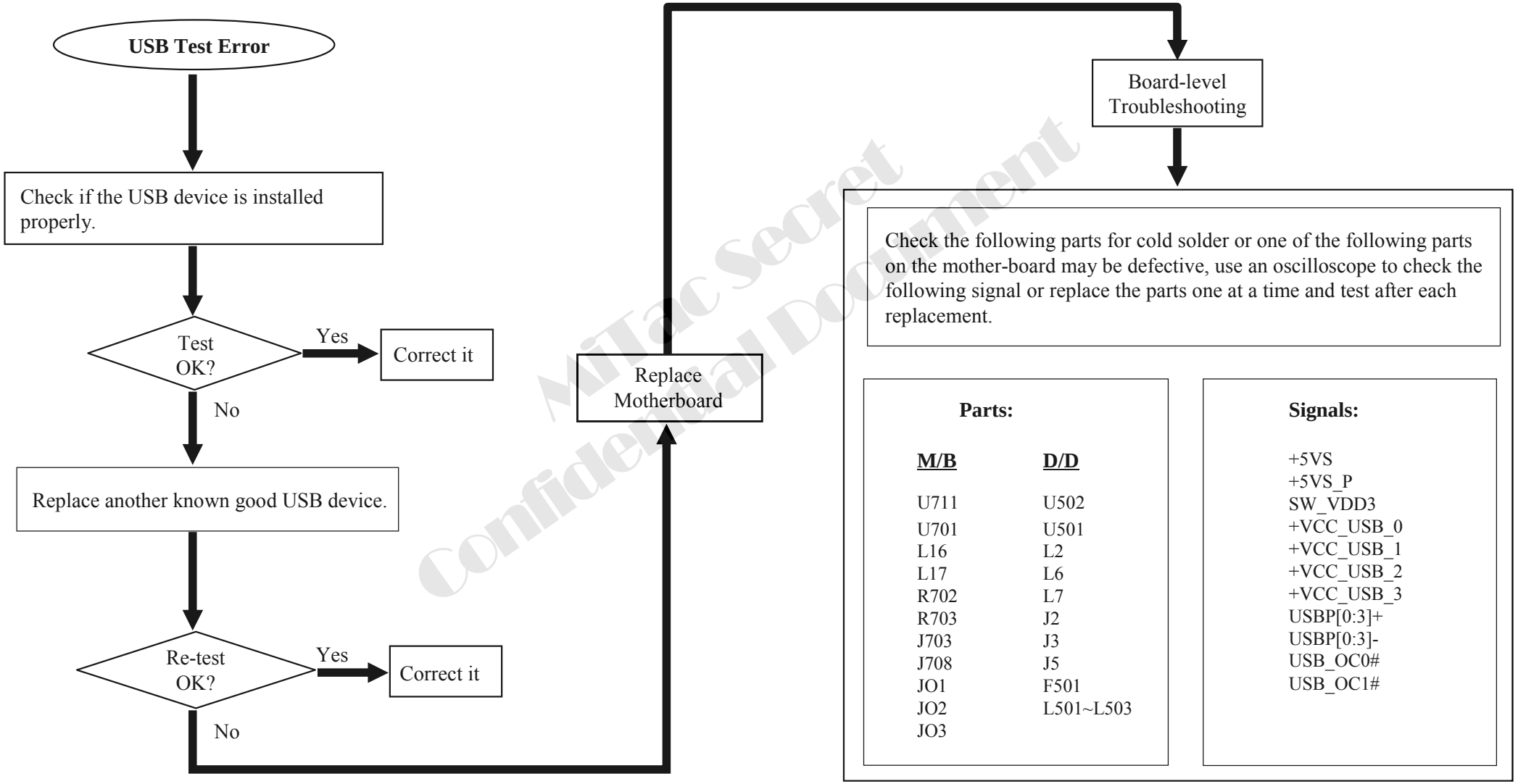
8.9 CD-ROM Drive Test Error (2)

An error message is shown when reading data from CD-ROM drive.



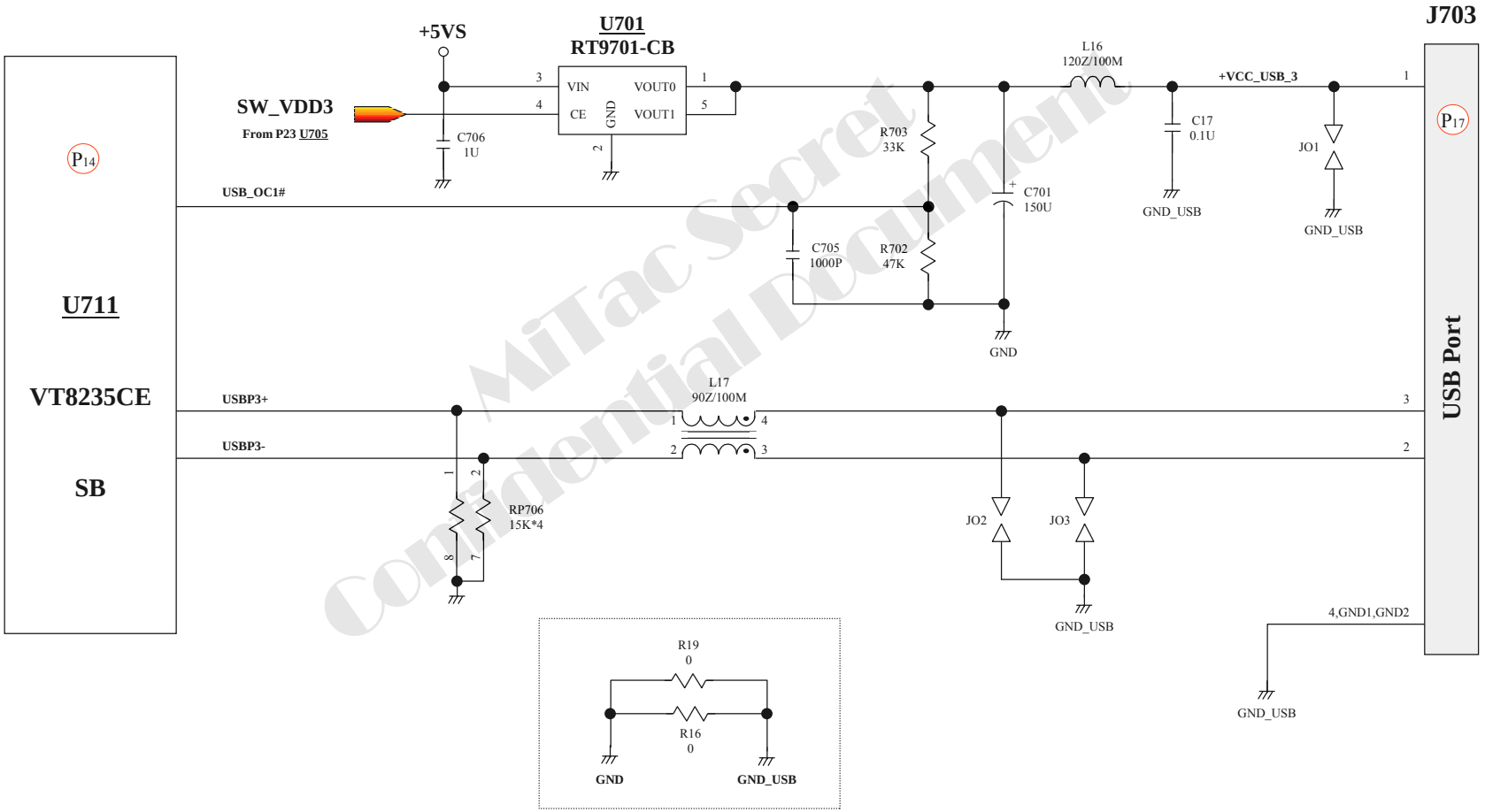
8.10 USB Port Test Error (1)

An error occurs when a USB I/O device is installed.



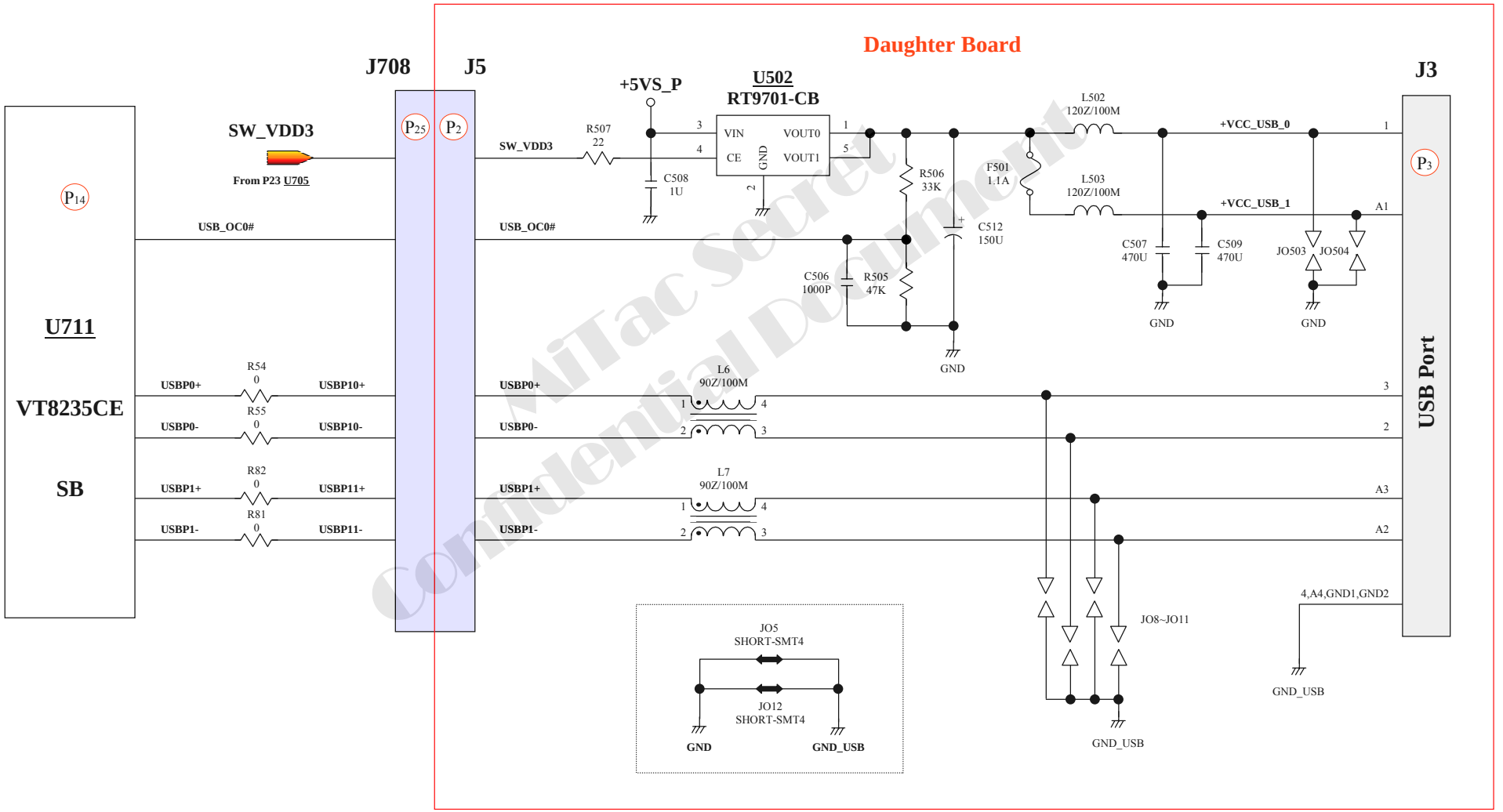
8.10 USB Port Test Error (2)

An error occurs when a USB I/O device is installed.



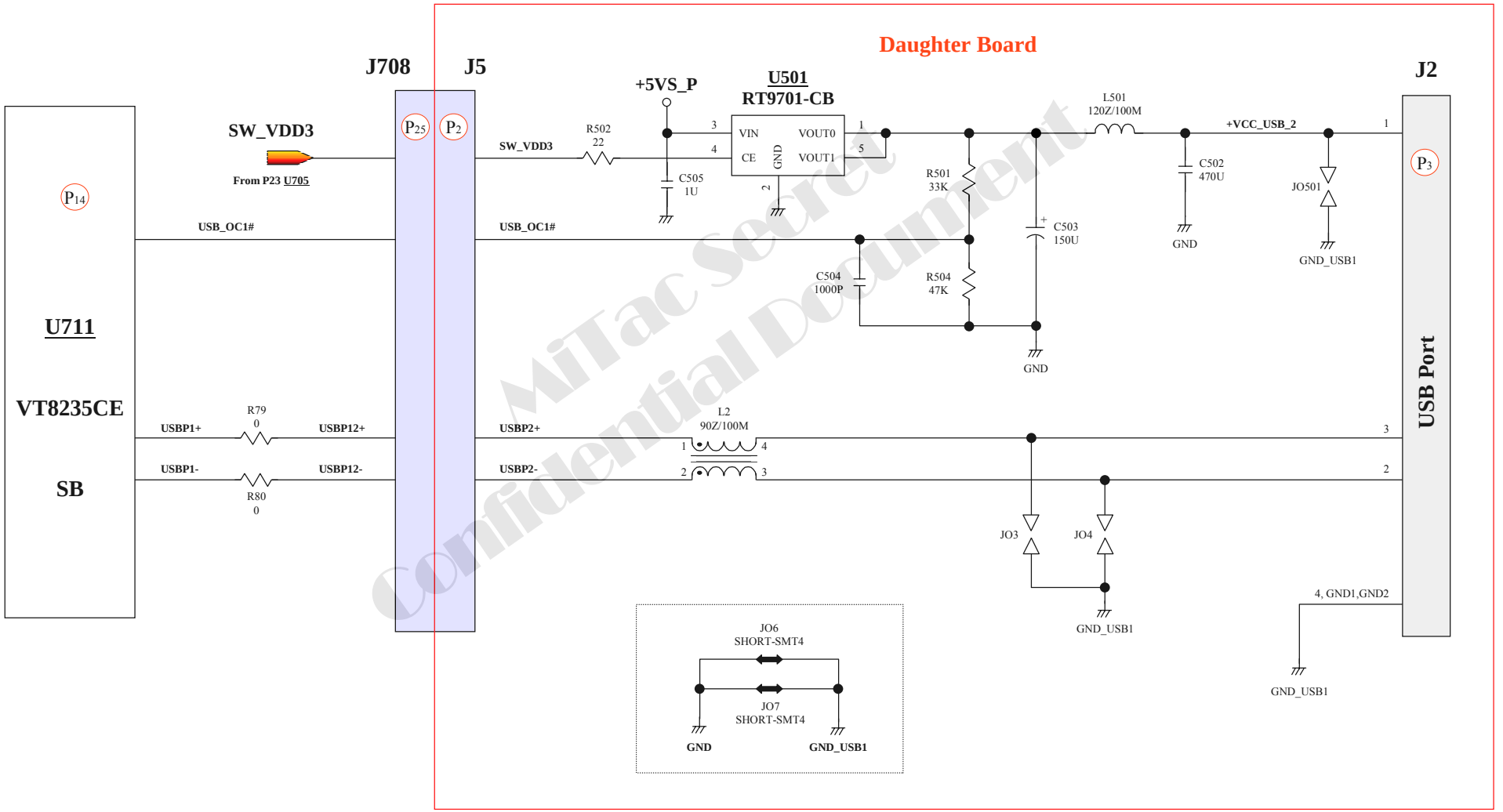
8.10 USB Port Test Error (3)

An error occurs when a USB I/O device is installed.



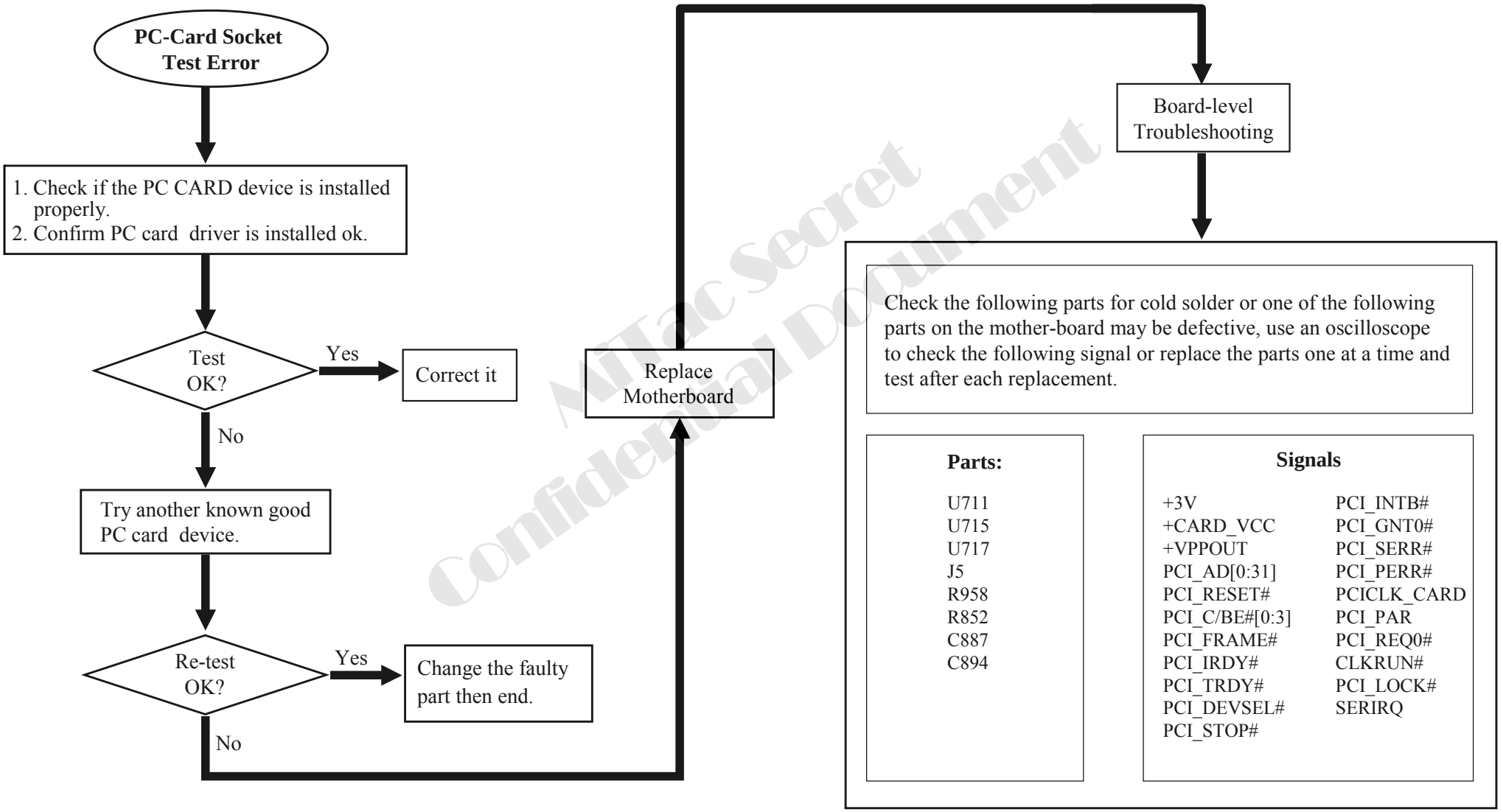
8.10 USB Port Test Error (4)

An error occurs when a USB I/O device is installed.



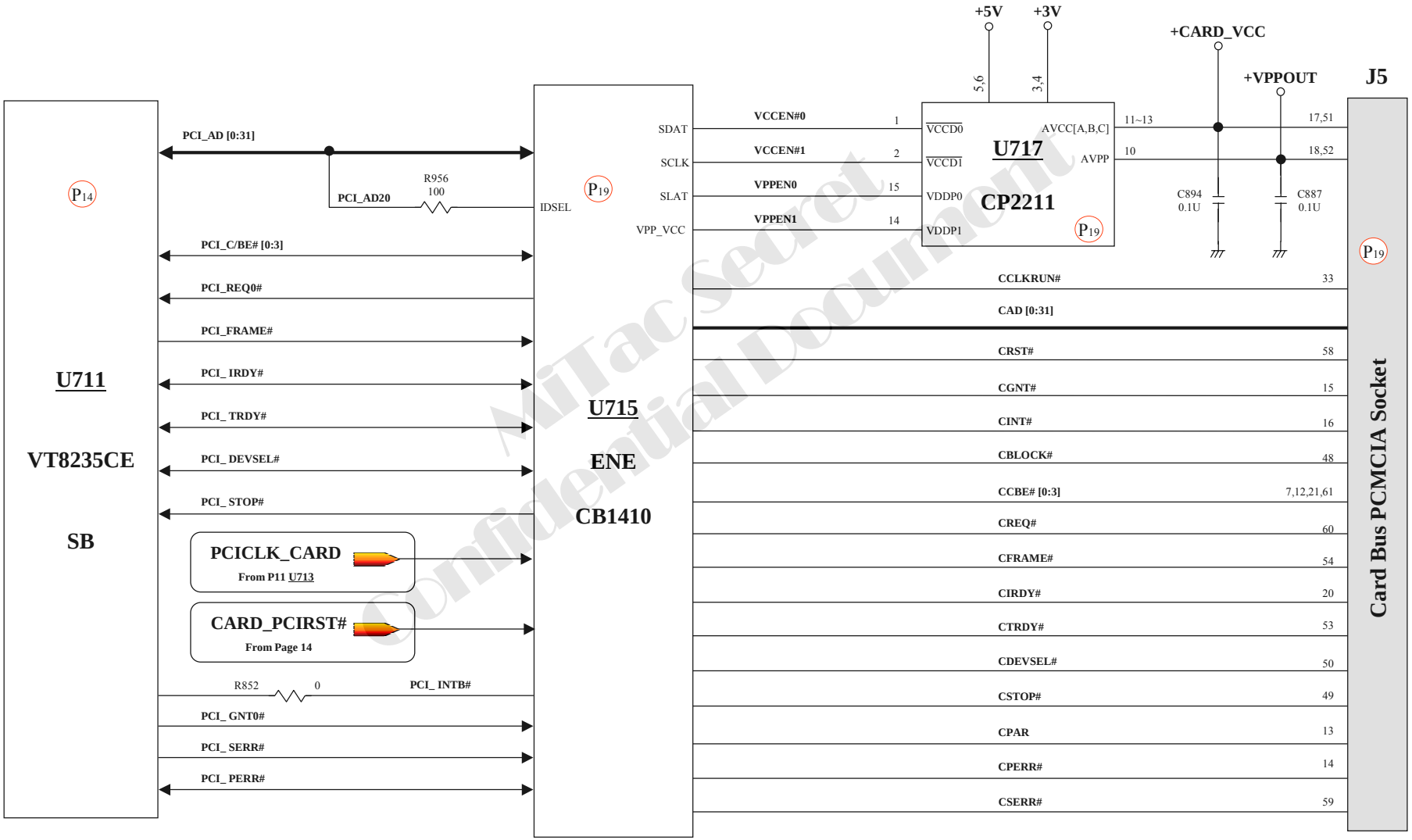
8.11 PC-Card Socket Test Error (1)

An error occurs when a PC card device is installed.



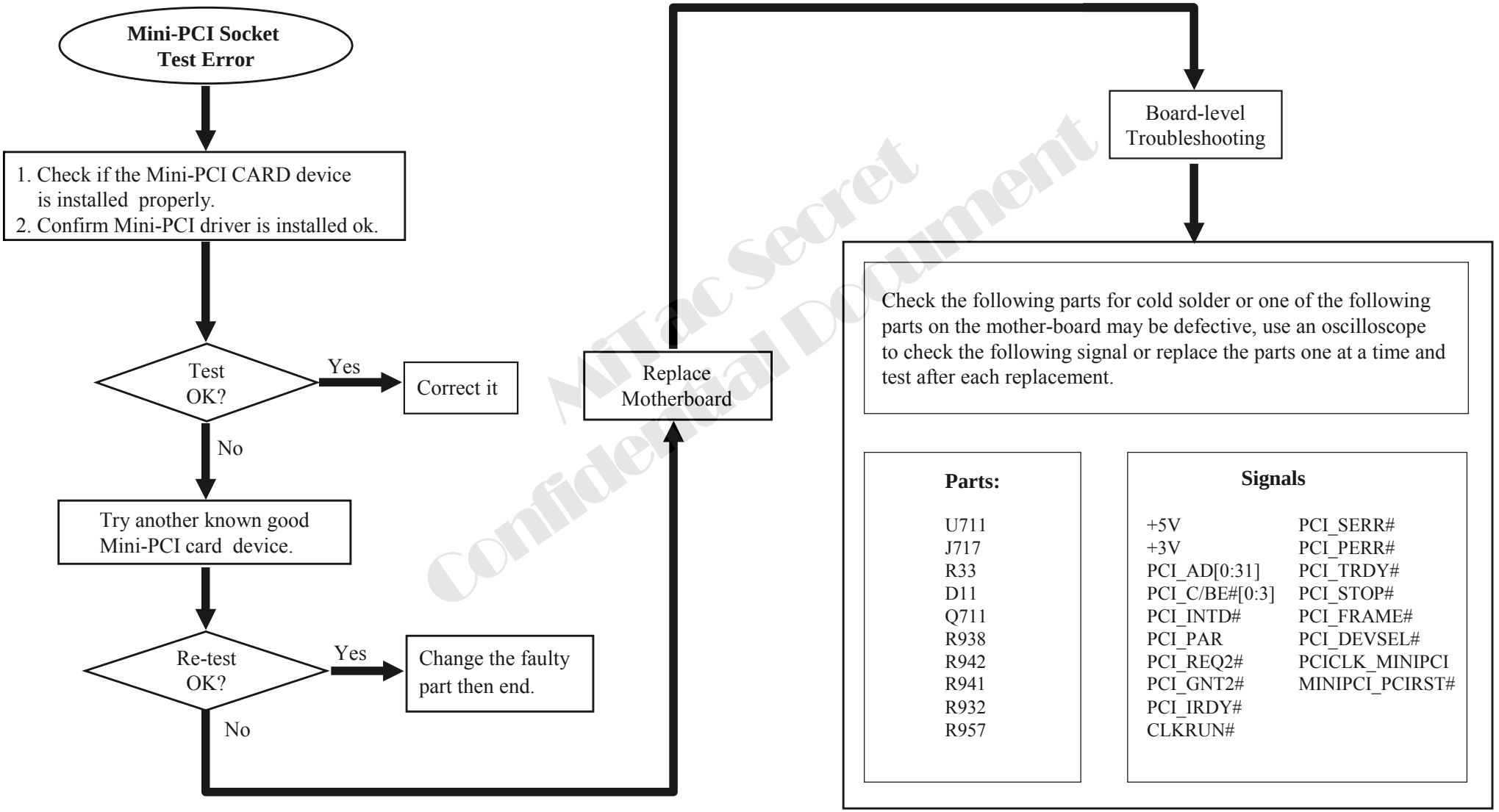
8.11 PC-Card Socket Test Error (2)

An error occurs when a PC card device is installed.



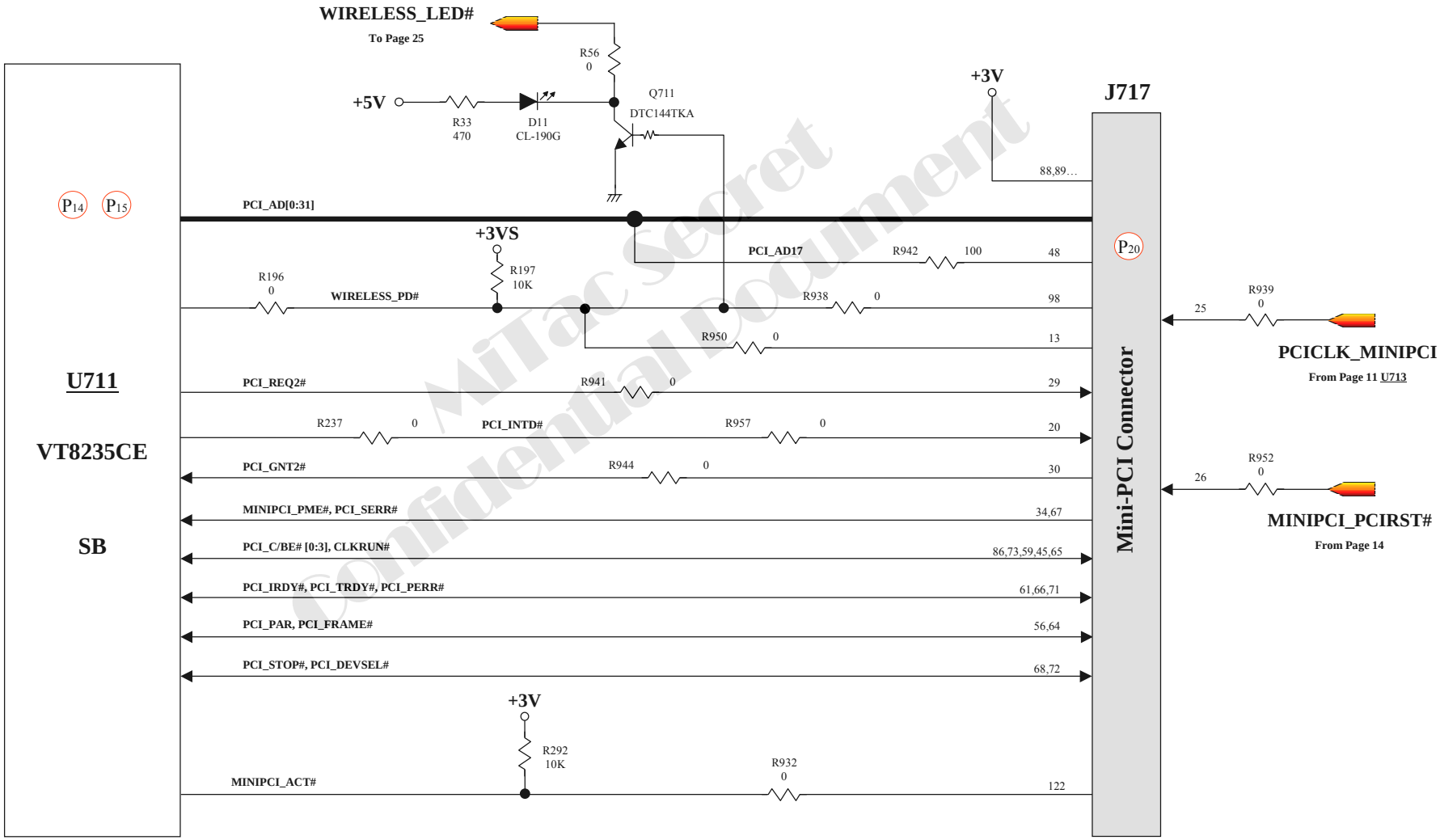
8.12 Mini-PCI Socket Test Error (1)

An error occurs when a PC card device is installed.



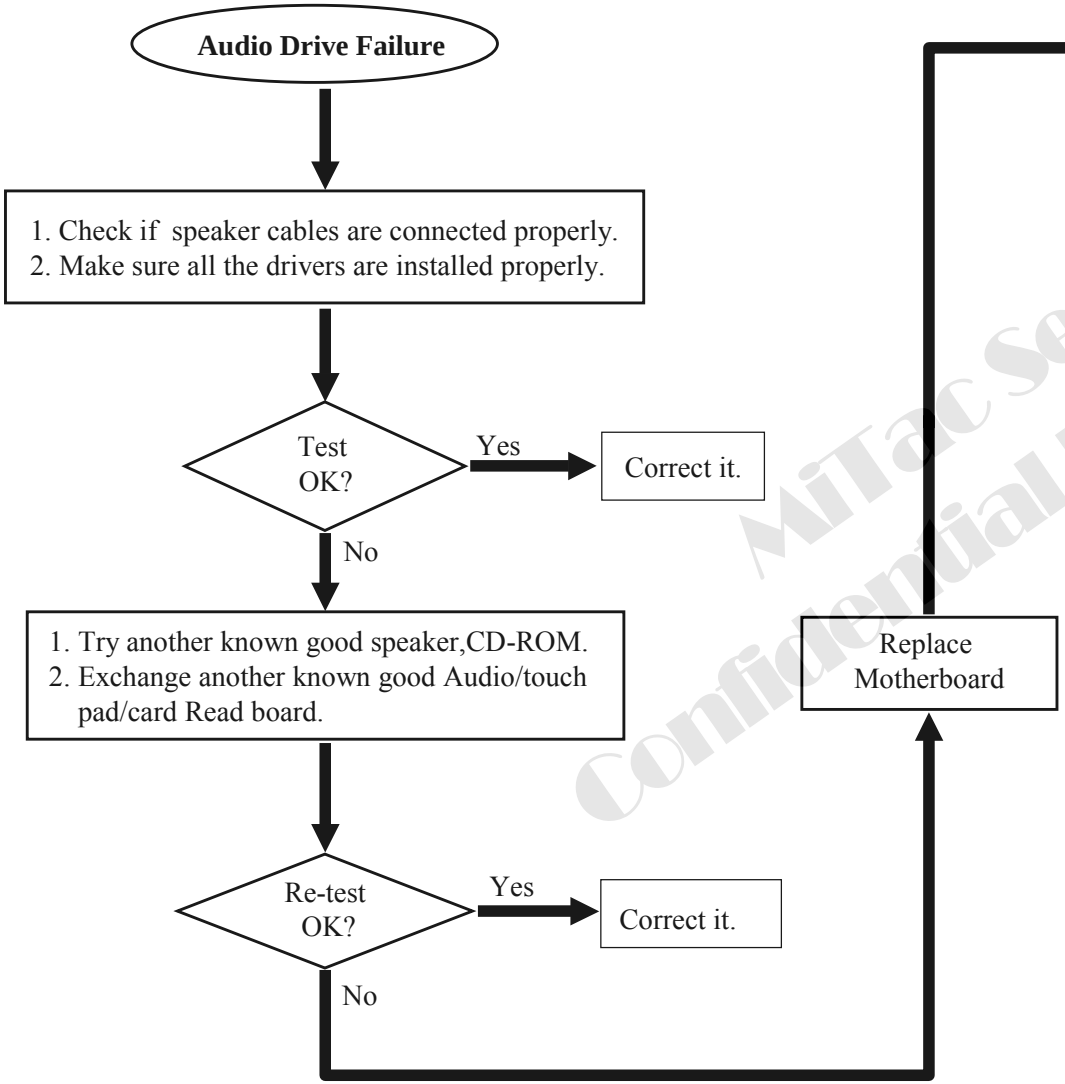
8.12 Mini-PCI Socket Test Error (2)

An error occurs when a PC card device is installed.



8.13 Audio Test Error (1)

No sound from speaker after audio driver is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

Parts:

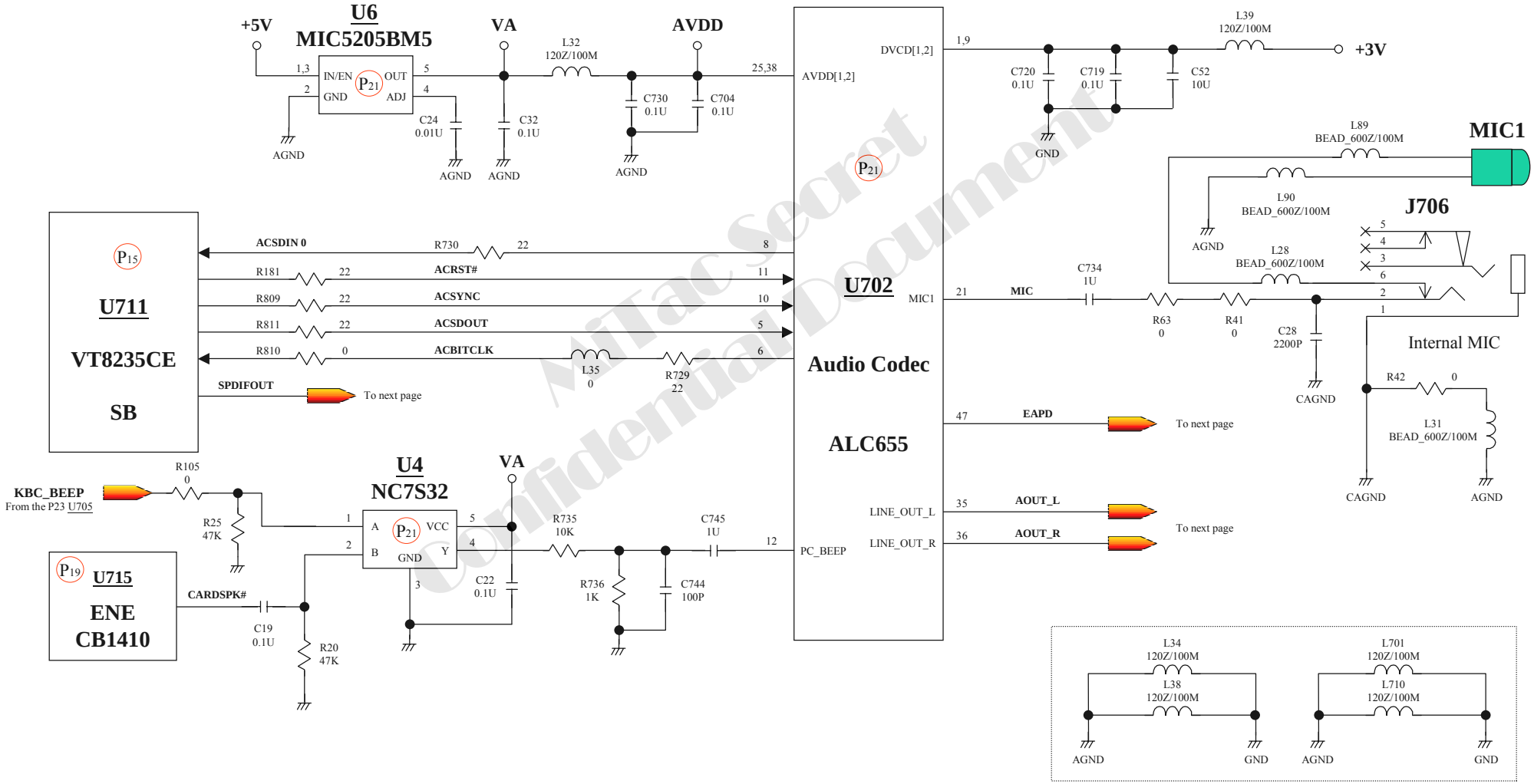
U702	Q10
U7	L702
U711	L707~L709
J706	L37
J704	L42
J709	MIC1
J710	U5
U6	Q5~Q7
U4	L21~L25
L89	L30~L32
L90	R43
L28	R44

Signals

+5V	AMPVDD
VA	DEVICE_DECT#
AVDD	SPK_OFF#
AOUT_R	DECT_HP#OPT
AOUT_L	SPDIFOUT
ACRST#	
ACSDOUT	
ACSDIN0	
ACSYNC	
ACBITCLK	
PC_BEEP	
MIC_INT	

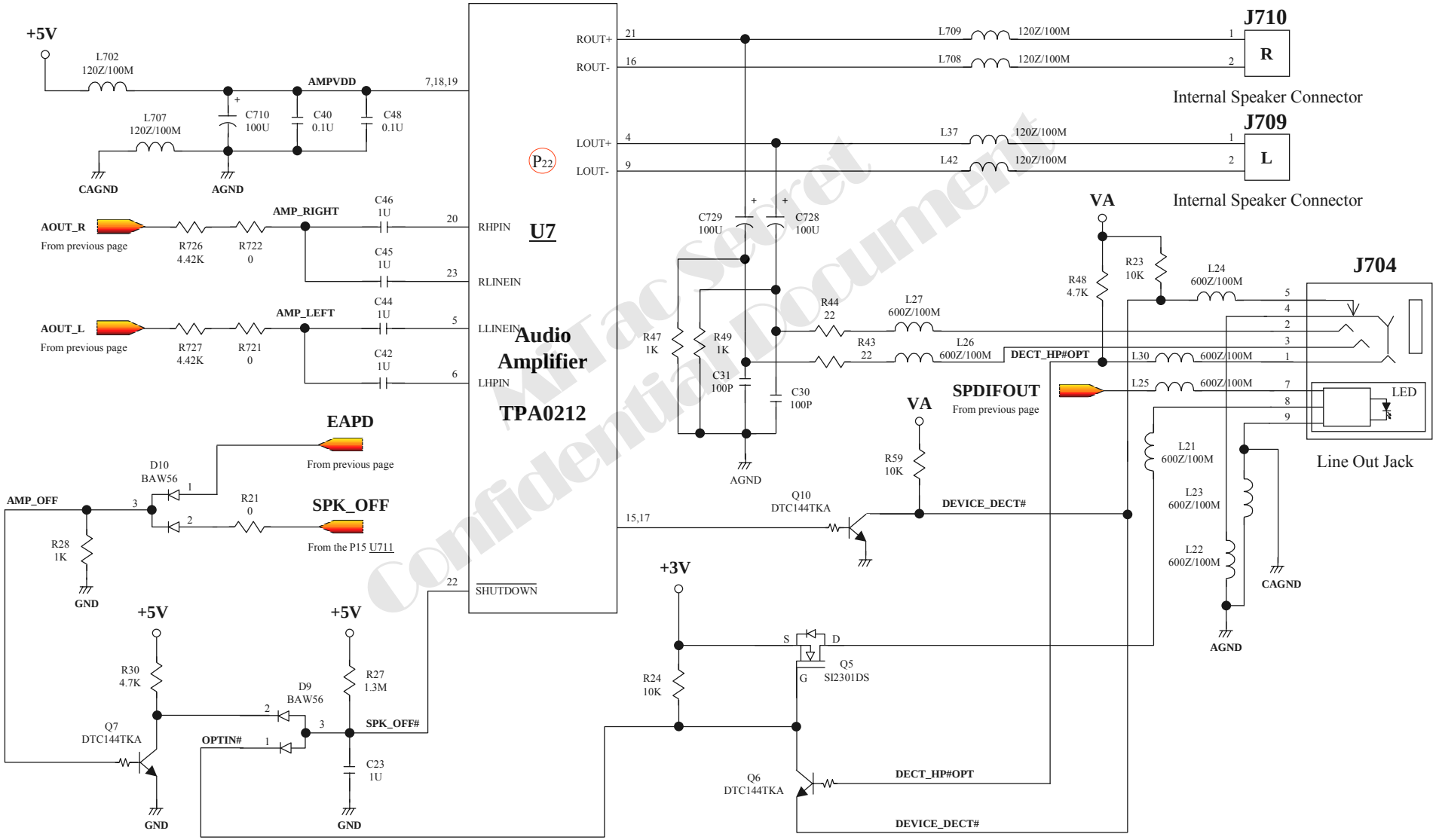
8.13 Audio Test Error (2) – Audio IN

No sound from speaker after audio driver is installed.



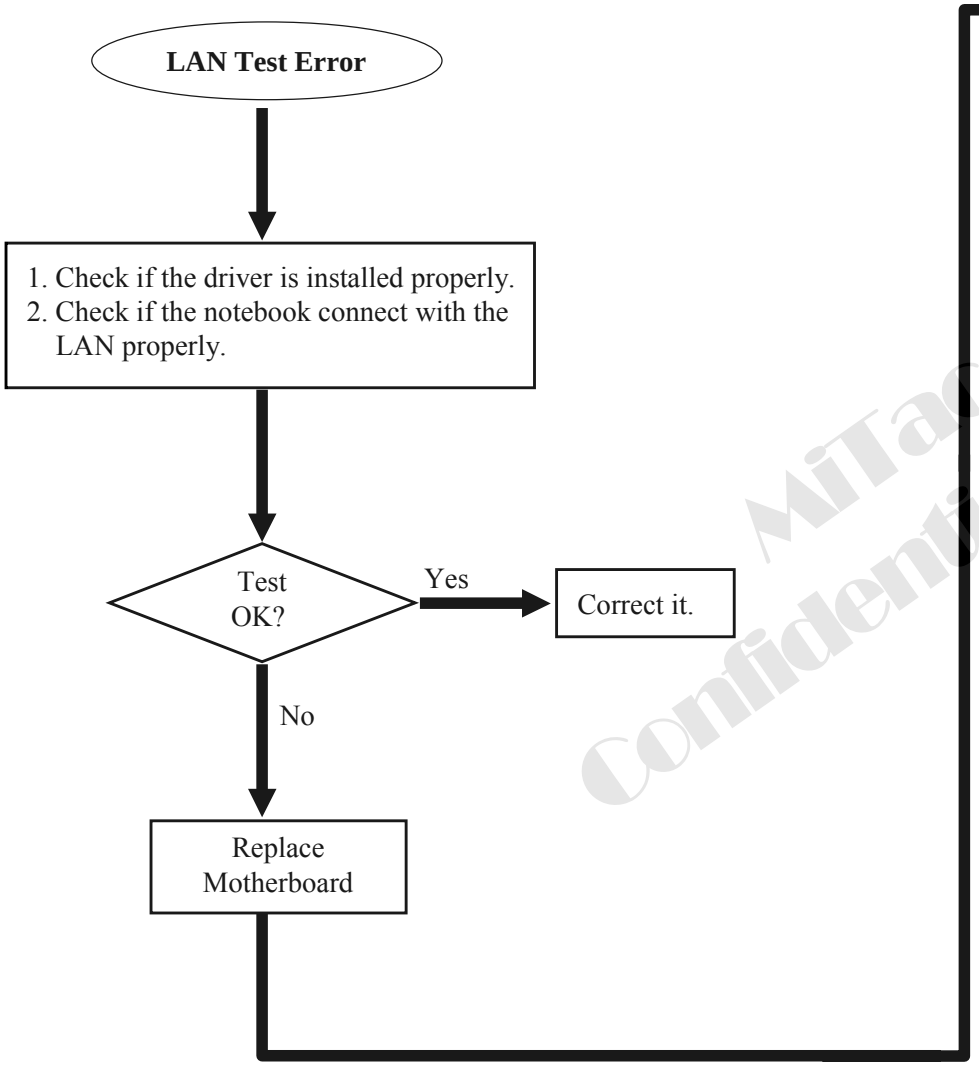
8.13 Audio Test Error (3) – Audio OUT

No sound from speaker after audio driver is installed.



8.14 LAN Test Error (1)

An error occurs when a LAN device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

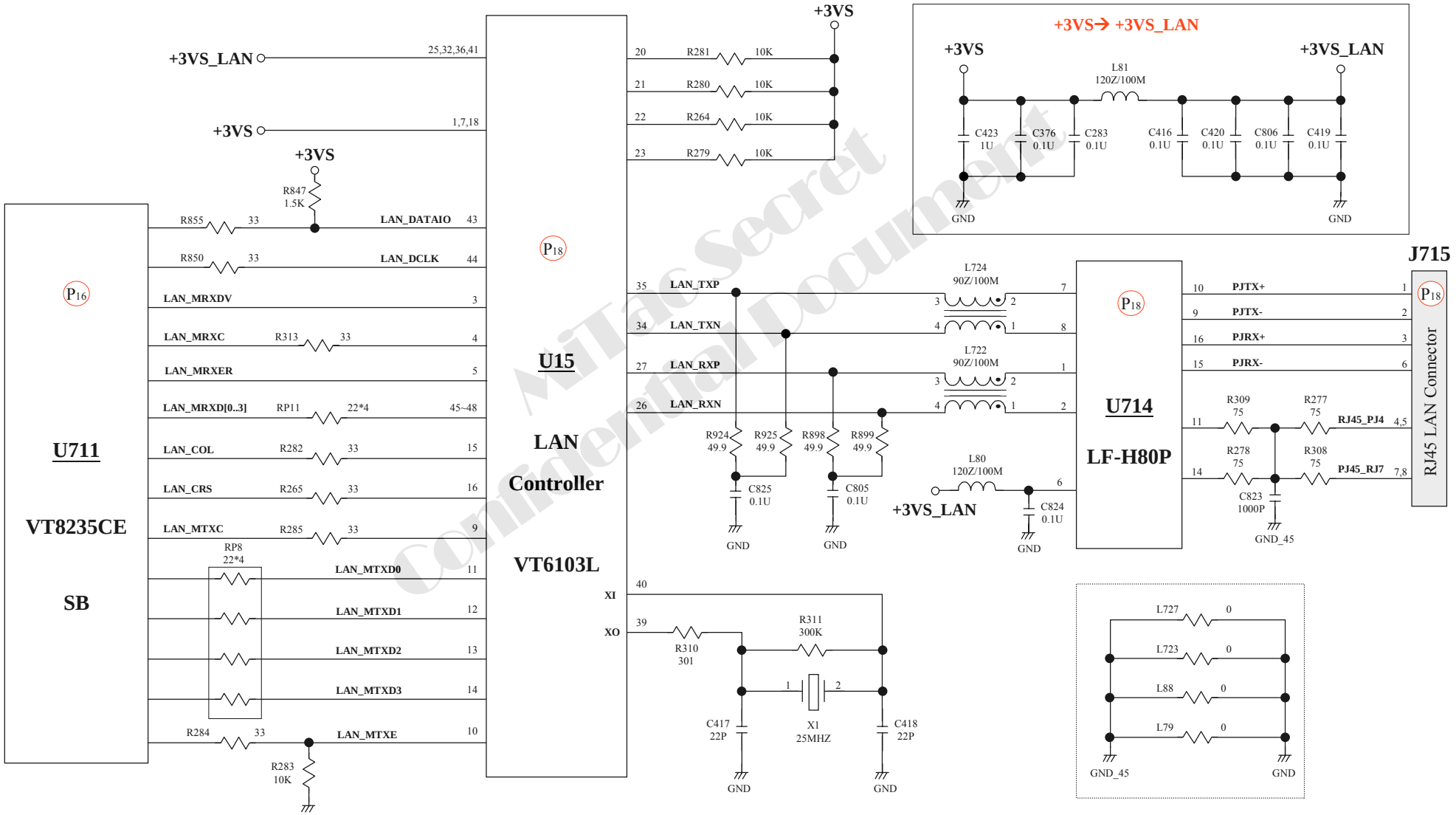
U711	U714
U15	L724
R284	L722
RP8	J715
R850	L80
L81	R924
R285	R925
R282	R898
R265	R899
R311	R847
RP11	R855
X1	

Signals

+3VS	LAN_CRS
+3VS_LAN	LAN_TXP
LAN_MTXD[0:3]	LAN_TXN
LAN_MRXD[0:3]	LAN_RXP
LAN_MRXDV	LAN_RXN
LAN_MRXER	
LAN_MRXC	
LAN_MTXE	
LAN_MTXC	
LAN_DCLK	
LAN_DADAIO	
LAN_COL	

8.14 LAN Test Error (2)

An error occurs when a LAN device is installed.



9. Spare Part List - 1

Part Number	Description	Location(S)
526268710001	LTXXNON;8666/T5IG/OC40D/1XUIXX/1	
523468690051	HDD ASSY;40GB,2.5",MHT2040AT,V40+ FW0022,FUJITSUI,8066	
523402379051	HDD DRIVE;40GB,2.5",MHT2040AT,V40+ FW0022,FUJITSUI	
451686900071	HDD ME KIT;8066	
340686900016	SHIELDING ASSY;HDD,8066	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
324180786912	IC,CPU,Celeron-M 360,1.4GHZ(Dothan),MICRO-FCPGA,479P,INTEL	
323768710001	DDR SODIMM MODULE;DDR333 256MB PC2700 CL2.5 NT256D64SH8C0GM-6K,Na	
416268710001	LF PF;15",B150XG01,15",XGA,AU,8666	
441686900004	LCD ASSY;15",AU,B150XG01,8066	
413000020606	LCD;B150XG01,15",XGA,AU	
412682200001	PCB ASSY;INVERTER BD,DA-1A08-B,PWR	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
411682200001	PWA;PWA-INVERTER BD,DA-1A08-B,PWR	
411682200002	PWA;PWA-INVERTER BD,SMT,DA-1A08-B,PWR	
411682200003	PWA;PWA-INVERTER BD,SMT TOP,DA-1A08-B,PWR	
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R17
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R16,R20,R22
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,SMT	C14A,C14B

Part Number	Description	Location(S)
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only HolyStone	C19
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C16,C17,C6
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,SMT	C9
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	C11
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C15A
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM02B,only A	J2
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SMO2B	
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	LED1
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-T011-NNNA,S	CN1
291000020221	CON;HDR,MA,11P*1,1.25MM,R/A,ACES,85204-1100,SMT,PWR	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190,SMT,PRC	LED3,LED5
288114148004	DIODE;1N4148WS,75V,200mW,SOD-323,SMT	D1
272010680301	CAP;68P,2KV,5%,1206,NPO,SMT,only HolyStone	C18
272010680401	CAP;68P ,CR,2KV,10%,1206,NPO,SMT,PRC	
273001050126	XFMR;CI8.5,25T/2150T,292mH,Varnish Twice,SMT,c	T1
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
411682200004	PWA;PWA-INVERTER BD,SMT BOT,DA-1A08-B,PWR	
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R19
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R18,R21,R23
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	R14B
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R5

9. Spare Part List - 2

Part Number	Description	Location(S)
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C12
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C20,C21
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	C13,C3,C8
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,MPS	U1
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	LED2
295000010120	FUSE;FAST,1.5A,63V,1206,SMT,PRC	F1
295000010149	FUSE;FAST,1.5A,63VDC,1206,SMT,043301.5	
316682200001	PCB;PWA-INVERTER BD (DA-1A08-B);PWR	R0E
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000-2	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190,SMT,PRC	LED4,LED6
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,SMT	C5
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R14A
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PRC	C22,C7
344600000608	BOX;PVC,T=0.5MM,PRC	
221674320005	CARTON; INVERTER, E-NOTE INVERTER BD	
451686900031	LCD ME KIT;15",8066	
342686900005	HINGE;HOUSING,LCD,L,8066	
342686900012	HINGE;L,SZS,8066	
342686900004	HINGE;HOUSING,LCD,R,8066	
342686900013	HINGE;R,SZS,8066	
342686900003	BRACKET;LCD,HOUSING,R,8066	
342686900002	BRACKET;LCD,HOUSING,L,8066	
422686900003	WLEN ASSY;CABLE,8066	

Part Number	Description	Location(S)
422686900002	WIRE ASSY;LCD,HSD150PX14,8066	
422686900005	WIRE ASSY;LCD,HSD150PX14,MPT,8066	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
422686900004	WIRE ASSY;INVERTER,8066	
422686900006	WIRE ASSY;INVERTER,MPT,8066	
346669900004	INSULATOR;INVERTER,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
346686900013	CONDUCTIVE TAPE;HOUSING,LCD,I-CABLE,8066	
345677000018	CONDUCTIVE TAPE;LCD,LYNX	
340686910002	HOUSING ASSY;LCD,ID2,8066	
340686910004	COVER ASSY;LCD,ID2,8066	
346677000012	MYLAR;COVER,LCD,LYNX	
431687100001	CASE KIT;8666	
451687100051	HOUSING KIT;8666	
340686900011	SPEAKER ASSY;L,8066	
340686900012	SPEAKER ASSY;VECO,L,8066	
340686900010	SPEAKER ASSY;R,8066	
340686900013	SPEAKER ASSY;VECO,R,8066	
340687100001	COVER ASSY;8666	
340687100002	HOUSING ASSY;8666	
340686900002	COVER ASSY;CPU,8066	
340686900003	COVER ASSY;HDD,8066	

9. Spare Part List - 3

Part Number	Description	Location(S)
344686900006	COVER;HINGE,8066	
340686900004	COVER ASSY;KB,8066	
340686900009	SHIELDING ASSY;COVER,8066	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
422674300071	WIRE ASSY;MDC,E-NOTE	
341680900001	SPC SCREW;#4-1/4,8050	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
422686900001	WIRE;CABLE,TP,8066	
346670500014	INSULATOR;MDC,TETRA	
344684000040	DUMMY CARD;PCMCIA,8050M	
345686300002	SPONGE;HDD,8050FX	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PUM1950	
412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I,MANGUSTA	
411686900004	PWA;PWA-8066,DAUGHTER BD	
411686900005	PWA;PWA-8066,DAUGHTER BD,T/U	
411686900006	PWA;PWA-8066,DAUGHTER BD,SMT	
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR517,PR518
271035012712	RES;.012,1W,1%,2010,CYNTEC,SMT	PR525
271035012711	RES;.012,1W,1%,2010,LR2010,IRC,SMT	
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR511,PR526
271061000002	RES;0 ,1/16W,0402,SMT	R3
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R1,R4

Part Number	Description	Location(S)
271061333501	RES;33K ,1/16W,5% ,0402,SMT	R501,R506
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R504,R505
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR521,PR524,R2
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR1,PR2
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR506
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR515,PR516,PR522
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR512,PR513,PR523
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR510
271071196211	RES;19.6K,1/16W,1% ,0603,SMT	PR508
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR505
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR504
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR502,PR503
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R502,R507
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	PR519,PR520
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR509
271072474101	RES;470K ,1/10W,1% ,0603,SMT	PR514
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC1
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	PC503
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC518,PC519
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	PC517,PC540,PC541,PC546,PC54
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	PC522,PC544,PC545
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC510,PC511,PC515,PC521,PC53
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC2,PC504,PC508,PC516,PC520,
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SMT	PC513,PC514
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC501,PC502

9. Spare Part List - 4

Part Number	Description	Location(S)
272075470302	CAP;47P ,CR,50V ,5%,0603,NPO,SMT	PC506,PC507
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y5V	C505,C508
272105102501	CAP;1000P,50V ,+/-20%,0402,X7R,SMT	C3,C504,C506,C9
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C7
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C1,C5,C8
272105471403	CAP;470P ,50V,10%,0402,X7R,SMT	C502,C507,C509
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C503,C512,PC542,PC543
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L12
273000150156	FERRIET CHIP;120OHM/100MHZ,2012,6A,MAGIC	PL501,PL502,PL503
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012,TDK	L2,L6,L7
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,5A,MAGIC	L11,L13,L501,L502,L503
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY TDK.	FA1
273000990167	INDUCTOR;10UH,30%,SPC-10039-100	PL504
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QFN,SMT	PU501
286309701003	IC;RT9701CB,POWER DISTRI SW,SOT23-5,5P,RICH	U501,U502
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	PD502
288100056003	DIODE;BAW56,70V,215mA,SOT-23	
288100140007	DIODE;B140,40V,1A,SMA,DIODES,SMT	PD503,PD505
288100014007	DIODE;SS14,40V,1A,SMA	
288100014010	DIODE;SS14,40V,1A,SMA,VISHAY	
288100840001	DIODE;SM840B,40V,8A,STD-202	PD504

Part Number	Description	Location(S)
288204825001	TRANS;AM4825,P-MOS,9.3A,19mOHM,SO8,SMT	PQ504
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SMT	
288204914001	TRANS;AO4914,DUAL N-MOSFET,WITH SCHOTTK	PU502,PU503
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ501,PQ502,PQ503,PQ505,PQ5
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	
291000021107	CON;HDR,MA,11P*1,1.25MM,SMT,ACECON	J4
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F501
295000010163	FUSE;NORMAL,7A/24VDC,0433007,1206,LITTELFU	PF501
295000010193	FUSE;FAST,7A/32V,1206,SMT	
297040100034	SW;PUSH BUTTOM,5P,SPST,12V/50MA,H4.3,W/Z G	SW2
331000008033	CON;USB,FM,H15.64,R/A,4P*2,2522A,SUYIN,TETR	J3
316686900002	PCB;PWA-8066/Daughter BD	R01
273000990054	INDUCTOR;10UH,D124C,+/-20%,TOKO,SMT	PL506
291000913003	CON;SPEED,30P B/B male SMT CON,T03-112-0297	J5,J6
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT,PANASONIC	PC526,PC527,PC528,PC530
291000010421	CON;USB,HDR,FM,4P*1,H6.9,R/A,020133MR004S51	J2
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	J1
297140200006	SW;COVER SWITCH,SPST,30VDC,0.1A,H13.7,4P,SM	SW1
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
624200010140	LABEL;5*20,BLANK,COMMON	
346686900005	INSULATOR;DAUGHTER,BD,8066	
347210010010	GASKET;2,10,010,010,TennRich	
347210040012	GASKET;2,10,040,012,TennRich	
345686900010	SPONGE;DB,USB,8066	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	

9. Spare Part List - 5

Part Number	Description	Location(S)
242600000452	LABEL;BLANK,7MM*7MM,PRC	
411687100001	PWA;PWA-8666,MOTHER BD	
411687100002	PWA;PWA-8666,MOTHER BD,T/U	
411687100003	PWA;PWA-8666,MOTHER BD,SMT	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L34,L38,L49,L701,L710,R14,R26
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R84,R85
271012000301	RES;0 ,1/8W,5% ,1206,SMT	PR712
271013102301	RES;1K ,1/4W ,5% ,1206,SMT	PR61,PR728,PR73,PR75
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR729
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR703
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR743
271061000002	RES;0 ,1/16W,0402,SMT	PR15,PR16,PR17,PR18,PR19,PR3
271061010101	RES;1,1/16W,1%,0402,SMT	PR5
271061100102	RES;10,1/16W,1%,0402,SMT	PR13,PR14,PR2
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR721,R321,R322,R323,R324,R32
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R209,R210,R225,R226,R256,R86,
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PR36,PR730,R229,R47,R49,R52,R
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R160,R216,R253,R28,R296,R297,
271061103501	RES;10K ,1/16W,5% ,0402,SMT	PR723,PR727,R112,R124,R127,R1
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR49,PR6,PR67,PR740,PR741,PR
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R109,R154,R45,R57,R75,R78,R92
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR34,PR48,PR50,PR71,PR72,R31
271061106501	RES;10M ,1/16W,5% ,0402,SMT	R857
271061127212	RES;12.7K,1/16W,1%,0402,SMT	PR35
271061133311	RES;13.3K,1/16W,1%,0402,SMT	PR11,PR32

Part Number	Description	Location(S)
271061135101	RES;1.3M,1/16W,1%,0402,SMT	PR31,R27
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R119
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R172,R847
271061153102	RES;15K ,1/16W,1% ,0402,SMT	PR731,PR732,R287,R396,R73
271061184302	RES;180K ,1/16W, 5%,0402,SMT	R972
271061196212	RES;1.96K,1/16W,1%,0402,SMT	PR3
271061201101	RES;200 ,1/16W, 1%,0402,SMT	R116,R122,R146,R148,R152
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R181,R259,R305,R371,R43,R44,R
271061221313	RES;220 ,1/16W, 5%,0402,SMT	R36,R37,R38,R386,R389,R392
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R300,R301,R302,R70,R840,R841
271061232111	RES;2.32K,1/16W,1%,0402,SMT	PR12
271061249312	RES;249K,1/16W,1%,0402,SMT	PR40
271061270102	RES;27.4 ,1/16W, 1%,0402,SMT	R107,R151,R96
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R796,R798
271061301112	RES;301 ,1/16W,1% ,0402,SMT	R310
271061302101	RES;3K ,1/16W,1% ,0402,SMT	R230
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R224,R265,R282,R284,R285,R313
271061331304	RES;330 ,1/16W,5% ,0402,SMT	R291,R929
271061333501	RES;33K ,1/16W,5% ,0402,SMT	R703
271061361101	RES;360 ,1/16W,1% ,0402,SMT	R228,R289
271061390501	RES;39, 1/16W, 5%,0402,SMT	R118
271061464112	RES;4.64K ,1/16W,1% ,0402,SMT	R794
271061471501	RES;470 ,1/16W,5% ,0402,SMT	R33,R341,R377,R382
271061472102	RES;4.7K ,1/16W,1% ,0402,SMT	R288,R947
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R13,R167,R168,R17,R170,R174,R

9. Spare Part List - 6

Part Number	Description	Location(S)
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R20,R25,R702
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR77,R164
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R895
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R211,R212,R254,R342,R343,R344
271061510303	RES;51, 1/16W, 5%,0402,SMT	R115,R132,R136,R149
271061549011	RES;54.9 ,1/16W,1% ,0402,SMT	R108,R147,R95,R97,R98
271061562102	RES;5.6K ,1/16W, 1%,0402,SMT	R275,R317,R720
271061562212	RES;56.2K,1/16W,1%,0402,SMT	PR29
271061576411	RES;576K ,1/16W,1% ,0402,SMT	PR10
271071442311	RES;442K,1/16W,1% ,0603,SMT	PR705
271061604011	RES;60.4 ,1/16W,1% ,0402,SMT	R169,R223
271061649212	RES;6.49K,1/16W,1% ,0402,SMT	R901
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R120,R247
271061682501	RES;6.8K ,1/16W,5% ,0402,SMT	R64,R65,R68,R69
271061753101	RES;75,1/16W,1%,0402,SMT	R11,R12,R277,R278,R308,R309,R
271061806311	RES;80.6K,1/16W,1% ,0402,SMT	PR38
271061820501	RES;82 ,1/16W,5% ,0402,SMT	R214
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L15,L22,L23,L31,L35,L711,L723
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR714,PR722
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR716
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR52,PR54,PR55,PR706,PR717
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR58
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR708
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R272,R273
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R133,R134,R135,R137,R138,R139

Part Number	Description	Location(S)
271071182101	RES;1.8K ,1/16W,1% ,0603,SMT	PR719
271071183101	RES;18K ,1/16W,1% ,0603,SMT	PR733
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR22,PR734,PR737
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR711
271071205101	RES;2M ,1/16W,1% ,0603,SMT	PR710
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R106
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR702
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR60
271071274911	RES;27.4 ,1/16W,1% ,0603,SMT	R255
271071287311	RES;287K ,1/16W,1% ,0603,SMT	PR709
271071301011	RES;301 ,1/16W,1% ,0603,SMT	PR720
271071304301	RES;300K ,1/16W,5% ,0603,SMT	R311
271071333101	RES;33K ,1/16W,1% ,0603,SMT	PR51
271071433301	RES;43K ,1/16W,5% ,0603,SMT	R958
271071453211	RES;45.3K,1/16W,1% ,0603,SMT	PR738
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR56,PR57
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR4,PR70,PR742
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR23
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR724
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR53
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR59
271071665011	RES;665 ,1/16W,1% ,0603,SMT	R314
271071752101	RES;7.5K ,1/16W,1% ,0603,SMT	PR718
271071823102	RES;82K,1/16W,1%,0603,SMT	PR704
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR707

9. Spare Part List - 7

Part Number	Description	Location(S)
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SMT	RP22,RP23,RP53,RP54
271571220301	RP;22*8 ,16P ,1/16W,5% ,1606,SMT	RP13,RP5,RP7,RP704,RP705,RP7
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SMT	RP32,RP33,RP34,RP35,RP36,RP3
271586026101	RES;.02 ,2W,1%,2512,SMT	PR701
271591220301	RP;22*4,8P,1/16W,5%,0804,SMT	RP10,RP12,RP14,RP15,RP16,RP1
271591330302	RP;33*4,8P,1/16W,5%,0804,SMT	RP39
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP4
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP706,RP9
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP701,RP8
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP702
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP2
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP3,RP703
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC729
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C109,C114,C115,C116,C117,C118
272001106703	CAP;10U,10V,+80-20%,0805,Y5V,SMT ,YAGEO	C200,C203,C204,C207,C211,C218
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y5V,SMT	C133,C763,C890
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C384,C63,C851
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC7,PC754,PC760
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C427,C428,C431,C434,C435,C461
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT ,AVX	PC40,PC715,PC731,PC739,PC746
272011106419	CAP;10U,10V,+-10%,X5R,1206,SMT	
272013106503	CAP;10U,25V,+-20%,X5R,1206,Mitsubishi	PC10,PC11,PC32,PC34,PC35,PC7
272013106502	CAP;10U,25V,+/-20%,1206,X5R,SMT	
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT ,PANASONIC	PC9
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C823

Part Number	Description	Location(S)
272071225401	CAP;2.2U ,CR,6.3V ,10%,0603,X5R,SMT	C106,C112,C154,C158,C159
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	PC23
272072105702	CAP;1U ,CR,16V,+80-20%,0603,Y5V,SMT	PC743
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC709,PC732
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC24,PC703,PC704,PC708,PC718
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,SMT	PC13,PC22,PC717,PC720,PC726,
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,SMT	C787,C789
272101015401	CAP;1U,6.3V,+-10%,0402,X5R,SMT	C110,C111,C162,C166,C168,C169
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SMT	C334,C339,C34,C35,C377,C424,C
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y5V	C170,C182,C205,C221,C224,C225
272102224701	CAP;.22U ,10V ,+80-20%,0402,Y5V,SM	C25,C736
272103331401	CAP;33P ,25V ,+/-10%,0402,NPO,SMT	C10,C329,C330,C331,C337,C342,
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SMT	C14,C15,C16,C2,C3,C4,C415,C53,
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,SMT	C164,C30,C31,C744,PC1,PC18,PC
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SMT	C163,C165,C167,C179,C180,C186
272105102501	CAP;1000P,50V ,+/-20%,0402,X7R,SMT	C160,C171,C183,C184,C185,C188
272105103402	CAP;.01U ,CR,25V ,10%,0402,X7R,SMT	C174,C175,C176,C206,C208,C212
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C155,C24,C244,PC20,PC28,PC29,
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C101,C103,C105,C108,C113,C130
272105181403	CAP;180P,50V,10%,0402,SMT	PC749
272105220402	CAP;22P ,50V ,+ -10%,0402,NPO,SMT	C100,C417,C418,C467,C480,C76,
272105221403	CAP;220P ,CR,50V ,10%,0402,X7R,SMT	C102,C104,PC6,PC751
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,SMT	C28,C414,C762
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C11,C12,C13
272105331301	CAP;330P ,50V,5%,0402,NPO,SMT	C5,C6,C7

9. Spare Part List - 8

Part Number	Description	Location(S)
272105332402	CAP;3300P,50V,10%,0402,SMT	PC17
272105390302	CAP;39P ,50V ,5% ,0402,NPO,SMT	C772,C773
272105470402	CAP;47P ,50V ,+ -10%,0402,NPO,SMT	C272,C274,C275,C375
272431227516	CAP;220U,2V,20%,7343,SDK-CAP	PC710,PC711,PC712,PC713,PC71
272431227528	CAP;220U,2.5V,TPE-MC,20%,POSCAP,H1.8,7343,SMT	
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC762,PC763
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,SMT	C710,C728,C729
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,SMT	CP1
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,SMT	L21,L24,L25,L26,L27,L28,L30,L3
273000130312	FERRITE CHIP;50OHM/100M,1608,MAGIC	L11,L12,L2
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L39,L4,L47,L5,L50,L51,L52,
273000150156	FERRIET CHIP;120OHM/100MHZ,2012,6A,MAGIC	PL1,PL2,PL3,PL702,PL703,PL70
273000150307	FERRITE BEAD;120 OHM/100MHZ,3A,0805,MAG	L16,L32,L69,L702,L707
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012,TDK	L17,L722,L724
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;TWI	L720
273000500236	CHOCK COIL; 4.7UH,45mOHM,2.5A,5.8X5.2X4.5,KJ	PL707,PL709
273000500239	CHOCK COIL;33UH,97mOHM,20%,2.7A,KRH124-33	PL706
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	
273000500237	CHOCK COIL; 3.0UH,35mOHM,3.5A,6.7X6.7X4.0,KJ	PL705
273000990180	INDUCTOR;3.0UH,30%,SPC06703,H2.85,TMP,SMT	
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U714
274012500420	XTAL;25MHz,30PPM,16PF,8*4.5,2P,SMT,eCERA	X1
274012500415	XTAL;25MHZ,20PF,30PPM,8.0*4.5,SMT	
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X705
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70-5P	U2,U3

Part Number	Description	Location(S)
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,14P	U712
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14P	U716
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT23-5	U4
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BITS,SO8,SMT	U710
284500655003	IC;ALC655,AUDIO CODEC,LQFP,48P,SMT	U702
284501623001	IC;VT1623M,TV ENCODER,TQFP,64P,SMT	U708
284501634002	IC;VT1634AL,LVDS TRANSMITTER,LQFP,48P,SMT	U703
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU11
284506103008	IC;VT6103L,LAN-PHY,LQFP48,SMT	U15
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,16P,SMT	U707
284508235008	IC;VT8235CE,SOUTH BRIDGE,BGA,487P,SMT	U711
284595090202	IC;ICS950902,CLOCK GEN,SSOP56,56P,SMT	U713
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,SMT	U7
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU701
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ708
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU702
286302211008	IC;CP2211,POWER DISTRI SW,REV D3,ENE,SSOP16	U717
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATOR,SOT-223	U12
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QFN,SMT	PU705
286303734001	IC;LTC3734,PWM CONTROLLER,32-QFN,SMT	PU1
286305234001	IC;FAN5234MTCX,PWM,TSSOP,16P,FAIRCHILD	PU704
286308800014	IC;AME8800,0.3A,1.5V,REG,SOT89	U14
286308800022	IC;AME8800MEFT,0.3A,1.8V,REG,SOT89N,SMT	U10
286309167001	IC;RT9167-47CB,200MA LDO REGULATOR,SOT-25	U6
286309701003	IC;RT9701CB,POWER DISTRI SW,SOT23-5,5P,RICH	U701

9. Spare Part List - 9

Part Number	Description	Location(S)
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V,SOT143,SMT	U13
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D19,PD707
288203004001	DIODE;SKS30-04AT,40V,3A,SMT,SMA,MITSUBISHI	PD702,PD704,PD706
288100034004	DIODE;SSA34,40V,3A,SMA	
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D20,D21
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT23	PD3
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	D16
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	D9,PD5
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D3,D7,D8
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,ON	PD1,PD2
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,SMT	PD701
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-23	D705,D706,D707,PD79
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D10,D22,D704
288104148001	DIODE;RLS4148,200MA,500MW,MELF,SMT	D701,D702
288200114001	TRANS;DTC114TKA,10K,N-MOSFET,SOT23	Q12
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q25,Q26,Q28,Q35
288200144020	TRANS;DTC144TKA,NPN,SOT-23,SMT,PANASONI	Q32,Q38,Q39,Q703
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q40,Q705,Q707,Q9
288202215001	TRANS;MUN2215T1,N-MOSFET,SC59,SMT	Q713,Q714
288202222019	TRANS;MMBT2222ALT1,NPN,TO236AB,ON	PQ707
288202237002	TRANS;MUN2237T1,NPN,SOT-23,SMT,ON	Q22
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	Q10,Q29,Q30,Q31,Q34,Q36,Q37,(
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q21,Q23,Q33,Q5,Q701,Q710
288203414001	TRANS;AO3414,N-CHANNEL FET,SOT-23	Q14,Q16
288203904022	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB,ON	PQ3

Part Number	Description	Location(S)
288204406001	TRANS;AO4406,N-MOS,.0165OHM,SO8	PU5,PU6
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0065OHM,SO	PU10
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOIC-8	PU9
288204435003	TRANS;FDS4435,P-MOSFET,35mOHM,SO,8P,MRS	Q8,U8,U9
288200144002	TRANS;DTA144WK,PNP,SMT	PQ709
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	Q11,Q41,Q42
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ4,PQ5,PQ6,PQ7,PQ704,PQ705
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,SMT,ACES	J711
291000010619	CON;HDR,MA,6P,ACES,87151-0607,SMT	J3
291000012031	CON;HDR,MA,10P*2,1MM,H5.4,R/A,SMT,ACES-881	J1
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A,SMT,ACES	J712,J714
291000024426	CON;HDR,FM,22P*2,2MM,R/A,SMT,SUYIN,200062F	J718
291000143007	CON;FPC/FFC,88018-3000,15P*2,.8MM,BD/BD,SMT	J720
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85202-2605,ACE	J2
291000251246	MINIPCI SOCKET;124P,R/A,0.8MM,H=6,SMT,B27-1	J717
291000256843	CON;IC CARD,68P,UP,STANDOFF 0.0 MM ,MPT,29	J5
291000614793	IC SOCKET;UPGA479M,479P,MOLEX	U704
291000811008	CON;PHONE JACK,2 IN 1,7.0MM,ALLTOP,SMD	J715
291000913002	CON;SPEED,30P B/B female SMT CON,T02-109-0297	J707,J708
291000920607	CON;STEREO JACK,6P,W9.5,933100000180,SMT,AC	J706
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D11,D12,D28,D29,D31,D32,D33
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	D13
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,SMD	F4
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F3
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF701

9. Spare Part List - 10

Part Number	Description	Location(S)
295000010163	FUSE;NORMAL,7A/24VDC,0433007,1206,LITTELFU	PF1
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F2
295000100006	FUSE;FAST,2A/63V,R433002,1206,SMT	F1
331040050023	CON;HDR,BTB R/A,0.8MM,S-TECH1507,DIP,50P,AI	J713
331040050018	CON;HDR,BTB R/A,0.8MM,S-TECH1507,DIP,50P	
331720015084	CON;D,FM,15P/3R,R/A,070915FR015S201ZU,SUYIN,	J701
331870007007	CON;MINI DIN,7P,R/A,W/GROUND,33007S-07T	J702
342674500002	STAND OFF;AM20-30,GP3	MTG701,MTG702
273000500241	CHOCK COIL;2.8UH,15mOHM,25%,8.0A,KRH105R-	PL710
273000500111	CHOCK COIL;3UH,14mOHM,7.5A,10039P	
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ701
288204814001	TRANS;SI4814,26.5mOHM,N_MOS ,SMT	PU703,PU8
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SMT	PQ702,PQ703,PQ706
331000007056	CON;BATT,C10367-10701,7 PIN,ALLTOP	J705
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,5A,MAGIC	L20,L43,L44,L45,L46,L67,L68,L7
284500800003	IC;PN800CD,NORTH BRIDGE,HSBGA,829P	U709
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,SMT,ACES	J709,J710
272070475701	CAP;4.7U,CR,6.3V,+80-20%,0603,Y5V,SMT	C214,C239,C256,C268,C269,C285
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TUV	C280,C282
481687100002	F/W ASSY;KBC,8666	U705
242600000145	LABEL;10*10,BLANK,COMMON	
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,80P,SMT	
316687100001	PCB;PWA-8666/M BD	R02
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	

Part Number	Description	Location(S)
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/PCB SMT,PRC	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
273000150352	CHOKE COIL;QXC24CD121U,120OHM/100MHZ,201	L703,L704,L705,L706
297120200002	DIP SW,4P,24VDC,25mA,SMT,FHDS-02F-T/R	SW701,SW702
271061564101	RES;560K ,1/16W,1% ,0402,SMT	PR33
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR726
286301410003	IC;CB1410B0,PCI/CARDBUS,LFBGA,144P,ENE	U715
331660020004	DIMM SOCKET;DDR SODIMM 200P, CA0075 STD	J719
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0115 RVS	J716
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW1,SW2
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R982,R983
274018000303	XTAL;8MHZ,30PPM,16PF,8*4.5,2P,SMT,eCERA	X702
274010800405	XTAL;8Mhz,30PPM,16PF,8*4.5,2P,SMT,TXC	
274011431449	XTAL;14.318MHZ,32PF,50PPM,8*4.5,2P	X703,X704
274011431414	XTAL;14.318MHZ,32PF,50PPM,8*4.5,2P	
272431154501	CAP;150U ,6V3 ,7343, T520V157M006ASE040 ,-/+20	C701,C758
343685200001	EMI FINGER;3X2MM,H2.5,SME-0025RA,U-TEK	TP10,TP38
342600002081	FINGER;EMI GROUNDING SMD FINGER H=7.0MM,S	TP40,TP41,TP42,TP717
271071221101	RES;220 ,1/16W,1% ,0603,SMT	R996
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	C519,C520
271071562101	RES;5.6K ,1/16W,1% ,0603,SMT	R926
331840010017	CON;STEREO JACK,10P,W/SPDIF,R/A,3-RD-1-A039	J704

9. Spare Part List - 11

Part Number	Description	Location(S)
273000500100	CHOKE COIL;0.47µH,20%,55A,3.5M	PL701
288204430002	TRANS;AO4430,N-MOS,18A,30V,7.5mOHM,SO8,AO	PU2,PU3,PU4
271061183102	RES;18K,1/16W,1%,0402,SMT	R340
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,FM-10B1P-07	MIC1
481687100001	F/W ASSY;SYS BIOS,8666	U16
242600000145	LABEL;10*10,BLANK,COMMON	
283468140001	IC;FLASH,512K*8,PLCC32,LPC,SST49LF040,SST	
283468180001	IC;FLASH,512K*8,LPC & FWH,SST49LF004B,PLCC32	
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,SMT	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
245600010007	FLOW CARD;M/B,WHITE	
242600000385	LABEL;27*10,LAN ID BAR CODE	
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANYO	PC705,PC706
331040004031	CON;USB,FM,H7.85,R/A,4P*1,020173MR004SXXXZ	J703
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MOLEX	
346686900006	INSULATOR;DDR,8066	
346686900007	INSULATOR;PCMCI,8066	
346687100001	INSULATOR;MB,8666	
345686900004	SPONGE;SPEAKER,LEFT,MB,8066	
331000000314	CON HOLDER;PCMCIA,R-BTN ,MPT,929100000241	J5
347210040012	GASKET;2,10,040,012,TennRich	

Part Number	Description	Location(S)
347207060007	GASKET;2,07,060,007,TennRich	
347205030025	GASKET;2,05,030,025,TennRich	
347210010010	GASKET;2,10,010,010,TennRich	
347210015020	GASKET;2,10,015,020	
345686900007	SPONGE;RTC,BATT,8066	
346684000014	INSULATOR;RJ11,BACK,8050M	
343686700001	HEATSINK;NORTH BRIDGE,CHEETAH	
347110003015	GASKET;1,10,003,015	
451687100091	HEATSINK ME KIT;8666	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
340686900017	HEATSINK ASSY;FORCECON,8066	
340686900006	HEATSINK ASSY;CPU,8066	
442686900002	BATT ASSY;11.1V,4.4AH,LI,3S2P,PANASONIC,8X66,MSL POWER	
441686900002	BATT ASSY;8066/11.1V,2200mH,PANASONICS,6CELL,PWR	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
225600000054	TAPE;INSULATING,POLYESTER FILM,17.5MM,130'C,PRC	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,UL,PRC	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242669600005	LABEL;LOT NUMBER,RACE	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=7,BLACK;PWR	
333025000005	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=13,BLACK;PWR	
338536010053	TF041-BATTERY;LI,3.6V/2.2AH,CGR18650C,PAN,PWR	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342683700006	CONTACT PLATE;W5L63T0.13mm,GE BATT,PWR	

9. Spare Part List - 12

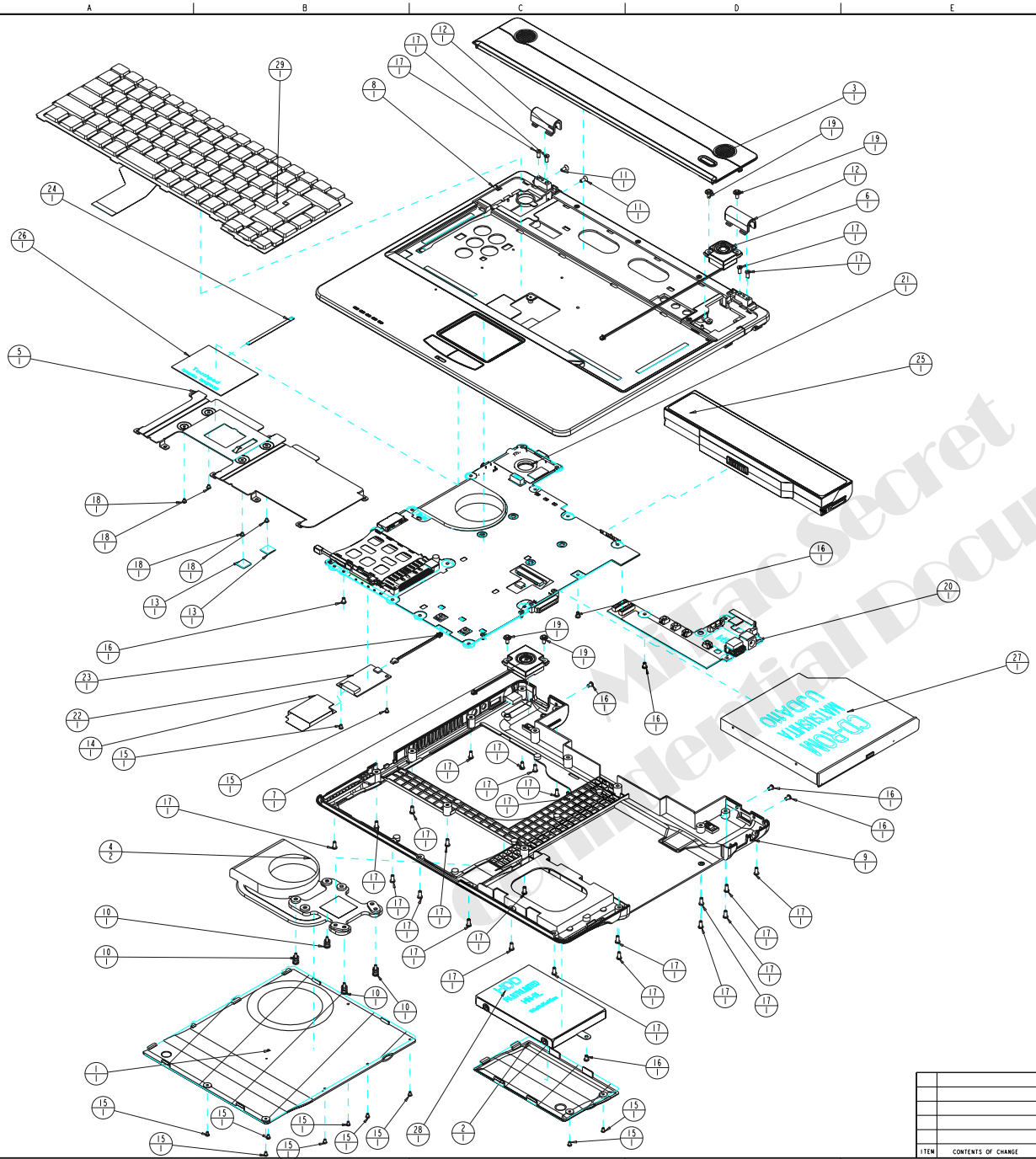
Part Number	Description	Location(S)
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BLAC,WEASEL	
346681800004	INSULATOR;BATT,ASSY,L129W15T0.25MM,8677C,PWR	
346686900012	INSULATOR;FIBRE,T=1.2mm,L=25mm,W=7.5mm,PWR	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDAIN	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
411686900009	PWA;PWA-8066/BATT PANASONICS CELLS,BOARD,PWR	
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C10345-10701	CON1
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*7MM,8175	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
335152000085	FUSE; 128 DC-7A/50V 139℃only UCHIHASHI（內橋	F2
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*8in,PRC	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14,N/C,TELECORE,PRC	
310111103027	THERMISTOR;10K,1%,RA,DISK,103AT-4,only 爲勤	RT1
411686900010	PWA;PWA-8066/BATT PANASONICS CELLS,GAUGE BD,SMT,PWR	
271044100101	RES;0.010,1.5W, 1%,2512,SMT;PWR	R6
271045507103	RES;0.050,1W, 1%,2512,SMT, only KOA;PWR	R24,R24A,R24C
271071000002	RES;0 ,1/16W,5% ,0603,SMT	C16,R31
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R14,R15,R16,R20,R21
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R5,R7,R8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R18,R22,R23,R9
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R10,R3
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R1A,R1B

Part Number	Description	Location(S)
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R17B
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071331301	RES;330 ,1/16W,5% ,0603,SMT	C14
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R17A
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V SMT only TDK	C14A,C14B,C4A,C4B
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R SMT only TDK	C13
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R SMT only TDK	C10,C11,C12,C15,C3,C5,C6,C7,C8
272075223702	CAP; 0.22U CR 50V +80-20% 0603 Y5V SMT only TI	C1,C2,C20A,C24,C25
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7R SMT only TDK	C4
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SMT	IC2
283467530001	IC;EEPROM,S24CC02A,2K,SO8,SMT,ONLY SEIKO;PWR	
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC1
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	IC3
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PRC	IC4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	ZD3,ZD4
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SMT	D2
288111544001	DIODE; 1SR-154-400 400V 1.0A SMT	D1
288200144008	TRANS;DTA144EKA,PNP,SMT	Q1
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323,SMT	D3
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,PWR	Q3,Q5
316687600003	PCB;PWA-8965-8066/BATTERY BD,PWR	R0A
332110020195	WIRE;#20,UL1007,125MM,BLACK,PWR	CN5
332110026133	WIRE;#26,UL1007,93MM,YELLOW,YIYI,PRC,PWR	CN2
332110026135	WIRE;#26,UL1007,40MM,ORANGE,PRC,PWR	CN3
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,7368	

9. Spare Part List - 13

Part Number	Description	Location(S)
344686900001	COVER;BATTERY,8066	
344686900002	HOUSING;BATTERY,8066	
342686900010	CONTACT PLATE;T=0.13mm,L=85mm,PWR	
346686900015	INSULATOR;FIBER,T=0.25mm,107*12,PCB,PWR	
242686900001	LABEL;BATT,11.1V/4.4AH,LI,PANASONIC,8066	
342503200004	CONTACT PLATE;W4L63T0.15,1/4,T TAPE,7521/GRAMPUS	
346684400004	INSULATOR;FIBER,UL94V-0,2CELL,D=18mm,T=0.25mm,ADHESIVE W204,PWR	
442681400051	AC ADPT ASSY;19V,3.43A,HIPRO HP-OK065B03 BLACK,Calypso	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERICA	
523468710001	DVD COMBO ASSY; UJ-DA760,8X24X24X24X, PANASONIC,8666	
451686900061	ODD ME KIT;8066	
342672200010	BRACKET;CD-ROM,8500	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NLK	
523410484014	DVD COMBO DRIVE; UJ-DA760,8X24X24X24X, PANASONIC	
340683400010	BEZEL ASSY;COMBO,MKE,730,8050F	
373101713502	T-SCREW;B.M1.7L3.5,HD04t0.25,0,BCT	
531068540011	KBD;88,UI,K011718M5,JME,BLACK,8011	
461686900001	PACKING KIT;NORMAL,8066	
221686920001	CARTON;NON-BRAND,8066	
222670820003	PE BAG;L560*W345,7521N	
222682800001	PROTECTION PAPER;LCD/KB,BEN Q,8089P	
224682800001	PALLET;COMPLEX,1200*1000*126,8089P	
227686900002	END CAP;L/R,NORMAL,8066	
242600000157	LABEL;BAR CODE,125*65,COMMON	
221682850003	CARD BOARD;TOP/BTM,PALLET,BEN Q,8089P	

Part Number	Description	Location(S)
221682850007	CARD BOARD;FRAME,PALLET,BEN Q,8089P	
221686950001	CARD BOARD;PARTITION,PALLET,8066	
541668690001	AK;N-B,8066	
221682840001	AK BOX;BEN Q,8089P	
222672730001	PE BUBBLE BAG;200*240mm,AMM-9019	
221682850006	PARTITION;BEN Q,AK BOX,8089P	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222682800002	PE BAG;302*208MM,BEN Q,8089P	
242669900009	LABEL;BLANK,60*80MM,7170	
451686900001	LABEL KIT;N-B,8066	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8640C	
242686900002	LABEL;N-B,RATING,8066	
		P/N:526268710001



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340686900002	COVER ASSY,CUP,8066	1	ASSEMBLY	
2	340686900003	COVER ASSY,HDD,8066	1	ASSEMBLY	
3	340686900004	COVER ASSY-KB-8066	1	ASSEMBLY	
4	340686900006	HEATSINK ASSY;CPU,8066	2	ASSEMBLY	
5	340686900009	SHIELDING ASSY;COVER,8066	1	ASSEMBLY	
6	340686900010	SPEAKER ASSY;R,8066	1	ASSEMBLY	
7	340686900011	SPEAKER ASSY;L,8066	1	ASSEMBLY	
8	340687100001	COVER ASSY;8666	1	ASSEMBLY	
9	340687100002	HOUSING ASSY,8066	1	ASSEMBLY	
10	341677000002	SPRING-SCREW-HEATSINK-LYNX	4	PART	
11	341680900001	SPC SCREW;#4-1/4,8050	2	PART	
12	344686900006	COVER;HINGE,8066	2	PART	
13	345686300002	SPONGE;HDD,8050FX	2	PART	
14	346670500014	INSULATOR;MDC,TETRA	1	PART	
15	370102030301	SPC-SCREW; M2L3,K-HEAD,I,NIB,NLK	11	PART	
16	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	7	PART	
17	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	26	PART	
18	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	4	PART	
19	371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	4	PART	
20	411686900004	DB ASSY;8066	1	ASSEMBLY	
21	411687100001	MB ASSY;8666	1	ASSEMBLY	
22	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
23	422674300071	WIRE ASSY;MDC,E-NOTE	1	ASSEMBLY	
24	422686900001	CABLE FFC;TP,8066	1	PART	
25	441686900002	BATT ASSY-8066	1	ASSEMBLY	
26	442680900051	TOUCH PAD;SYNATICS,TM42P-313	1	PART	
27	451680900038	COMBO MEKIT;QSI,SBW242,8050	1	ASSEMBLY	
28	451686900071	HDD;MEKIT,8066	1	ASSEMBLY	
29	531020237661	KBD;89,US,K0117I8MI,LYNX	1	PART	

ITEM	CONTENTS OF CHANGE	BVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL: RANGE	Pla	Met	Tes	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	19-Oct-04	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.50	DRAWING NAME	HOUSING KIT;8666		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 451 6871 00001 R 00		

MiTAC Technology Corp.

model name:8666-STRU

file name:8666-STRU-EXP

SHEET NO. 1 of 1

8666 R00

PROJECT CODE G175
PRODUCT CODE 6871

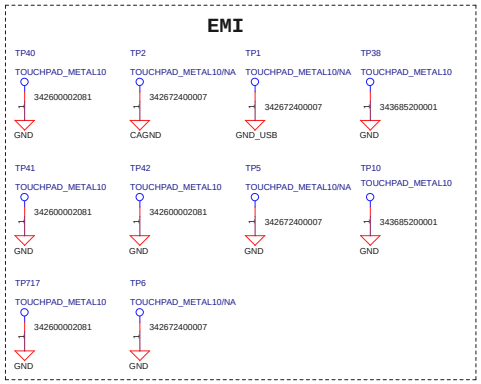
PCB P/N 316687100001
ASSY P/N 411687100001

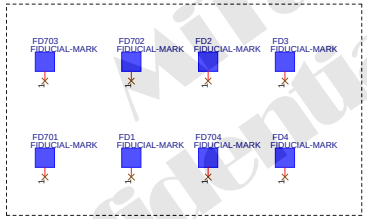
PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
CARDBUS	PCI_INTB#	PCI_REQ0# / PCI_GNT0#	AD20
MINIPCI	PCI_INTD#	PCI_REQ2# / PCI_GNT2#	AD17

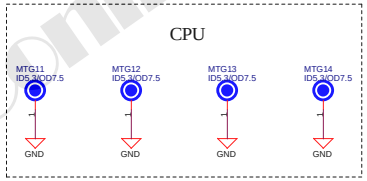
POWER STATUS

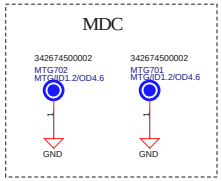
S0/S1	S3	S4	S5	POWER	NOTE
V	V	V	V	DVMAIN(19V)	
V	V	V	V	VDD3	
V	V	V	V	VDD3S	
V	V	V	V	VDD3_AVREF	
V	V	V	V	VDD5	
V	V			+2.5VS_DDR	
V	V			+5VS	
V	V			+3VS	
V	V			+1.5VS	
V				+5V	
V				+3V	
V				+1.25V_DDR	
V				+2.5V	
V				+1.8V	
V				+1.5V	
V				+VCCP(+1.05V)	
V				+VCCQ(+1.05V)	
V				+VCCA(+1.8V)	
V				+VCC_CORE	

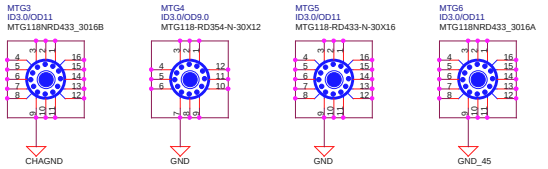
REVISION	TAPEOUT DAY	HISTORY
R00	2004/10/14	Initial Release.
R0A		
R01		

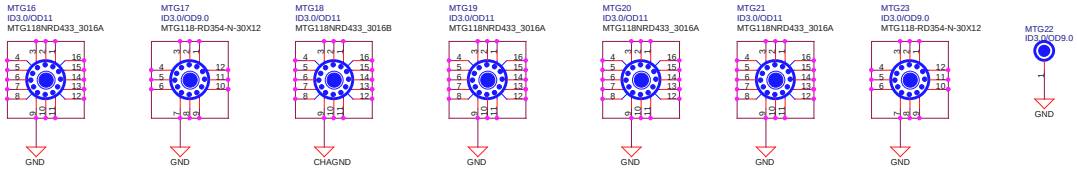












PCB STACK 1.2mm

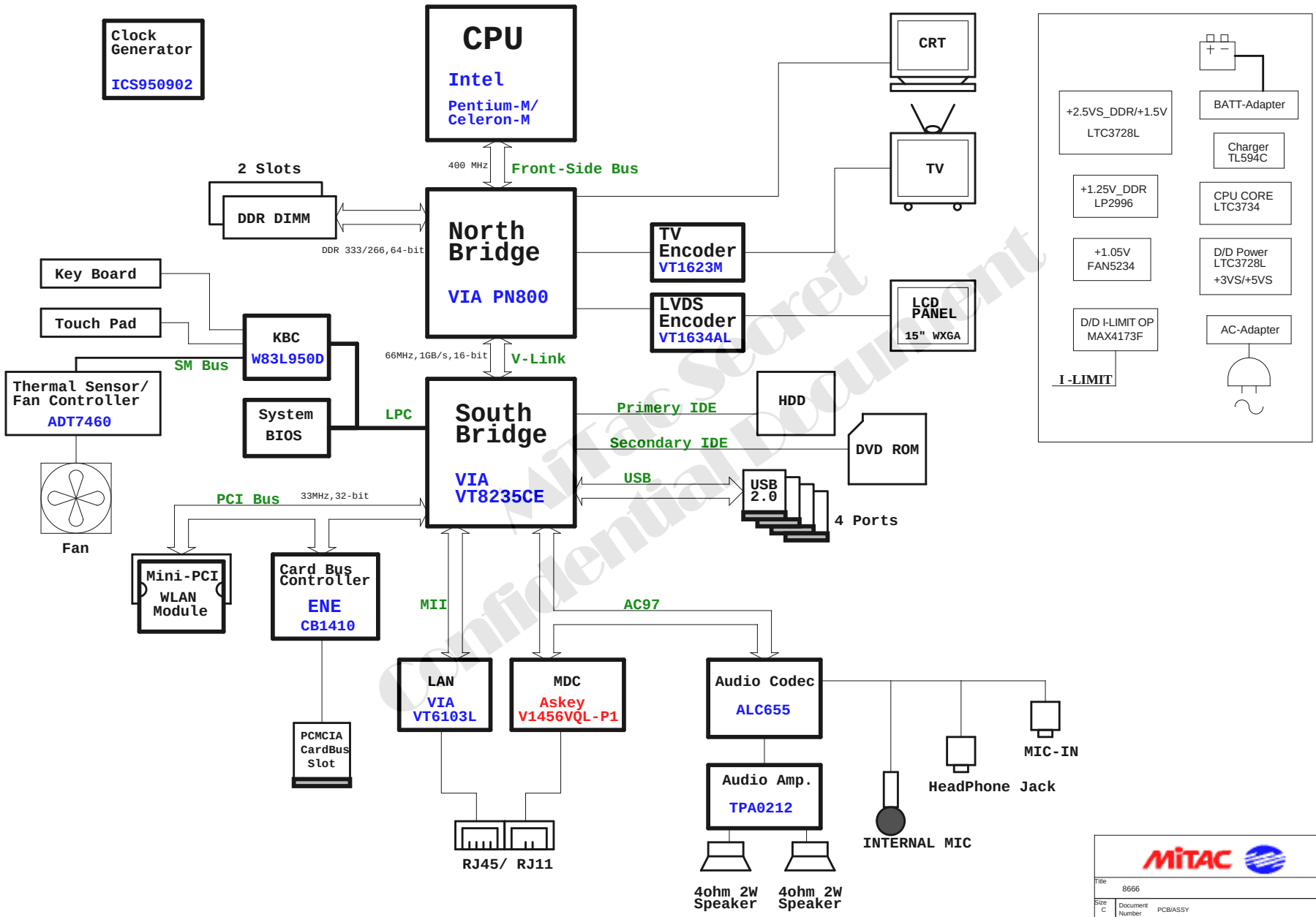
	Component side	layer 1: 1/2 oz
4 mil		
	Ground 1	layer 2: 1/2 oz
6 mil		
	Signal layer (IN1)	layer 3: 1/2 oz
7 mil		
	Signal layer (IN2)	layer 4: 1/2 oz
6 mil		
	Power layer	layer 5: 1/2 oz
7 mil		
	Signal layer (IN3)	layer 6: 1/2 oz
6 mil		
	Ground 2	layer 7: 1/2 oz
4 mil		
	Solder side	layer 8: 1/2 oz

DRAWN	DESIGN	CHECK	ISSUES

MiTAC

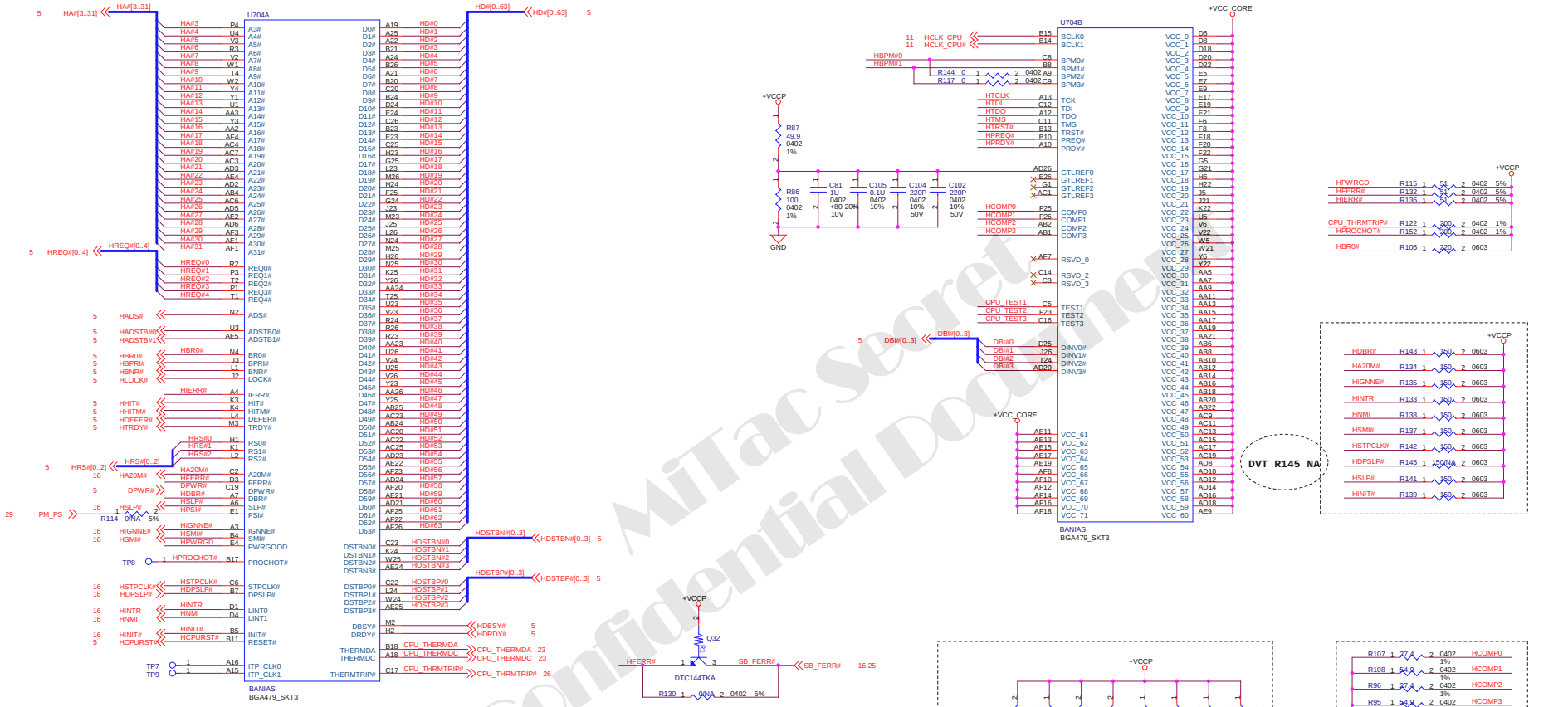
Title: 8666
Size: C | Document Number: PCB/ASSY | Rev: R00
Date: Monday, December 13, 2004 | Sheet 1 of 31

8666 SYSTEM BLOCK DIAGRAM



VCC : PROCESSOR CORE POWER SUPPLY.
VCCA : ISOLATE POWER FOR INTERNAL PLL.
VCCP : PROCESSOR I/O POWER SUPPLY.
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.

CPU-BANIAS (1/2)

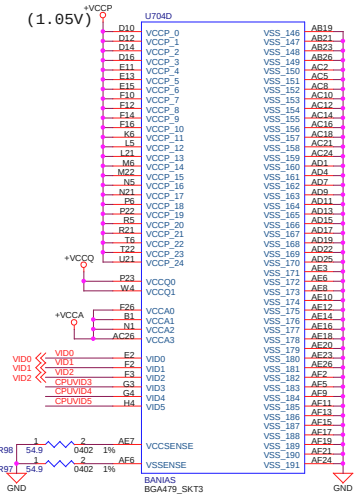


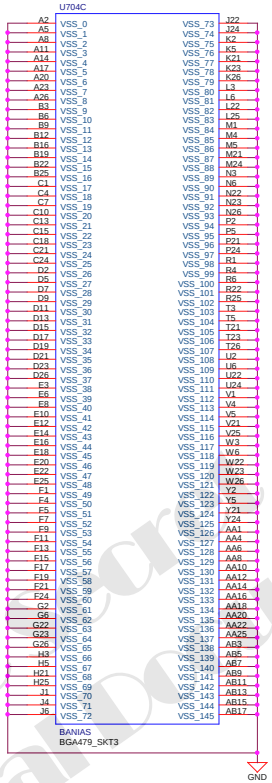
VCCA	Version	SW701
1.5V	Dothan A2 533MHz ES Dothan B 533MHz	Pin3 --> OFF Pin4 --> ON
1.8V	Before Dothan A2 533MHz ES	Pin3 --> ON Pin4 --> OFF

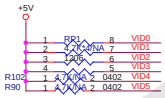
MiTAC

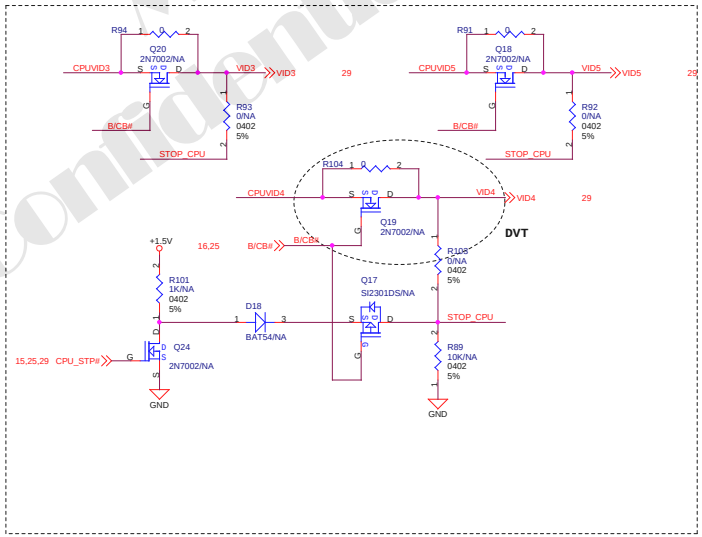
Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 3 of 31	

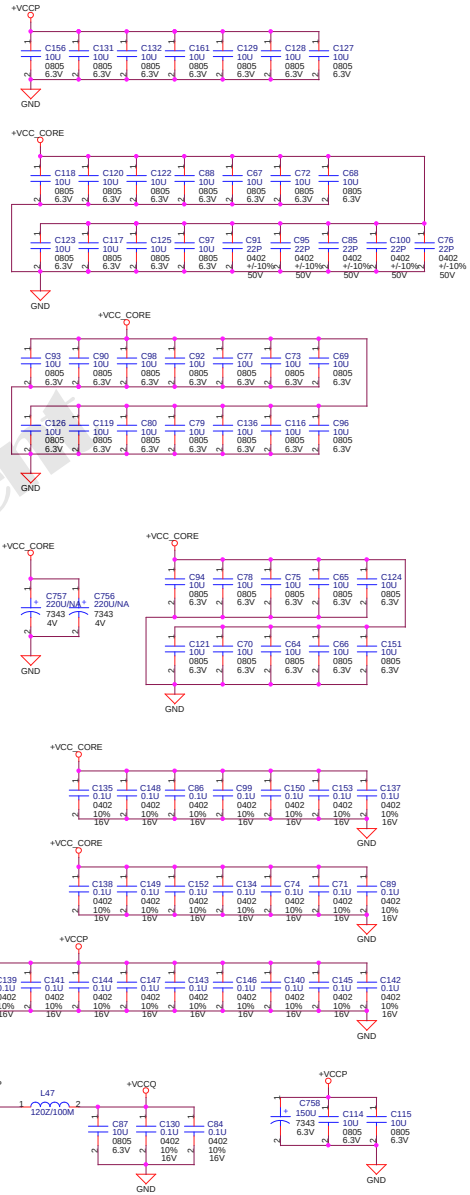
CPU-BANIAS (2/2)











VID						
5	4	3	2	1	0	VCC-Core
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212

VID						
5	4	3	2	1	0	VCC-Core
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

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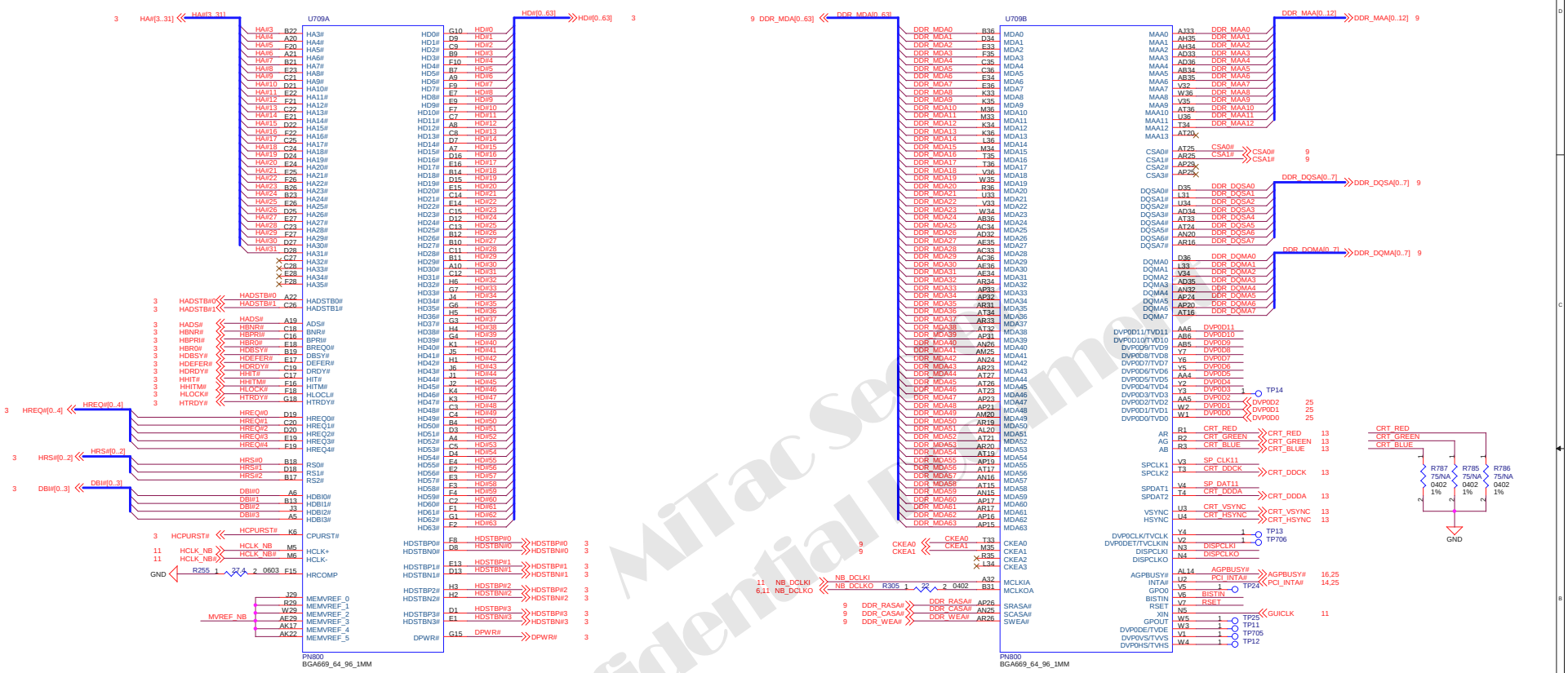
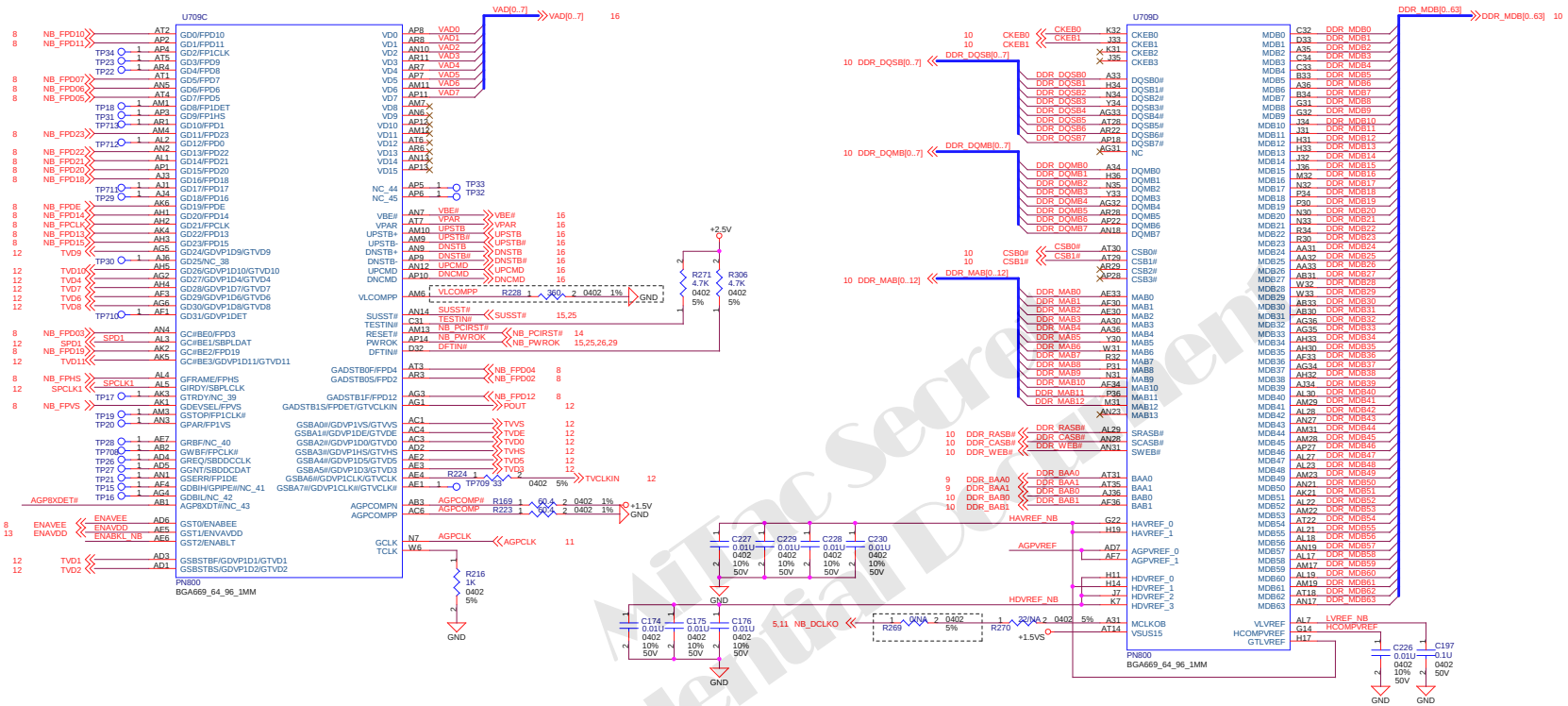
Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 4 of 31	

NB VIA PN800 (1/3)



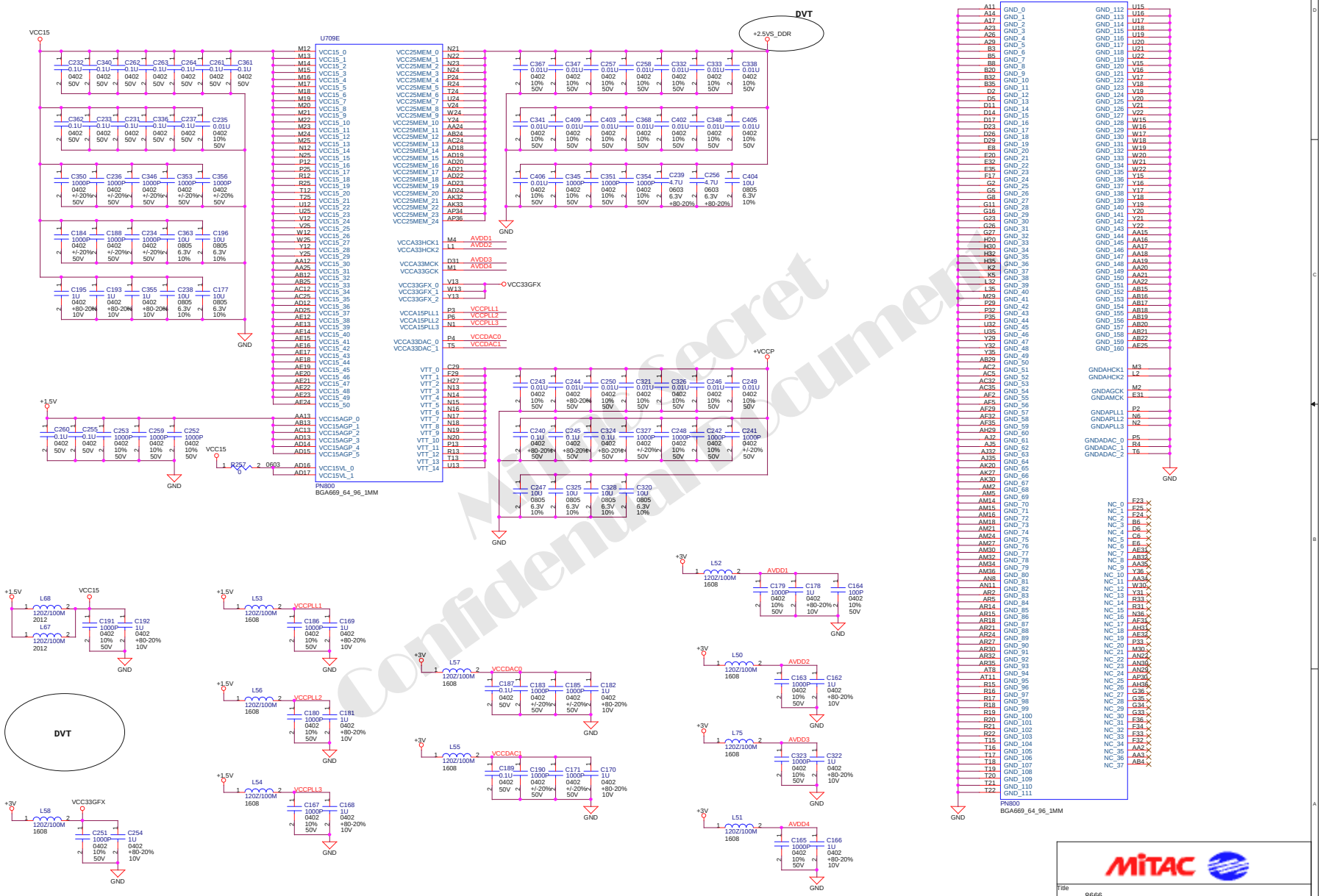
NB VIA PN800 (2/3)



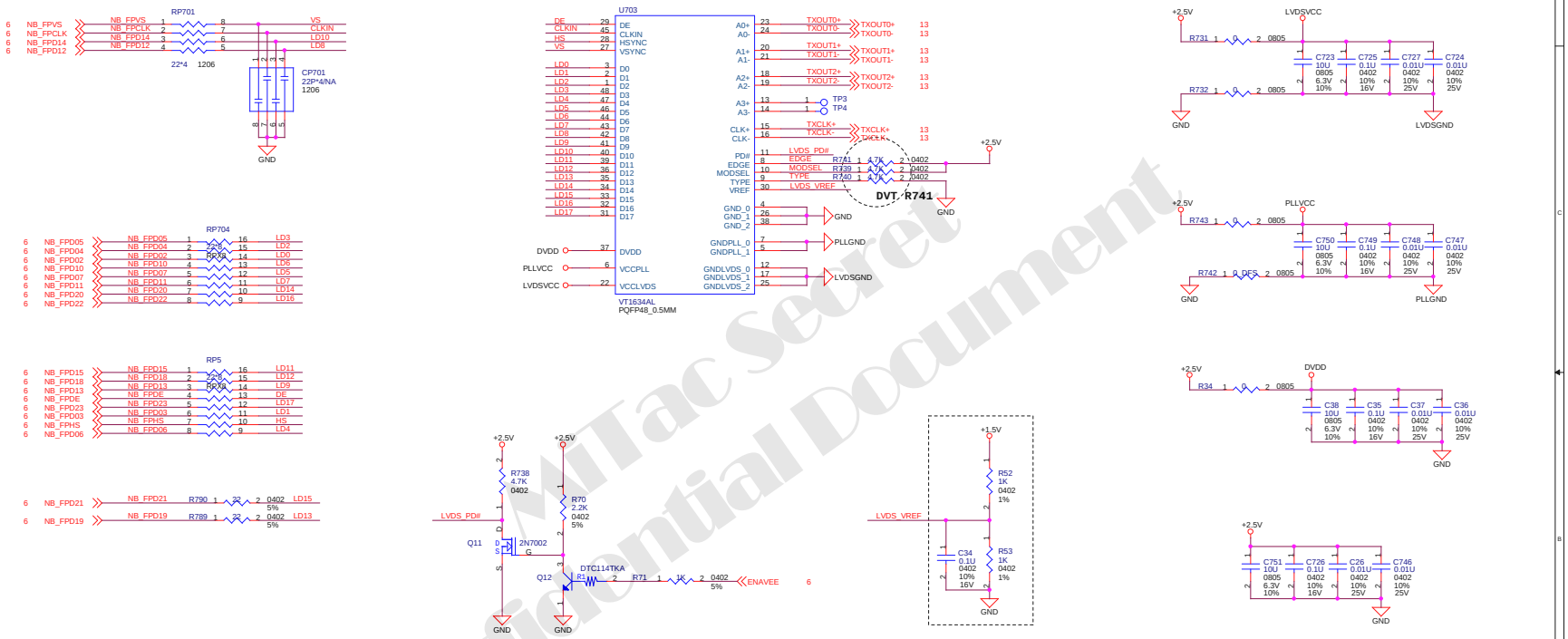
MiTAC

Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 6 of 31	

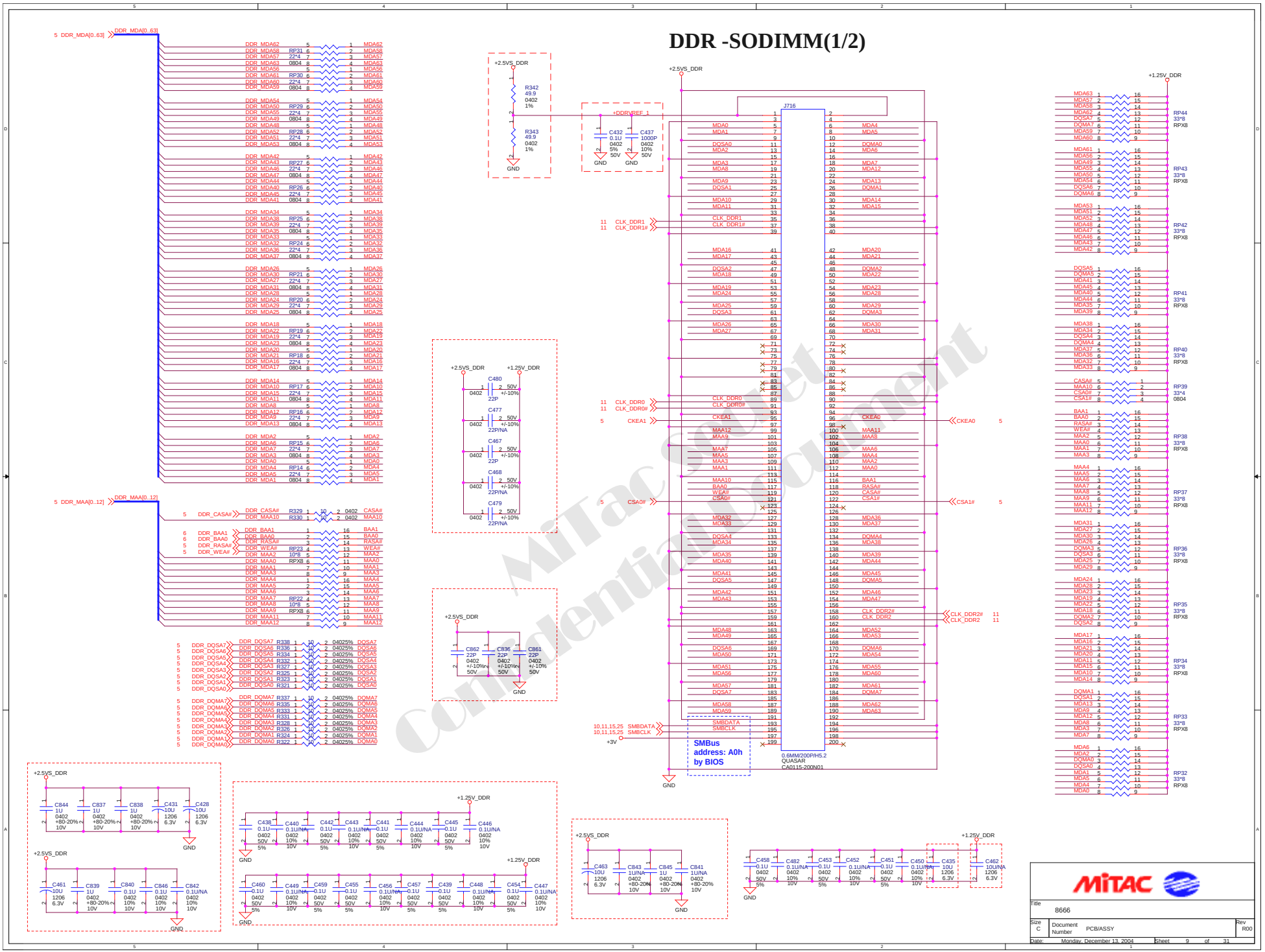
NB VIA PN800 (3/3)



LVDS TRANSMITTER(VT1634AL)

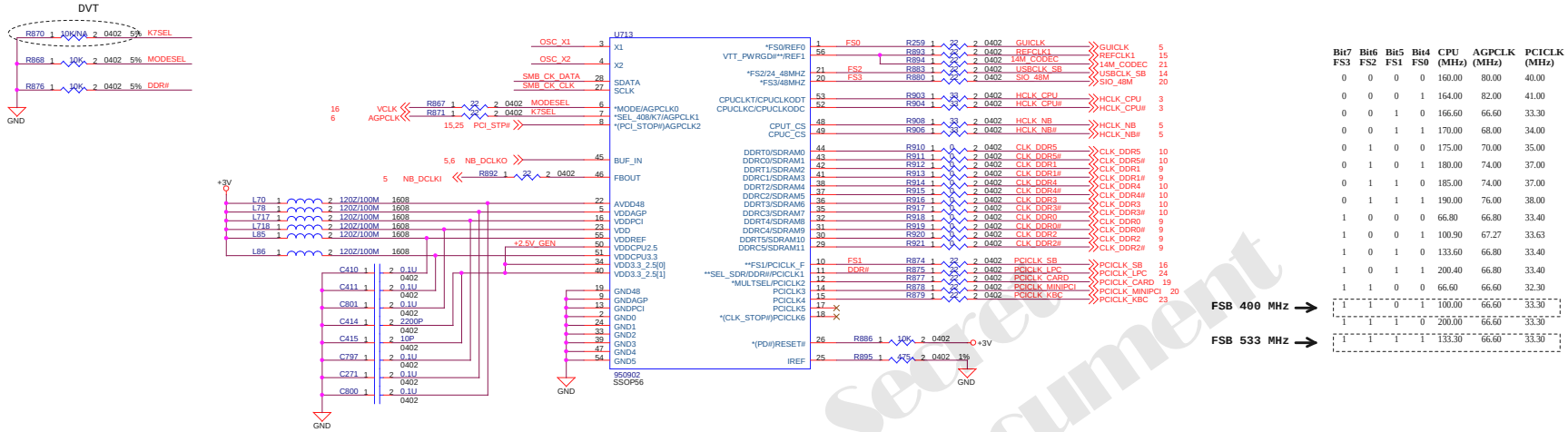


Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 8 of 31	



DDR -SODIMM(2/2)

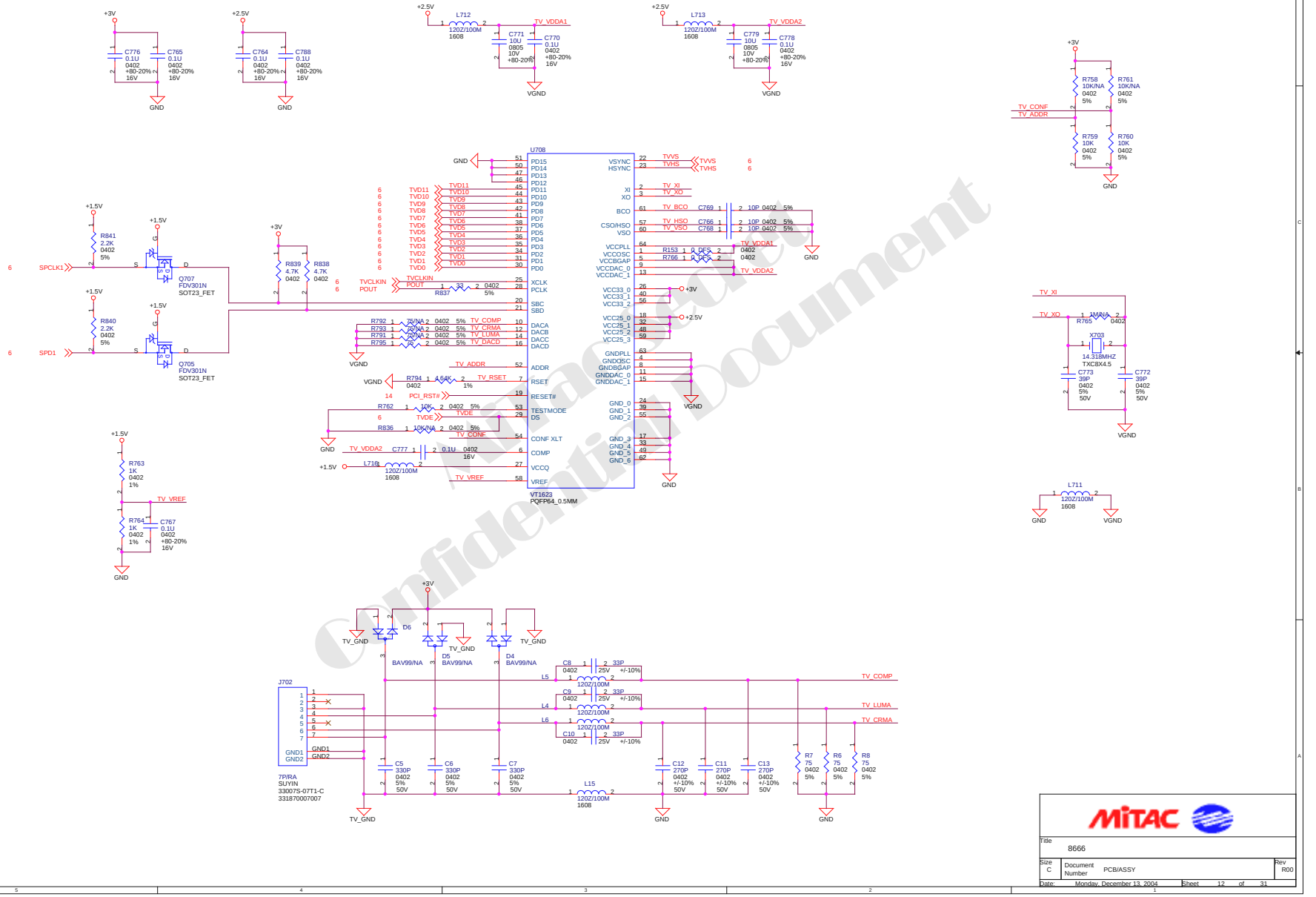
CLOCK SYNTHERIZER



Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU (MHz)	AGPCLK (MHz)	PCICLK (MHz)
0	0	0	0	160.00	80.00	40.00
0	0	0	1	164.00	82.00	41.00
0	0	1	0	166.60	66.60	33.30
0	0	1	1	170.00	68.00	34.00
0	1	0	0	175.00	70.00	35.00
0	1	0	1	180.00	74.00	37.00
0	1	1	0	185.00	74.00	37.00
0	1	1	1	190.00	76.00	38.00
1	0	0	0	66.80	66.80	33.40
1	0	0	1	100.90	67.27	33.63
1	0	1	0	133.60	66.80	33.40
1	0	1	1	200.40	66.80	33.40
1	1	0	0	66.60	66.60	32.30
1	1	0	1	100.00	66.60	33.30
1	1	1	0	200.00	66.60	33.30
1	1	1	1	133.30	66.60	33.30

Title	8666
Size	C
Document Number	PCB/ASSY
Rev	R00
Date:	Monday, December 13, 2004
Sheet	11 of 31

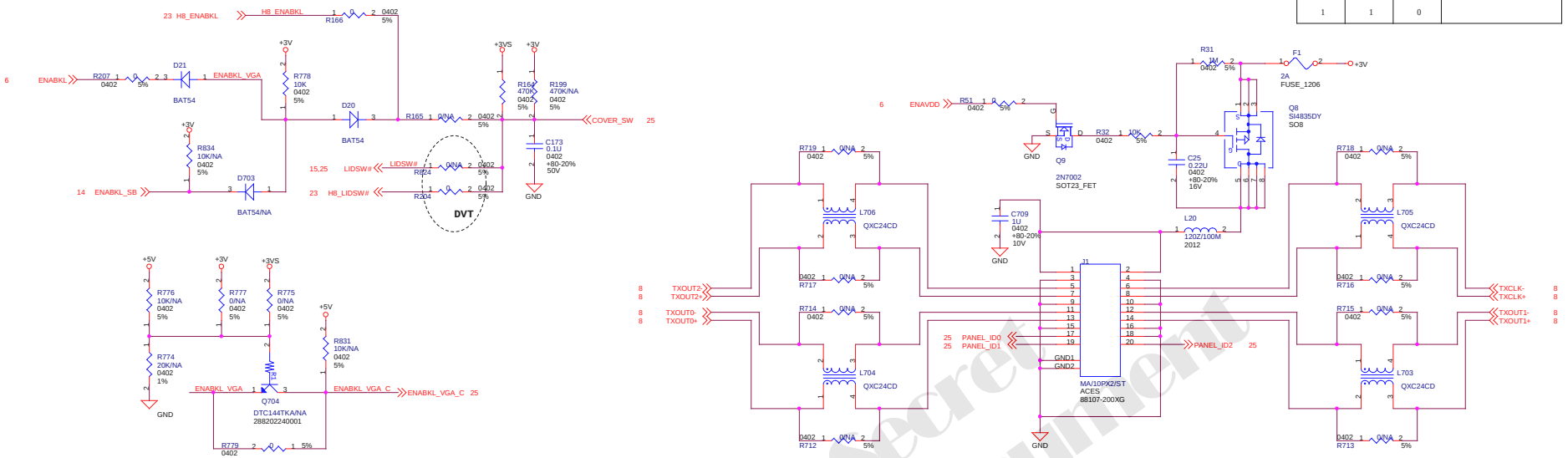
TV ENCODER (VT1623M)



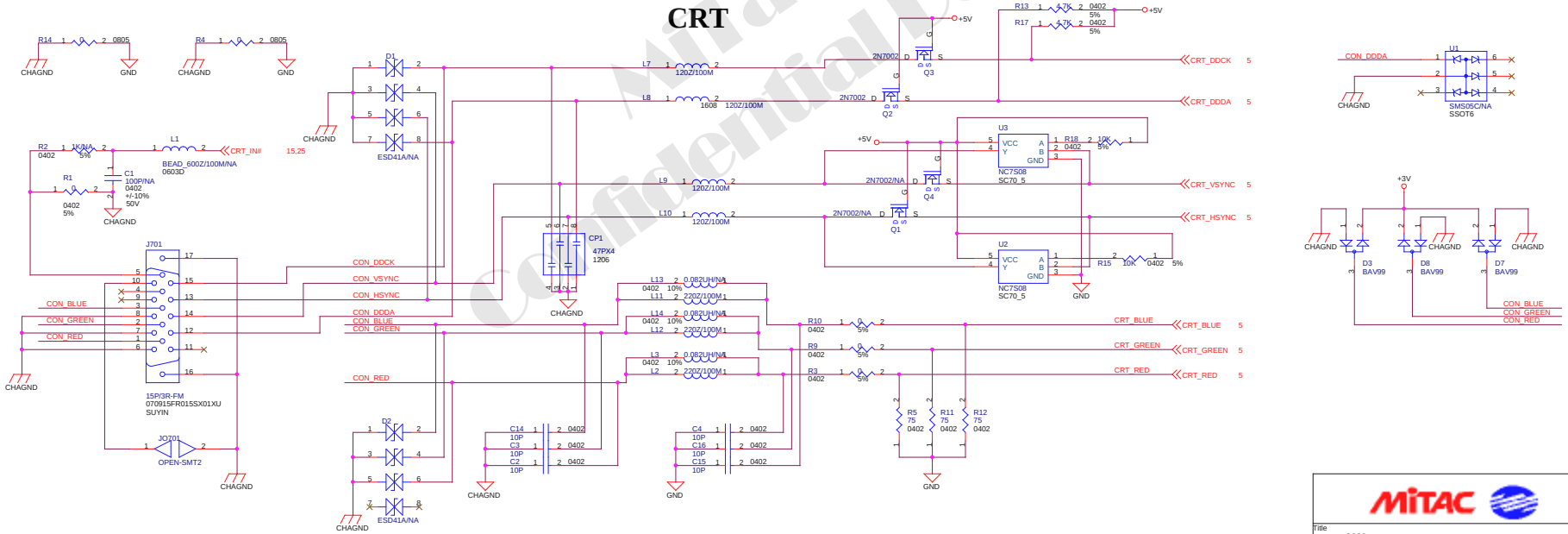
Display (CRT / LCD)

Pannel ID

LCD_ID0	LCD_ID1	LCD_ID2	PANEL TYPE
0	0	1	
1	0	1	
0	1	1	
0	1	0	
1	1	0	

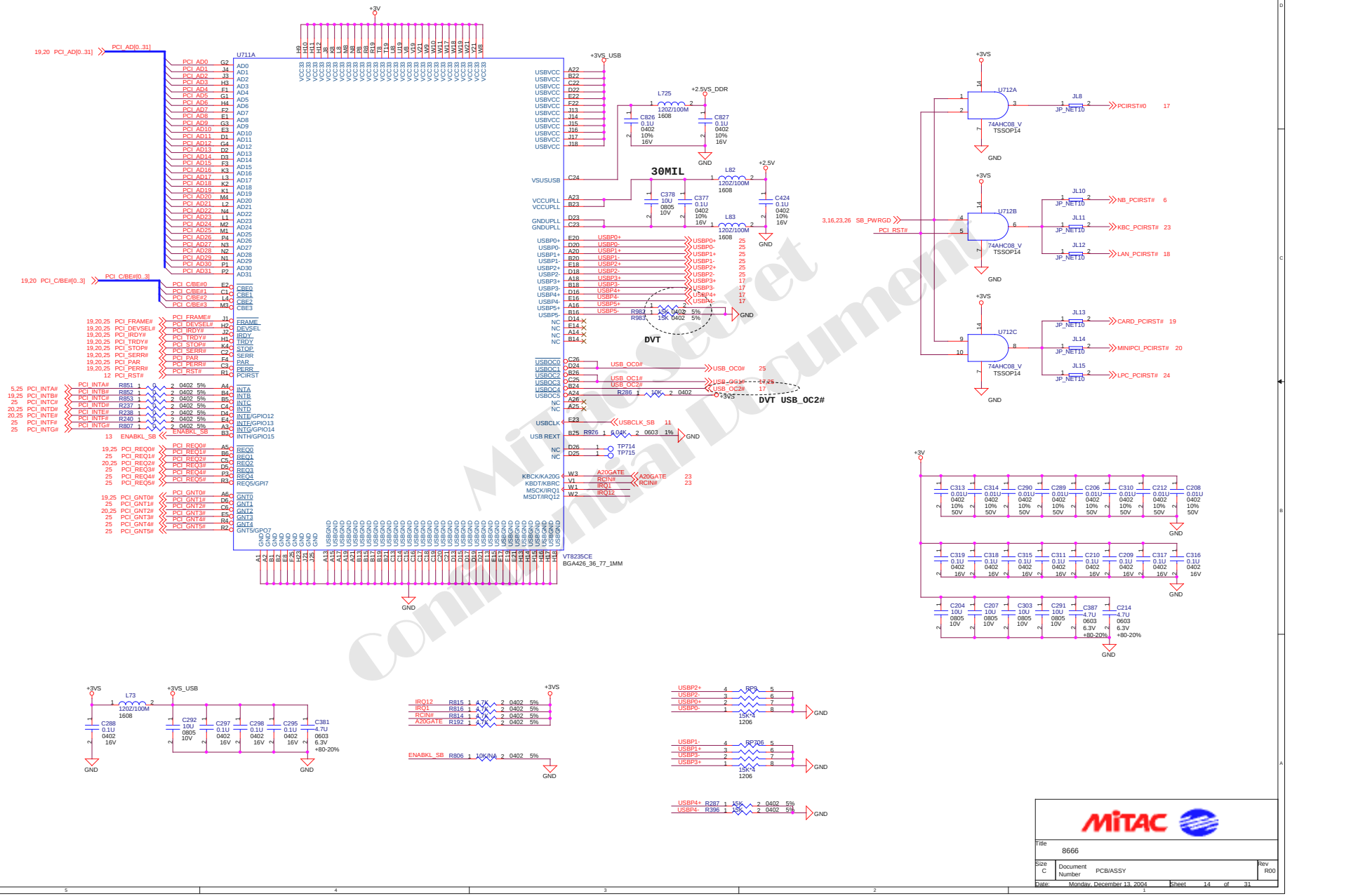


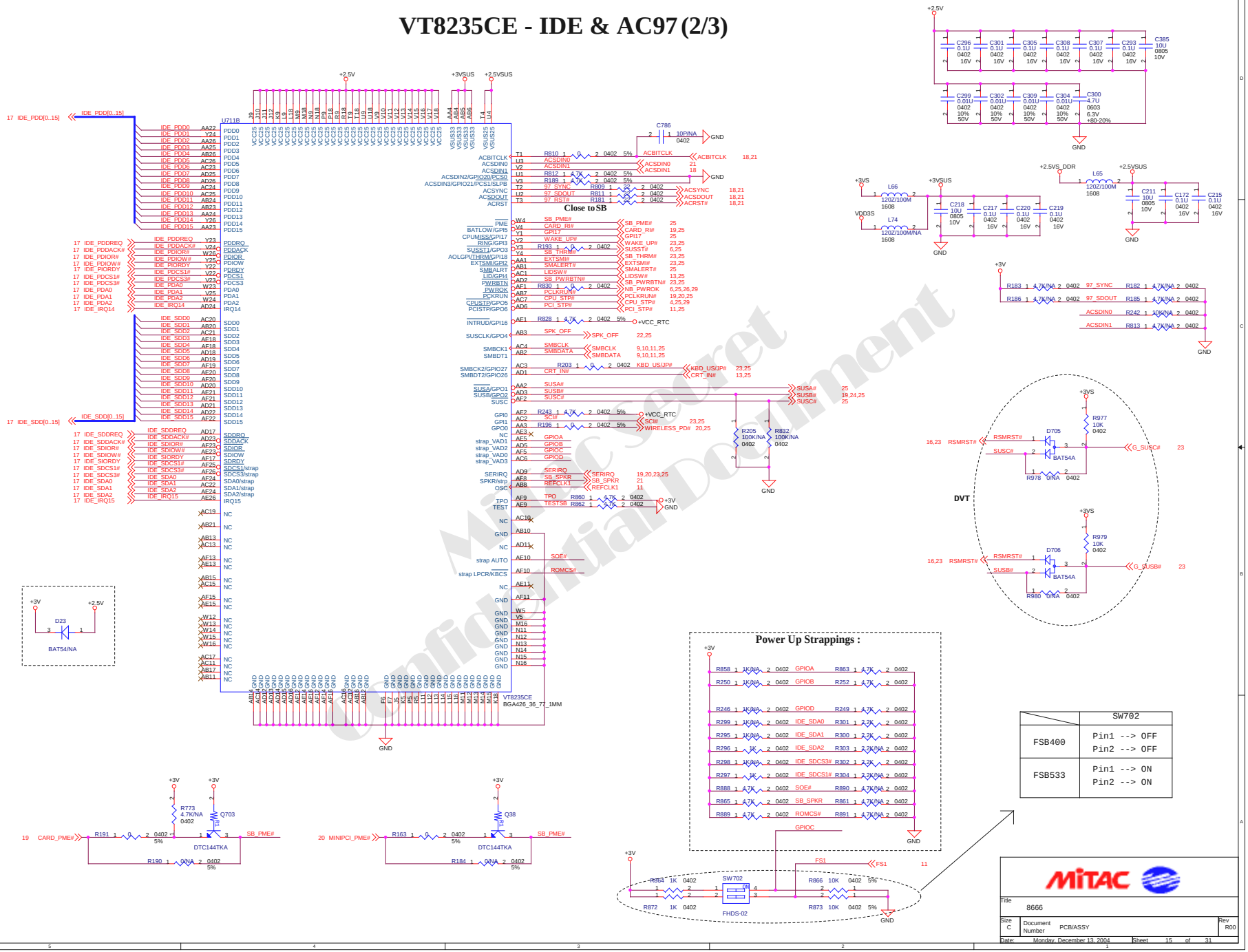
CRT



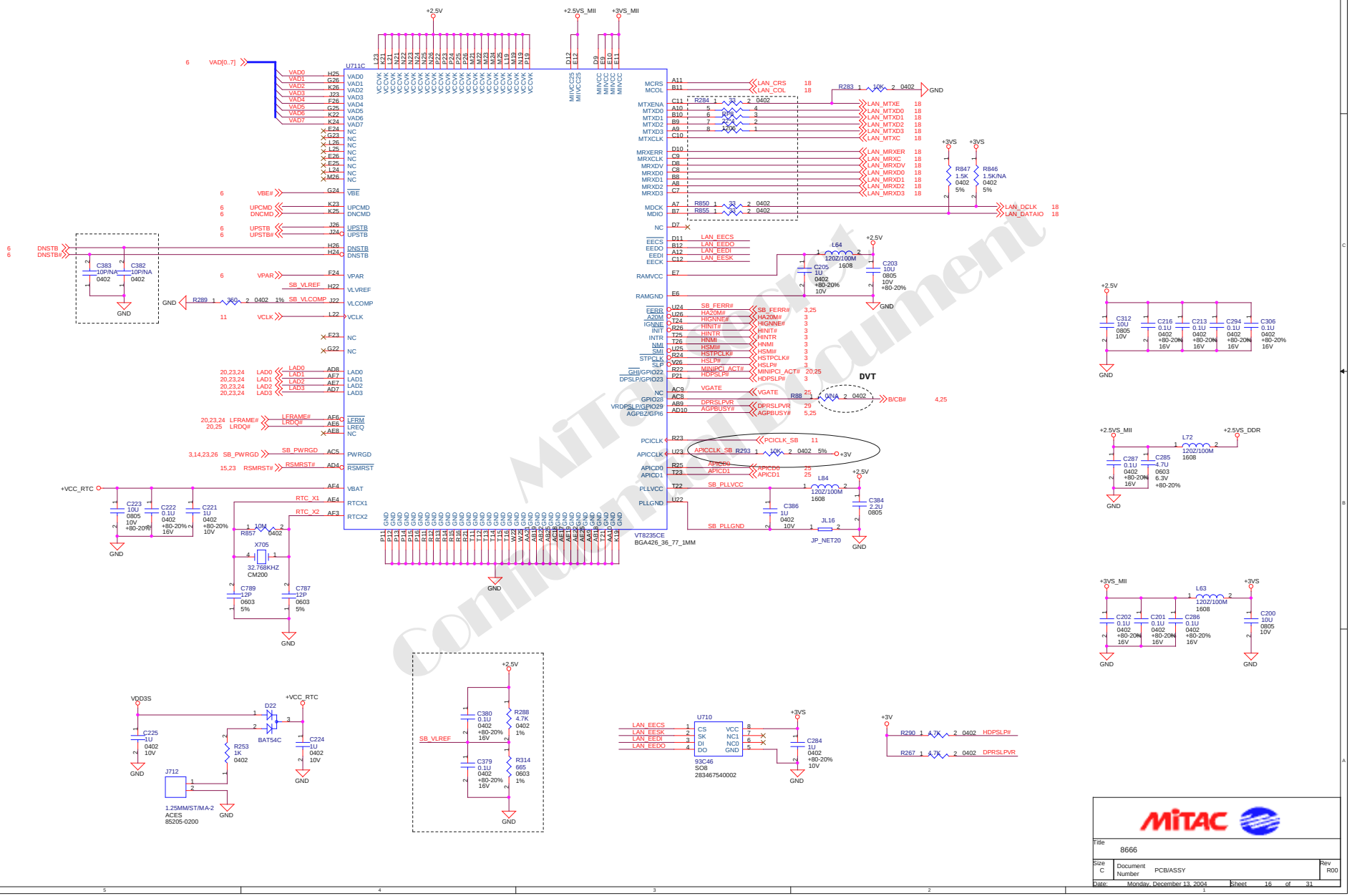
Title	8666		
Size C	Document Number PCB/ASSY		Rev R00
Date: Monday, December 13, 2004	Sheet 13	of 31	

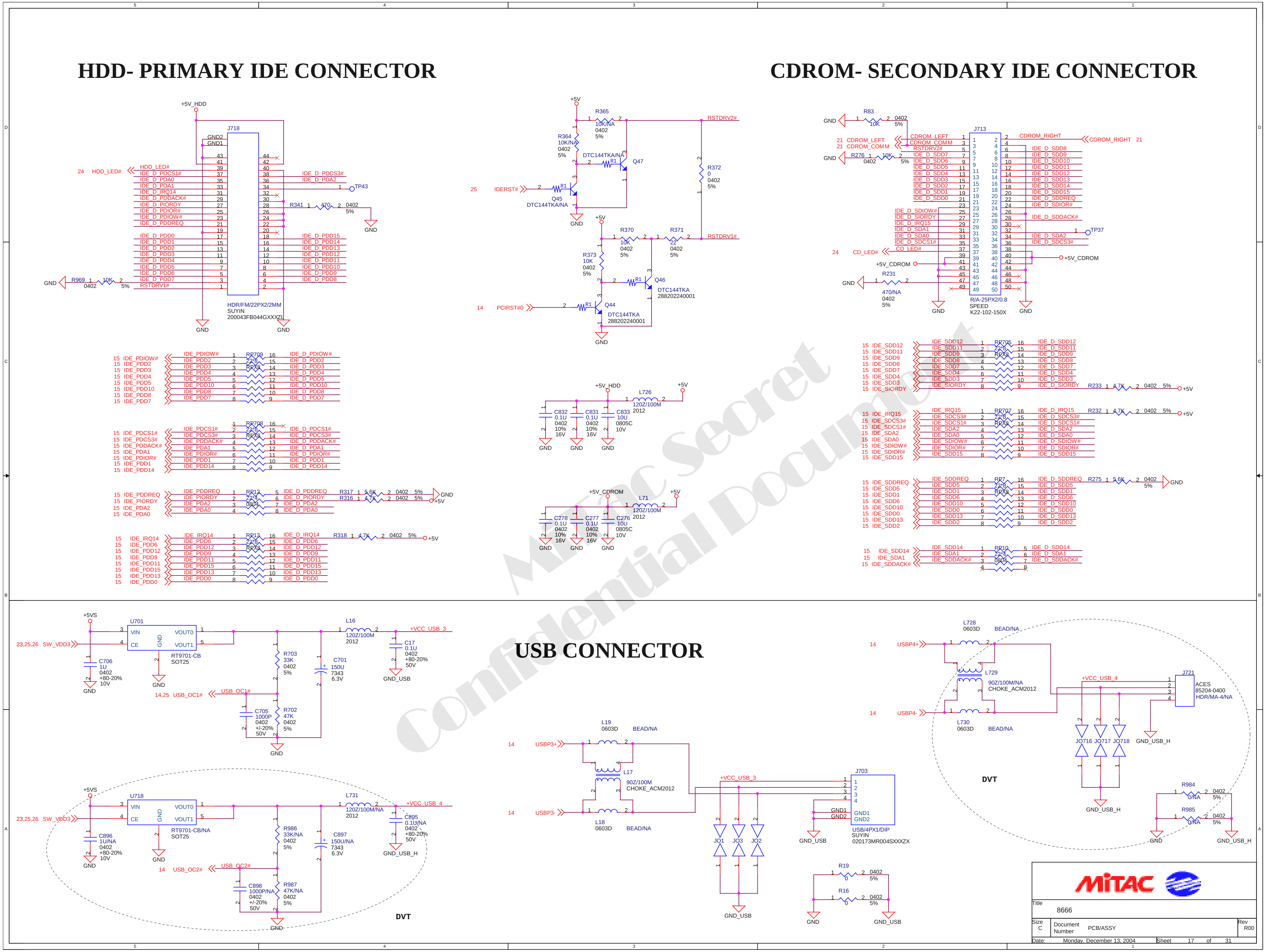
VT8235CE - PCI & USB (1/3)



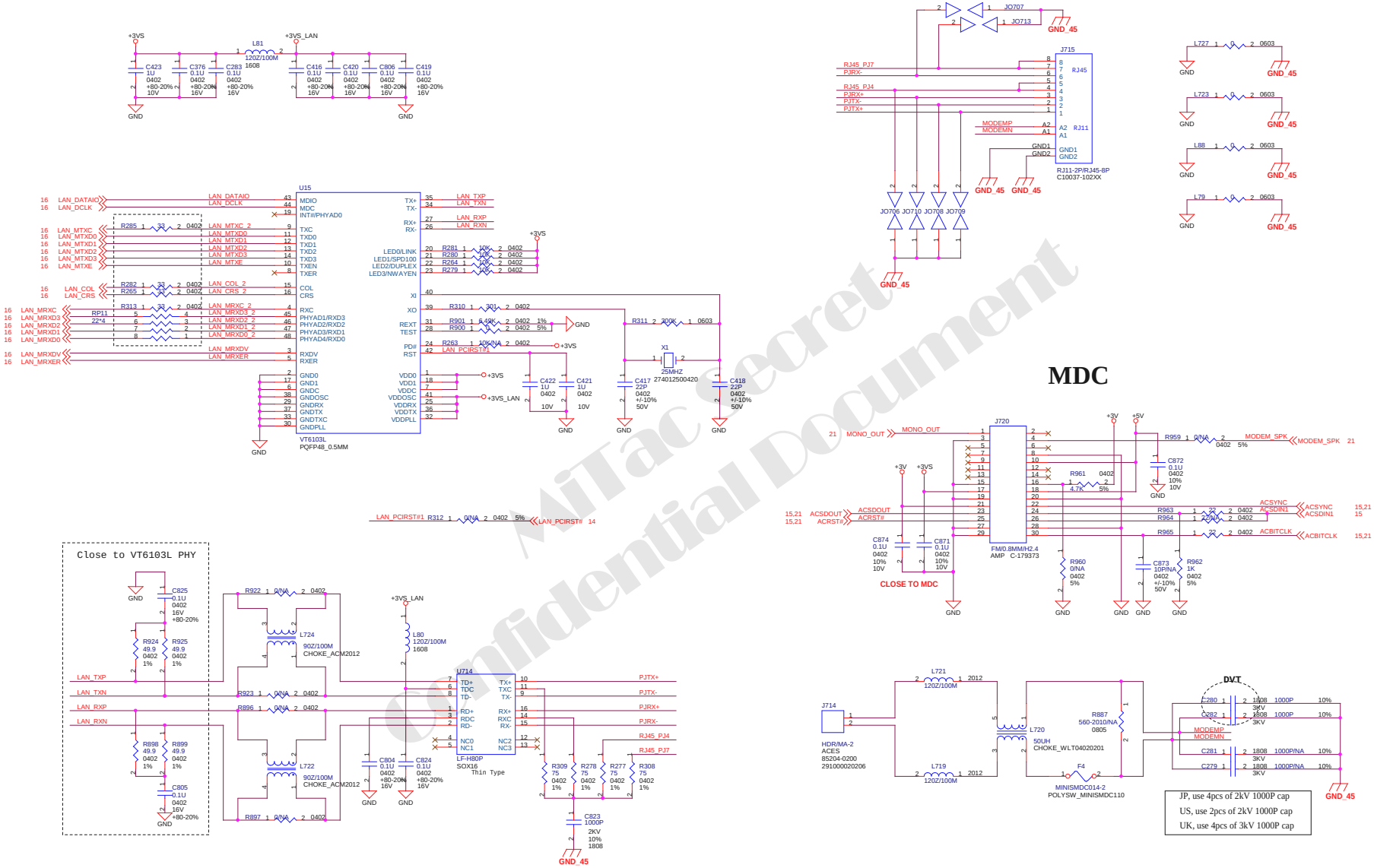


VT8235CE - VLINK & LAN (3/3)





LAN PHY(VT6103L)&MDC

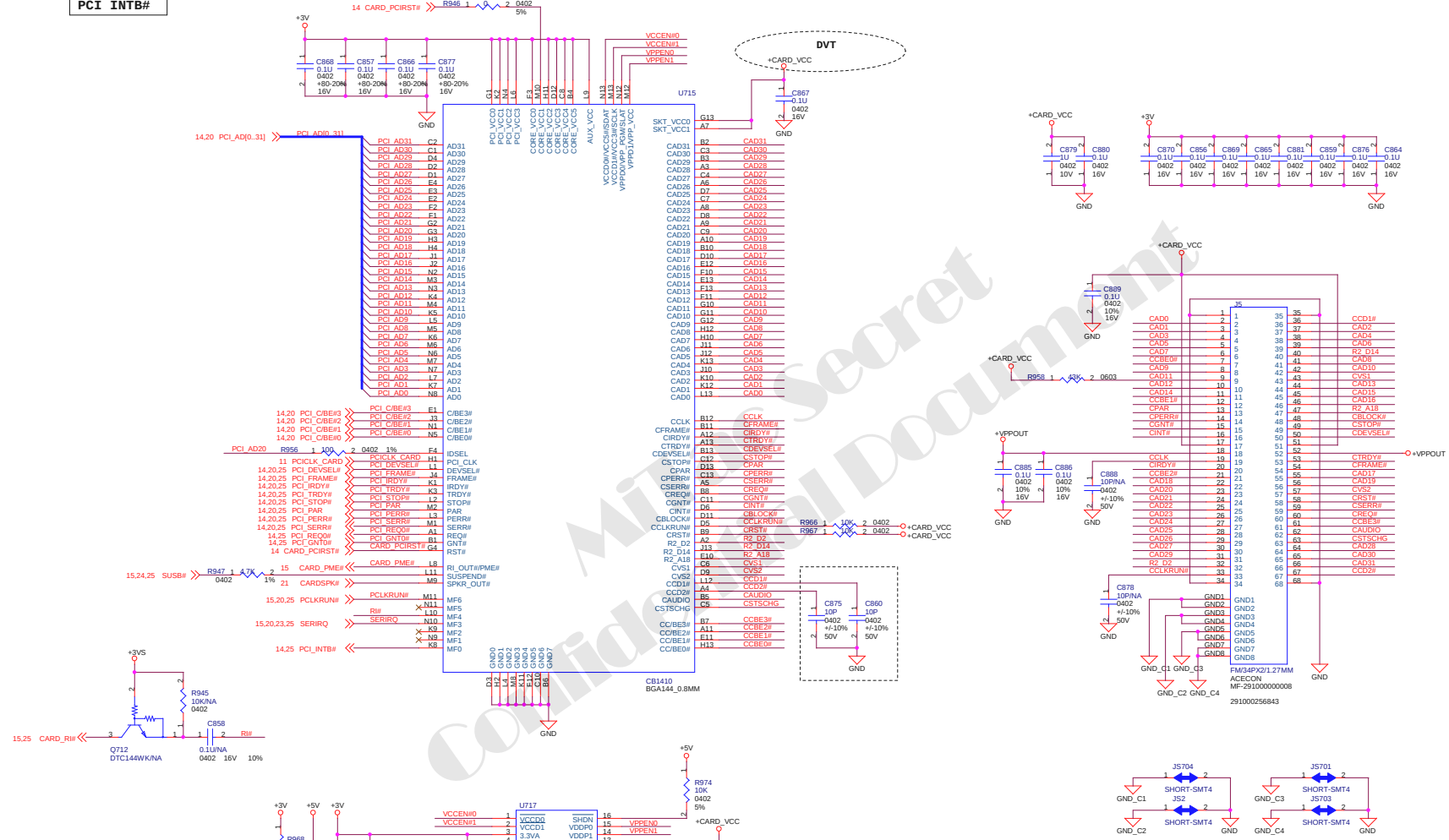


Title	8666
Size	C
Document Number	PCB/ASSY
Rev	R00
Date	Monday, December 13, 2004
Sheet	18 of 31

PCMCIA(ENE CB1410)

CB1410

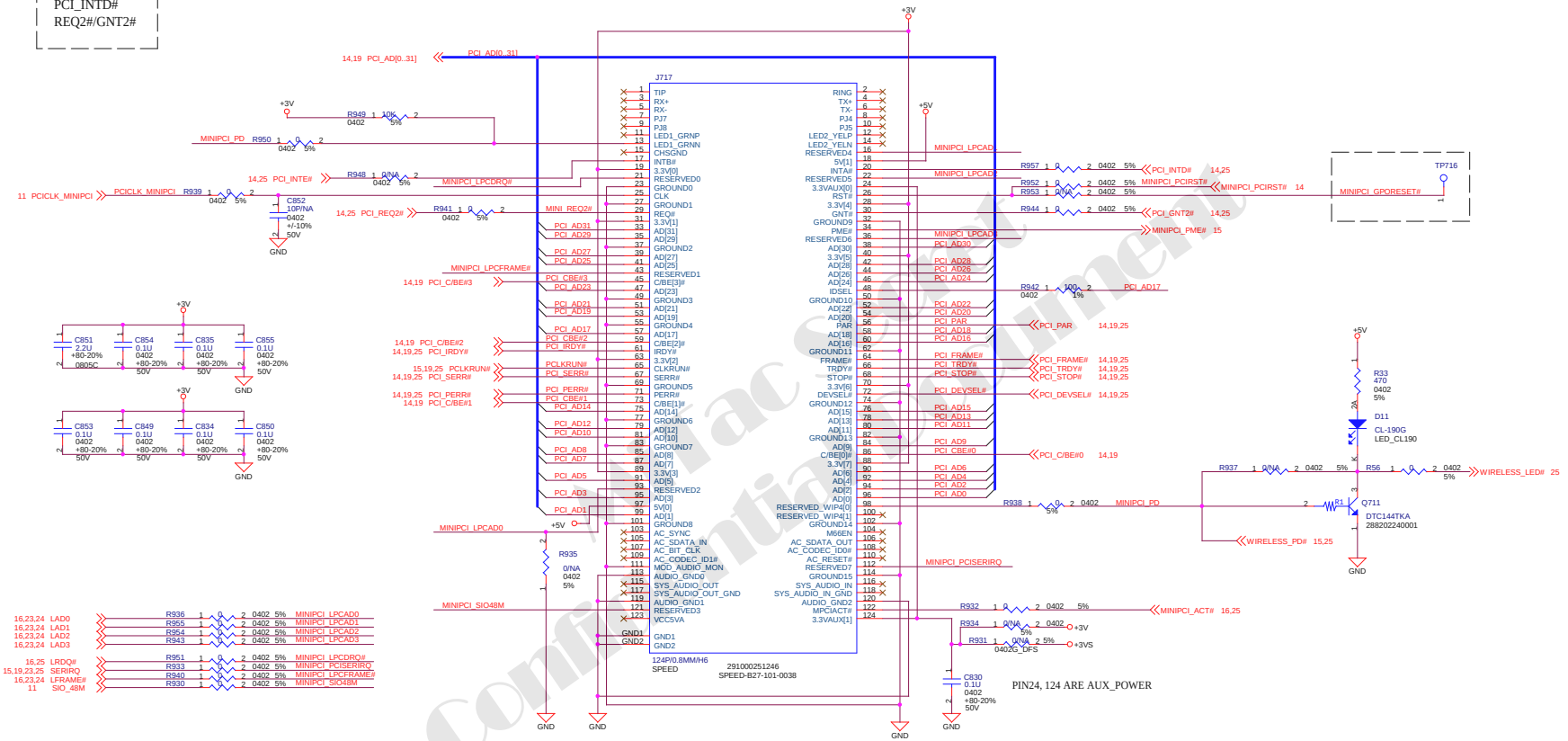
IDSEL:AD20
PCI REQ0#
PCI GNT0#
PCI INTB#



Title	8666
Size C	Document Number PCB/ASSY Rev R00
Date: Monday, December 13, 2004	Sheet 19 of 31

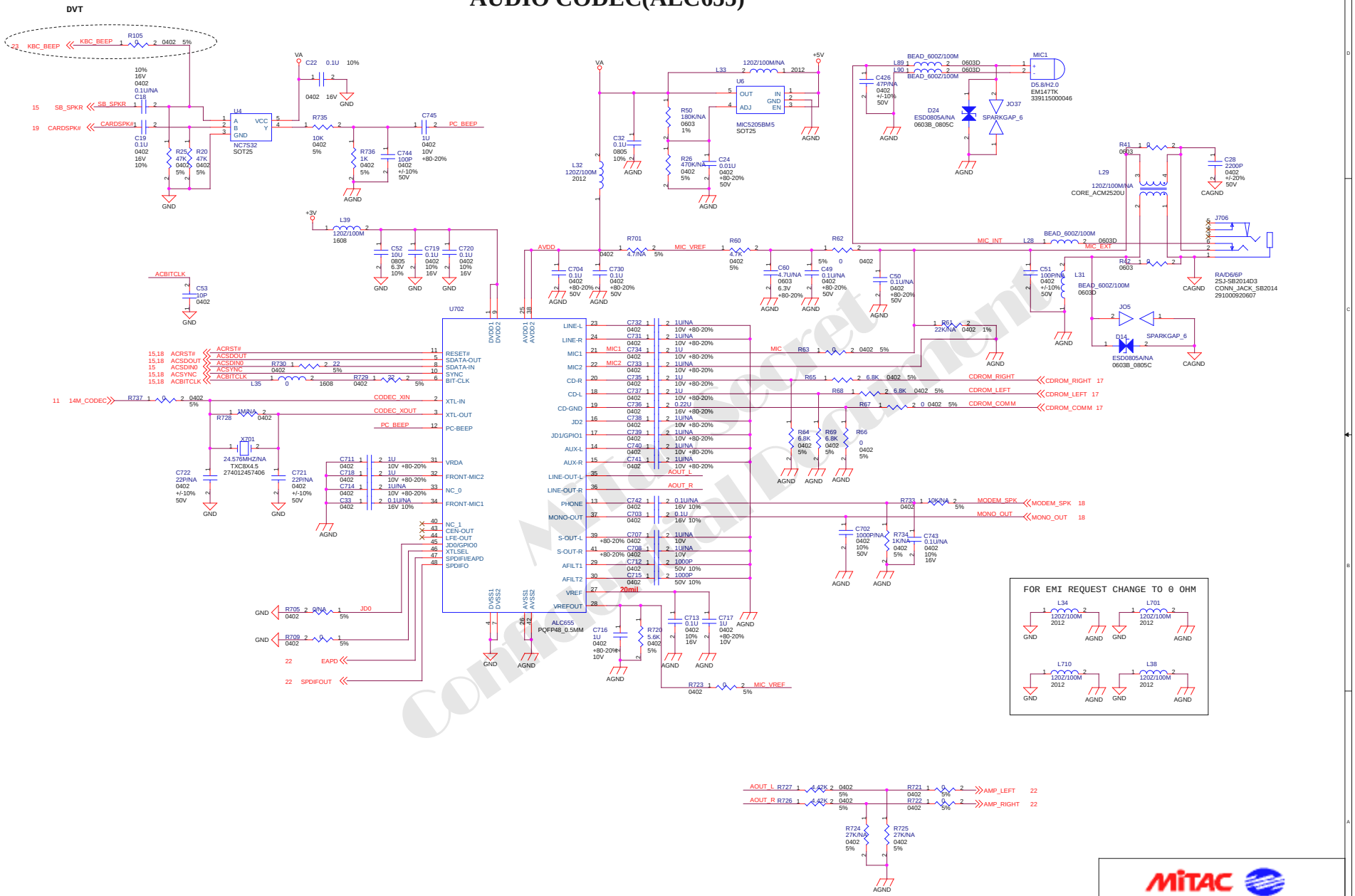
MINI-PCI

MINI-PCI
AD17
PCI_INTD#
REQ2#/GNT2#



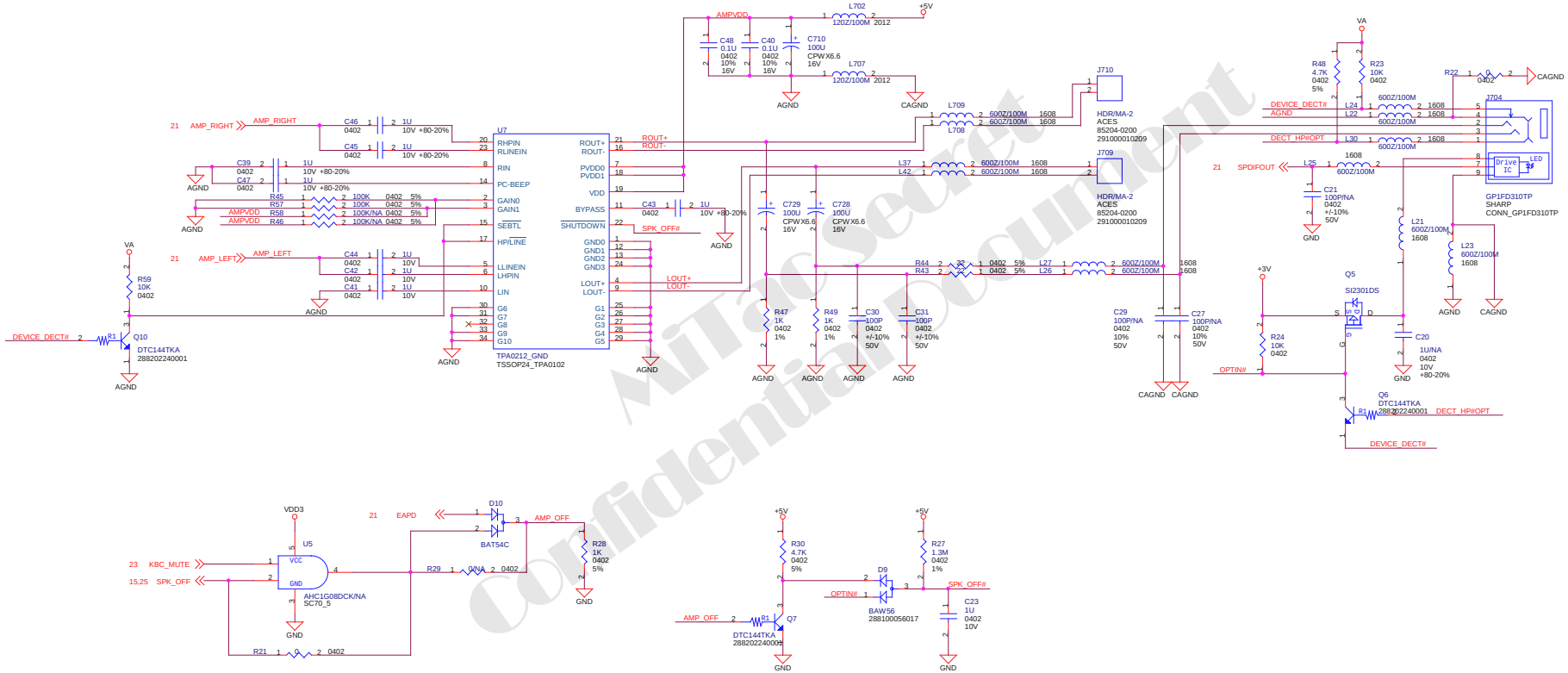
Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 20 of 31	

AUDIO CODEC(ALC655)

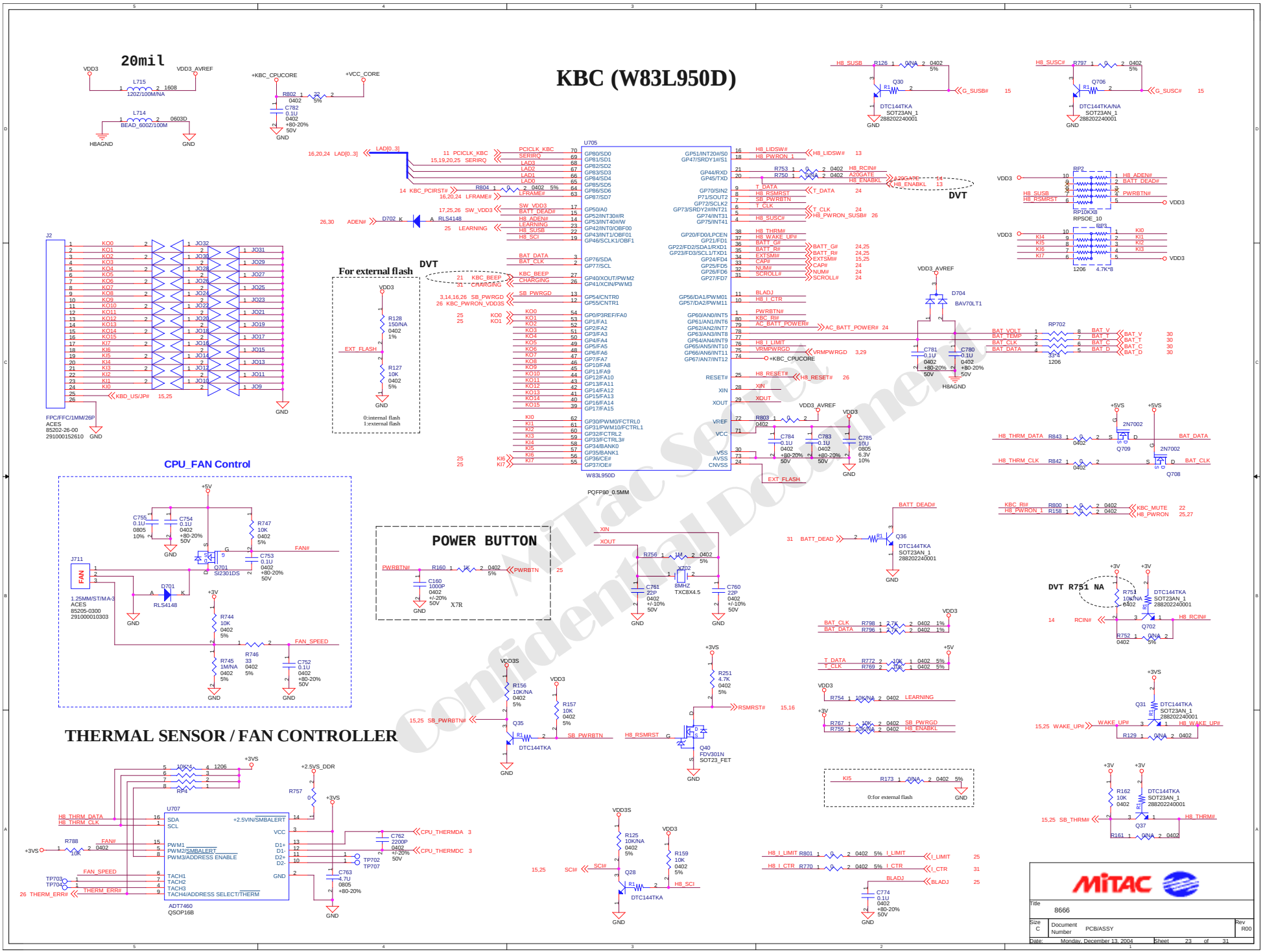


AUDIO AMPLIFIER(TPA0212)

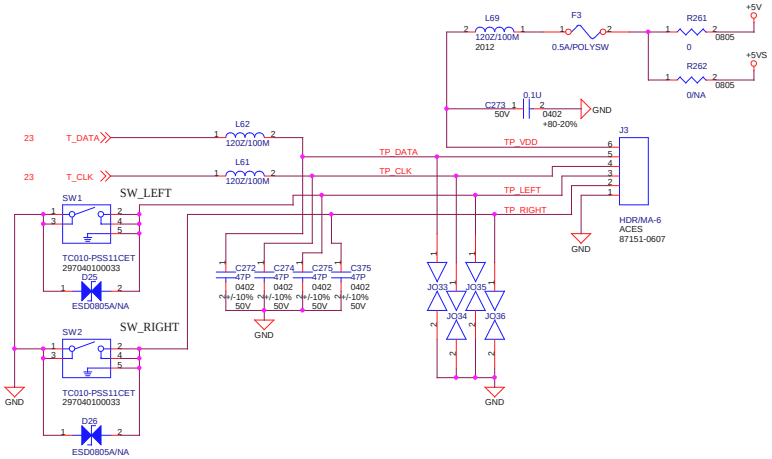
DEVICE_DECT#	DECT_HP#/OPT	REMARK
0	0	HP in
0	1	OPT in
1	0	no this condition
1	1	on device



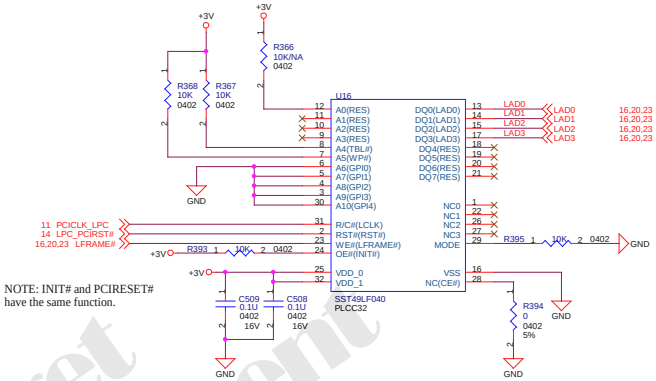
Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 22 of 31	



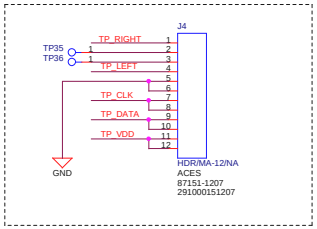
TOUCH_PAD



SYSTEM BIOS



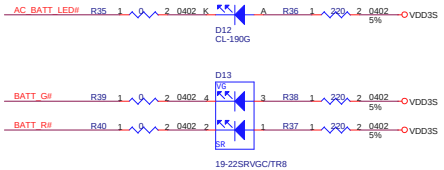
NOTE: INIT# and PCIRESET# have the same function.

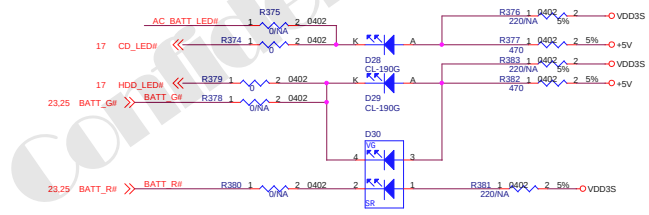


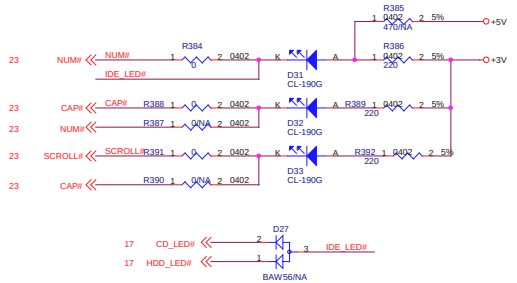
For RHEA series project used

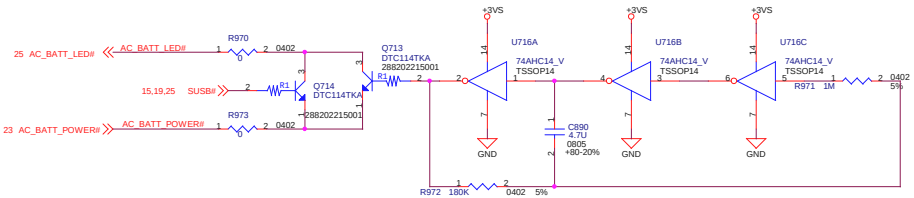
LED

	D38	D40/D42	D39	D41	D43
8666	ODD	HDD	NUM	CAP	SCROLL
NEC	AC/BATT	BATT STATUS	HDD/ODD	NUM	CAP





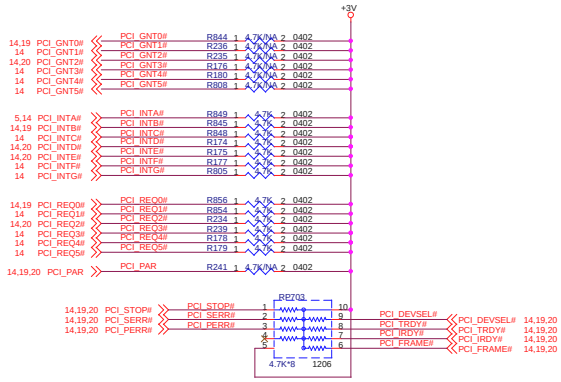




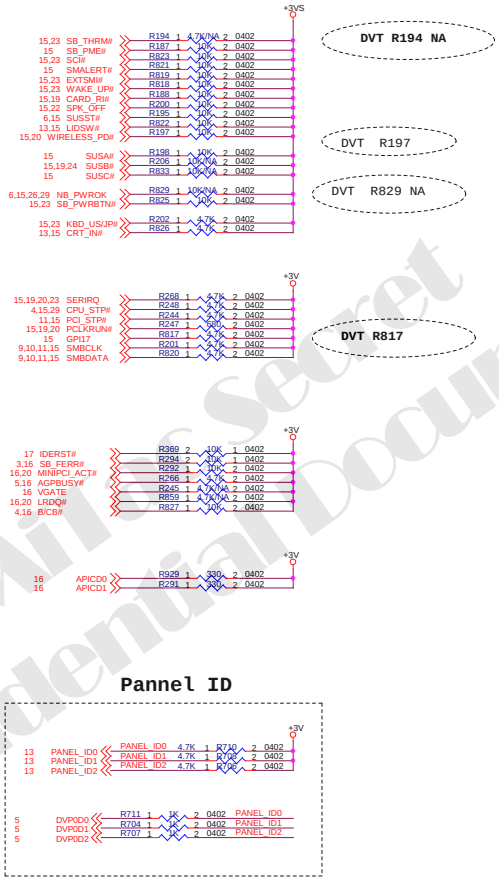
MiTAC	Title	8666	
	Size C	Document Number PCB/ASSY	Rev R00
	Date: Monday, December 13, 2004	Sheet 24 of 31	

PULL -HIGH

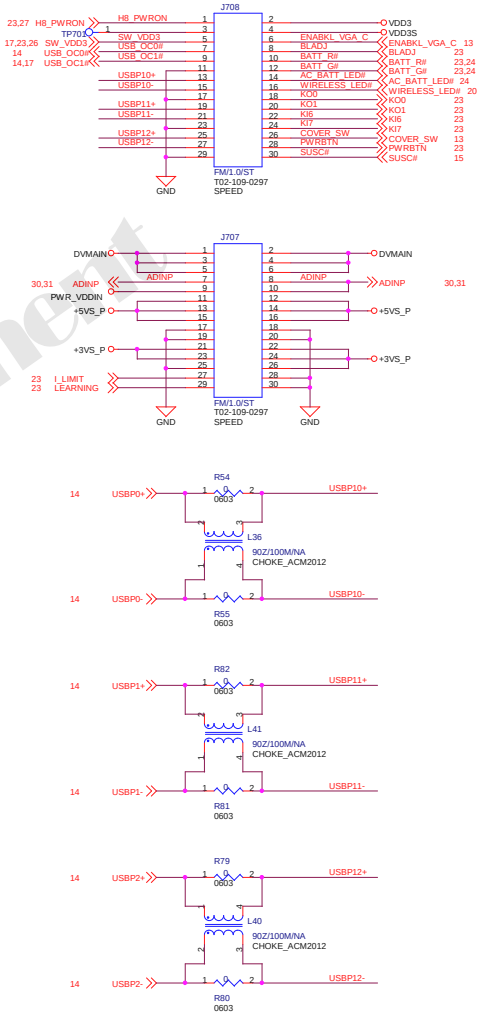
PCI PULL HIGH



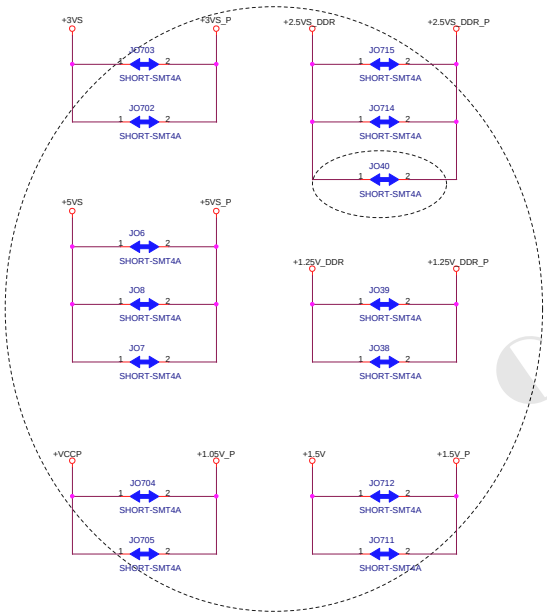
GPIO PULL HIGH



DAUGHTER BOARD CONNECTOR



DVT



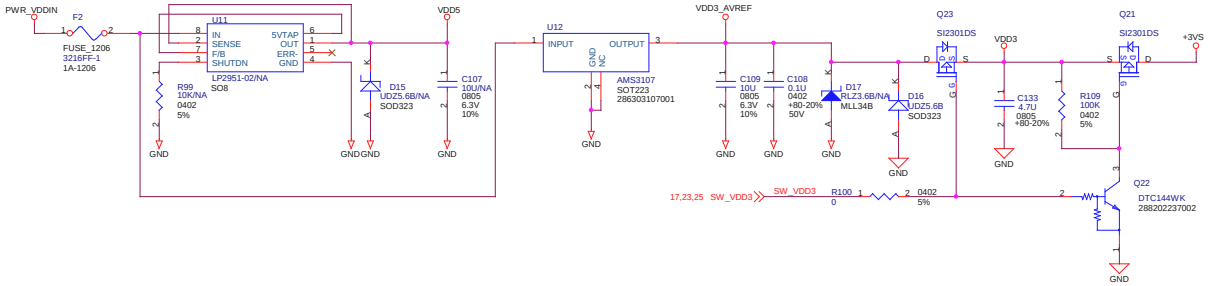
MiTAC

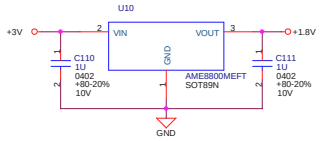
Title: 8666

Size: C | Document Number: PCB/ASSY | Rev: R00

Date: Monday, December 13, 2004 | Sheet 25 of 31

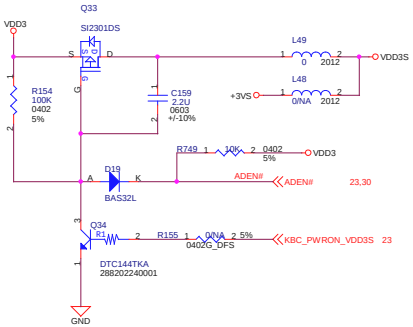
POWER ON PERPHERIAL CIRCUIT

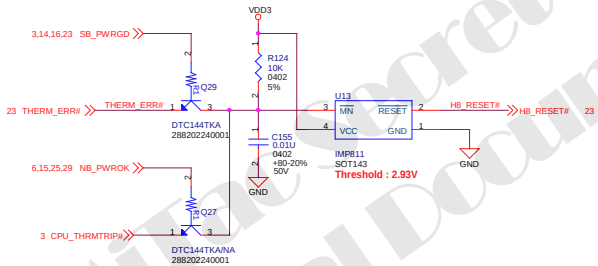


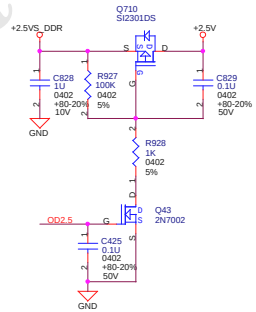


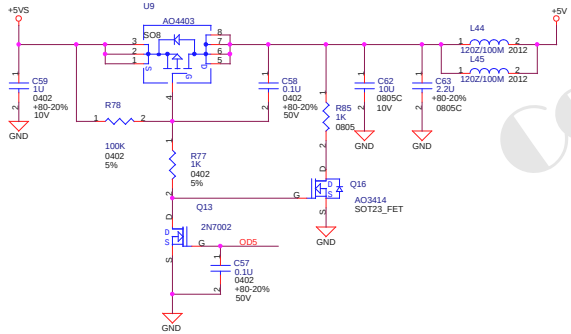
300mA LDO REGULATOR

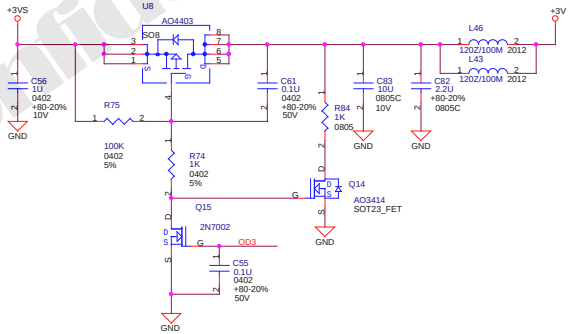
H8 RESET#

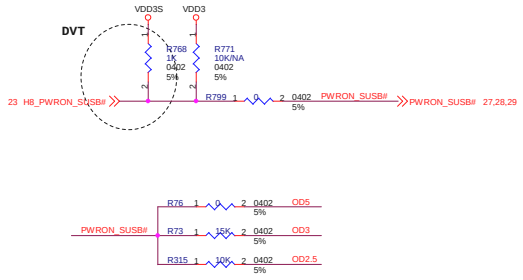






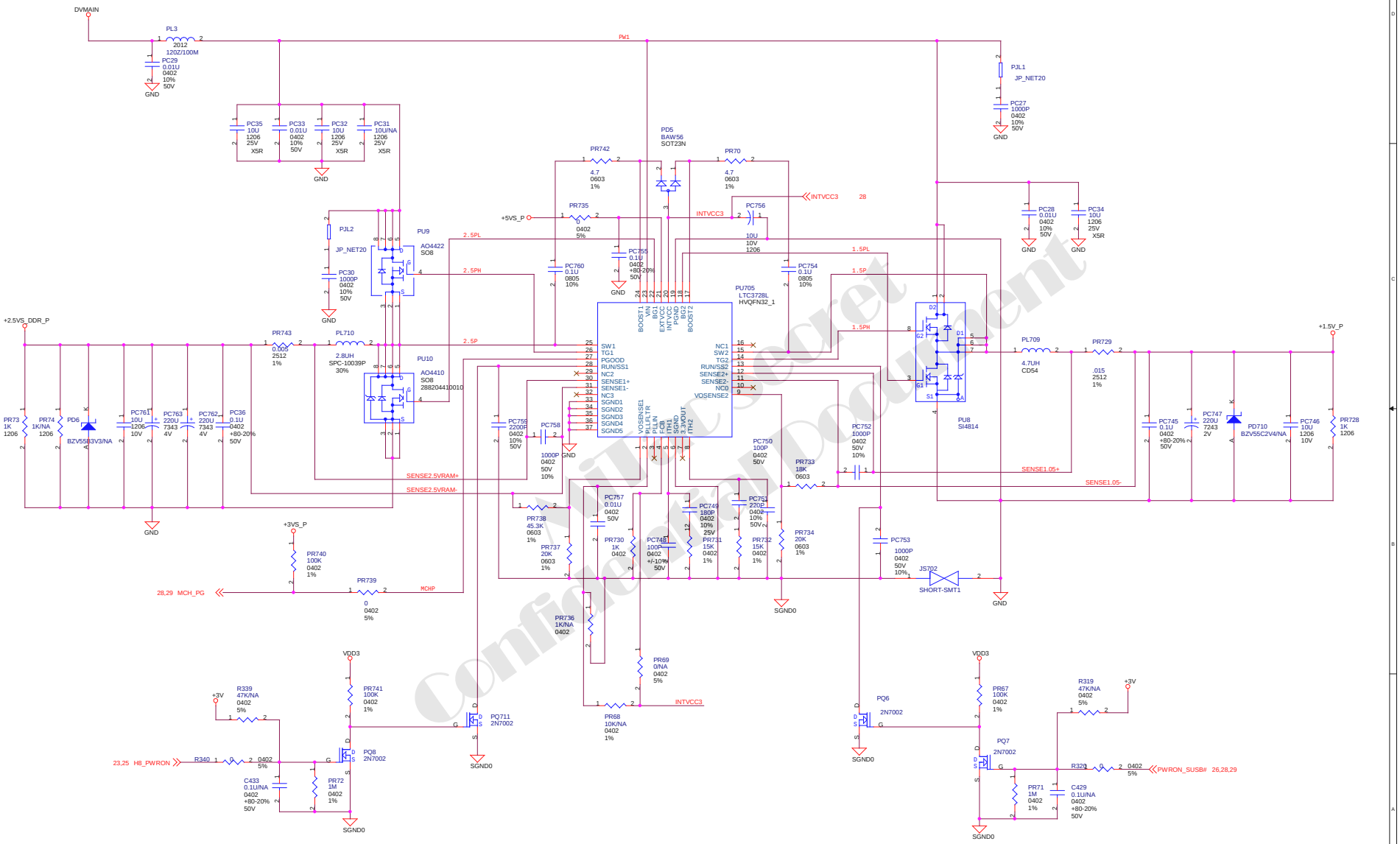




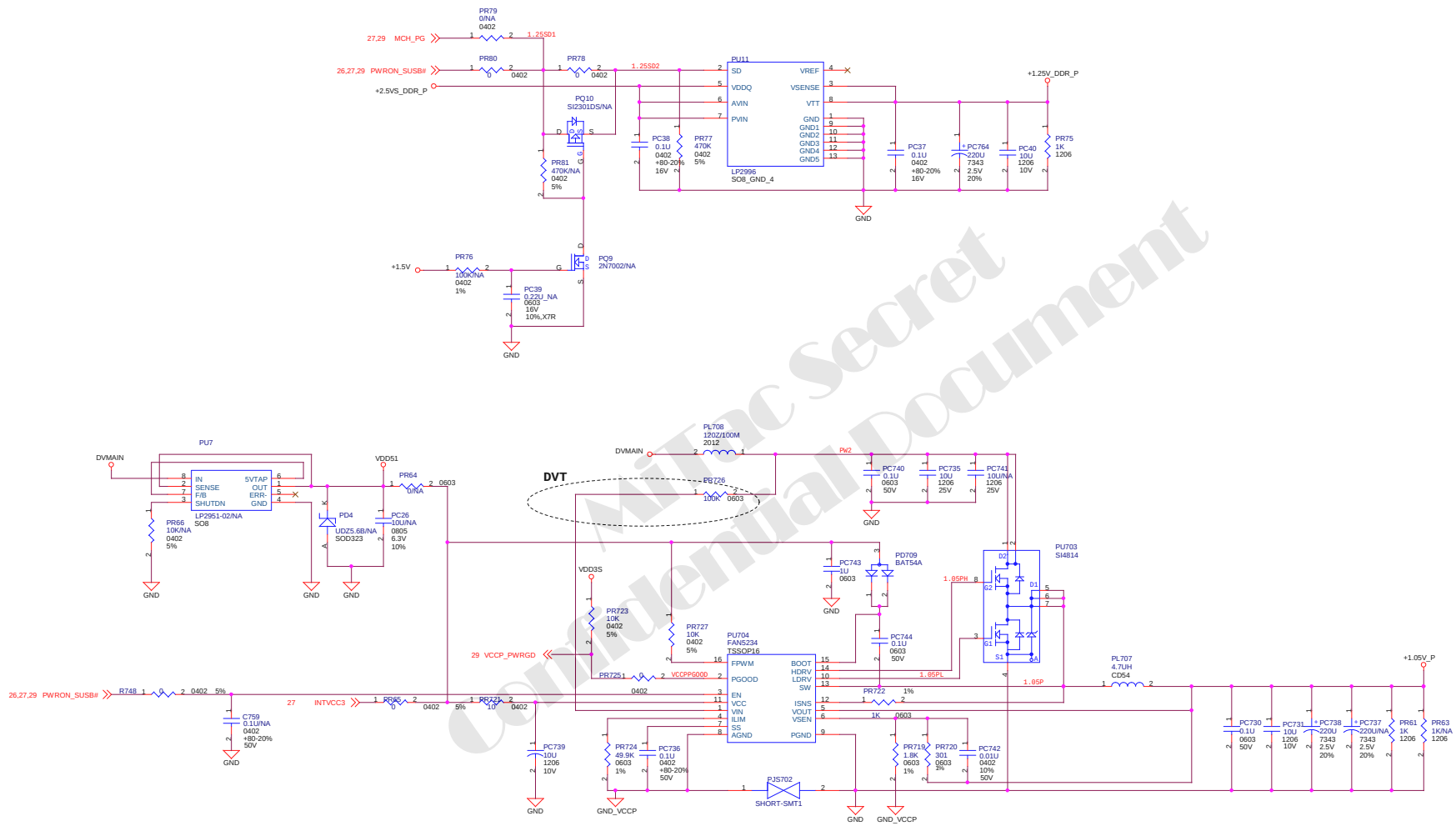


Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 26 of 31	

+2.5VS_DDR_P/+1.5V_P

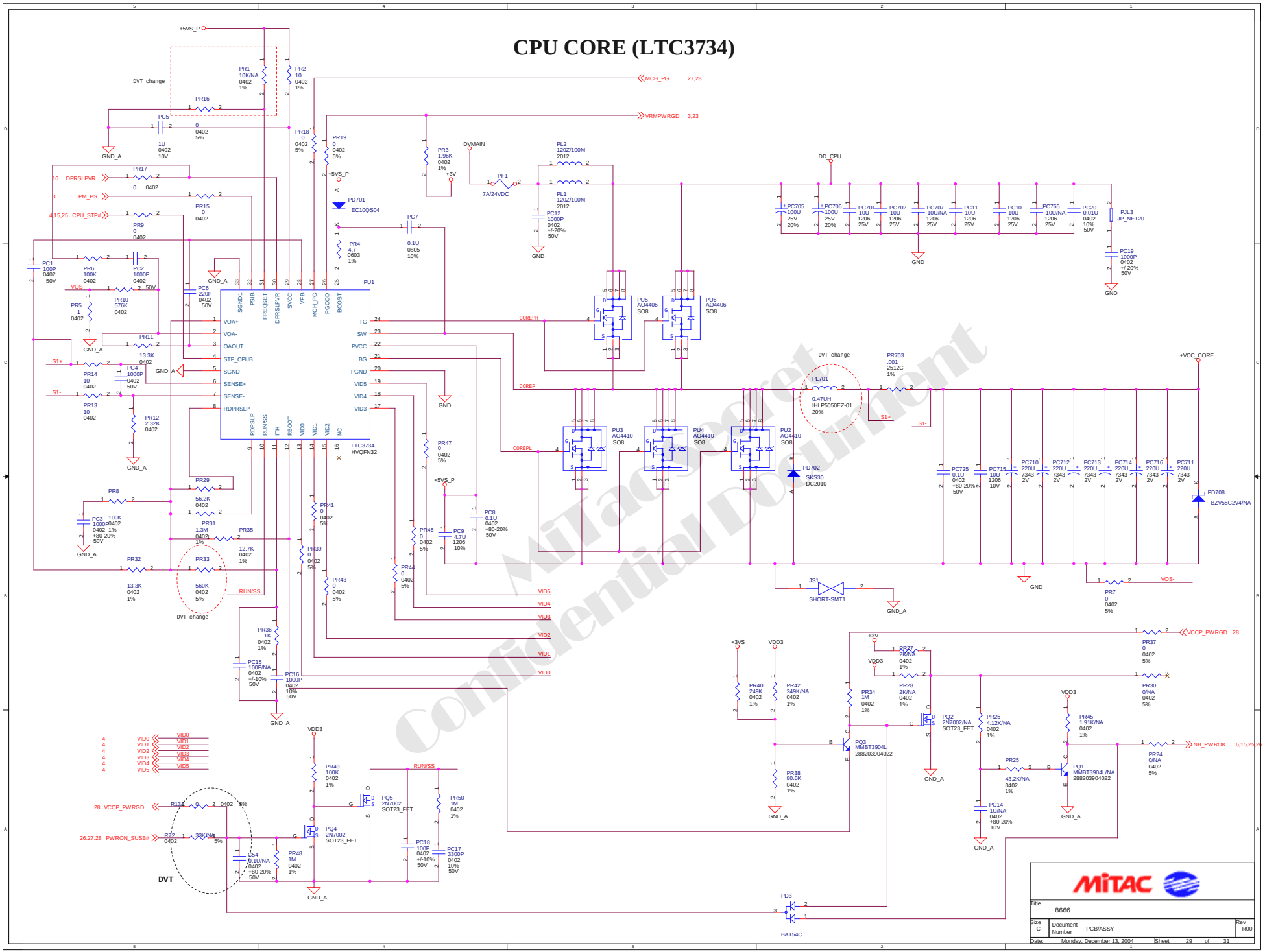


+1.25V_DDR_P/+1.05V_P

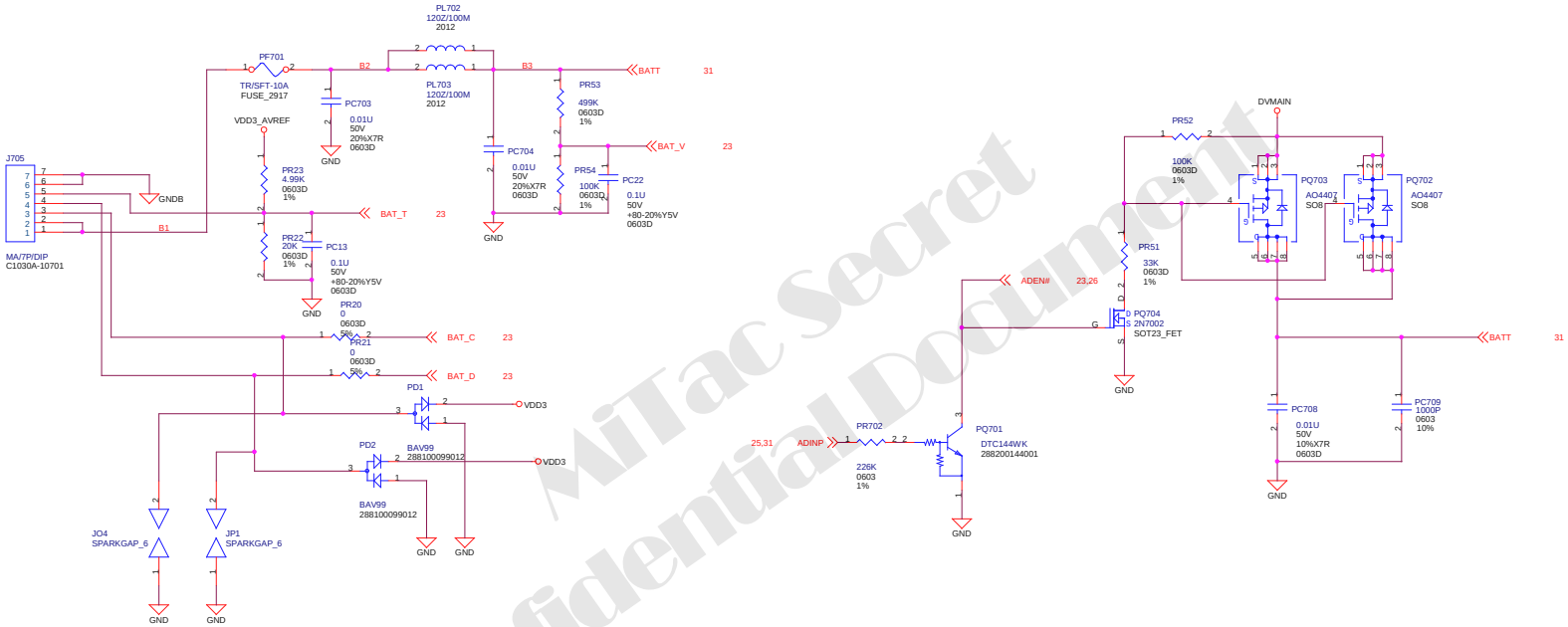


MiTAC

Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 28 of 31	



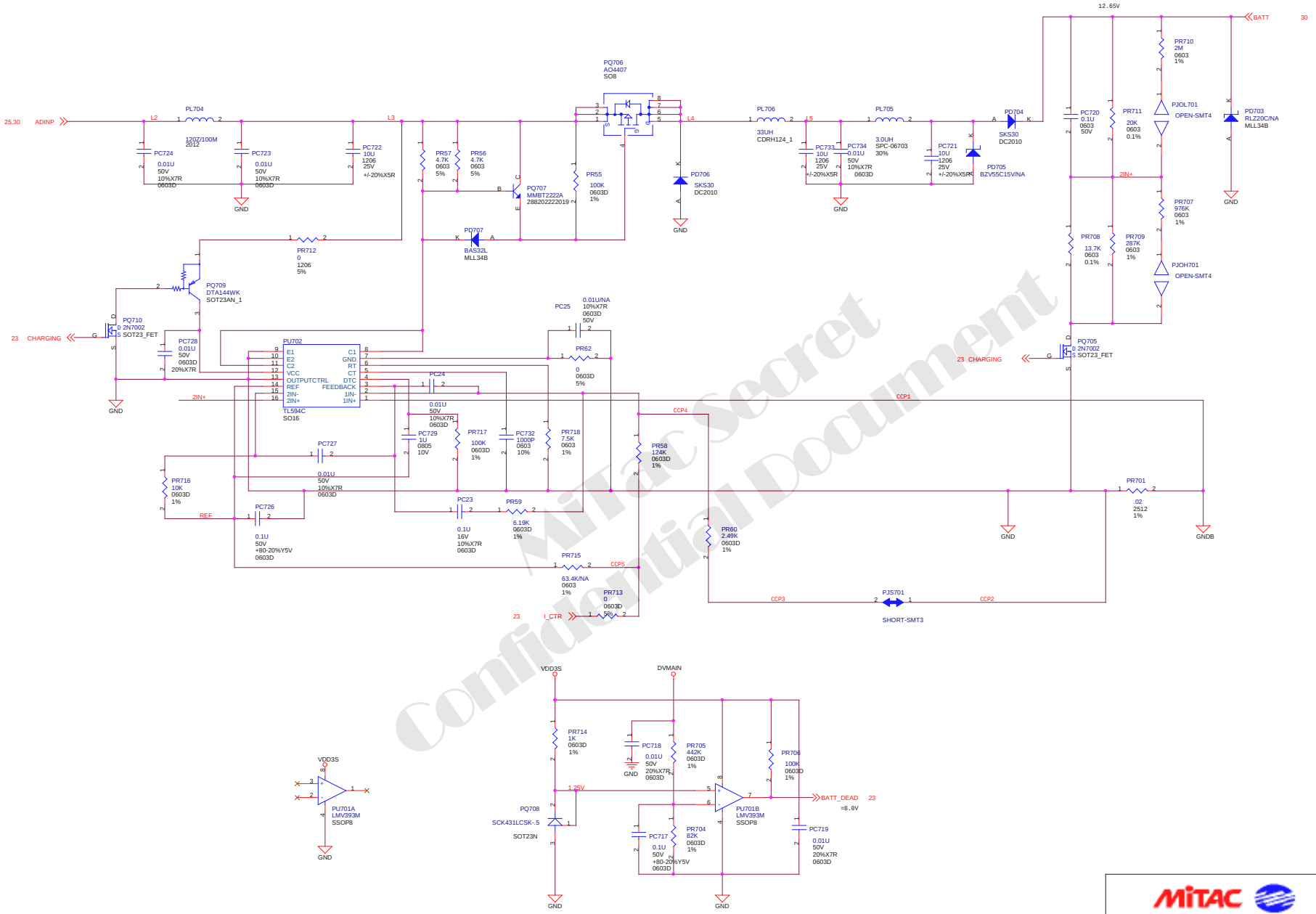
BATTERY CONNECTOR



MiTAC

Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 30 of 31	

CHARGER/DISCHARGER

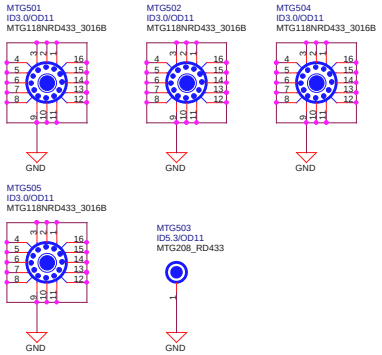


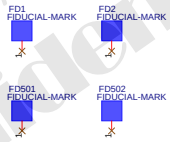
Title	8666	
Size C	Document Number PCB/ASSY	Rev R00
Date: Monday, December 13, 2004	Sheet 31 of 31	

8066/8666 Daughter Board R00

PROJECT CODE G173 **PCB P/N 316686900002**
PRODUCT CODE 6869 **ASSY P/N 411686900004**

REVISION	TAPEOUT DAY	HISTORY
R00	2004/09/13	Initial Release.
R0A		
R01		





DRAWN	DESIGN	CHECK	ISSUES

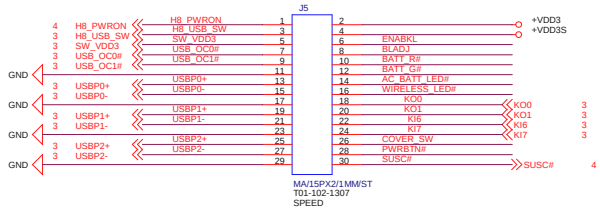
MiTAC

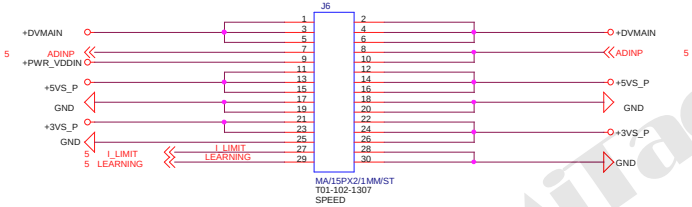
Title: 8X66 DD B/D

Size C | Document Number PCB/ASSY | Rev R00

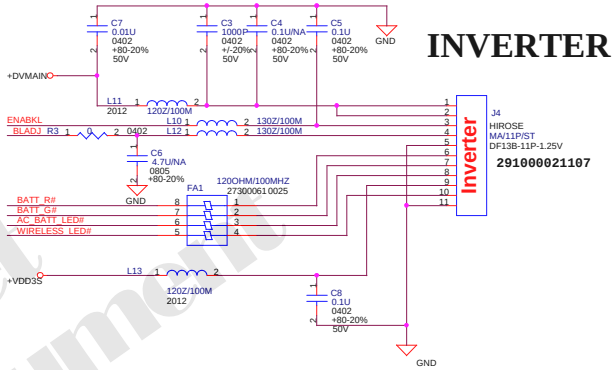
Date: Thursday, October 14, 2004 Sheet 1 of 5

BOARD TO BOARD CNN

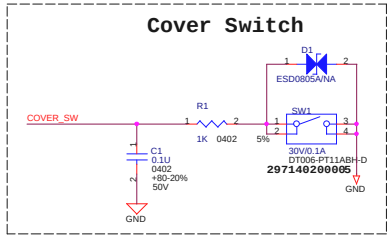




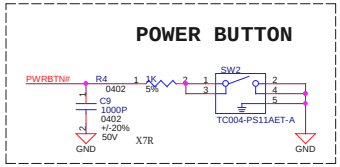
INVERTER



Cover Switch

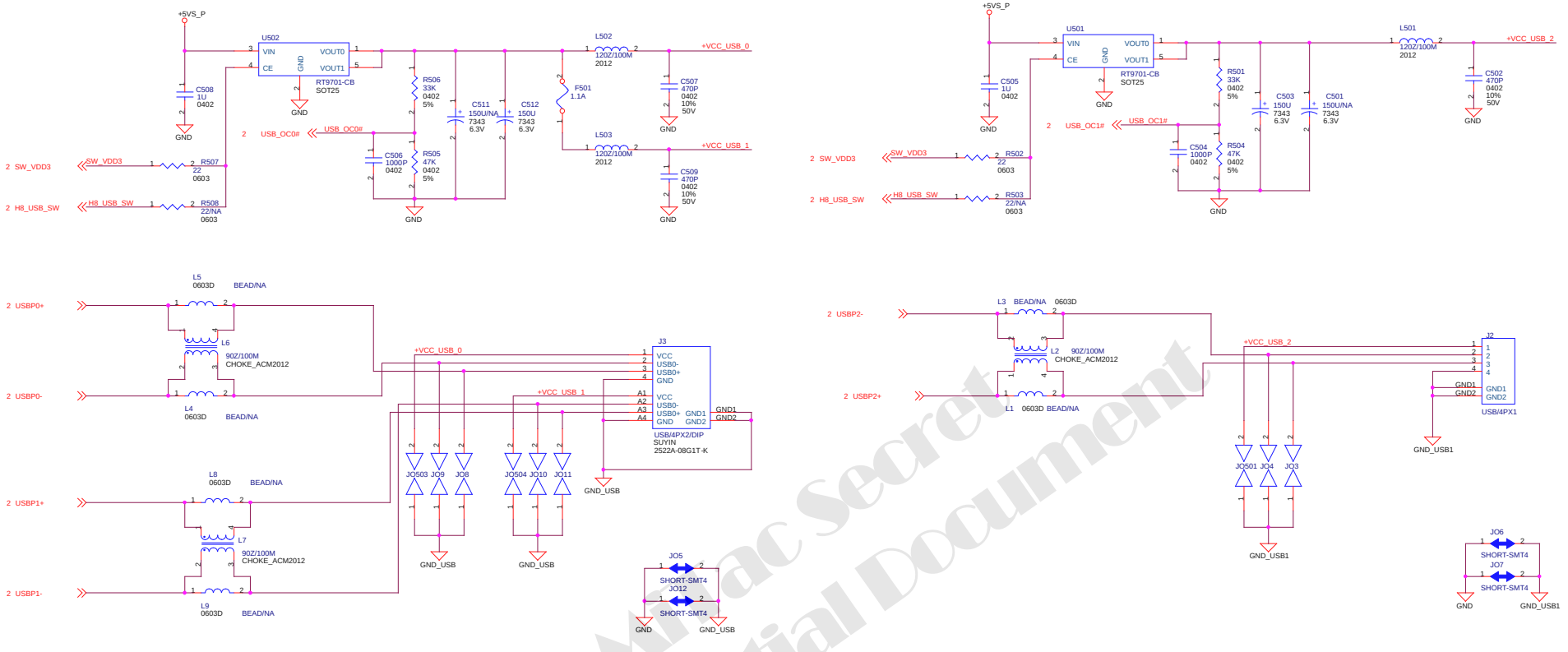


POWER BUTTON

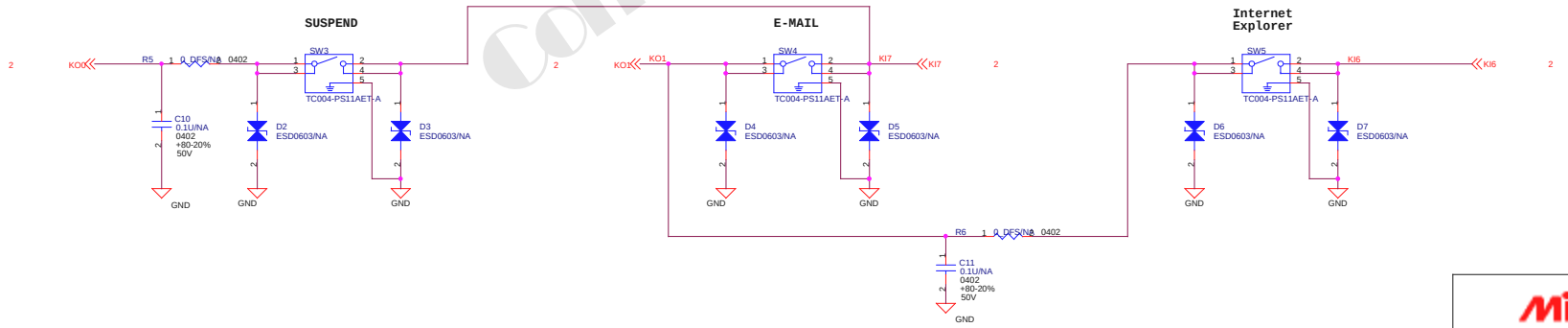


Title	8X66 DD B/D	
Size C	Document Number PCB/ASSY	Rev R00
Date: Thursday, October 14, 2004	Sheet 2 of 5	

USB CONNECTOR

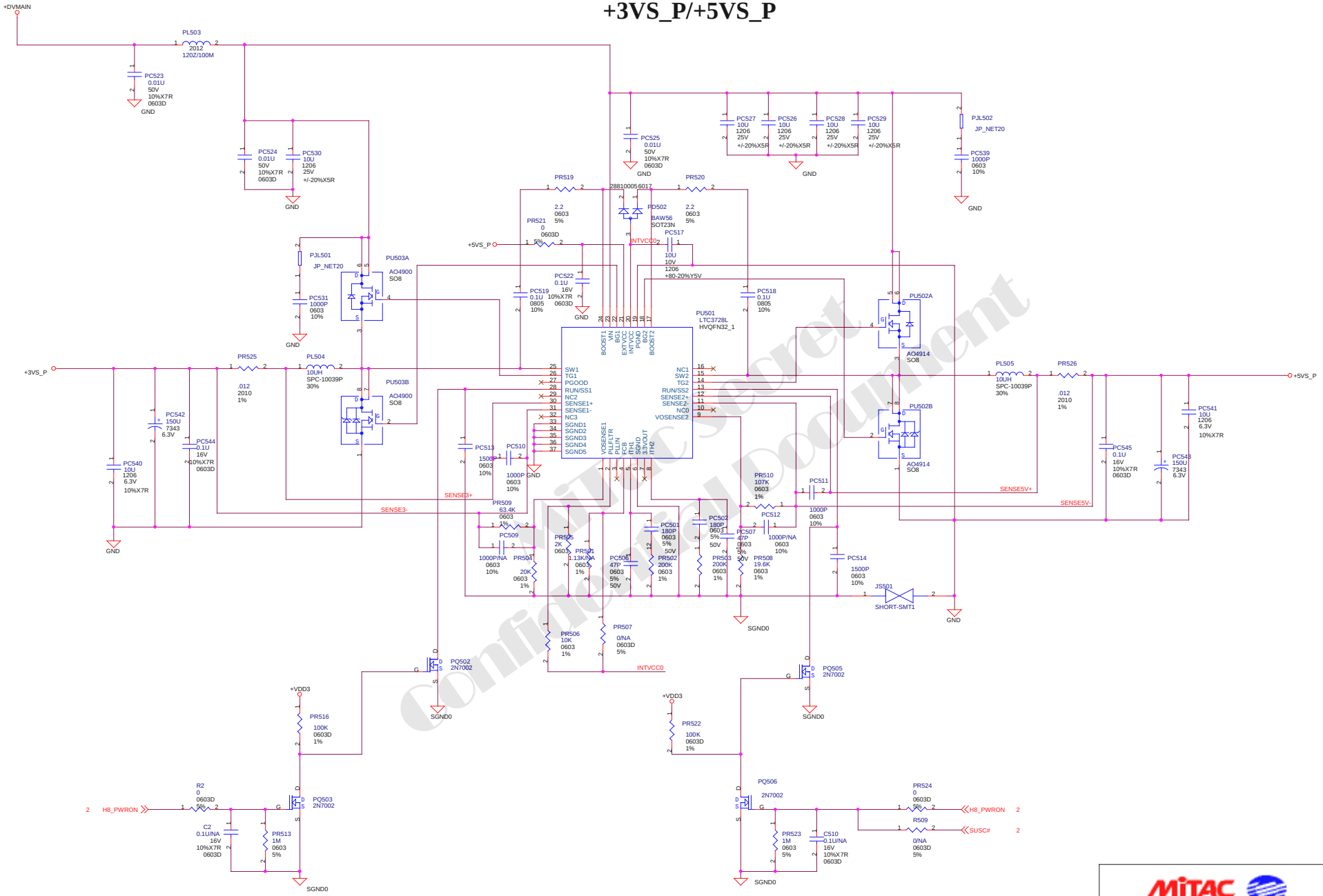


QUICK KEY



Title	8X66 DD B/D		
Size C	Document Number PCB/ASSY		Rev R00
Date: Thursday, October 14, 2004	Sheet 3	of 5	

+3VS_P/+5VS_P



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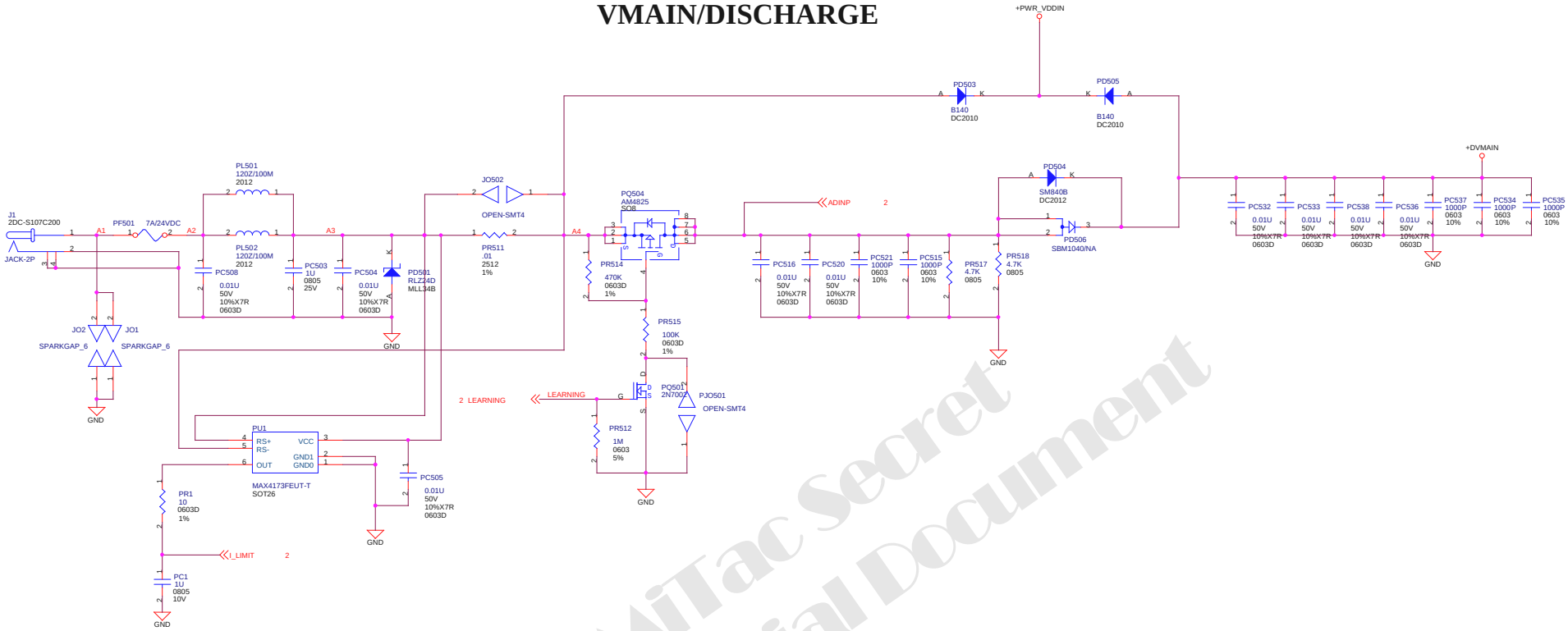
Title	8X66 DD B/D	
Size C	Document Number PCB/ASSY	Rev R00
Date: Thursday, October 14, 2004	Sheet 4 of 5	

VMAIN/DISCHARGE



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Title	8X66 DD BD	
Size C	Document Number PCB/ASSY	Rev 00
Date: Thursday, October 14, 2004	Sheet 5 of 5	

Reference Material

- Intel Pentium M Processor Data Sheet — *Intel,INC*
- VIA PN800 North Bridge Data Sheet — *VIA,INC*
- VIA VT8235CE South Bridge Data Sheet — *VIA,INC*
- Clock Generator ICS950902 — *ICS,INC*
- 8666 Hardware Engineering Specification — *Technology.Corp./MiTAC*

SERVICE MANUAL FOR 8666

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