SERVICE MANUAL FOR

8650

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MiTAC

8650 N/B Maintenance

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MITAC 8650 portable notebook computer system.

1.1.2 System Overview

The MITAC 8650 model is designed for Intel Banias processor with 400 MHz FSB with Micro-FCPGA package. It can support Banias 1.5 G~1.9 GHz.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as Wireless LAN indicator, Power indicator, Battery status indicator, ODD, HDD, Num Lock, Caps Lock, Scroll Lock. It also equipped with LAN, 56 K Fax Modem, 3 USB ports, and audio line out, external microphone function.

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The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC3200 DDR400 SDRAM.

The VIA PN800 Mobile North Bridge integrates a high performance CPU interface for Intel Pentium 4/Pentium-M processor, a full featured AGP port controller, Integrated Graphics with 2D/3D/Video Controllers, a advanced high-performance DDR400 SDRAM controller, and high bandwidth Ultra V-Link host controller connecting with VIA VT8235CE South Bridge.

The VIA VT8235CE integrates Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller With AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Inter-operable with VIA Host-to-V-Link Host Controller.

The VIA VT6103L is a Fast Ethernet 10/100 1-port PHY/Transceiver with MII interface, and meet all applicable IEEE 802.3, 10Base-T and 100Base-Tx standards.

The ENE CB1410 CardBus controller functions as a single slot PCI to Cardbus bridge. The CB1410 compliant with PCI Local Bus Specification Rev2.2, PC99 System Design Guide, and PC Card Standard 8.0.

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, plug and play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	Mobile Pentium-M Processor 1.3G ~ 1.9 GHz Thermal spec 35 W TDP
Core logic	VIA PN800 + VIA VT8235CE chipset
VGA Control	North Bridge Integrated
System BIOS	SST49LF040
Memory	DDR RAM :DDR333 Nanya NT512D64S8HBAFM-6K DDR400 Micron, MT8VDDT3264HD
Video Memory	Share memory
Clock Generator	ICS 950902
LVDS	VIA VT1634AL
LAN PHY	VIA VT6103L
PCMCIA	ENE CB1410
Audio System	AC97 CODEC: Advance Logic, Inc, ALC655 Power Amplifier: TI TPA0212
Modem	AC97 Link: MDC (Mobile Daughter Card) Askey : V1456VQL-P1(INT)

1.2.1 Intel Banias Processors in Micro-FCPGA Package

Intel Banias Processors with 593 pins Micro-FCBGA package.

It has the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400 MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.2.2 Clock Generator

The ICS950902 is a single chip clock solution for desktop designs using the VIA P4X/P4M/KT/KN266/333 style chipsets with PC133 or DDR memory. The ICS950902 is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread

percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1 MHz increment.

➢ **Recommended Application**

VIA P4X/P4M/KT/KN266/333 style chipsets

➢ **Output Features**

- 1- Pair of differential CPU clocks @ 3.3 V (CK408) /1- Pair of differential open drain CPU clocks (K7)
- 1- Pair of differential push pull CPU_CS clocks @ 2.5 V
- 3- AGP @ 3.3 V
- 7- PCI @ 3.3 V (1- Free running)
- 1- 48 MHz @ 3.3 V fixed
- 1- 24_48 MHz @ 3.3 V (Default 48 MHz I2C select only)
- 2- REF @ 3.3 V, 14.318 MHz
- 12- SDRAM (6 pair - DDR) selectable

➢ **Features/Benefits**

- Programmable output frequency
- Programmable output divider ratios
- Programmable output rise/fall time
- Programmable output skew
- Programmable spread percentage for EMI control
- DDR output buffer supports up to 200 MHz
- Watchdog timer technology to reset system if system malfunctions
- Programmable watch dog safe frequency
- Support I2C Index read/write and block read/write operations
- Uses external 14.318 MHz crystal

1.2.3 PN800 Mobile North Bridge

The PN800 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome Pro graphics/video controllers used for the implementation of mobile personal computer systems

based on 800/533/400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors.The complete mobile chipset consists of the PN800 North Bridge (829 pin HSBGA) and the VT8235-CE V-Link South Bridge (539-pin BGA). The PN800 integrates VIA's PT800 system controller with high-performance UniChrome Pro 3D/2D graphics accelerator plus flat panel, DVI monitor and TV out interfaces. The PN800 provides superior performance between the CPU,DRAM, V-Link bus and internal AGP 8x graphics controller bus with pipelined, burst, and concurrent operation. The VT8235-CE is a highly integrated peripheral controller which includes V-Link-to-PCI/ V-Link-to-LPC controllers, Ultra DMA IDE controller,USB2.0 host controller, 10/100 Mb networking MAC, AC97, and system power management controllers.

- **Host CPU Interface**

  The PN800 supports 800/533/400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors. It implements a twelve level In-Order-Queue and supports Intel Hyper-Threading Technology to maximize system performance for multi-threaded software applications. DBI and Pentium M bus protocol, as well as Intel Speed Step Technology, are supported which effectively reduce overall system power consumption.

- **AGP Interface**

  The PN800 AGP controller is AGP 3.0 compliant with up to 2.1 GB/second data transfer rate capability. It supports asynchronous AGP and CPU interfaces for flexible system configuration. Deep read (1024-byte) and write (512-byte) FIFOs are integrated for optimal bus utilization and minimum data transfer latency.

➢ Memory Controller

The PN800 SDRAM Controller supports two sets of 64-bit memory data, address and control signals to minimize signal loading and up to 4 double-sided DDR400/333/266 DIMMs for 8 GB maximum physical memory. The DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and the memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64/128/256/512/1024 Mb DRAMs in x8 and x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus. The PN800 North Bridge is pin compatible with the PN880 North Bridge which connects to the memory modules in exactly the same manner while supporting true 128-bit operation (simultaneous memory access on both sets of 64-bit memory data/address/control signals).

➢ Ultra V-Link

The PN800 North Bridge interfaces to the South Bridge through a high speed (up to 1 GB/sec) 8x, 66 MHz Data Transfer interconnect bus called "Ultra V-Link". Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-link operation. The combined PN800 North Bridge and VT8235-CE South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead.In addition, advanced features are supported such as CPU write-back forward to PCI master, and CPU write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

➢ System Power Management

For sophisticated power management, the PN800 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. Enhanced Intel Speed Step™ Technology enables minimization of CPU power consumption while sustaining processing power. The PN800 graphics accelerator implements dynamic clock gating for inactive functions to achieve maximum power savings. The system can also be switched to standby or suspend states to further reduce power consumption when idle.Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down are supported. Coupled with the VT8235-CE South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

➢ 3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the PN800 North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

- **128-bit 2D Graphics Engine**

The PN800 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths. The PN800 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversion and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

- **Video Capture**

The PN800 North Bridge implements an optional Video Capture Port which supports various video capture standards, including ITU-R BT656, VIP 1.1 and VIP 2.0 and is compliant with the most common video capture formats: 16/32-bit RGB and YUV422. With the integrated video capture feature, the PN800 can provide high performance video effects for video capturing and playback.

- **LCD, DVI Monitor and TV Output Display Support**

The PN800 provides three “Digital Video Port” interfaces: FPDP, GDVP1, and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit/dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VIA VT1631, NSC DS90C387R or Chrontel CH7017). The PN800 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT

color panels, in either SDR (1 pixel/clock) or DDR (2 pixels/clock) modes. UXGA and higher resolutions require dual-edge data transfer (DDR) mode which is supported by the VIA VT1631 LVDS transmitter chip Digital Video Port 0 (DVP0) is normally used for interfacing to a TV encoder (such as the VIA VT1622A or VT1622AM using 3.3V signal levels), however if DVP0 is used for video capture, Digital Video Port 1 (GDVP1) may be configured for support of an external TV encoder (VIA VT1623 or VT1623M using low-voltage 1.5 V signal levels). If GDVP1 is not being used for TV out, it can optionally be used to drive a DVI resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth, and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

1.2.4 VT8235CE Highly Integrated South Bridge

The VT8235 Version CE South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 Version CE includes standard intelligent peripheral controllers:

a) IEEE 802.3 compliant 10/100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHY ceiver.

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel

commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 Version CE also supports the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0/1.1 and Universal HCI v2.0/1.1 compliant. The VT8235 Version CE includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

i) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts DMA

channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of onboard peripherals for Windows family compliance.

The VT8235 Version CE also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 Version CE supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (double words) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

1.2.5 LVDS Transmitter: VT1634AL

The VT1634AL LVDS (Low Voltage Differential Signaling) transmitter is designed to support pixel data transmission from a Host to Flat Panel Display ranging from VGA to WXGA resolutions. The transmitter converts 24-bit of CMOS/TTL input data into 4 LVDS (Low Voltage Differential Signaling) output data streams. With an input clock at 85 MHz, the maximum transmission rate of each LVDS line is 595 Mbps, for an aggregate throughput rate of 2.38 Gbps. A phase-locked transmit clock is transmitted in parallel with the output data streams over the 4-channel LVDS link. The VT1634AL is designed to be compatible with Graphics Memory Controller Hub by implementing two data per clock .Two input modes are supported: one port of 12-bit (two data per clock) input for 24-bit RGB. In this mode, input data will be clocked on both rising and falling edges in LVTTL level operation, or clocked on the cross over of differential clock signals in the low swing operation. Each input data width will be 1/2 of clock cycle. The other mode is 18-bit input for 18-bit RGB.The VT1634AL is an ideal solution to solve EMI and cable size problems for high-resolution flat panel display applications. The VT1634AL provides

a reliable industry standard interface based on LVDS technology that delivers the bandwidth needed for high resolution panels while maximizing bit times, and keeping clock rates low to reduce EMI and shielding requirements.

Product Features

- Compiles with open LDI specification for digital display interfaces
- Compatible with TIA/EIA-644 LVDS standard
- Supports input pixel clock from 25 MHz to 85 MHz
- Supports LVDS panel resolution from VGA through WXGA (1280x800/1280x768)
- Single channel LVDS transmitter function
- Supports 18-bit/24-bit panel type
- Supports 24-bit TFT LCD with Conventional or Non-Conventional Color Mappings
- Supports MSB/LSB color data mapping option for 24-bit panel
- Narrow Bus Reduces Cable Size and Cost
- PLL Requires No External Components
- Power Down (PD#) Mode control

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- Supports Both LVTTL and Low Voltage Level Input (Capable of 1.0 to 1.8 V)
- 2.5 V Supply Voltage
- Small Package LQFP-48 Low-Profile Quad Flat Package (7x7x1.4 mm)

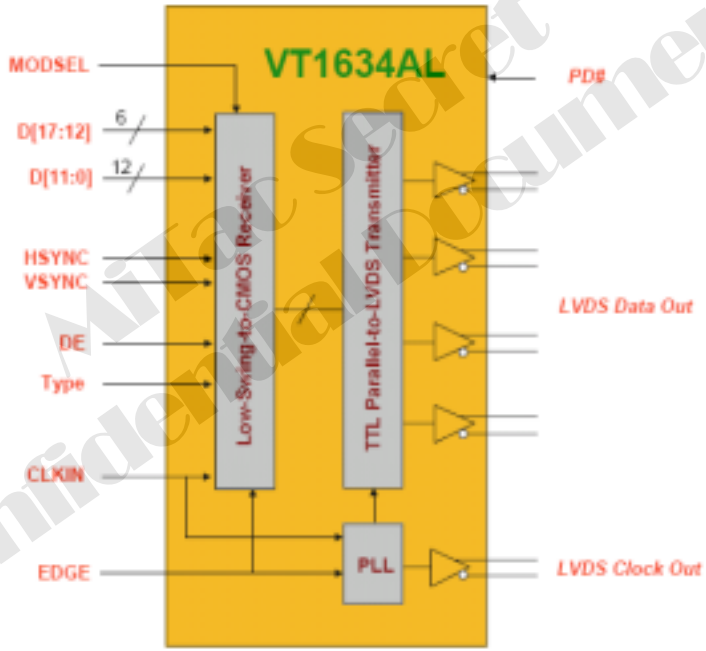


Figure 1: VT1634AL

1.2.6 CardBus: CB1410

Features

- 3.3 V operation with 5 V tolerant
- LFBGA 144-ball package
- Compliant with
  - PCI Local Bus Specification, Revision 2.2
  - PCI Bus Power Management Interface Specification, Revision 1.1
  - PCI Mobile Design Guide, Version 1.1
  - Advanced Configuration and Power Interface Specification, Revision 1.0
  - PC 99 System Design Guide
  - PC Card Standard 8.0
  - Interrupt configuration
  - Supports parallel PCI interrupts
  - Supports parallel IRQ and parallel PCI interrupts
  - Supports serialized IRQ and parallel PCI interrupts
  - Supports serialized IRQ and PCI interrupts

- Power Management Control Logic
- Supports CLKRUN# protocol
- Supports SUSPEND#
- Supports PCI PME# from D3, D2, D1 and D0
- Supports PCI PME# from D3Cold
- Supports D3STATE# (CB1410 only)
- Power switch interface
- CB1410 supports parallel 4 wire power switch interface
- Misc Control Logic
- Supports serial EEPROM interface
- Supports socket activity LED
- Supports 5 GPIOs and GPE#
- Supports standard zoomed video port
- Supports SPKROUT, CAUDIO and RIOUT#
- Supports PCI LOCK#

1.2.7 AC'97 Audio System: Advance Logic, Inc, ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-Bit volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3 V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M 24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (win nXP/ME/ 2000/98/NT), EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48 KHz sampling rate
- Compliant with AC'97 2.3 specifications

  - 14.318 MHz-24.576 MHz PLL to save crystal
  - 12.288 MHz BITCLK input can be consumed
  - Integrated PCBEEP generator to save buzzer
  - Interrupt capability
  - Three analog line-level stereo inputs with 5-bit

- Volume control: Line_In, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP
- Phone-In
- Two software selectable MIC inputs
- Applications (software selectable)
- Boost preamplifier for MIC input
- 50 mW/20 amplifier
- External Amplifier Power Down (EAPD) capability
- Power management and enhanced power saving features

- Stereo MIC record for AEC/BF application
- Supports power off CD function
- Adjustable VREFOUT control supports double sampling rate (96 KHz) of DVD audio playback
- Support 48 KHz of SPDIF output is compliant with AC'97 rev2.3 specification
- Power support: Digital: 3.3 V; Analog: 3.3 V/5 V

1.2.8 MDC: PC-TEL Modem Daughter Card PCT2303W (Askey V1456VQL-P1)

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chipset is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on

PCT303W). The chipset eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chipset dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

The chipset is fully programmable to meet world-wide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chipset include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent world-wide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

❖ **Features**

- Virtual com port with a DTE throughout up to 460.8 Kbps
- G3 Fax compatible
- Auto dial and auto answer
- Ring detection

❖ **Codec/DAA Features**

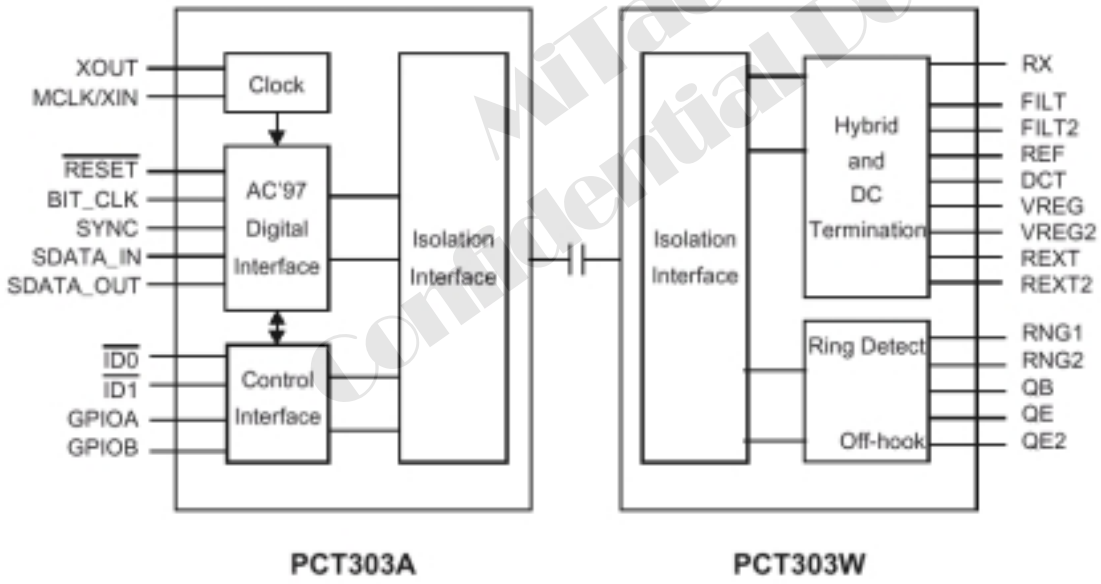
- AC97 2.1 compliant

- 86dB dynamic range TX/RX paths
- 2-4-wire hybrid
- Integrated ring detector
- High voltage isolation of 4000 V
- Support for “Caller ID”
- Compliant with FCC Part68, CTR21, Net4 and JATE
- Low power standby
- Low profile SOIC package 16 pins 10x3x1.55 mm
- Low power consumption
- 10 mA @ 3.3 V operation
- 1 mA @ 3.3 V power down
- Integrated modem codec

❖ **Standard Features**

- Data
  - ITU-T V.90 (56 Kbps), V.34 (4.8 Kbps to 33.6 Kbps), V.32 bis (4.8 Kbps to 14.4 Kbps), V.22 bis (1.2 bps to 2.4 Kbps), V.21 and Bell 103 and 212 A(300 to 1200 bps) modulation protocol.
  - Data Compression: ITU-T V.42bis MNP Class 5
  - Error Correction: ITU-T V.42 LAPM MNP 2-4
  - ITU-T V. 17, V.29, V.27ter, V.21, Channel 2, Group 3, EIA Class I

- Fax



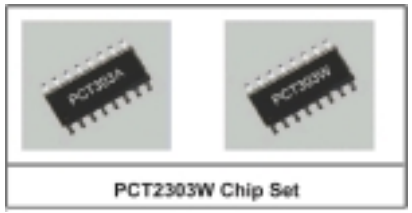


Figure 2: MDC PCT2303W

1.2.9 System Flash Memory (BIOS)

- Firmware Hub for Intel® 810, 810E, 815, 815E,815EP, 820, 840, 850 Chipsets
- Flexible Erase Capability
  - Uniform 4 KBytes Sectors
  - Uniform 16 KBytes overlay blocks for SST49LF002A
  - Uniform 64 KBytes overlay blocks for SST49LF004A
  - Top boot block protection
  - 16 KBytes for SST49LF002A
  - 64 KBytes for SST49LF004A
  - Chip-Erase for PP Mode
- Single 3.0-3.6 V Read and Write Operations
- Superior Reliability
- Firmware Hub Hardware Interface Mode
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top Boot Block

- Block Locking Register for all blocks
- Standard SDP Command Set
- Data# Polling and Toggle Bit for End-of-Write detection
- 5 GPI pins for system design flexibility
- 4 ID pins for multi-chip selection

1.2.10 Memory System: 64 MB, 128 MB, 256 MB, 512 MB (x64) 200-Pin DDR SDRAM SO-DIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64 MB (8 Megx64 [H]); 128 MB (16 Megx64, [H] and [HD]); 256 MB (32 Megx64 [HD]); 512 MB (64 Megx 64 [HD])
- VDD= VDDQ= +2.5 V ±0.2 V
- VDDSPD = +2.2 V to +5.5 V
- 2.5 V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge

- DQS edge-aligned with data for Reads; center-aligned with data for Writes
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6 µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125 µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.11 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHY Receiver is a Low-power, Physical-layer Device (PHY)

The VT6103L is a Physical Layer device for Ethernet 10Base-T and 100Base-TX using category 5 Unshielded and Type 1 Shielded cables. This VLSI device is designed for easy implementation of 10/100 Mb/s Fast Ethernet LANs. It interfaces to a MAC through an MII interface ensuring interoperability between products from different vendors.

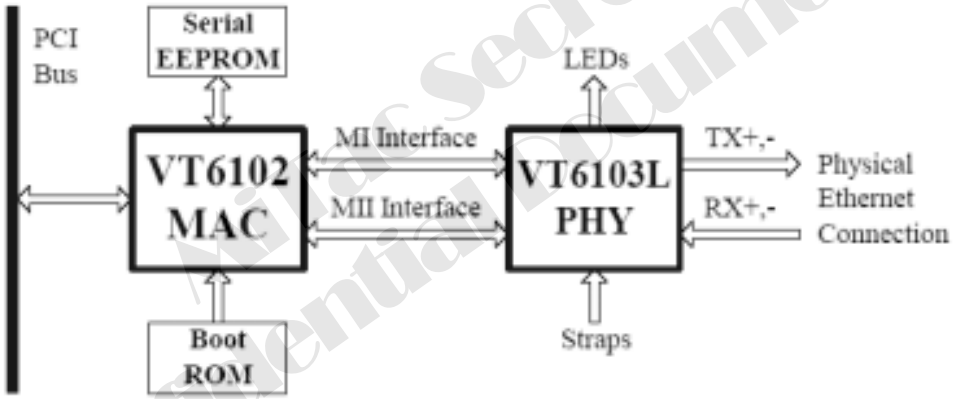


Figure 3: VT6103L PHY

Product Features

- Single Chip 100Base-TX/10Base-T Physical Layer Solution
- Dual Speed – 100/10 Mbps

8650 N/B Maintenance

- Half and Full Duplex
- MII Interface to Ethernet Controller
- MII Interface to Configuration & Status
- Auto Power Saving Mode
- Auto Negotiation: 10/100, Full/Half Duplex
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards
- On Chip Wave Shaping – No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs
  - Link Status
  - Duplex status
  - Speed Status
  - Collision
- 48 Pin LQFP Package

1.2.12 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2 k+256 bytes of RAM, four timer/counters, dual serial ports, 40 K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters.

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40 KB) and RAM size is 2 KB
- Support 4 Timer (8 bit) signal with 3 prescalers
- Support 2 PWM channels, 2 D-A and 8 A-D converters
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable

1.3 Other Functions

1.3.1 Hot Key Function (TBD)

Keys Combination	Feature	Meaning
Fn + F1	Wireless LAN	On/Off
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness Down	Decreases the LCD brightness.
Fn + F7	Brightness Up	Increases the LCD brightness.
Fn + F10	Mute system sound	On/Off Battery Low Beep
Fn + F11	LCD backlight On/Off	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power On/Off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode. Windows power management control panel set power button behavior.

You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

1.3.4.1 Three LED Indicators at Front Side

From left to right that indicate Battery Power, Battery Status and AC Power .

- Ac Power

  This LED lights green when the notebook was powered by AC power line, Flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by battery.

- Battery Power

  This LED lights green when the notebook is being powered by Battery, and flashes (on 1 second, off 1 second) when entered suspend to RAM state with AC powered. The LED is off when the notebook is in power off state or powered by AC adapter.

• Battery Status

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 seconds. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

1.3.4.2 Six LED Indicators

System have 6 status LED indicators at front side which to display system activity. From left to right that indicate Hard Disk, CD-ROM, Numlock, Caps Lock, Scroll Lock, Wireless LAN.

1.3.5 Battery Status

1.3.5.1 Battery Warning

- System also provides Battery capacity monitoring and gives users a warning signal to alarm they to store data before battery dead. This function also protects system from mal-function while battery capacity is low.
- Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.

- System will Suspend to HDD after 2 Minutes to protect users data.

1.3.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 11.5 V, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power On/Off Management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

- CR2032 3 V 220 mAh lithium battery.
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exists, CMOS battery life at less (220 mAh/5.8 uA) 4 years.

1.3.8 I/O Port

- One Power Supply Jack
- One External CRT Connector For CRT Display
- Supports four USB port for all USB devices
- One Modem RJ-11 phone jack for PSTN line
- One RJ-45 for LAN
- Headphone Out Jack
- Microphone Input Jack

1.3.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Power Management

The 8650 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full on Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without losing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.4.1.3 Standby Mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

- CPU: stop grant
- LCD: backlight off
- HDD: spin down

1.4.1.4 Suspend to DRAM & HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device .

- Suspend to DRAM
  - CPU: off
  - VIA PN800: partial off

- VGA: suspend
- PCMCIA: suspend
- Audio: off
- SDRAM: self refresh

➢ Suspend to HDD

- All devices are stopped clock and power-down
- System status is saved in HDD
- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: VIA VT8235CE GPIO Definitions (1)

Pin Name	Pin Number	MiTAC definition function	備註
GPI0 (VBAT)	AE2		4.7K to +VCC_RTC
GPI1 (VSUS33)	AC2	SCI#	10K to +3VS
GPI2 / EXTSMI# (VSUS33)	AA1	EXTSMI#	10K to +3VS
GPI3 / RING# (VSUS33)	Y2	WAKE_UP#	10K to +3VS
GPI4 / LID# (VSUS33)	AC1	LIDSW#	10K to +3VS
GPI5 / BATLOW# (VSUS33)	V4	CARD_RI#	10K to +3VS
GPI6 / AGPBZ#	AD10	AGPBUSY#	4.7K to +3V
GPI7 / REQ5#	R3	PCI_REQ5#	4.7K to +3V
GPI12 / GPO12 / INTE#	D4	PCI_INTE#	4.7K to +3V
GPI13 / GPO13 / INTF#	E4	MB_ID1	4.7K to +3V
GPI14 / GPO14 / INTG#	A3	MB_ID2	4.7K to +3V
GPI15 / GPO15 / INTH#	B3	ENABKL_SB	
GPI16 / INTRUDER# (VBAT)	AE1		4.7K to +VCC_RTC
GPI17 / CPUMISS	Y1	GPI17	4.7K to +3V
GPI18 / THRM# / AOLGPI	Y4	SB_THRM#	10K to +3V
GPI20 / GPO20 / ACSDIN2 / PCS0#	U1		4.7K to GND
GPI21 / GPO21 / ACSDIN3 / PCS1# / SLPB#	V3		4.7K to GND
GPI22 / GPO22 / GHI#	R22	MINIPCI_ACT#	10K to +3V
GPI23 / GPO23 / DPSLP#	P21	HDPSLP#	150ohm to +VCCP
GPI26 / GPO26 / SMBDT2 (VSUS33)	AD1	CRT_IN#	4.7K to +3VS

1.5 Appendix 1: VIA VT8235CE GPIO Definitions (2)

Continue to previous page

Pin Name	Pin Number	MiTAC definition function	備註
GPI27 / GPO27 / SMBCK2 (VSUS33)	AC3	KBD_US/JP#	4.7K to +3VS
GPI28 / GPO28	AC8	B/CB#	10K to +3V
GPI29 / GPO29 / VRDPSLP	AB9	DPRSLPVR	4.7K to +3V
GPO0 (VSUS33)	AA3	WIRELESS_PD#	10K to +3VS
GPO1 / SUSA# (VSUS33)	AA2	SUSA#	10K to +3VS
GPO2 / SUSB# (VSUS33)	AD3	SUSB#	
GPO3 / SUSST1# (VSUS33)	Y3	SUSST#	10K to +3VS
GPO4 / SUSCLK (VSUS33)	AB3	SPK_OFF	10K to +3VS
GPO5 / CPUSTP#	AC7	CPU_STP#	4.7K to +3V
GPO6 / PCISTP#	AD6	PCI_STP#	4.7K to +3V
GPO7 /GNT5#	R2	SB_BT_ON#	

1.6 Appendix 2: W83L950D KBC Pins Definitions (1)

Pin Name	Pin Number	MiTAC definition function	備註
GP0/P3REF/FA0	54	KO0	
GP1/FA1	53	KO1	
GP2/FA2	52	KO2	
GP3/FA3	51	KO3	
GP4/FA4	50	KO4	
GP5/FA5	49	KO5	
GP6/FA6	48	KO6	
GP7/FA7	47	KO7	
GP10/FA8	46	KO8	
GP11/FA9	45	KO9	
GP12/FA10	44	KO10	
GP13/FA11	43	KO11	
GP14/FA12	42	KO12	
GP15/FA13	41	KO13	
GP16/FA14	40	KO14	
GP17/FA15	39	KO15	
GP20/FD0/LPCEN	38	H8_THRM#	
GP21/FD1	37	H8_WAKE_UP#	
GP22/FD2/SDA1/RXD1	36	BATT_G#	
GP23/FD3/SCL1/TXD1	35	BATT_R#	
GP24/FD4	34	EXTSMI#	10K to +3VS
GP25/FD5	33	CAP#	
GP26/FD6	32	NUM#	

1.6 Appendix 2: W83L950D KBC Pins Definitions (2)

Continue to previous page

Pin Name	Pin Number	MiTAC definition function	備註
GP27/FD7	31	SCROLL#	
GP30/PWM0/FCTRL0	62	KI0	
GP31/PWM10/FCTRL1	61	KI1	
GP32/FCTRL2	60	KI2	
GP33/FCTRL3#	59	KI3	
GP34/BANK0	58	KI4	
GP35/BANK1	57	KI5	
GP36/CE#	56	KI6	
GP37/OE#	55	KI7	
GP40/XOUT/PWM2	27	KBC_BEEP	
GP41/XCIN/PWM3	26	CHARGING	
GP42/INT0/OBF00	23	LEARNING	
GP43/INT1/OBF01	22	H8_SUSB	10K to VDD3
GP44/RXD	21	H8_RCIN#	
GP45/TXD	20	A20GATE	4.7K to +3VS
GP46/SCLK1/OBF1	19	H8_SCI	10K to VDD3
GP47/SRDY1#/S1	18	H8_PWRON_1	
GP50/A0	17	SW_VDD3	
GP51/INT20#/S0	16	H8_LIDSW#	
GP52/INT30#/R	15	BATT_DEAD#	10K to VDD3
GP53/INT40#/W	14	H8_ADEN#	10K to VDD3
GP54/CNTR0	13	SB_PWRGD	4.7K to GND
GP55/CNTR1	12	KBC_PWRON_VDD3S	
GP56/DA1/PWM01	11	BLADJ	0.1U to GND

1.6 Appendix 2: W83L950D KBC Pins Definitions (3)

Continue to previous page

Pin Name	Pin Number	MiTAC definition function	備註
GP57/DA2/PWM11	10	H8_I_CTR	
GP60/AN0/INT5	1	PWRBTN#	10K to VDD3
GP61/AN1/INT6	80	BATT_LED#_1	
GP62/AN2/INT7	79	AC_POWER#	
GP63/AN3/INT8	78	BAT_VOLT	
GP64/AN4/INT9	77	BAT_TEMP	
GP65/AN5/INT10	76	H8_I_LIMIT	
GP66/AN6/INT11	75	VRMPWRGD	1K to +3VS_P
GP67/AN7/INT12	74	KBC_CPUCORE	
GP70/SIN2	9	T_DATA	10K to +5V
P71/SOUT2	8	H8_RSMRST	10K to VDD3
GP72/SCLK2	7	SB_PWRBTN	10K to VDD3
GP73/SRDY2#/INT21	6	T_CLK	10K to +5V
GP74/INT31	5	H8_PWRON_SUSB#	1K to VDD3S
GP75/INT41	4	H8_SUSC#	
GP76/SDA	3	BAT_DATA	2.7K to VDD3
GP77/SCL	2	BAT_CLK	2.7K to VDD3
GP80/SD0	70	PCICLK_KBC	
GP81/SD1	69	SERIRQ	4.7K to +3V
GP82/SD2	68	LAD3	
GP83/SD3	67	LAD2	
GP84/SD4	66	LAD1	
GP85/SD5	65	LAD0	

1.6 Appendix 2: W83L950D KBC Pins Definitions (4)

Continue to previous page

Pin Name	Pin Number	MiTAC definition function	備註
GP86/SD6	64	KBC_PCIRST#	
GP87/SD7	63	LFRAME#	
AVSS	73	GND	
VREF	72	VDD3_AVREF	
VCC	71	VDD3	
VSS	30	GND	
XOUT	29	XOUT	
XIN	28	XIN	
RESET#	25	H8_RESET#	
CNVSS	24	EXT_FLASH	10K to GND

1.7 Appendix 3: 8650 External Specifications, R00 (1)

8650 Prelimernary Specifications	
Model	**8650**
CPU	Intel Celeron-M Processor /VIA C7 FSB 400MHz
Chip Set	VIA PN800+VT 8235CE
L2 Cache	1M(Celeron-M, Dothan core)
System BIOS	512KB Flash EPROM - include System BIOS, VGA BIOS - Plug&Play capability -ACPI
Memory	0MB DDR266/333 SDRAM memory on board, support one channel - 2 memory DIMM slots for memory expansion - 200pin DDR333/400 SDRAM SO-DIMM Memory Module - Expandable to 1,024MB - 1.25-inch height memory module supported
Video Controller	SMA
Optical drive	Combo / DVD+RW, DVD-RW, DVD-Dual (12.7mm) Detected as 2nd Master (by ODD F/W)
FDD	N/A
HDD	2.5" 30GB/40GB/60GB/80GB HDD(9.5mm) 4200rpm or 5400rpm - Ultra DMA 100
Display	15.4" Wide WXGA TFT -Resolution: 1280x800

1.7 Appendix 3: 8650 External Specifications, R00 (2)

Continue to previous page

Keyboard	European keyboard layout(Use the Orignal KBD that 8050F model used) - 19mm key pitch / 3mm stroke - Hot key spec: Fn+F1 : Wireless LAN ON/OFF (for 8050FX, no function) Fn+F3/F4 : Volume down/up, Fn+F5 : LCD/CRT output change Fn+F6/F7: Brightness up/down, Fn+F11: Display ON/OFF, Fn+F12: Standby
Pointing Device	TouchPad (No scroll button)
PC Card Slot	TypeII x 1 -PCMCIA Standard Rev.2.1 , CardBus support , w/o ZV port
Audio System	Built-in Sound system - AC97 I/F - 16-bit Sampling and Playback - 16-bit stereo - Full duplex supported - 3D sound supported - AC-3 support - Built-in stereo speaker, Built-in microphone - Sound Volume control by Hot-Key (Fn + F3 : Volume down, Fn + F4 : Volume up)
I/O Port	USB(2.0) x 3 Reserved for 1 internal USB Mic-in x 1(Mono) Headphone-out/SPDIF x 1 (Stereo) Line-in x 1(Stereo) RJ-45 LAN Jack x 1 (with cap) RJ-11 Modem Jack x 1 (with cap) VGA port x 1 DC-in x 1 TV out H/W reserved (ME with Slide)

1.7 Appendix 3: 8650 External Specifications, R00 (3)

Continue to previous page

Communication	56Kbps(V.90) Fax Modem(MDC) and 100Base-TX LAN Wireless LAN (3B type Mini PCI Interface IEEE802.11b, g) Single Antenna
Battery	Li-ion Battery 2200mAh(6-cell) - Battery Life: (120min w/z 256M Memory, 1.4GHz CPU, Backlight: Mid.) -RTC bckup battery(Lithium) Standard -Power-ON charge available
Power Supply	65W Universal AC Adapter(100-240V)
Safety Lock	Kensington Lock x 1
Dimension	W353.8 x D250 x H25~32mm (B, D parts without painting)
Weight	3.0kg
OS	Windows XP Pro w/z SP2
Accessories	TBD
Windows Logo	Support PC2001 Specification - Need to get the Log files for Windows XP Pro, WHQL Certified
EMI / Safety / Regulation	EMI:CE/TUV/CB FCC PTT:CE

P: for pendding issue

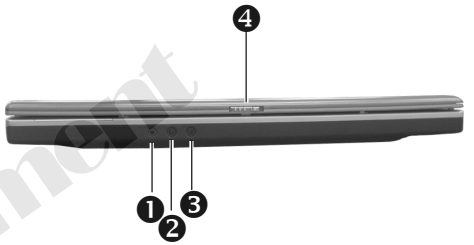
EMI: Golden Sample:-3db, MP: Under limit

Painting: ABCD w/o painting

2. System View and Disassembly

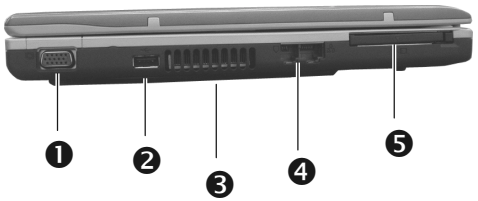
2.1 System View

2.1.1 Front View



❶ Line Out Connector
❷ Line In Connector
❸ MIC In Connector
❹ Top Cover Latch

2.1.2 Left-side View



❶ VGA Port
❷ USB Port
❸ Ventilation Openings
❹ RJ-11&RJ-45 Connector
❺ PCMCIA Card Socket

2.1.3 Right-side View

❶ CD-ROM/DVD-ROM Drive

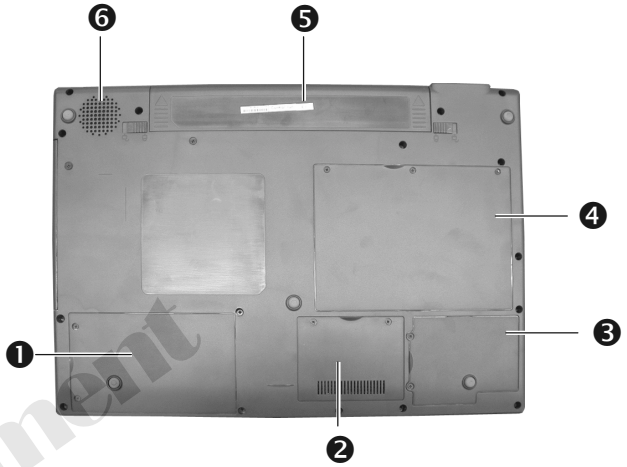
2.1.4 Rear View

❶ Kensington Lock

❷ Power Connector

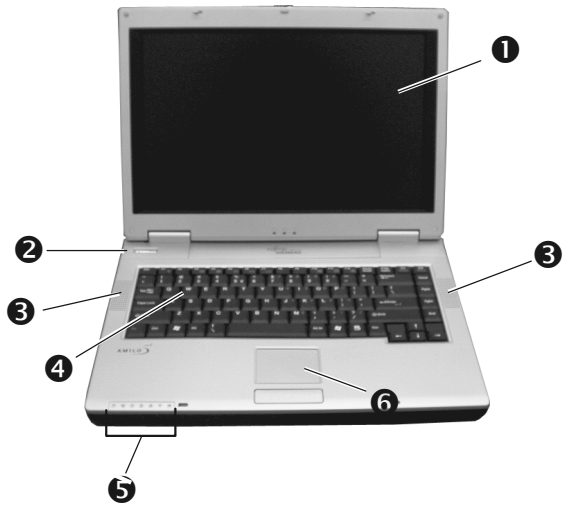
❸ USB Port*2

2.1.5 Bottom View



❶ Hard Disk Drive
❷ DDR SDRAM Card
❸ Modem & Wireless Card
❹ CPU
❺ Battery Park
❻ Stereo Speaker Set

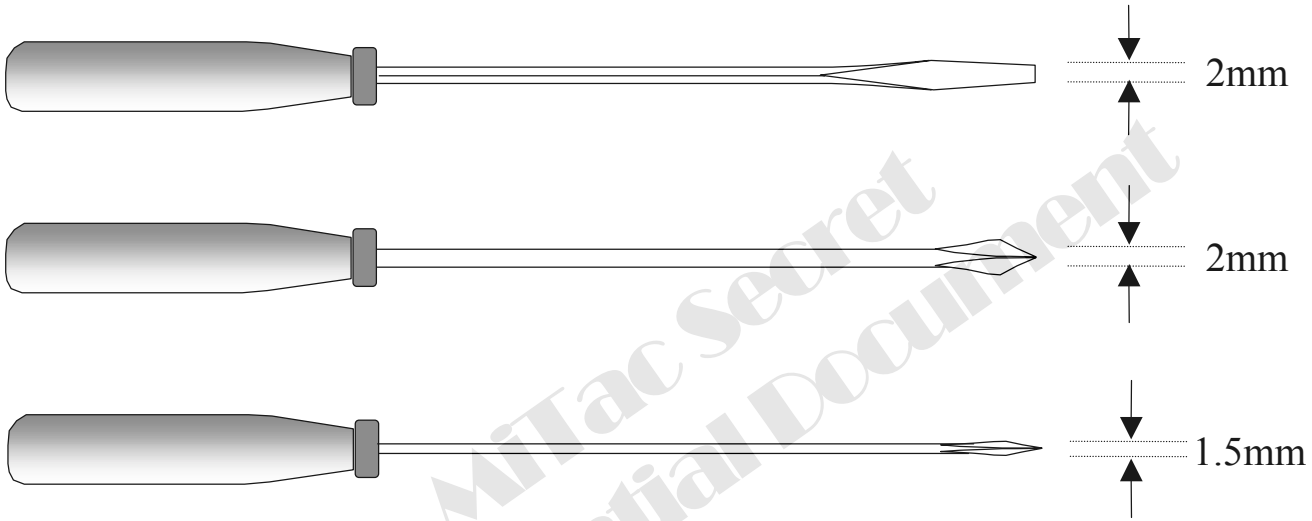
2.1.6 Top-open View



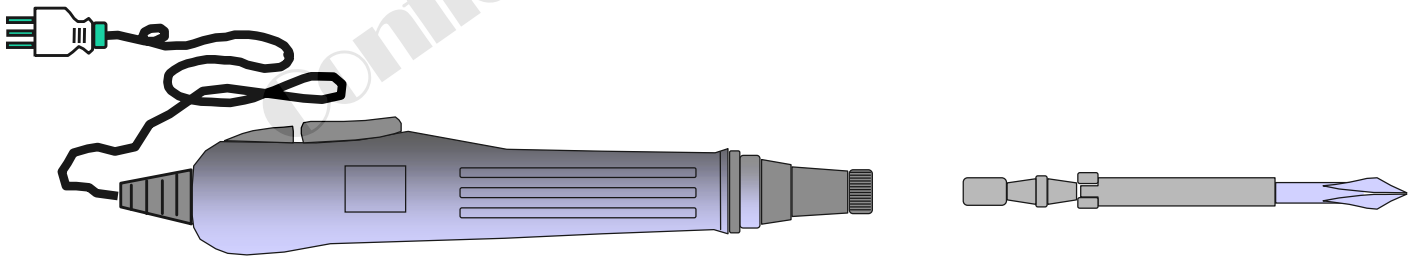
❶ LCD Screen
❷ Power Button
❸ Stereo Speaker Set
❹ Keyboard
❺ Device LED Indicators
❻ Touch Pad

2.2 Tools Introduction

1. Minus screw driver with bit size 2mm and 1.5mm for notebook assembly & disassembly. .



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

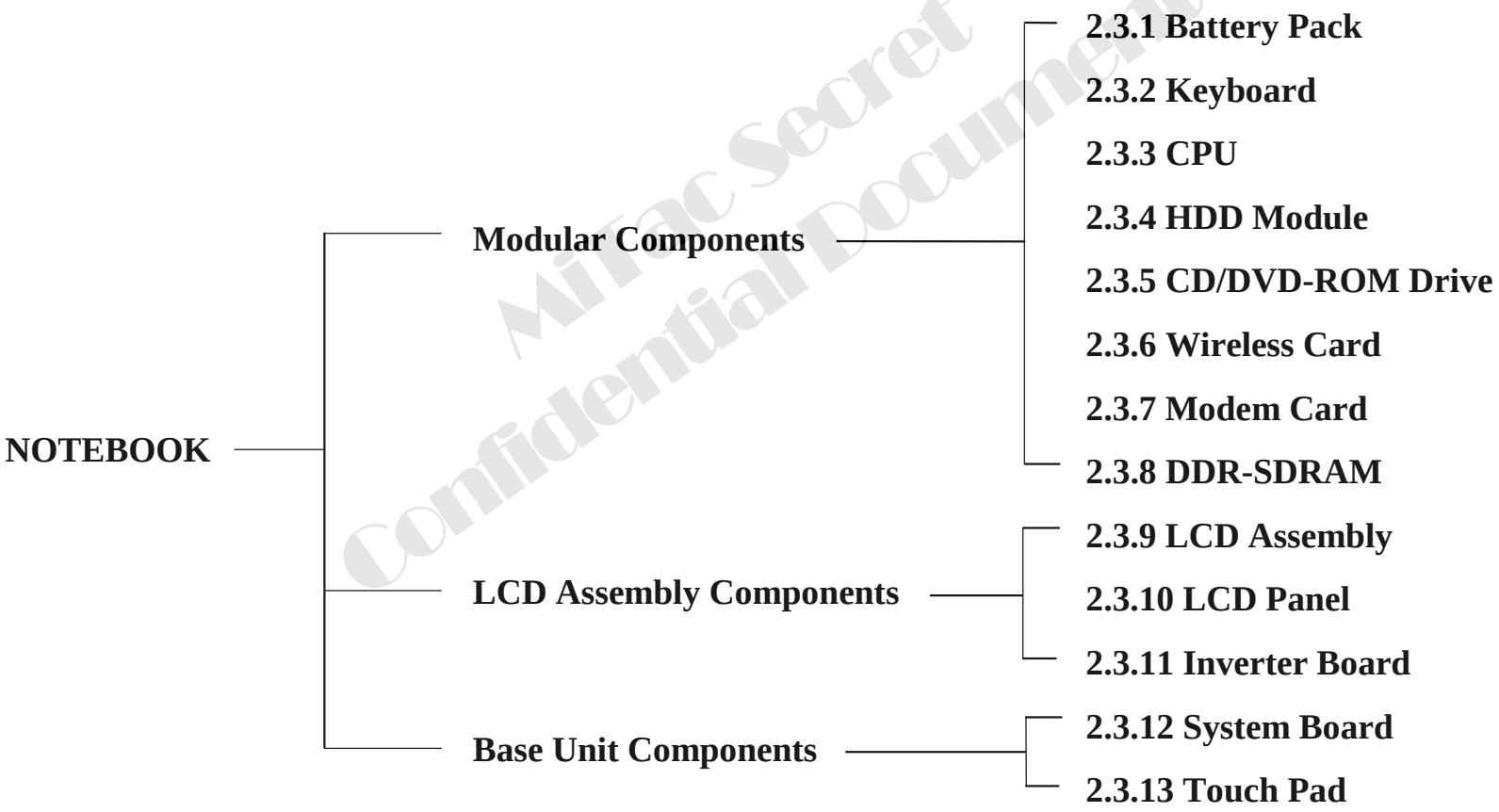
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide two release lever outwards to the “unlock” ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

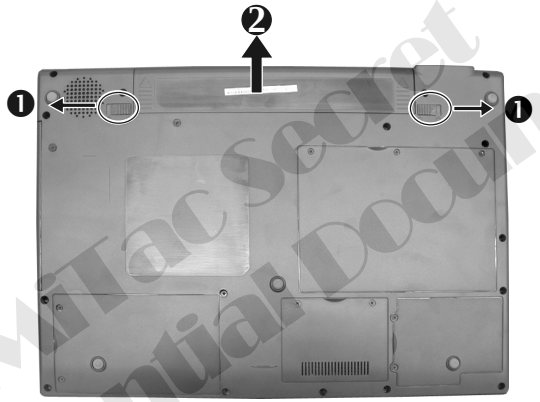


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” ( ) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Open the top cover.
3. Loosen five latches locking the keyboard. (Figure 2-2)
4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-3)

Figure 2-2 Loosen the five latches

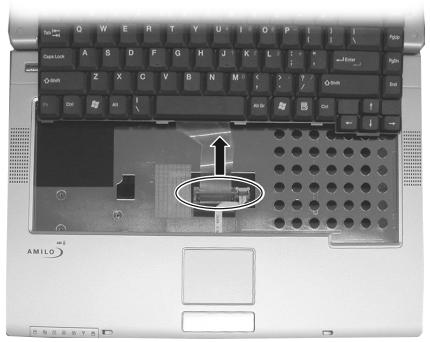


Figure 2-3 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with five latches.
2. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove three screws fastening the heatsink cover. (Figure 2-4)
3. Remove three spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-5)

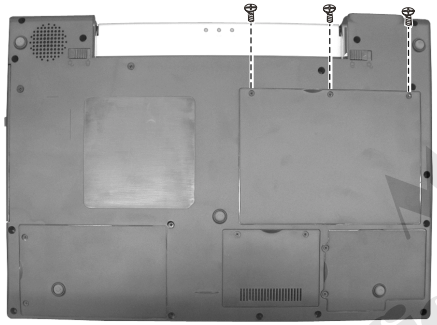


Figure 2-4 Remove three screws

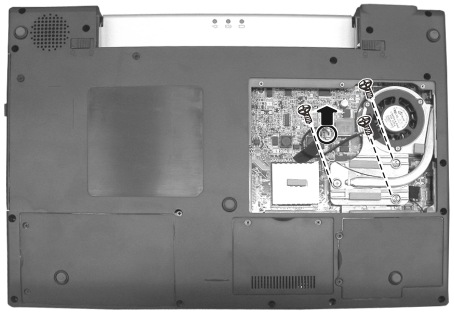


Figure 2-5 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screw driver, upraise the CPU socket to unlock the CPU. (Figure 2-6)

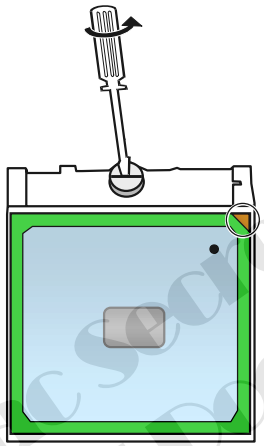


Figure 2-6 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with three spring screws.
3. Replace the CPU cover and secure with three screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove one screw and slide the HDD module out of the compartment. (Figure 2-8)

Figure 2-7 Remove the HDD compartment cover

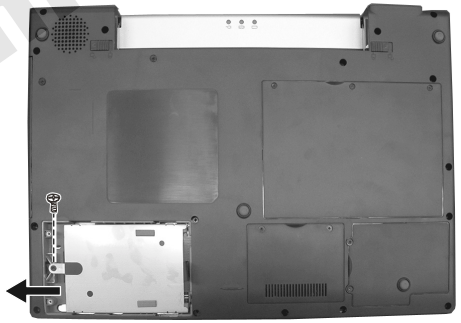


Figure 2-8 Remove HDD module

4. Remove four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-9)

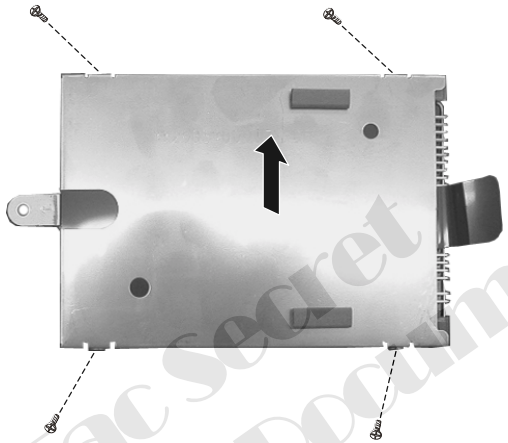


Figure 2-9 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-10)

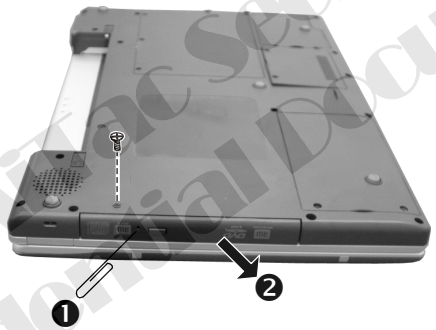


Figure 2-10 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.6 Wireless Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.3.1 Disassembly)
2. Remove two screws fastening the Mini PCI compartment cover. (Figure 2-11)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-12)

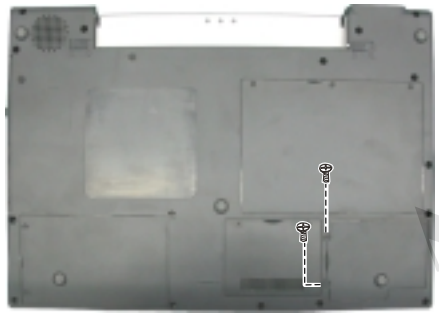


Figure 2-11 Remove two screws

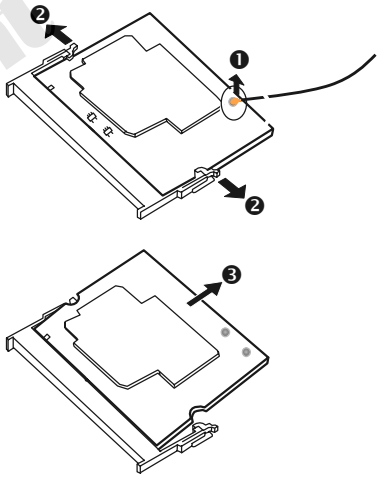


Figure 2-12 Remove the Wireless card

Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Tighten the screws to secure the wireless card compartment cover to the housing.
3. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening modem card's compartment cover. (Refer to steps 1-2 of section 2.3.6 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-13)
4. Lift up the modem card and disconnect the cord. (Figure 2-14)

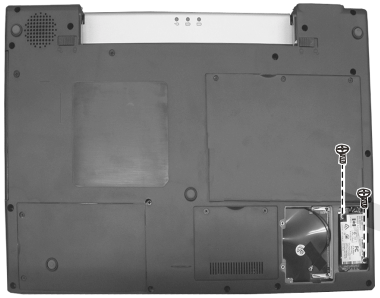


Figure 2-13 Remove two screws

Figure 2-14 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the modem card's compartment cover by two screws. (Refer to step 2 of section 2.3.6 reassembly).
4. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.8 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (See section 2.3.1 disassembly)
2. Remove two screws fastening the DDR compartment cover to access the SO-DIMM socket. (Figure 2-15)
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-16)

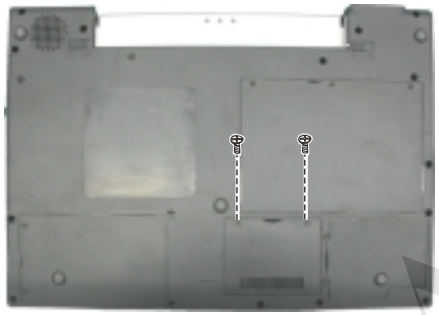


Figure 2-15 Remove the cover

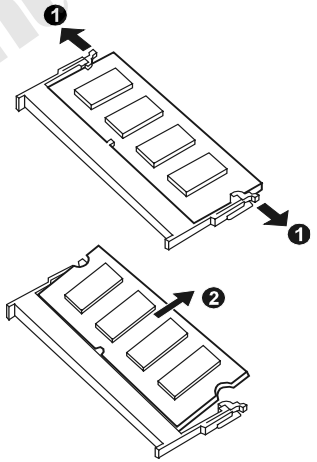


Figure 2-16 Remove the SO-DIMM

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace two screws to fasten the DDR compartment cover.
3. Replace the battery pack. (See section 2.3.1 reassembly)

2.3.9 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-drive, wireless card, modem card and DDR. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Remove nineteen screws on the bottom of notebook. (Figure 2-17)
3. Remove four screws that secure the hinge cover. (Figure 2-18)

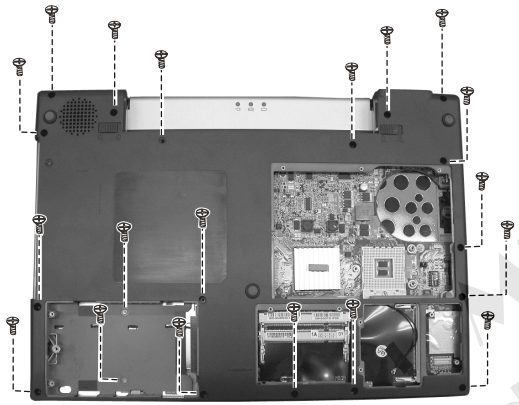


Figure 2-17 Remove nineteen screws

Figure 2-18 Remove four screws

4. Remove two screws and disconnect the touch pad's cable, then free the top cover. (Figure 2-19)
5. Remove two hinge covers. (Figure 2-20)

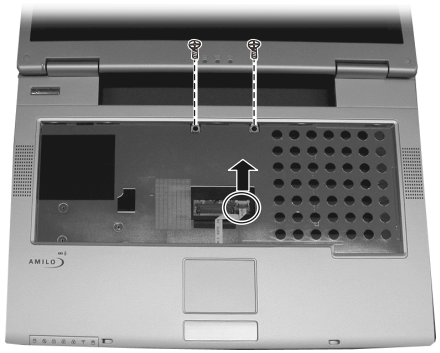


Figure 2-19 Free the top cover

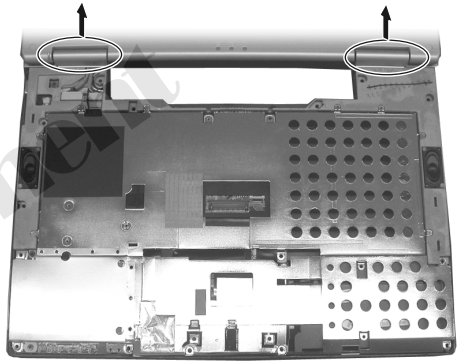


Figure 2-20 Remove the hinge covers

6. Disconnect two cables and remove four screws. (Figure 2-21)
7. Remove eight screws. (Figure 2-22)

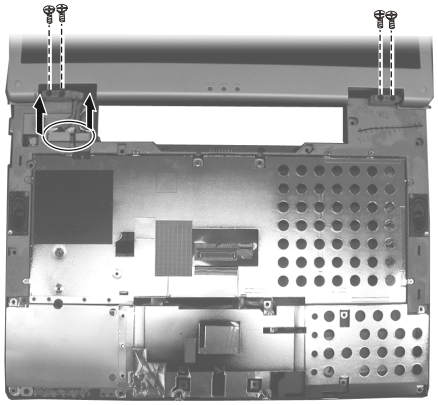


Figure 2-21 Remove four screws and Disconnect two cables

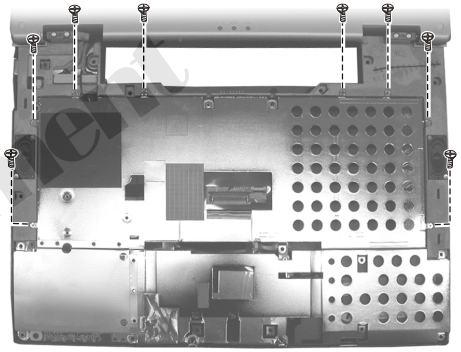


Figure 2-22 Remove eight screws

8. Carefully pull the antenna wires out. Now you can lift up the LCD ASSY from base unit. (Figure 2-23)

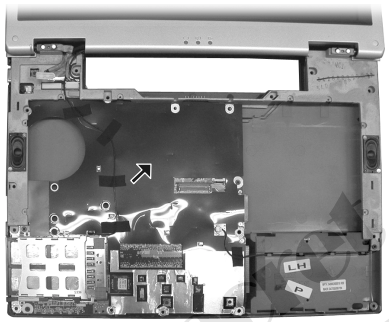


Figure 2-23 Free the LCD ASSY

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Rip the antenna wires back into Min-PCI compartment.
3. Reconnect two cables to the system board. Screw the hinge covers by two screws.
4. Replace the shield and secure with eight screws.
5. Replace the top cover and secure with two screws. And reconnect the touch pad's cable.
6. Upside down the notebook. secure the housing by nineteen screws and secure two screws in the rear.
7. Replace the DDR, modem card, Wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to sections 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 reassembly)

2.3.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.3.1, 2.3.2, 2.3.4, 2.3.5 and 2.3.9 Disassembly)
2. Remove two mylar pads and two screws on the corners of the panel. (Figure 2-24)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove ten screws and disconnect the cable. (Figure 2-25)

Figure 2-24 Remove LCD cover

Figure 2-25 Remove ten screws and disconnect the cable

5. Remove six screws that secure the LCD bracket. (Figure 2-26)
6. Disconnect the cable to free the LCD panel. (Figure 2-27)

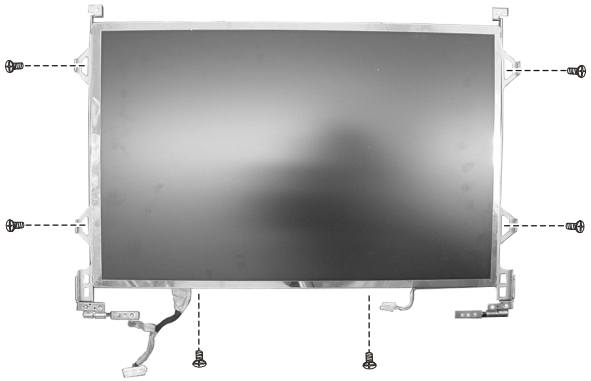


Figure 2-26 Remove six screws

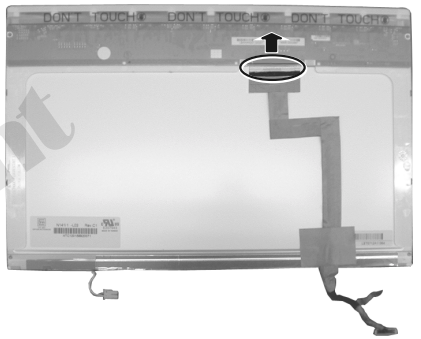


Figure 2-27 Free the LCD panel

Reassembly

1. Replace the cable to the LCD.
2. Attach the LCD panel's bracket back to LCD panel and secure with six screws.
3. Replace the LCD panel into LCD housing. And reconnect two cables to inverter board and secure with two screws.
4. Fasten the LCD panel by ten screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, CD/DVD-ROM drive, hard disk drive, keyboard, battery pack. (See sections 2.3.9, 2.3.5, 2.3.4, 2.3.2, and 2.3.1 reassembly)

2.3.11 Inverter Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.3.1, 2.3.2, 2.3.4, 2.3.5 and 2.3.9 Disassembly)
2. Remove the LCD cover and LCD panel. (Refer to the steps 1-4 of section 2.3.10 Disassembly)
3. Remove one screw fastening the inverter board and disconnect the cable, Then free the inverter board. (Figure 2-28)

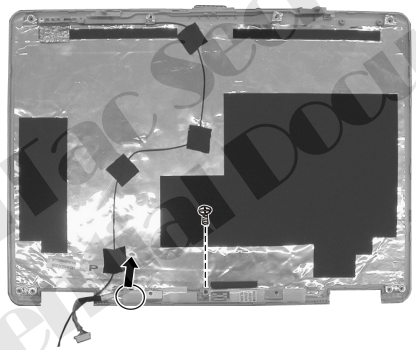


Figure 2-28 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD Panel and LCD cover. (Refer to section 2.3.10 reassembly)
3. Replace the LCD assembly. (Refer to section 2.3.9 reassembly)
4. Replace the CD/DVD-ROM drive hard disk drive, keyboard and battery pack. (Refer to sections 2.3.5, 2.3.4, 2.3.2 and 2.3.1 reassembly)

2.3.12 System Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive, Wireless card and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.4, 2.3.5, 2.3.6 and 2.3.9 Disassembly)
2. Remove four screws that secure the system board and disconnect one speaker's cables. Then lift it up from the housing. (Figure 2-29)
3. Disconnect the other speaker's cables from the system board and remove two screws, Then separate the bracket and free the system board. (Figure 2-30)

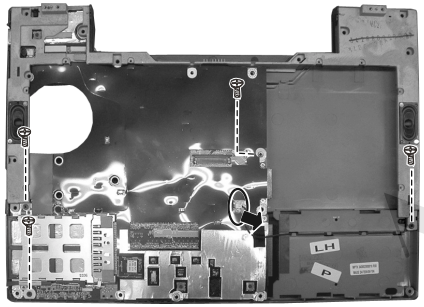


Figure 2-29 Remove four screws and disconnect the two cables

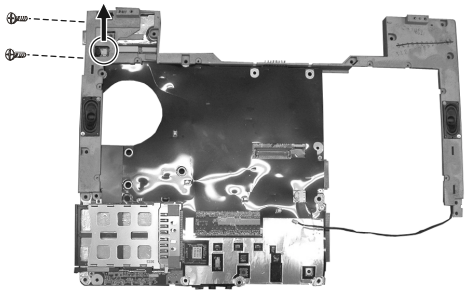


Figure 2-30 Free the system board

Reassembly

1. Fit the bracket and secure with two screws .
2. Turn over the system board. Reconnect the speaker's cords.
3. Replace the system board back into the housing and secure with four screws, then reconnect the cable.
4. Replace the LCD assembly, CD/DVD-ROM, HDD, keyboard and battery pack. (Refer to previous section reassembly)

2.3.13 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.3.1, 2.3.2, 2.3.4 and 2.3.5 Disassembly)
2. Remove the top cover. (See steps 1-5 in section 2.3.9 Disassembly)
3. Remove two screws and free the touch pad. (Figure 2-31).

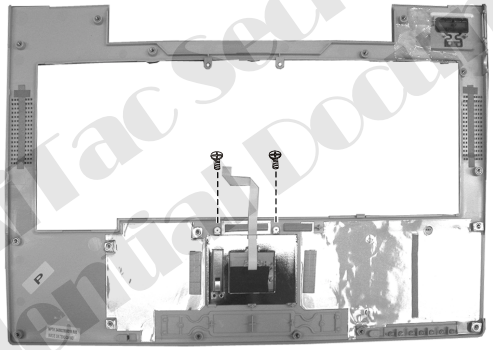


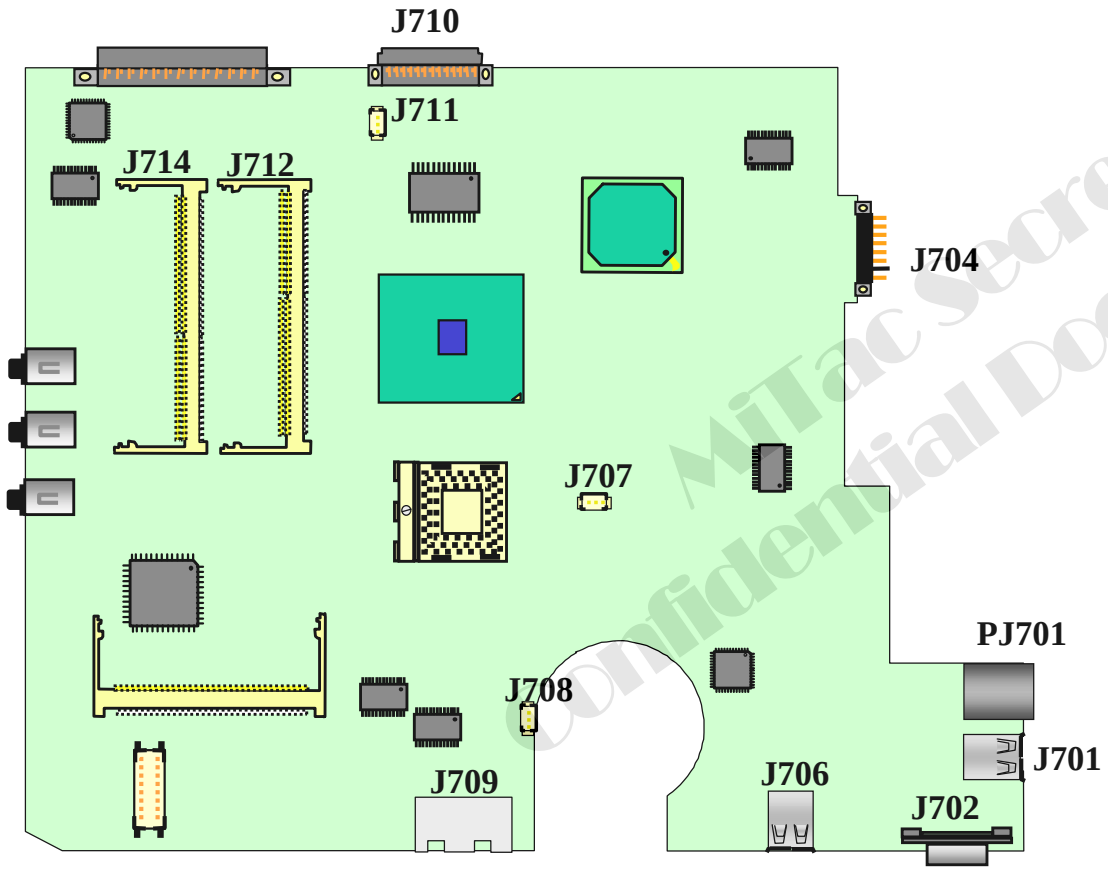
Figure 2-31 Remove the two screws

Reassembly

1. Replace the touch pad and secure two screws.
2. Replace the top cover. (Refer to the section in 2.3.9 reassembly)
3. Replace the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.3.1, 2.3.2, 2.3.4 and 2.3.5 Disassembly).

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side A) - 1

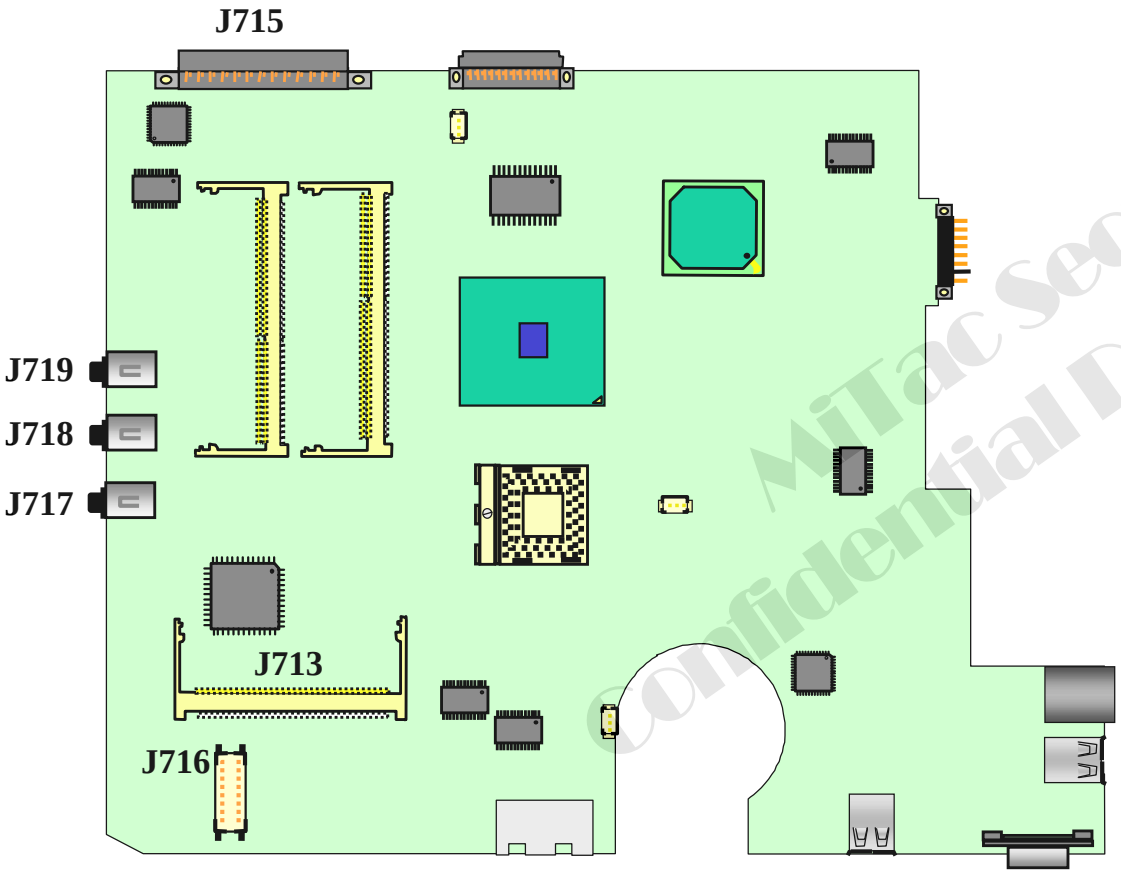


- PJ701: Power Jack
- J701,J706: USB port
- J702: External VGA Connector
- J704: Battery Connector
- J707: CPU Fan Connector
- J708: Modem Jump Wire Connector
- J709: RJ11 & RJ45 Connector
- J710: Secondary IDE Connector
- J711: RTC Connector
- J712,J714: Extend DDR SDRAM Socket

------ To next page ------

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side A) - 2



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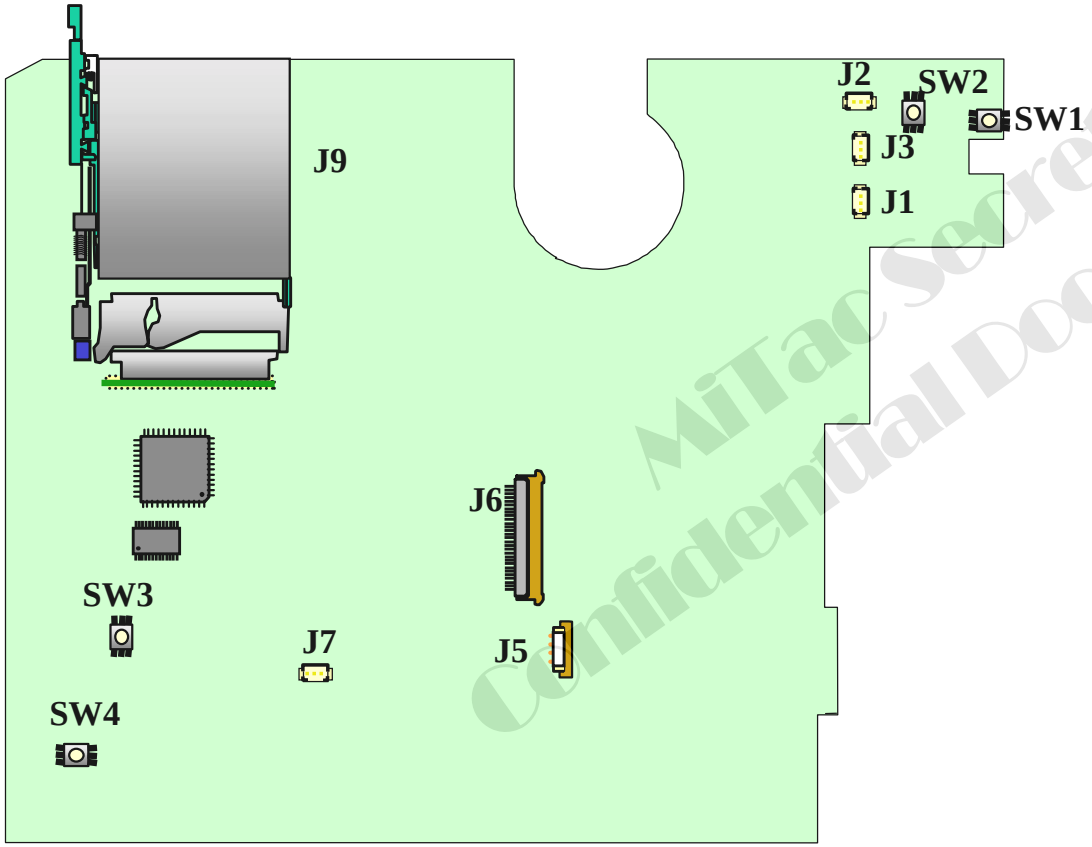
- J713: Mini-PCI Socket
- J715: Primary IDE Connector
- J716: MDC Board Connector
- J717: Line Out Jack
- J718: Line In Jack
- J719: Mic In Jack

3. Definition & Location of Connectors/Switches

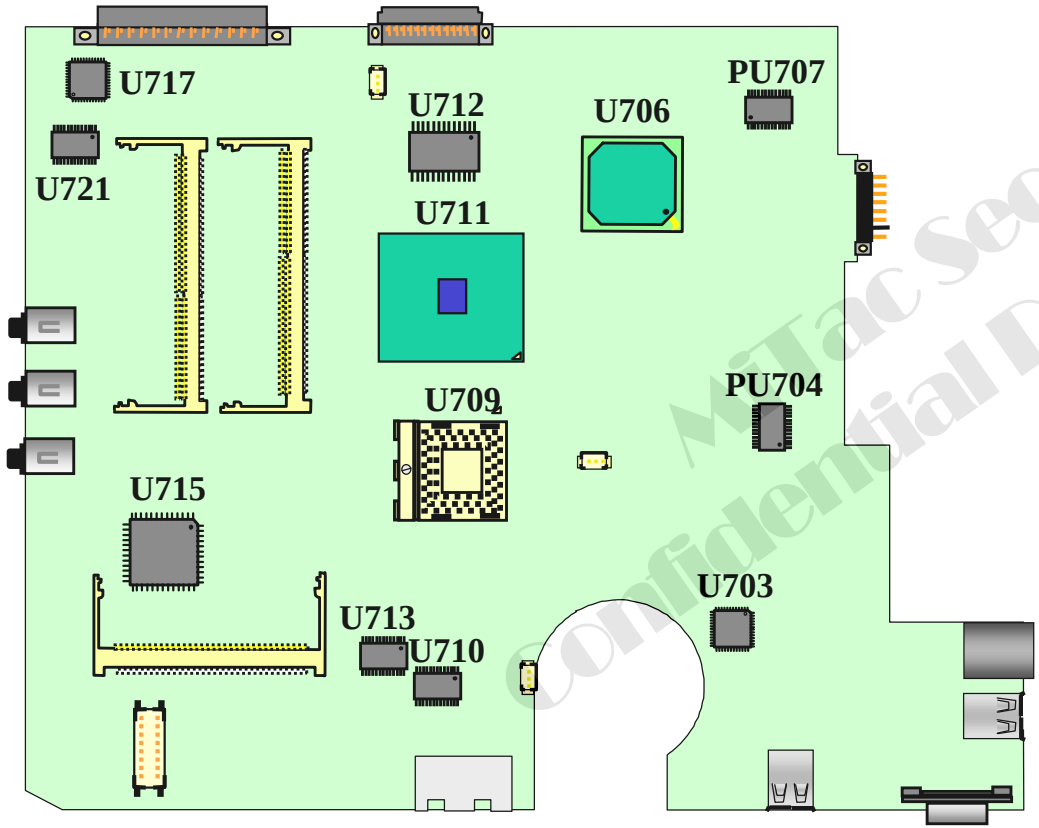
3.2 Mother Board (Side B)



- J1: LCD Inverter Board Connector
- J2: Internal Left Speak Connector
- J3: LCD Connector
- J5: Touch Pad Connector
- J6: Internal Keyboard Connector
- J7: Internal Right Speak Connector
- J9: PCMCIA Card Socket
- SW1: Cover Switch Button
- SW2: Power Button
- SW3: T/P Left Button
- SW4: T/P Right Button

4. Definition & Location of Major Components

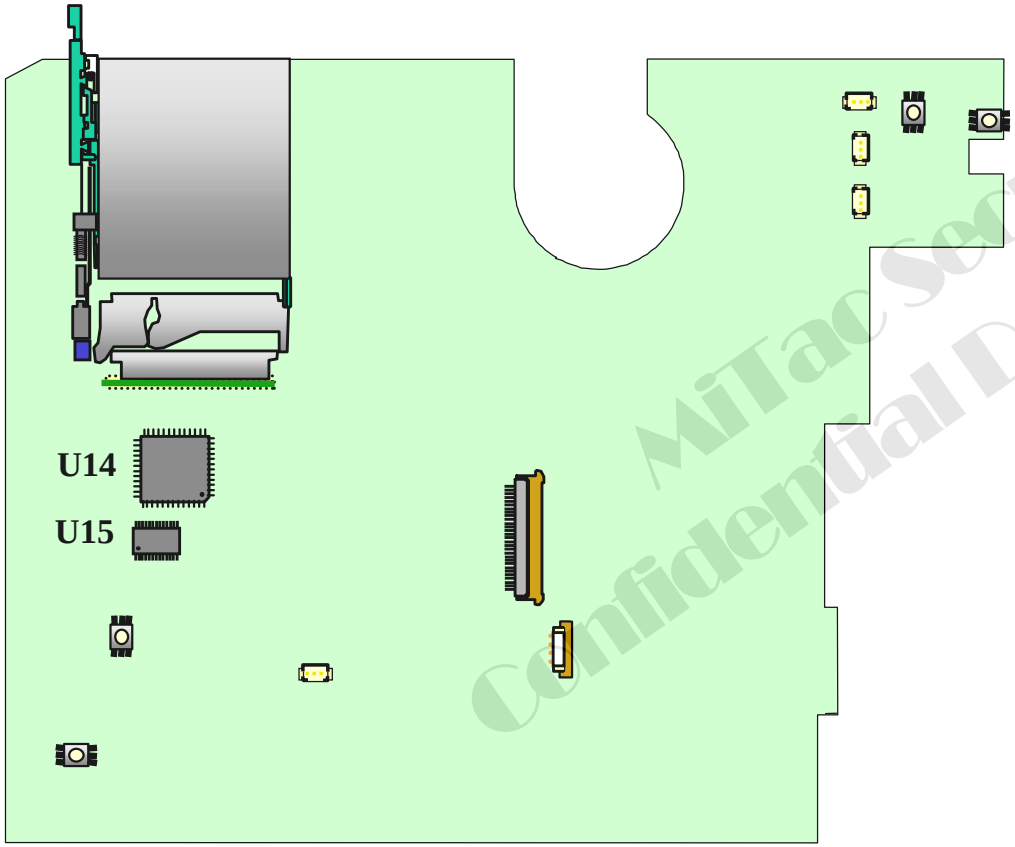
4.1 Mother Board (Side A)



- U703: VT1634AL LVDS Transmitter
- U706: SB VT8235CE
- U709: CPU (BANIAS) Socket
- U710: NS681680P LAN Buffer
- U711: NB VIA_PN800
- U712: ICS950902 Clock Synthesizer
- U713: VT6103L LAN Controller
- U715: ENE CB1410 Card Bus
- U717: KBC (W83L950D)
- U721: ALC655 Audio Codec
- PU704: ISL6218 CPU-CORE
- PU707: TL594C Battery Charging

4. Definition & Location of Major Components

4.2 Mother Board (Side B)



- U14: System Flash BIOS
- U15: TPA0212 Audio Amplifier

5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor CPU - 1

CPU Pin Description

`Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. Signals / Associated Strobe REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

CPU Pin Description Continue

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** Data Group / DSTBN#/DSTBP# / DINV# D[15:0]# / 0 / 0 D[31:16]# / 1 / 1 D[47:32]# / 2 / 2 D[63:48]# / 3 / 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Pentium M Processor CPU - 2

CPU Pin Description Continue

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

CPU Pin Description Continue

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Pentium M Processor CPU - 3

CPU Pin Description Continue

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

CPU Pin Description Continue

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Pentium M Processor CPU - 4

CPU Pin Description Continue

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

CPU Pin Description Continue

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 PN800 North Bridge - 1

CPU Interface

Signal Name	Pin #	I/O	Signal Description
HA[35:3]#	(see pin lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the North Bridge during cache snooping operations. Address signals up through HA[35]# allow future support of a 64 Gbyte memory space (the current design supports up to HA[33]# for support of 16 GB)..
HADSTB [1:0]#	C26, A22	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HASTB1# is the strobe for HA[31:17]# and HASTB0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see pin lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDBI[3:0]#	A5, J3, B13, A6	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTBP [3:0]# **HDSTBN [3:0]#**	D1, H3, E13, F8 E1, H2, D13, D8	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTBP3# / HDSTBN3# are the strobes for HD[63:48]# & HDBI3#; HDSTBP2# / HDSTBN2# are the strobes for HD[47:32]# & HDBI2#; HDSTBP1# / HDSTBN1# are the strobes for HD[31:16]# & HDBI1#; and HDSTBP0# / HDSTBN0# are the strobes for HD[15:0]# & HDBI0#.
ADS#	A19	IO	**Address Strob**e. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	B19	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	C19	IO	**Data Read**y. Asserted for each cycle that data is transferred.
HIT#	C17	IO	**Hi**t. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	F16	I	**Hit Modifie**d. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.

CPU Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
HLOCK#	F18	I	**Host Loc**k. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	F19, E19, D20, C20, D19	IO	**Request Comman**d. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G18	IO	**Host Target Read**y. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	B17, D18, B18	IO	**Response Signal**s. Indicates the type of response per the table below: **RS[2:0]# Response type RS[2:0]# Response type** 000 Idle State 100 Hard Failure 001 Retry Response 101 Normal Without Data 010 Defer Response 110 Implicit Writeback 011 Reserved 111 Normal With Data
DPWR#	G15	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
BREQ0#	E18	O	**Bus Request 0.** Bus request output to CPU.
BPRI#	C16	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PN800 drives this signal to gain control of the processor bus.
BNR#	C18	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	E17	IO	**Defe**r. The PN800 uses a dynamic deferring policy to optimize system performance. The PN800 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	K6	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock pin description group).

5.2 PN800 North Bridge - 2

DDR SDRAM Interface – "A" Data

Signal Name	Pin #	I/O	Signal Description
MDA[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMA[7:0]	AT16, AP20, AP24, AN32, AD35, V34, L33, D36	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSA[7:0]#	AR16, AN20, AT24, AT33, AD34, U34, L31, D35	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSA[3:0]#	AP25, AP29, AR25, AT25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEA[3:0]	L34, R35, M35, T33	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

DDR SDRAM Interface – "B" Data

Signal Name	Pin #	I/O	Signal Description
MDB[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMB[7:0]	AN18, AP22, AR28, AG32, Y33, N35, H36, A34	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSB[7:0]#	AP18, AR22, AT28, AG33, Y34, N34, H34, A33	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSB[3:0]#	AP28, AR29, AT29, AT30	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEB[3:0]	J35, K31, J33, K32	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

5.2 PN800 North Bridge - 3

AGP 8x / 4x Bus Interface

Signal Name	Pin #	I/O	Signal Description
GADSTB1F (GADSTB1 for 4x), **GADSTB1S** (GADSTB1# for 4x)	AG3 AG1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTB1F ("First" strobe) and GADSTB1# as GADSTB1S ("Second" strobe). GADSTB1 and GADSTB1# provide timing for 4x transfer mode.
GFRAME (GFRAME# for 4x)	AL4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GDEVSEL (GDEVSEL# for 4x)	AK1	IO	**Device Select (PCI transactions only).** Driven by the North Bridge when a PCI initiator is attempting to access main memory. Input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GIRDY (GIRDY# for 4x)	AL5	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AK3	IO	**Target Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when target is ready for data transfer.
AGP8XDET#	AB1	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode. Readable in Device 0 Function 0 Rx84[3].

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GADSTB assertion for AGP-style transfers and with GFRAME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE#[3:0] for 4x mode)	AK5, AK2, AL3, AN4	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AN3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE# **GDBIL**	AF4 AG4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Not**e: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F (GADSTB0 for 4x), **GADSTB0S** (GADSTB0# for 4x)	AT3 AR3	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTB0F ("First" strobe) and GADSTB0# as GADSTB0S ("Second" strobe). GADSTB0 and GADSTB0# provide timing for 4x mode.

5.2 PN800 North Bridge - 4

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GSBA[7:0]# (GSBA[7:0] for 4x)	AE1, AE4, AE3, AE2, AD2, AC3, AC4, AC1	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF (GSBSTB for 4x), **GSBSTBS** (GSBSTB# for 4x)	AD3 AD1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AE6, AE5, AD6	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting GPIPE# or start a PCI transaction by asserting GFRAME#. GST[2:0] are always outputs from the target (North Bridge) and inputs to the master (graphics controller).

AGP 8x / 4x Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
GWBF (GWBF# for 4x)	AB2	I	**Write Buffer Full.**
GRBF (GRBF# for 4x)	AE7	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GREQ (GREQ# for 4x)	AD4	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AD5	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AN1	IO	**System Error.**
GSTOP (GSTOP# for 4x)	AM3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).
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Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)
Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the GSBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only GSBA (GPIPE# isn't used in 8x mode).
Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

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CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR	R1	AO	**Analog Red.** Analog red output to the CRT monitor.
AG	R2	AO	**Analog Green.** Analog green output to the CRT monitor.
AB	R3	AO	**Analog Blue.** Analog blue output to the CRT monitor.
HSYNC	U4	O	**Horizontal Sync.** Output to CRT.
VSYNC	U3	O	**Vertical Sync.** Output to CRT.
RSET	V7	AI	**Reference Resistor.** Tie to GNDDAC through an external 82 Ω 1%%resistor to control the RAMDAC full-scale current value. See Design Guide for details.

I/O pads for the pins in the above table are powered by VCC33GFX (i.e., 3.3V I/O).

Digital Power / Ground

Signal Name	Pin #	I/O	Signal Description
VTT	(see pin lists	P	**Power** for **CPU I/O Interface Logic (15 Pins).** Typical 1.65V (CPU dependent)
VCC25MEM	(see pin lists	P	**Power** for **Memory I/O Interface Logic (25 Pins).** 2.5V ±5%.
VCC15VL	AD16-17	P	**Power** for **V-Link I/O Interface Logic (2 Pins).** 1.5V ±5%
VCC15AGP	(see pin lists	P	**Power** for **AGP Bus I/O Interface Logic (6 Pins).** 1.5V ±5%
VCC33GFX	V13, W13, Y13	P	**Power for Graphics Display I/O Logic (3 Pins).** 3.3V ±5%
VCC15	(see pin lists	P	**Power** for **Internal Logic (51 Pins).** 1.5V ±5%
VSUS15	AT14	P	**Suspend Power (1 Pin).** 1.5V ±5%
GND	(see pin lists	P	**Digital Ground (161 Pins).** Connect to main ground plane.

Ultra V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD15, **VD14,** **VD13,** **VD12,** **VD11,** **VD10,** **VD9,** **VD8,** **VD7,** **VD6,** **VD5**, **VD4**, **VD3**, **VD2**, **VD1**, **VD0**	AP13 AN13 AR6 AT6 AM12 AP12 AN6 AM7 AP11 AM11 AP7 AR7 AR11 AN10 AR8 AP8	IO	**V-Link Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD pins but are on the indicated pins of the South Bridge chip). Check the strap pin table for details.
VPAR	AT7	IO	**V-Link Parity.**
VBE#	AN7	IO	**V-Link Byte Enable.**
UPCMD	AN12	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	AM10	I	**V-Link Strobe from Client to Host.**
UPSTB–	AM9	I	**V-Link Complement Strobe from Client to Host.**
DNCMD	AP10	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	AN9	O	**V-Link Strobe from Host to Client.**
DNSTB–	AP9	O	**V-Link Complement Strobe from Host to Client.**

Note: I/O pads for the pins in the above table are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

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Dedicated Digital Video Port 0 (DVP0)

Signal Name	Pin #	I/O	Signal Description
TVD11 / DVP0D11 / CAPD11, **TVD10** / DVP0D10 / CAPD10 / strap, **TVD9** / DVP0D9 / CAPD9 / strap, **TVD8** / DVP0D8 / CAPD8 / strap, **TVD7** / DVP0D7 / CAPD7 / strap, **TVD6** / DVP0D6 / CAPD6 / strap, **TVD5** / DVP0D5 / CAPD5 / strap, **TVD4** / DVP0D4 / CAPD4 / strap, **TVD3** / DVP0D3 / CAPD3 / strap, **TVD2** / DVP0D2 / CAPD2 / strap, **TVD1** / DVP0D1 / CAPD1 / strap, **TVD0** / DVP0D0 / CAPD0 / strap	AA6 AB6 AB5 Y7 Y6 Y5 AA4 Y2 Y3 AA5 W2 W1	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVHS / DVP0HS / CAPHS	W4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS / CAPVS	V1	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	W3	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKIN / DVP0DET / CAPBCLK	V2	I	**TV Encoder 0 Clock In.** Feedback from TV encoder. Internally pulled down.
TVCLK / DVP0CLK / CAPACLK	Y4	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

SMB / I2C Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
SBPLCLK	GIRDY	AL5	IO	**I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT	GC#BE1	AL3	IO	**I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK	GREQ	AD4	IO	**I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT	GGNT	AD5	IO	**I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK2 **SPCLK1** / CAPD12 **SPDAT2,** **SPDAT1** / CAPD13	n/a n/a n/a n/a	T3 V3 T4 V4	IO	**Serial Port (SMB/I2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDATn pins are the data signals used for serial data transfer. SPxxx1 is typically used for DVI monitor communications and SPxxx2 is typically used for DDC for CRT monitor communications. These pins are programmed via "Sequencer" graphics registers (port 3C5) in the "Extended" VGA register space (see the UniChrome-II Graphics Registers document for additional details). The SPxxx1 registers are programmed via 3C5.31 ("IIC Serial Port Control 1") and the SPxxx2 registers are programmed via 3C5.26 ("IIC Serial Port Control 0"). In both registers, the clock out state is programmed via bit-5 and the data out state via bit-4, clock in status may be read in bit-3 and data in status in bit-2, and the port may be enabled via bit-0.

I/O pads for SPCLK[2:1] / SPDAT[2:1] above are powered by VCC33GFX (i.e., 3.3V I/O).
All other pins in the above table are powered by VCC15AGP (i.e., 1.5V I/O)

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CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP)

Signal Name	Pin #	I/O	Signal Description
		I	**Video Capture Data.** To configure DVP0 as a video capture port, pin DVP0D6 must be strapped low. Pin Function: 8-Bit Mode / 16-Bit Mode
CAPD15 / GPO0	V5		CAPBD7 / CAPAD15
CAPD14 / GPOUT	W5		CAPBD6 / CAPAD14
CAPD13 / SPDAT1	V4		CAPBD5 / CAPAD13
CAPD12 / SPCLK1,	V3		CAPBD4 / CAPAD12
CAPD11 / DVP0D11 / TVD11,	AA6		CAPBD3 / CAPAD11
CAPD10 / DVP0D10 / TVD10 / strap,	AB6		CAPBD2 / CAPAD10
CAPD9 / DVP0D9 / TVD9 / strap,	AB5		CAPBD1 / CAPAD9
CAPD8 / DVP0D8 / TVD8 / strap,	Y7		CAPBD0 / CAPAD8
CAPD7 / DVP0D7 / TVD7 / strap,	Y6		CAPAD7 / CAPAD7
CAPD6 / DVP0D6 / TVD6 / strap,	Y5		CAPAD6 / CAPAD6
CAPD5 / DVP0D5 / TVD5 / strap,	AA4		CAPAD5 / CAPAD5
CAPD4 / DVP0D4 / TVD4 / strap,	Y2		CAPAD4 / CAPAD4
CAPD3 / DVP0D3 / TVD3 / strap,	Y3		CAPAD3 / CAPAD3
CAPD2 / DVP0D2 / TVD2 / strap,	AA5		CAPAD2 / CAPAD2
CAPD1 / DVP0D1 / TVD1 / strap,	W2		CAPAD1 / CAPAD1
CAPD0 / DVP0D0 / TVD0 / strap	W1		CAPAD0 / CAPAD0
CAPHS / DVP0HS / TVHS	W4	I	**Video Capture Horizontal Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPVS / DVP0VS / TVVS	V1	I	**Video Capture Vertical Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.

CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP) (Continued)

Signal Name	Pin #	I/O	Signal Description
CAPAFLD / BISTIN	V6	I	**Video Capture "A"-Channel TV Field Indicator.** For capture port "A" (16-bit and 8-bit mode).
CAPBCLK / DVP0DET / TVCLKIN	V2	I	**Video Capture Clock B.** Port "B" (8-bit mode) input clock from external video decoder. Internally pulled down. Not used in 16-bit mode.
CAPACLK / DVP0CLK / TVCLK	Y4	I	**Video Capture Clock A.** Port "A" (16-bit and 8-bit mode) input clock from external video decoder. Internally pulled down.

Note: I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O)

DDR SDRAM Interface – Address

Signal Name	Pin #	I/O	Signal Description
MAA[13:0], MAB[13:0]	(see pin lists)	O	**Memory Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (MAA) and EA (MAB).
BAA[1:0], BAB[1:0]	AT35, AT31, AF36, AJ36	O	**Bank Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (BA) and EA (BB).
SRASA#, SCASA#, SWEA#, SRASB#, SCASB#, SWEB#	AP26, AN25, AR26, AL29, AN28, AN31	O	**Row Address, Column Address and Write Enable Command Indicators A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 Rx E8 (ScmdA) and EA (ScmdB).

Note: I/O pads for all SDRAM pins are powered by VCC25MEM. MD / DQS input voltage levels are referenced to MEMVREF.

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AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

Signal Name	AGP Name	Pin #	I/O	Signal Description
GTVD11 / GDVP1D11,	GC#BE3	AK5	O	**Data.**
GTVD10 / GDVP1D10,	GD26	AH5		
GTVD9 / GDVP1D9,	GD24	AG5		
GTVD8 / GDVP1D8,	GD30	AG6		
GTVD7 / GDVP1D7,	GD28	AH4		
GTVD6 / GDVP1D6,	GD29	AF3		
GTVD5 / GDVP1D5,	GSBA4#	AE2		
GTVD4 / GDVP1D4,	GD27	AG2		
GTVD3 / GDVP1D3,	GSBA5#	AE3		
GTVD2 / GDVP1D2,	GSBSTBS	AD1		
GTVD1 / GDVP1D1,	GSBSTBF	AD3		
GTVD0 / GDVP1D0	GSBA2#	AC3		
GTVHS / GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.** Internally pulled down.
GTVVS / GDVP1VS	GSBA0#	AC1	O	**Vertical Sync.** Internally pulled down.
GTVDE / GDVP1DE	GSBA1#	AC4	O	**Display Enable.** Internally pulled down.
GTVCLKIN / FPDET	GADSTB1S	AG1	I	**Clock In.** Input from TV encoder. Internally pulled down.
GTVCLK / GDVP1CLK	GSBA6#	AE4	O	**Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK# / GDVP1CLK#	GSBA7#	AE1	O	**Clock Out Complement.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.
I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).
Note: If the FPD port is enabled and TV-out capability is required at the same time, the dedicated TV-out port (DVP0) must be used because pin AG1 will be dedicated to the FPDET function.

AGP-Multiplexed Digital Video Port 1 (GDVP1) – DVI Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
GDVP1D11 / GTVD11,	GC#BE3	AK5	O	**Data.**
GDVP1D10 / GTVD10,	GD26	AH5		
GDVP1D9 / GTVD9,	GD24	AG5		
GDVP1D8 / GTVD8,	GD30	AG6		
GDVP1D7 / GTVD7,	GD28	AH4		
GDVP1D6 / GTVD6,	GD29	AF3		
GDVP1D5 / GTVD5,	GSBA4#	AE2		
GDVP1D4 / GTVD4,	GD27	AG2		
GDVP1D3 / GTVD3,	GSBA5#	AE3		
GDVP1D2 / GTVD2,	GSBSTBS	AD1		
GDVP1D1 / GTVD1,	GSBSTBF	AD3		
GDVP1D0 / GTVD0,	GSBA2#	AC3		
GDVP1HS / GTVHS	GSBA3#	AD2	O	**Horizontal Sync.**
GDVP1VS / GTVVS	GSBA0#	AC1	O	**Vertical Sync.**
GDVP1DE / GTVDE	GSBA1#	AC4	O	**Data Enable.**
GDVP1DET	GD31	AF1	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK / GTVCLK	GSBA6#	AE4	O	**Clock.**
GDVP1CLK# / GTVCLK#	GSBA7#	AE1	O	**Clock Complement.**

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24-Bit / Dual 12-Bit Flat Panel Display Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD23 / **FPD0D11,**	GD11	AM4	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes.
FPD22 / **FPD0D10,**	GD13	AN2		Two FPD interface modes, 24-bit and dual 12-bit, are supported.
FPD21 / **FPD0D09,**	GD14	AL1		Strapping pin DVP0D4 is used to select the interface mode to theLVDS transmitter chip:
FPD20 / **FPD0D08,**	GD15	AP1		Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit
FPD19 / **FPD0D07,**	GC#BE2	AK2		In "24-bit" mode, only one set of control pins is required. However, in dual 12-bit mode, the
FPD18 / **FPD0D06,**	GD16	AJ3		PN800 provides two sets of control signals that are required for certain LVDS transmitter chips.
FPD17 / **FPD0D05,**	GD17	AJ1		In 24-bit mode, two operating modes are supported:
FPD16 / **FPD0D04,**	GD18	AJ4		3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge
FPD15 / **FPD0D03,**	GD23	AH3		transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1
FPD14 / **FPD0D02,**	GD20	AH1		Single data rate: each clock rising edge transmits a complete 24-bit pixel
FPD13 / **FPD0D01,**	GD22	AK4		In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1
FPD12 / **FPD0D00,**	GADSTB1F	AG3		Double data rate: each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPD11 / **FPD1D1**1,	GD1	AP2		
FPD10 / **FPD1D1**0,	GD0	AT2		
FPD09 / **FPD1D0**9,	GD3	AT5		
FPD08 / **FPD1D0**8,	GD4	AR4		
FPD07 / **FPD1D0**7,	GD5	AT1		
FPD06 / **FPD1D0**6,	GD6	AN5		
FPD05 / **FPD1D0**5,	GD7	AT4		

24-Bit / Dual 12-Bit Flat Panel Display Interface (Continued)

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD04 / **FPD1D0**4,	GADSTB0F	AT3	O	
FPD03 / **FPD1D0**3,	GC#BE0	AN4		
FPD02 / **FPD1D0**2,	GADSTB0S	AR3		
FPD01 / **FPD1D0**1,	GD10	AR1		
FPD00 / **FPD1D00**	GD12	AL2		
FPHS	GFRAME	AL4	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPVS	GDEVSEL	AK1	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPDE	GD19	AK6	O	**Flat Panel Data Enable.** 24-bit mode or port 0 in dual 12-bit mode
FPDET	GADSTB1S	AG1	I	**Flat Panel Detect.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK	GD21	AH2	O	**Flat Panel Clock.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK#	GWBF	AB2	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 in dual 12-bit mode. For double-data-rate data transfers.
FP1HS	GD9	AP3	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS	GPAR	AN3	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE	GSERR	AN1	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET / GTVCLKIN	GD8	AM1	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK	GD2	AP4	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK#	GSTOP	AM3	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. For double-data-rate data transfers.

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Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description	Power Plane
HCLK+	M5	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 / 166 / 200 / 266 MHz). This clock is used by all PN800 logic that is in the host CPU domain.	**VTT**
HCLK–	M6	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
MCLKOA	B31	O	**Memory (SDRAM) Clock A.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
MCLKIA	A32	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKOA.	**VCC25MEM**
MCLKOB	A31	O	**Memory (SDRAM) Clock B.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
DISPCLKI	N3	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to GND if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	N4	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**
GCLK	N7	I	**AGP Clock.** Clock for AGP logic.	**VCC15AGP**
XIN	N5	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
RESET#	AM13	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the PN800 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VSUS15**
PWROK	AP14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VSUS15**
SUSST#	AN14	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test (Continued)

Signal Name	Pin #	I/O	Signal Description	Power Plane
AGPBUSY# / NMI	AL14	O	**AGP Interface Busy.** Connect to a South Bridge GPIO pin for monitoring the status of the internal AGP bus. See Design Guide for details. Pin function selectable with Device 0 Function 0 RxBE[7] (default = NMI).	**VCC25MEM**
GPOUT / CAPD14	W5	O	**General Purpose Output.** This pin reflects the state of SRD[0].	**VCC33GFX**
GPO0 / CAPD15	V5	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].	**VCC33GFX**
INTA#	U2	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TCLK	W6	I	**Test Clock.** This pin is used for testing and must be connected to GND through a 1K-4.7K ohm resistor for all board designs.	**VCC33GFX**
TESTIN#	C31	I	**Test In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
DFTIN#	D32	I	**DFT In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
BISTIN / CAPAFLD	V6	I	**BIST In.** This pin is used for testing and must be tied to GND with a 1K-4.7K ohm resistor on all board designs.	**VCC33GFX**

Flat Panel Power Control (Muxed with AGP)

Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD	ST1	AE5	IO	**Enable Panel VDD Power.**
ENAVEE	ST0	AD6	IO	**Enable Panel VEE Power.**
ENABLT	ST2	AE6	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

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Compensation

Signal Name	Pin #	I/O	Signal Description	Power Plane
HRCOMP	F15	AI	**Host CPU Compensation.** Connect 20.5 §Ù 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.	**VTT**
VLCOMPP	AM6	AI	**V-Link Compensation.** Connect a 360Ω 1% resistor to ground.	**VCC15VL**
AGPCOMPN	AB3	AI	**AGP N Compensation.** Connect a 60.4Ω1% resistor to VCC15AGP.	**VCC15AGP**
AGPCOMPP	AC6	AI	**AGP P Compensation.** Connect a 60.4Ω1% resistor to ground.	**VCC15AGP**

Reference Voltages

Signal Name	Pin #	I/O	Signal Description	Power Plane
GTLVREF	H17	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HDVREF[0:3]	H11, H14, K7, J7	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically using a resistive voltage divider. See Design Guide.	**VTT**
HAVREF[0:1]	H19, G22	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HCOMPVREF	G14	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF [0:5]	J29, R29, W29, AE29, AK22, AK17	P	**Memory Voltage Reference.** 0.5 VCC25MEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCC25MEM**
VLVREF	AL7	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**
AGPVREF[0:1]	AF7, AD7	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Analog Power / Ground

Signal Name	Pin #	I/O	Signal Description
VCCA33HCK1	M4	P	**Power for Host CPU Clock PLL 1** (3.3V ±5%). Host CPU Clock PLL 1 generates 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, and 200 MHz.
GNDAHCK1	M3	P	**Ground for Host CPU Clock PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA33HCK2	L1	P	**Power for Host CPU Clock PLL 2** (3.3V ±5%). Host CPU Clock PLL 2 generates 500 MHz for CPU / DRAM frequencies of multiples of 166 MHz.
GNDAHCK2	L2	P	**Ground for Host CPU Clock PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	D31	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	E31	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33GCK	M1	P	**Power for AGP Clock PLL** (3.3V ±5%)
GNDAGCK	M2	P	**Ground for AGP Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA15PLL1	P3	P	**Power for Graphics Controller PLL 1** (1.5V ±5%).
GNDAPLL1	P2	P	**Ground for Graphics Controller PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA15PLL2	P6	P	**Power for Graphics Controller PLL 2** (1.5V ±5%).
GNDAPLL2	N6	P	**Ground for Graphics Controller PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA15PLL3	N1	P	**Power for Graphics Controller PLL 3** (1.5V ±5%).
GNDAPLL3	N2	P	**Ground for Graphics Controller PLL 3.** Connect to main ground plane through a ferrite bead.
VCCA33DAC[1:2]	T5, P4	P	**Power for DAC.** (3.3V ±5%)
GNDADAC[1:3]	T6, P5, R4	P	**Ground for DAC.** Connect to main ground plane through a ferrite bead.

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V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VD[7:0]	(see pin list)	IO	**Data Bus.** These pins are also used to send strap information to the chipset north bridge. At power up, VD7 reflects the state of a strap on SDCS3#, VD[6:4] reflect the state of straps on pins SDA[2:0], and VD[3:0] reflect the state of straps on pins Strap_VD3-0. The specific interpretation of these straps is north bridge chip design dependent.
VPAR	F24	IO	**Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235CE (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.
VBE#	G24	IO	**Byte Enable.**
VCLK	L22	I	**V-Link Clock.**
UPCMD	K23	O	**Command from Client-to-Host.**
DNCMD	K25	I	**Command from Host-to-Client.**
UPSTB	J26	O	**Strobe from Client-to-Host.**
UPSTB#	J24	O	**Complement Strobe from Client-to-Host.**
DNSTB	K26	I	**Strobe from Host-to-Client.**
DNSTB#	H24	I	**Complement Strobe from Host-to-Client.**

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	U26	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).
FERR#	U24	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T24	OD	**Ignore Numeric Error.** This pin is connected to the CPU iPignore errorlr pin.
INIT#	R26	OD	**Initialization.** The VT8235 Version CE asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
INTR	T25	OD	**CPU Interrupt.** INTR is driven by the VT8235 Version CE to signal the CPU that an interrupt request is pending and needs service.
NMI	T26	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 Version CE generates an NMI when PCI bus SERR# is asserted.
SLP#	V26	OD	**Sleep.** Used to put the CPU to sleep.
SMI#	U25	OD	**System Management Interrupt.** SMI# is asserted by the VT8235 Version CE to the CPU in response to different Power-Management events.
STPCLK#	R24	OD	**Stop Clock.** STPCLK# is asserted by the VT8235 Version CE to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 §Ù pullup resistors to VCC_CMOS (see Design Guide).

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Advanced Programmable Interrupt Controller (APIC) Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	T23	O	**Internal APIC Data 1.** Function 0 Rx58[6] = 1
APICD0	R25	O	**Internal APIC Data 0.** Function 0 Rx58[6] = 1
APICCLK	U23	I	**APIC Clock.**

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VRDSLP / GPI29/ GPO29	AB9	OD	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selectsthe proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0.
GHI# / **GPI22/ GPO22**	R22	OD	**CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0.
DPSLP# / GPI23/ GPO23	P21	OD	**CPU Deep Sleep.** This pin performs the DPSLP# function if Device 17 Function 0RxE5[3]=0.
CPUMISS / GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ# / GPI6	AD10	I	**AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinlist)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME#assertion and data is driven or received in following cycles.
CBE[3:0]#	M3, L4, C1, E2	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byteenables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	H2	IO	**Device Select.** The VT8235 Version CE asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235 Version CE-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	J1	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	J2	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	H1	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	K4	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
SERR#	C2	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 Version CE can be programmed to generate an NMI to the CPU.
PERR#	C3	_	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle.
PAR	F4	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.

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PCI Bus Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
INTA# **INTB#** **INTC#** **INTD#** **INTE#** / GPI12, / GPO12, **INTF#** / GPI13, / GPO13, **INTG#** / GPI14, / GPO14, **INTH#** / GPI15, / GPO15	A4 B4 B5 C4 D4 E4 A3 B3	I	**PCI Interrupt Request**. The INTA# through INTD# pins are typically connected to thePCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# NTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#
REQ5# / GPI7, **REQ4#,** **REQ3#,** **REQ2#,** **REQ1#,** **REQ0#**	R3 P3 D5 C5 B6 A5	I	**PCI Request.** These signals connect to the VT8235 Version CE from each PCI slot (oreach PCI master) to request the PCI bus. To use pin R3 as REQ5#, Function 0 RxE4 mustbe set to 1 otherwise this pin will function as General Purpose Input 7.
GNT5# / GPO7, **GNT4#,** **GNT3#,** **GNT2#,** **GNT1#,** **GNT0#**	R2 R4 E5 C6 D6 A6	O	**PCI Grant.** These signals are driven by the VT8235 Version CE to grant PCI access to aspecific PCI master. To use pin R2 as GNT5#, Function 0 RxE4 must be set to 1otherwise this pin will function as General Purpose Output 7.
PCIRST#	R1	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus.
PCICLK	R23	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AB7	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 Version CE drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 §Ù resistor if the function is not used. Refer to the ihPCI Mobile Design Guidelo and applicable VIA North Bridge Design Guide (KT400A, CLE266, or P4X400) for more details.

LAN Controller - Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	B11	I	***PD***	**MII Collision Detect.** From the external PHY.
MCRS	A11	I	***PD***	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	A7	O	***PD***	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	B7	IO	***PD***	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C9	I	***PD***	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	C7, A8, B8, C8	I	***PD***	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	D8	I	***PD***	**MII Receive Data Valid.**
MRXERR	D10	I	***PD***	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	C10	I	***PD***	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	A9, B9, B10, A10	O	***PD***	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	C11	O	***PD***	**MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY.
MIIVCC	D9, E9, E10, E11	**Power**		**MII Interface Power.** 3.3V ±5%.
MIIVCC25	D12, E12	**Power**		**MII Suspend Power.** 2.5V ±5%.
RAMVCC	E7	**Power**		**Power For Internal LAN RAM.** 2.5V ±5%.
RAMGND	E6	**Power**		**Ground For Internal LAN RAM.**

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Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	**D11**	**O**		Serial EEPROM Chip Select.
EECK	**C12**	**O**		Serial EEPROM Clock.
EEDO	**B12**	**I**		Serial EEPROM Data Output. **Connect to EEPROM Data Out pin.**
EEDI	**A12**	**O**		Serial EEPROM Data Input. **Connect to EEPROM Data In pin.**

Low Pin Count (LPC) Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	**AF6**	**IO**		LPC Frame.
LREQ#	**AE6**	**IO**		LPC DMA / Bus Master Request.
LAD[3-0]	**AD7, AE7, AF7, AD8**	**IO**	**PU**	LPC Address / Data.

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

System Management Bus (SMB) Interface (I 2 C Bus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AC4	IO	**SMB / I 2 C Channel 1 Clock.**
SMBCK2 / GPI27 / GPO27	AC3	IO	**SMB / I 2 C Channel 2 Clock.** Rx95[2] = 0
SMBDT1	AB2	IO	**SMB / I 2 C Channel 1 Data.**
SMBDT2 / GPI26 / GPO26	AD1	IO	**SMB / I 2 C Channel 2 Data.** Rx95[2] = 0
SMBALRT#	AB1	I	**SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	E20	IO	**USB 2.0 Port 0 Data +**
USBP0Œ	D20	IO	**USB 2.0 Port 0 Data Œ**
USBP1+	A20	IO	**USB 2.0 Port 1 Data +**
USBP1Œ	B20	IO	**USB 2.0 Port 1 Data Œ**
USBP2+	E18	IO	**USB 2.0 Port 2 Data +**
USBP2Œ	D18	IO	**USB 2.0 Port 2 Data Œ**
USBP3+	A18	IO	**USB 2.0 Port 3 Data +**
USBP3Œ	B18	IO	**USB 2.0 Port 3 Data Œ**
USBP4+	D16	IO	**USB 2.0 Port 4 Data +**
USBP4Œ	E16	IO	**USB 2.0 Port 4 Data Œ**
USBP5+	A16	IO	**USB 2.0 Port 5 Data +**
USBP5Œ	B16	IO	**USB 2.0 Port 5 Data Œ**
USBCLK	E23	I	**USB 2.0 Clock.** 48MHz clock input for the USB interface
USBOC0#	C26	I	**USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1#	D24	I	**USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low.
USBOC2#	B26	I	**USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low.
USBOC3#	C25	I	**USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low.
USBOC4#	B24	I	**USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low.
USBOC5#	A24	I	**USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low.
USBVCC	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V
USBGND	(see pin list)	**Power**	**USB 2.0 Port Differential Output Interface Logic Ground.**
VSUSUSB	C24	**Power**	**USB 2.0 Suspend Power.** 2.5V ±5%.
VCCUPLL	A23, B23	**Power**	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%.
GNDUPLL	C23, D23	**Power**	**USB 2.0 PLL Analog Ground.**

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UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY /PDDMARDY /PDSTROBE	Y22	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Read**y. Output flow control. The device mayassert DDMARDY to pause output transfers **Primary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY /SDDMARDY /SDSTROBE	AF17	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Read**y. Output flow control. The devicemay assert DDMARDY to pause output transfers **Secondary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# /PHDMARDY /PHSTROBE	W26	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Read**y. Primary channel input flow contro**l.** Thehost may assert HDMARDY to pause input transfers **Primary Host Strob**e. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# /SHDMARDY /SHSTROBE	AF23	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Read**y. Input flow control. The host mayassert HDMARDY to pause input transfers **Host Strobe** B. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# /PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# /SSTOP	AE23	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	Y23	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	AD17	I	**Secondary Device DMA Request.** Secondary channel DMA request

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (Continued)

Signal Name	Pin #	I/O	Signal Description
PDDACK#	Y24	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	AD23	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	AD24	I	**Primary Channel Interrupt Request.**
IRQ15	AE26	I	**Secondary Channel Interrupt Request.**
PDCS1#	V22	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	V23	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1# / strap	AF25	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the EExx pins.
SDCS3# / strap	AF26	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VD[7].
PDA[2-0]	W24, V25, W23	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0] / strap	AE24, AC22, AF24	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4].
PDD[15-0]	(see pin list)	IO	**Primary Disk Data.**
SDD[15-0]	(see pin list)	IO	**Secondary Disk Data.**

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AD9	I	**Serial IRQ.** This pin has an internal pull-up resistor.

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AC97 Audio / Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	T3	O	**AC97 Reset.**
ACBTCK	T1	I	**AC97 Bit Clock.**
ACSYNC	T2	O	**AC97 Sync.**
ACSDO	U2	O	**AC97 Serial Data Out.**
ACSDIN0 (VSUS33)*f*	U3	I	**AC97 Serial Data In 0.**
ACSDIN1 (VSUS33)*f*	V2	I	**AC97 Serial Data In 1.**
ACSDIN2 / GPIO20 / PCS0#	U1	I	**AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1
ACSDIN3 / GPIO21 / PCS1# / SLPBTN#	V3	I	**AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1

Resets, Clocks, and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	**AC5**	**I**	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic **powered by VBAT.**
PWROK#	**AF1**	**O**	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	**R1**	**O**	**PCI Reset.** Active low reset signal for the PCI bus. The VT8235 Version CE will assert this pin during power-up or from the control register.
OSC	**AB8**	**I**	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	**AE4**	**I**	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	**AF3**	**O**	**RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	**AE9**	**I**	**Test.**
TPO	**AF9**	**O**	**Test Pin Output.** Output pin for test mode.
NC	**(see pin list)**	**–**	**No Connect.** Do not connect.

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK / IRQ1	**W1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. **Rx51[2]=0** Interrupt Request **1. Interrupt input 1.**
MSDT / IRQ12	**W2**	**IO / I**	**PU**	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**2. Interrupt input 12.
KBCK / KA20G	**W3**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	**V1**	**IO / I**	**PU**	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / strap	**AF10**	**O**		**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC BIOS ROM.

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

Speaker

Signal Name	Pin #	I/O	PU	Signal Description
SPKR / strap	**AF8**	**O**		**Speaker.** Strap low to enable (high to disable) CPU frequency **strapping.**

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General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 ***(VBAT)***	**AE2**	**I**	General Purpose Input 0. **Status on PMIO Rx20[0]**
GPI1 ***(VSUS33)***	**AC2**	**I**	General Purpose Input 1. **Status on PMIO Rx20[1]**
GPI2 / EXTSMI# ***(VSUS33)***	**AA1**	**I**	General Purpose Input 2. **Status on PMIO Rx20[4]**
GPI3 / RING# ***(VSUS33)***	**Y2**	**I**	General Purpose Input 3. **Status on PMIO Rx20[8]**
GPI4 / LID# ***(VSUS33)***	**AC1**	**I**	General Purpose Input 4. **Status on PMIO Rx20[11]**
GPI5 / BATLOW# ***(VSUS33)***	**V4**	**I**	General Purpose Input 5. **Status on PMIO Rx20[12]**
GPI6 / AGPBZ#	**AD10**	**I**	General Purpose Input 6. **Status on PMIO Rx20[5]**
GPI7 / REQ5#	**R3**	**I**	General Purpose Input 7. **RxE4[2] = 0**
GPI12 / GPO12 / INTE#	**D4**	**I**	General Purpose Input 12. **RxE4[4] = 0, 5B[1]=0**
GPI13 / GPO13 / INTF#	**E4**	**I**	General Purpose Input 13. **RxE4[4] = 0, 5B[1]=0**
GPI14 / GPO14 / INTG#	**A3**	**I**	General Purpose Input 14. **RxE4[4] = 0, 5B[1]=0**
GPI15 / GPO15 / INTH#	**B3**	**I**	General Purpose Input 15. **RxE4[4] = 0, 5B[1]=0**
GPI16 / INTRUDER# ***(VBAT)***	**AE1**	**I**	General Purpose Input 16. **Status on PMIO Rx20[6]**
GPI17 / CPUMISS	**Y1**	**I**	General Purpose Input 17. **Status on PMIO Rx20[5]**
GPI18 / THRM# / AOLGPI	**Y4**	**I**	General Purpose Input 18. **Rx8C[3] = 0**
GPI20 / GPO20 / ACSDIN2 / PCS0#	**U1**	**I**	**General Purpose Input 20.** RxE4[6]=1, E5[1]=0, **PMIO 4C[20] = 1**
GPI21 / GPO21 / ACSDIN3 / PCS1# / SLPBTN#	**V3**	**I**	**General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1
GPI22 / GPO22 / GHI#	**R22**	**I**	**General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1
GPI23 / GPO23 / DPSLP#	**P21**	**I**	**General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1

General Purpose Inputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPI26 / GPO26 / SMBDT2 ***(VSUS33)***	**AD1**	**I**	**General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0
GPI27 / GPO27 / SMBCK2 ***(VSUS33)***	**AC3**	**I**	**General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0
GPI28 / GPO28	**AC8**	**I**	**General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1
GPI29 / GPO29 / VRDSLP	**AB9**	**I**	**General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1

Note: Register references above are Device 17 Function 0 unless indicated otherwise.
Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0# / GPIO20 / ACSDIN2	**U1**	**O**	Programmable Chip Select 0. **RxE4[6]=1, E5[1]=1**
PCS1# / GPIO21 / ACSDIN3 / SLPBTN#	**V3**	**O**	Programmable Chip Select 1. **RxE4[6]=1, E5[2]=1**

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General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO0 ***(VSUS33)***	**AA3**	**O**	General Purpose Output 0.
GPO1 / SUSA# ***(VSUS33)***	**AA2**	**O**	General Purpose Output 1. **Rx94[2] = 1**
GPO2 / SUSB# ***(VSUS33)***	**AD3**	**O**	General Purpose Output 2. **Rx94[3] = 1**
GPO3 / SUSST1# ***(VSUS33)***	**Y3**	**O**	General Purpose Output 3. **Rx94[4] = 1**
GPO4 / SUSCLK ***(VSUS33)***	**AB3**	**O**	General Purpose Output 4. **Rx95[1] = 1**
GPO5 / CPUSTP#	**AC7**	**O**	General Purpose Output 5. **RxE4[0] = 1**
GPO6 / PCISTP#	**AD6**	**O**	General Purpose Output 6. **RxE4[1] = 1**
GPO7 / GNT5#	**R2**	**O**	General Purpose Output 7. **RxE4[2] = 0**
GPO12 / GPI12 / INTE#	**D4**	**O**	General Purpose Output 12. **RxE4[4]=1, 5B[1]=0**
GPO13 / GPI13 / INTF#	**E4**	**O**	General Purpose Output 13. **RxE4[4]=1, 5B[1]=0**
GPO14 / GPI14 / INTG#	**A3**	**O**	General Purpose Output 14. **RxE4[4]=1, 5B[1]=0**
GPO15 / GPI15 / INTH#	**B3**	**O**	General Purpose Output 15. **RxE4[4]=1, 5B[1]=0**
GPO20 / GPI20 / ACSDIN2 / PCS0#	**U1**	**OD**	General Purpose Output 20. **RxE4[6]=1, E5[1]=0**
GPO21 / GPI21 / ACSDIN3 / PCS1# /SLPBTN#	**V3**	**OD**	General Purpose Output 21. **RxE4[6]=1, E5[2]=0**
GPO22 / GPI22 / GHI#	**R22**	**OD**	General Purpose Output 22. **RxE5[3]=1, PMIO 4C[22]=1**
GPO23 / GPI23 / DPSLP#	**P21**	**OD**	General Purpose Output 23. **RxE5[3]=1, PMIO 4C[23]=1**
GPO26 / GPI26 / SMBDT2 ***(VSUS33f)***	**AD1**	**OD**	General Purpose Output 26. **Rx95[2] = 1, 95[3] = 1**
GPO27 / GPI27 / SMBCK2 ***(VSUS33f)***	**AC3**	**OD**	General Purpose Output 27. **Rx95[2] = 1, 95[3] = 1**

General Purpose Outputs (Continued)

Signal Name	Pin #	I/O	Signal Description
GPO28 / GPI28	**AC8**	**OD**	General Purpose Output 28. **RxE5[3] = 1, PMIO 4C[28]=1**
GPO29 / GPI29 / VRDSLP	**AB9**	**OD**	General Purpose Output 29. **RxE5[3] = 1, PMIO 4C[29]=1**

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: Default pin functions are underlined in the table above.

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	**AD2**	**I**	**Power Button.** Used by the Power Management subsystem to monitor an external **system on/off button or switch. Internal logic powered by VSUS33.**
SLPBTN# / GPIO21/ ACSDIN3 / PCS1#	**V3**	**I**	**Sleep Button.** Used by the Power Management subsystem to monitor an external sleepbutton or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1
RSMRST#	**AD4**	**I**	**Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.
EXTSMI# / GPI2	**AA1**	**IOD**	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only)
PME#	**W4**	**I**	**Power Management Event.** (10K PU to VSUS33 if not used)
SMBALRT#	**AB1**	**I**	**SMB Alert**. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used)

5.3 VT8235CE South Bridge - 9

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
LID# / GPI4	**AC1**	**I**	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used)
INTRUDER# / GPI16	**AE1**	**I**	**Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6]
THRM# / GPI18/ AOLGPI	**Y4**	**I**	**Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIORx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-4]).
RING# / GPI3	**Y2**	**I**	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used)
BATLOW# / GPI5	**V4**	**I**	**Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only)
CPUSTP# / GPO5	**AC7**	**O**	**CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO6	**AD6**	**O**	**PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1	**AA2**	**O**	**Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used)
SUSB# / GPO2	**AD3**	**O**	**Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used)
SUSC#	**AF2**	**O**	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used)

Power Management and Event Detection (Continued)

Signal Name	Pin #	I/O	Signal Description
SUSST1# / GPO3	**Y3**	**O**	**Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33.
SUSCLK	**AB3**	**O**	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., KT400A, CLE266, or P4X400) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS / GPI17	**Y1**	**I**	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AOLGPI / GPI18/ THRM#	**Y4**	**I**	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pinmay be used as AOLGPI, GPI18 and THRM# all at the same time.

Strap Pins for VT8235 Version CE Configuration

Signal Name	Pin #	Function	Description	Note
Strap_AUTO	**AE10**	**Auto Reboot**	L: Enable Auto Reboot **H: Disable Auto Reboot (Default)**	
SPKR	**AF8**	**CPU Frequency Strapping**	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping (Default)	
KBCS#	**AF10**	**Internal Keyboard** Controller	L: Disable internal KBC H: Enable internal KBC (Default)	
SDCS1#	**AF25**	Eliminate External LAN EEPROM	L: Enable. Use external EEPROM (Default) H: Disable. Do not use external EEPROM	

5.3 VT8235CE South Bridge - 10

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VSUS33	AA4, AB4-6	P	**Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the ihsoft-offlÉD state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT#
VSUS25	T4, U4	P	**Suspend Power.** 2.5V ±5%.
VSUSUSB	C24	P	**USB Suspend Power.** 2.5V ±5%.
VBAT	AF4	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VLVREF	H22	P	**V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers.
VLCOMP	J22	AI	**V-Link Compensation.**
VCCVK	(see pin list)	P	**V-Link Compensation Circuit Voltage.** 2.5V ±5%
MIIVCC	D9, E9-11	P	**LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead.
MIIVCC25	D12. E12	P	**LAN MII Suspend Power.** 2.5V ±5%.
LANVCC	E7	P	**LAN Power.** 2.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
LANGND	E6	P	**LAN Ground.** Connect to GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0Œ, P1+, P1Œ, P2+, P2Œ, P3+, P3Œ, P4+, P4Œ, P5+, P5Œ). Connect to VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.
VCCUPLL	A23, B23	P	**USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead.
GNDUPLL	C23, D23	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	T22	P	**PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead.
PLLGND	U22	P	**PLL Analog Ground.** Connect to GND through a ferrite bead.

Power and Ground （Continued）

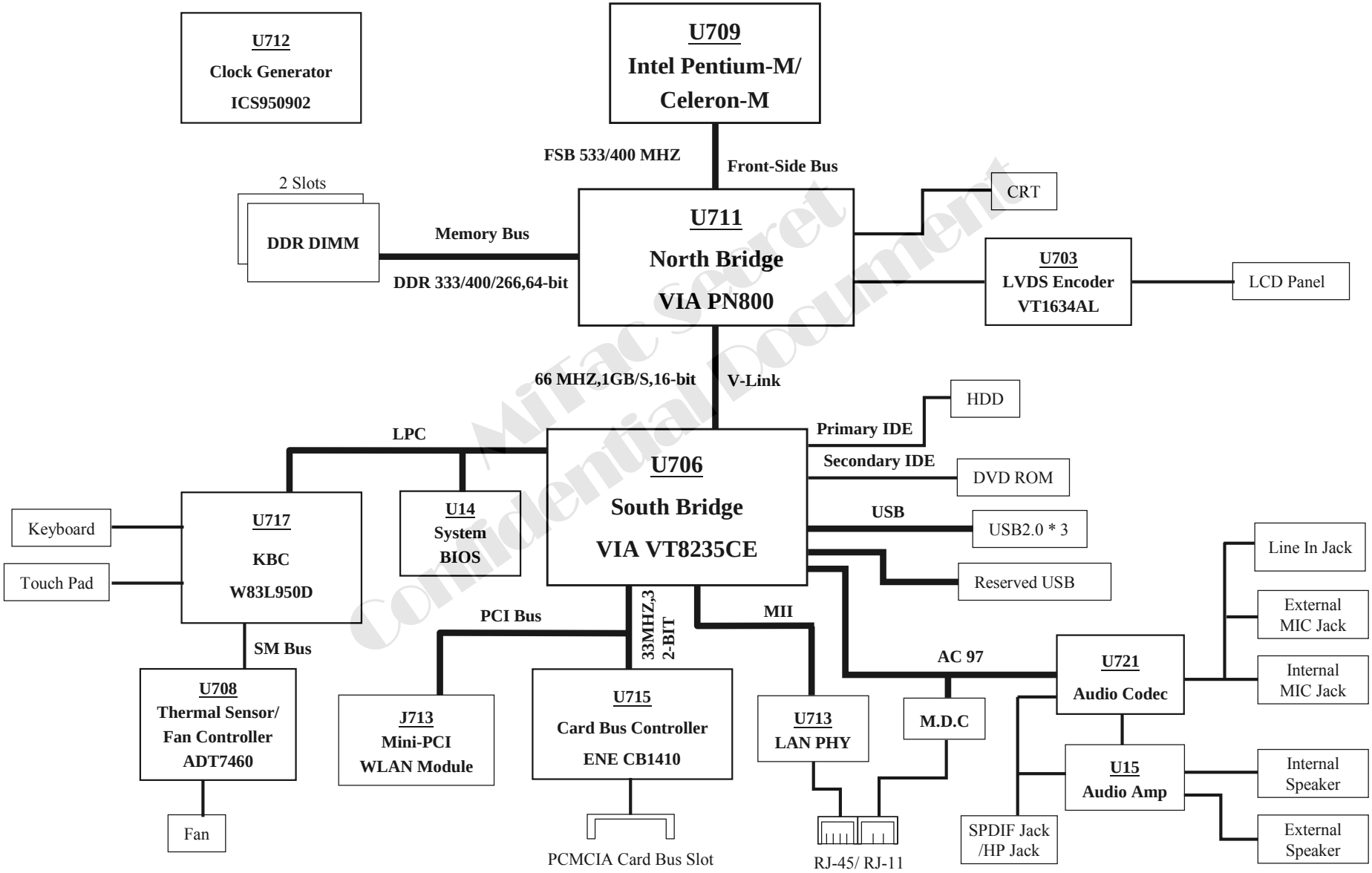
Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)	P	I/O Power. **3.3V ±5%**
VCC	(see pin list)	P	Core Power. **2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.**
GND	(see pin list)	P	**Ground.** Connect to primary motherboard ground plane.

Strap Pins for North Bridge Configuration

Signal Name	Pin #	Function	Description	Note
SDCS3#	AF26	NB Configuration	SDCS3# signal state is reflected on signal pinVD[7] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA2	AE24	NB Configuration	SDA2 signal state is reflected on signal pinVD[6] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA1	AC22	NB Configuration	SDA1 signal state is reflected on signal pinVD[5] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
SDA0	AF24	NB Configuration	SDA0 signal states is reflected on signal pinsVD[4] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD3	AC6	NB Configuration	Strap_VD3 signal state is reflected on signal pinVD[3] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD2	AD5	NB Configuration	Strap_VD2 signal state is reflected on signal pinVD[2] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**
Strap_VD1	AE5	NB Configuration	Strap_VD1 signal state is reflected on signal pin, VD[1] during power up for North Bridge configuration.	**Check the North Bridge DS for details**
Strap_VD0	AF5	NB Configuration	Strap_VD0 signal state is reflected on signalpin, VD[0] during power up for North Bridgeconfiguration.	**Check the NorthBridge DS fordetails**

Note: Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]
Internal Pulldowns are present on all LAN pins

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port-378H by the Mini PCI debug board.

7.2 Error Codes (1)

Following is a list of error codes in sequent display on the Mini PCI debug board.

Code	POST Routine Description
10h	Signals that Reset occurred
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register configure through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter
1Ch	Initialize video
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test DMA controller
25h	Initialize 8237A controller
26h	Initialize INT vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign-on messages displayed

7.2 Error Codes (2)

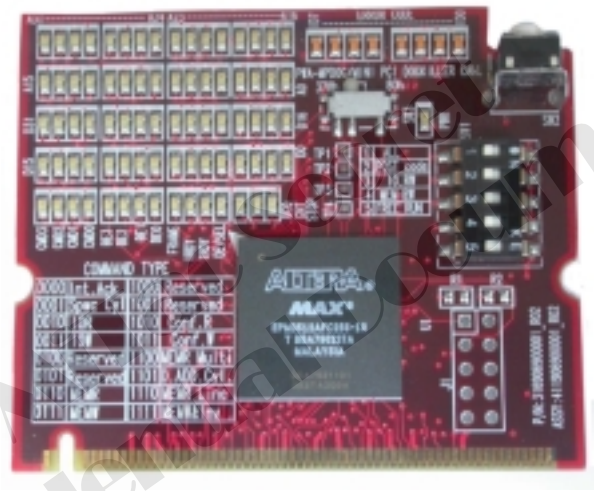
Following is a list of error codes in sequent display on the Mini PCI debug board.

Code	POST Routine Description
30h	OEM initialization of keyboard controller
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update keyboard controller output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search for and initialize the mouse
3Eh	Update NUMLOCK status
3Fh	OEM initialization of COM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's initialization of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot:



P/N: 411906900001
Description: PWA-MPDOG;Mini PCI Dogkeller Card
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 No Display (*2)
- 8.3 LCD No Display or Picture Abnormal
- 8.4 External Monitor No Display or Color Abnormal
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Disk Drive Test Error
- 8.8 CD-ROM Drive Test Error
- 8 .9 USB Port Test Error
- 8 .10 PC Card Socket Test Error
- 8 .11 Mini-PCI Socket Test Error
- 8 .12 Audio Test Error
- 8 .13 LAN Test Error

8650 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Ø Check whether there are any voltage feedback control to turn off the power.
- Ø Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Ø Check which power will cause no display.
- Ø Check which reset signal will cause no display.
- Ø Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

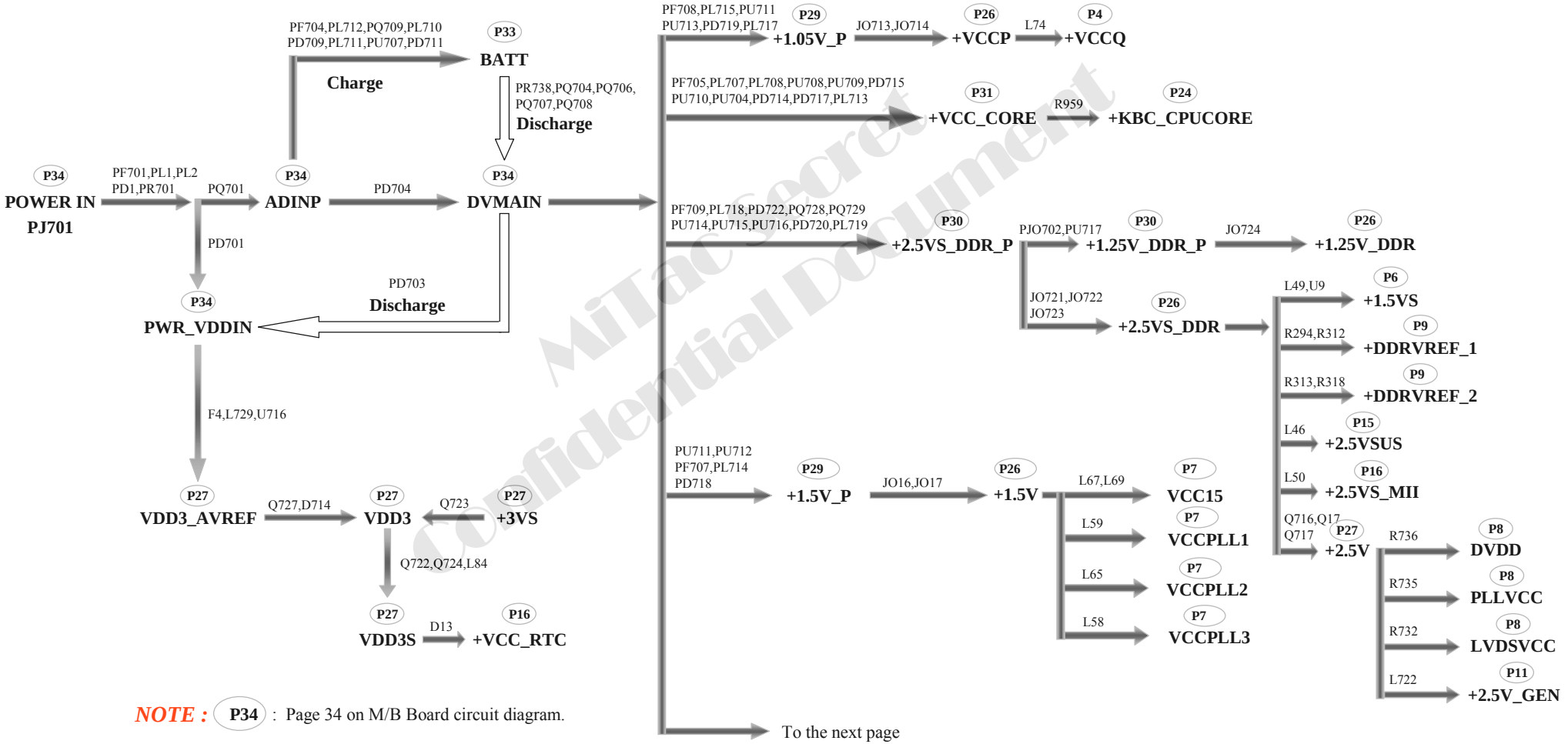
- Ø S5: *Soft Off*
- Ø S0: *Working*

For detail please refer the ACPI specification

8.1 No Power (1)

When power button is pressed, nothing happens, power indicator does not light up.

Main Voltage Map



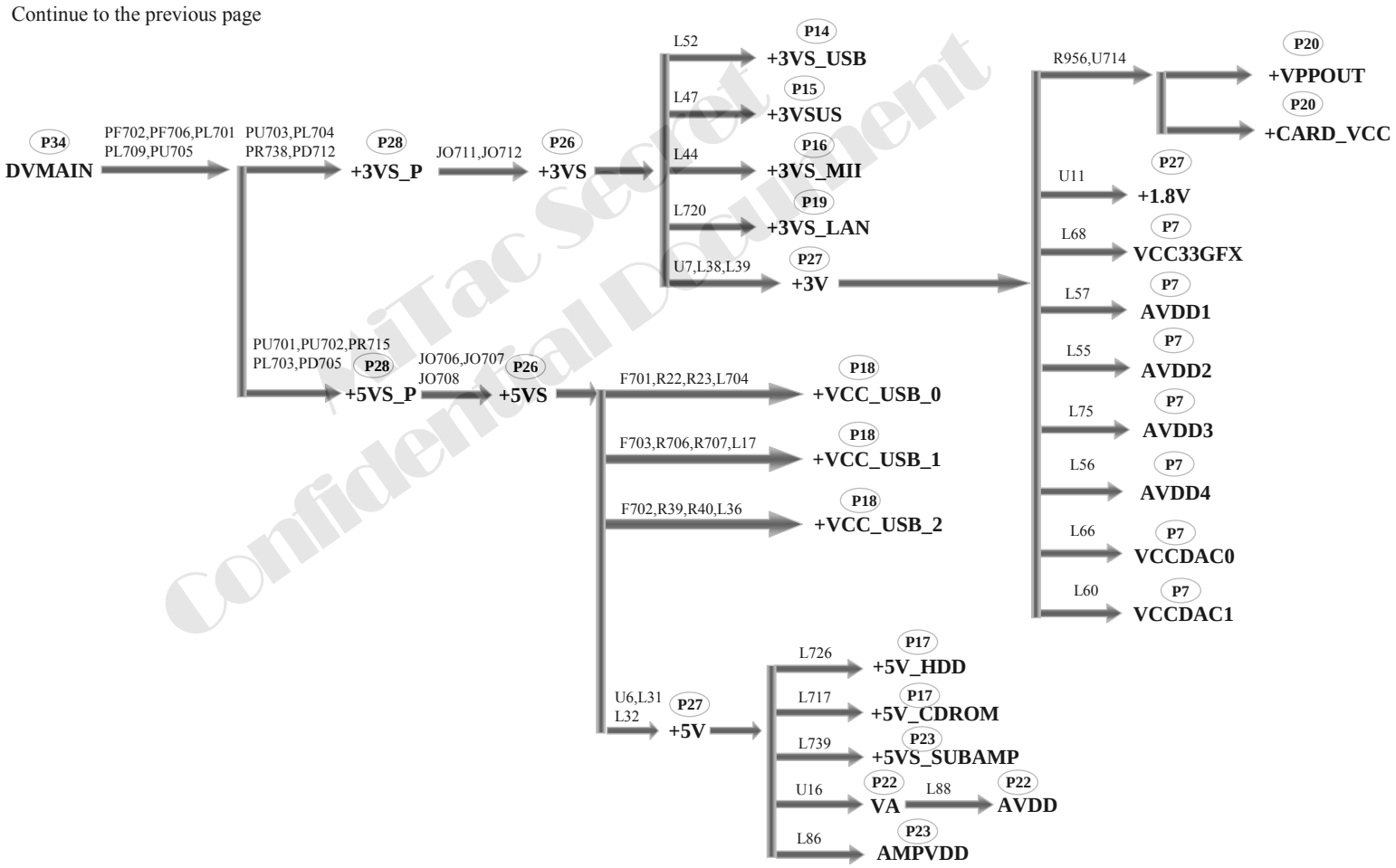
NOTE : **P34** : Page 34 on M/B Board circuit diagram.

PF701 : Through by part PF701.

8.1 No Power (2)

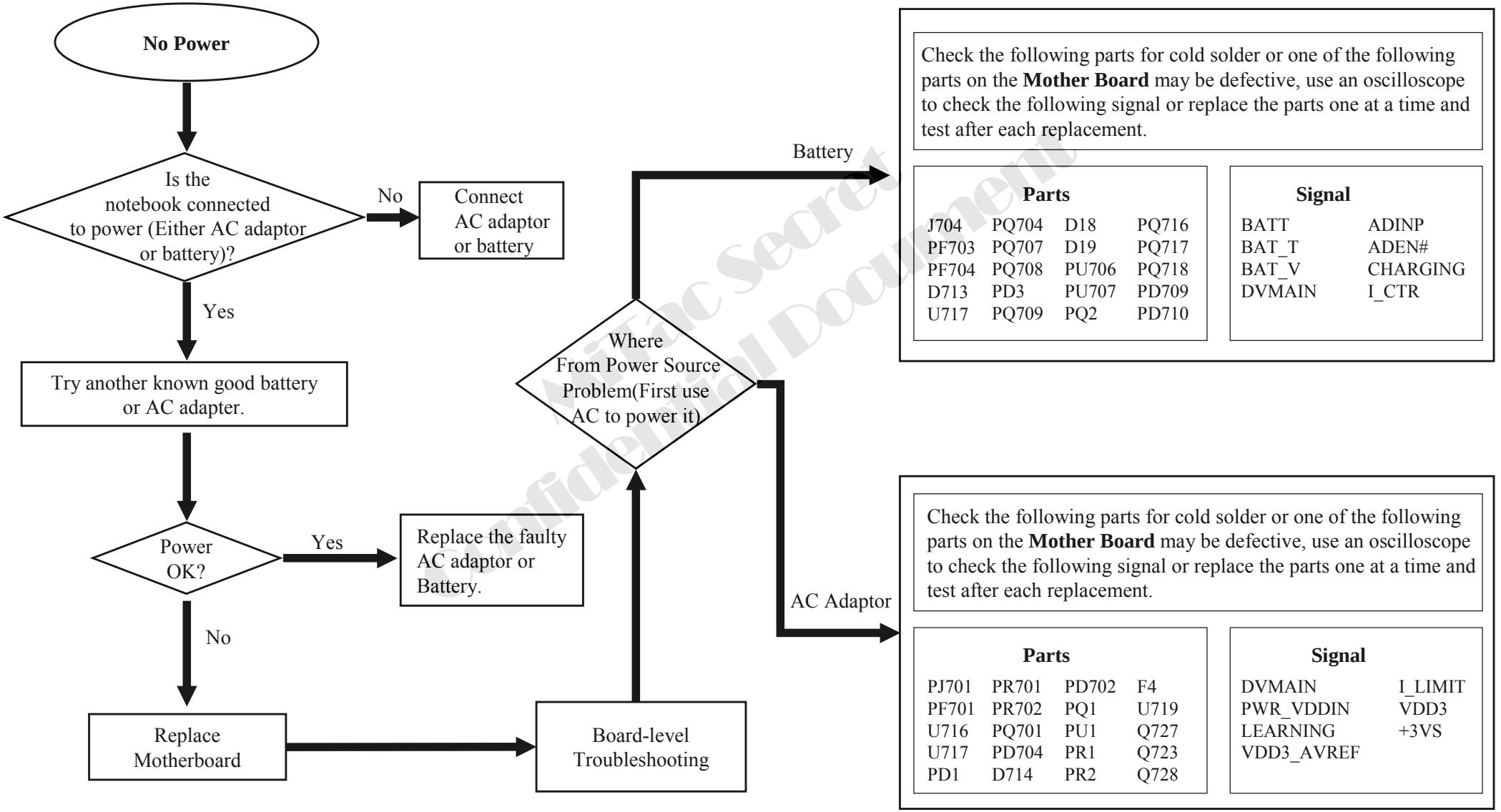
When power button is pressed, nothing happens, power indicator does not light up.

Main Voltage Map



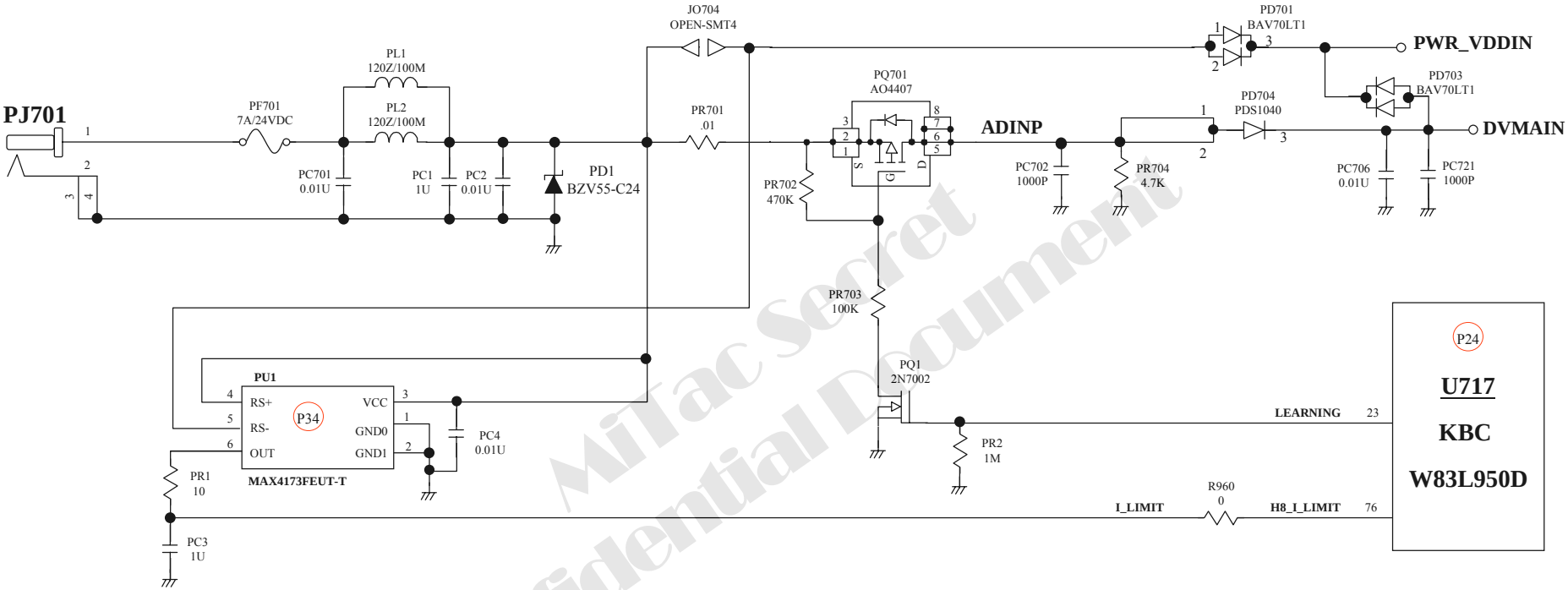
8.1 No Power (3)

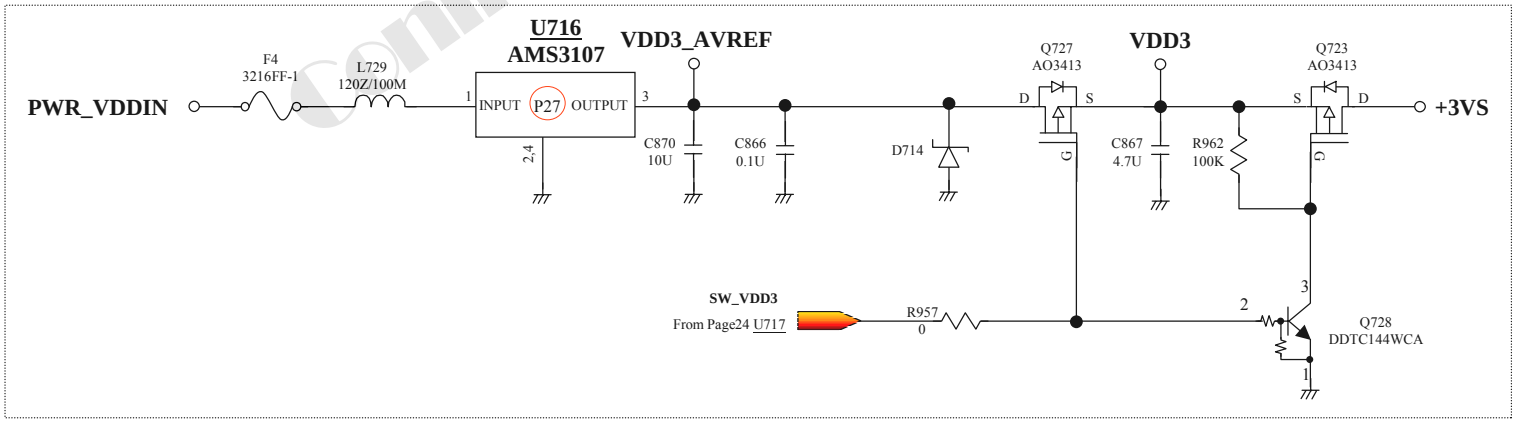
When power button is pressed, nothing happens, power indicator does not light up.



8.1 No Power (4)

When power button is pressed, nothing happens, power indicator does not light up.

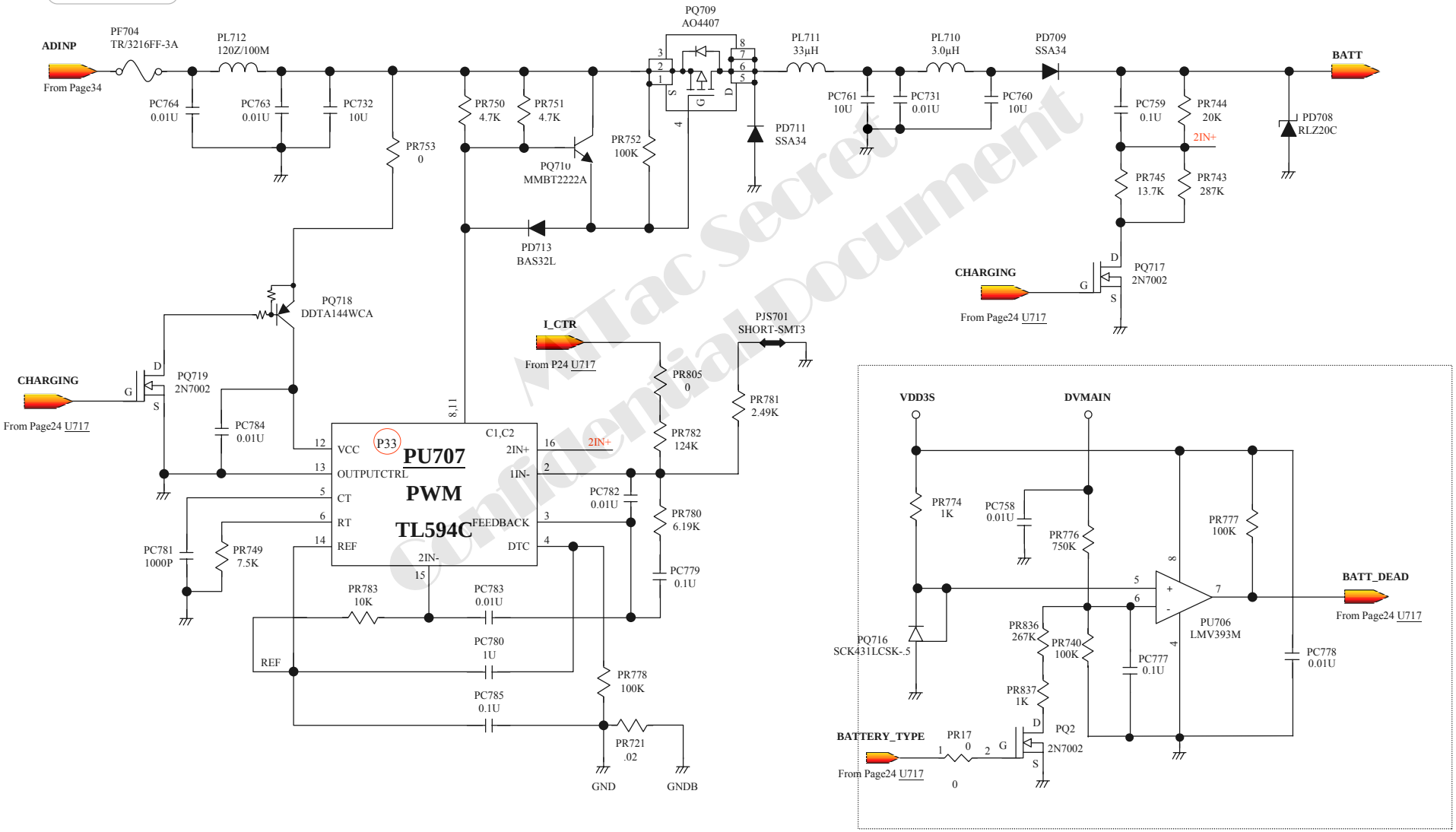




8.1 No Power (5)

When power button is pressed, nothing happens, power indicator does not light up.

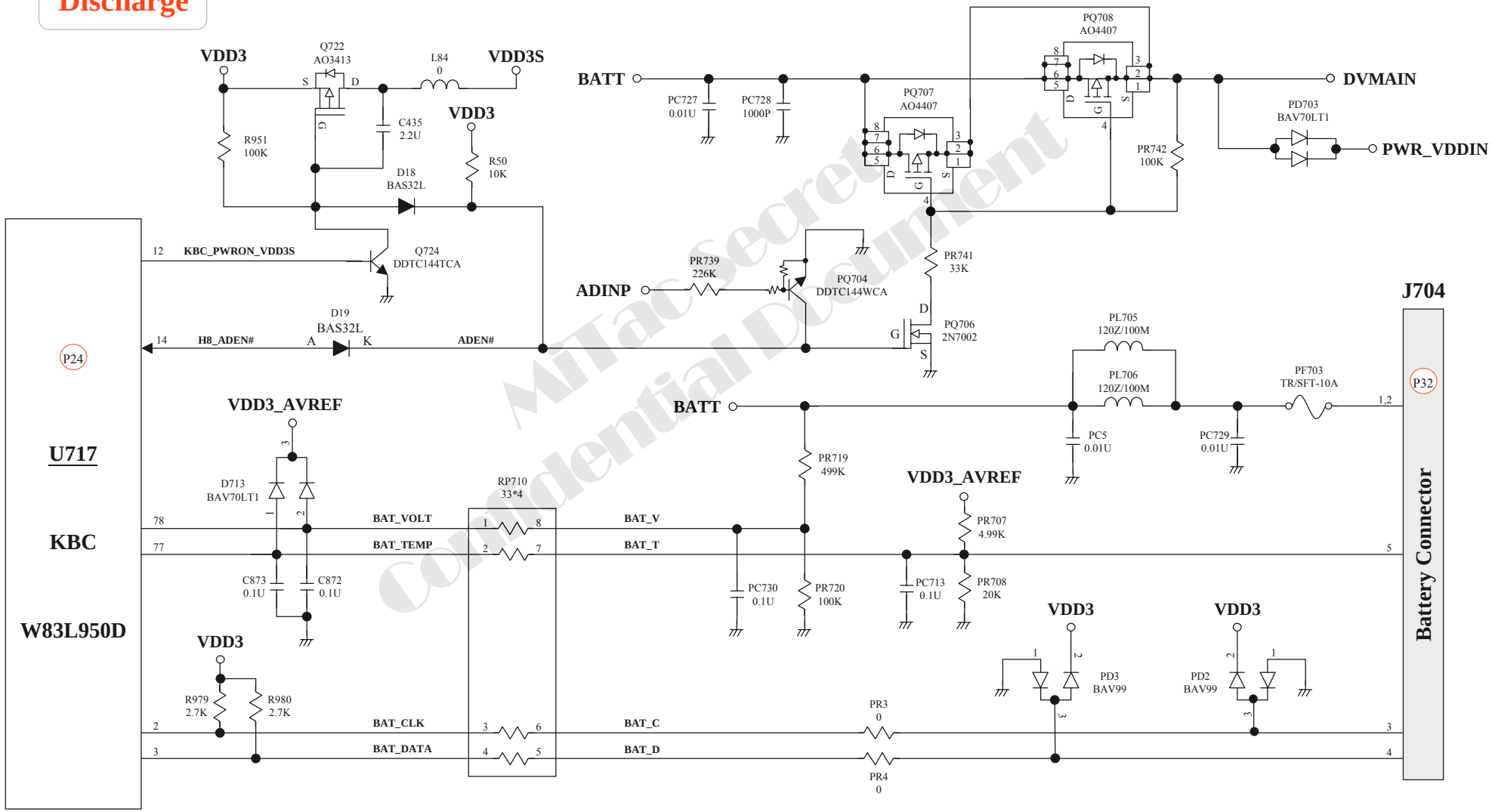
Charge



8.1 No Power (6)

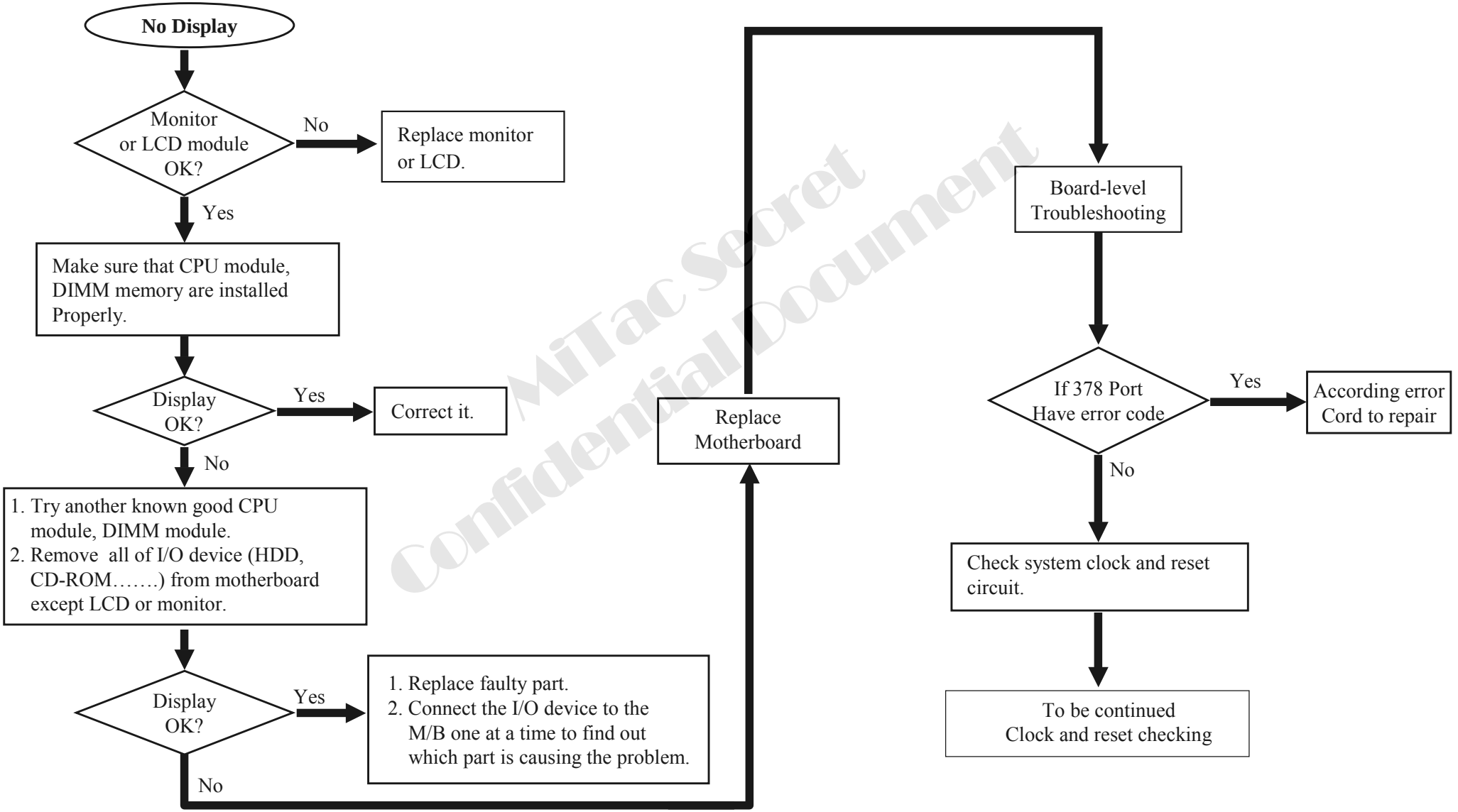
When power button is pressed, nothing happens, power indicator does not light up.

Discharge



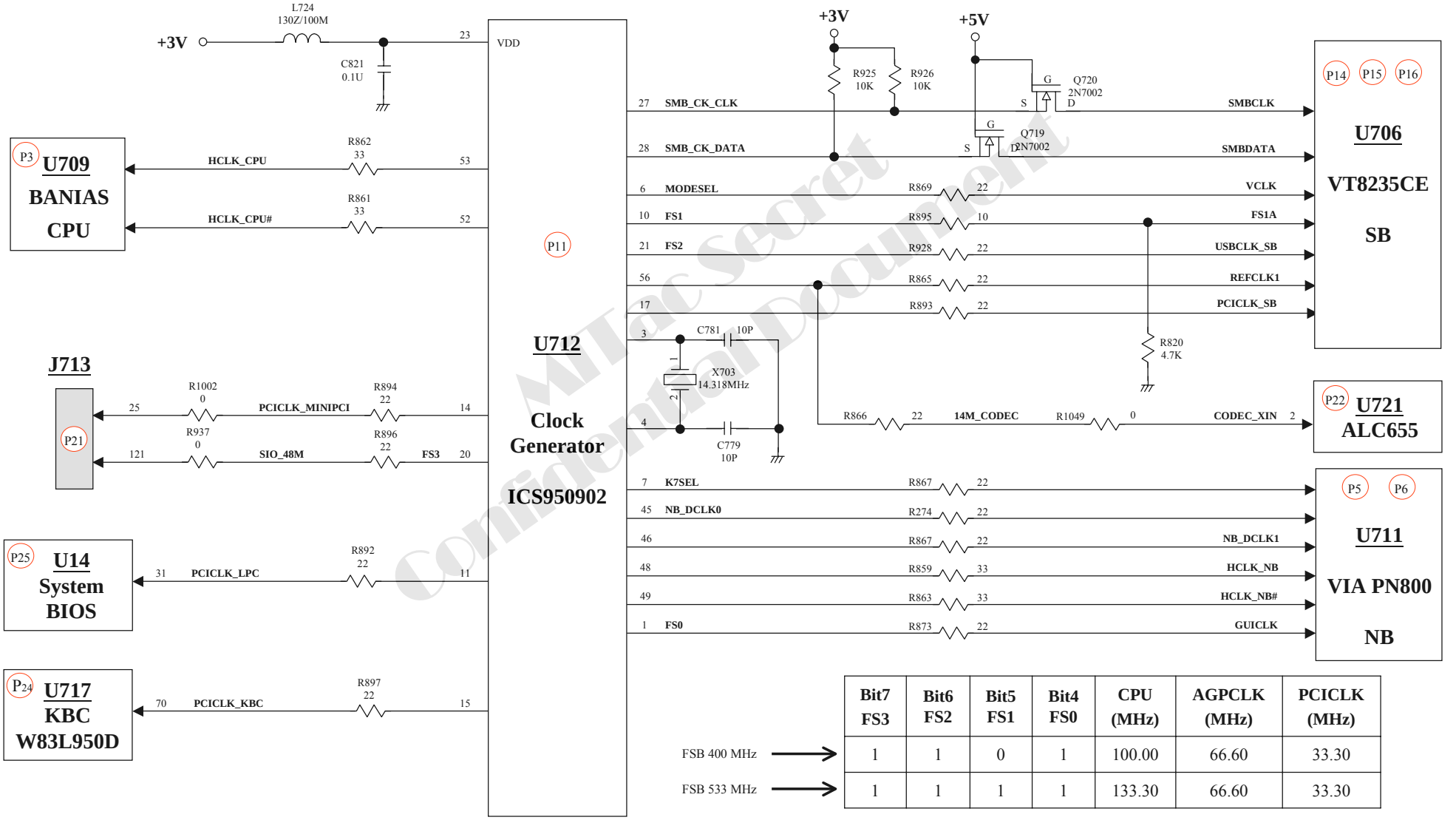
8.2 No Display (1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



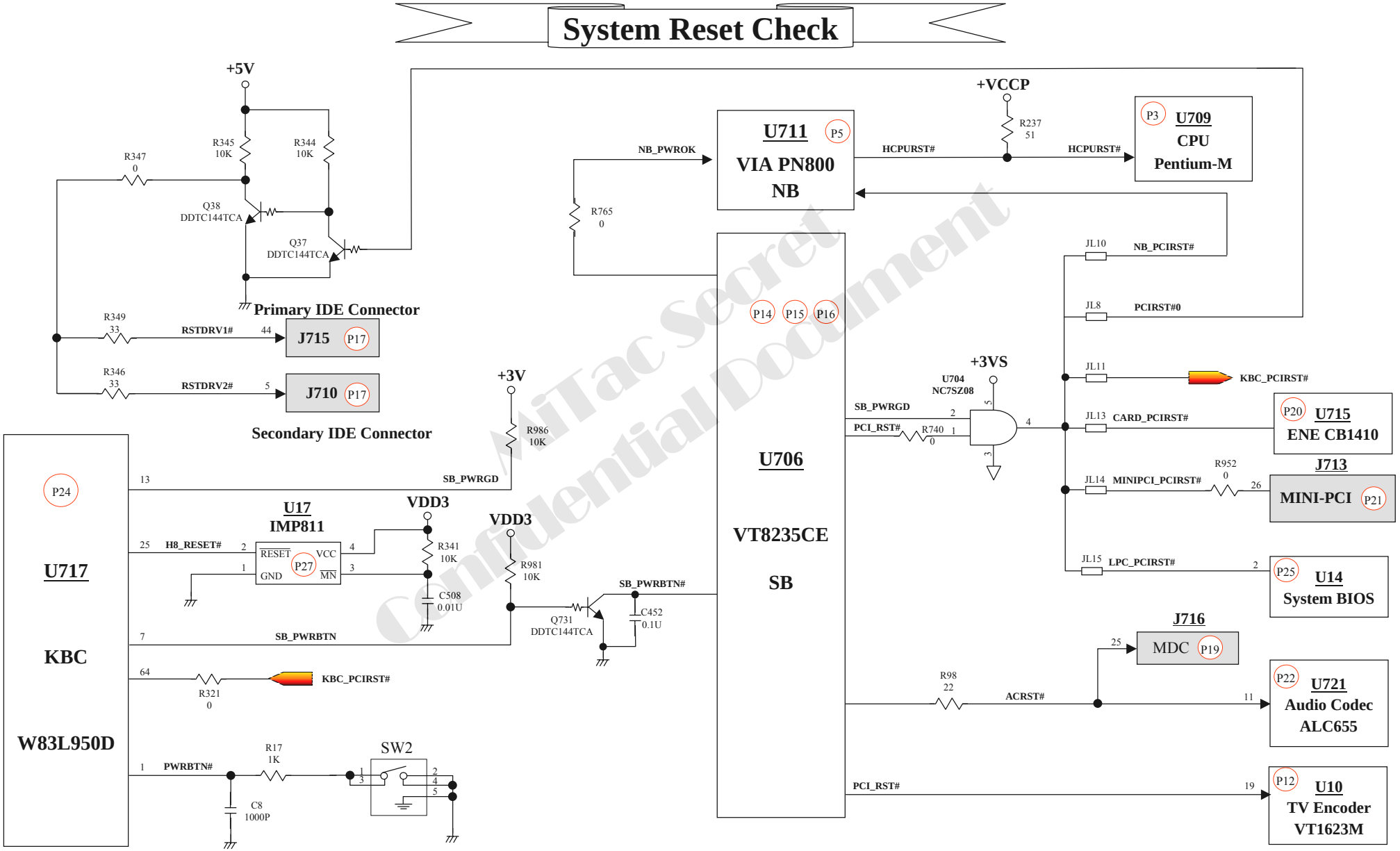
8.2 No Display (2)

System Clock Check



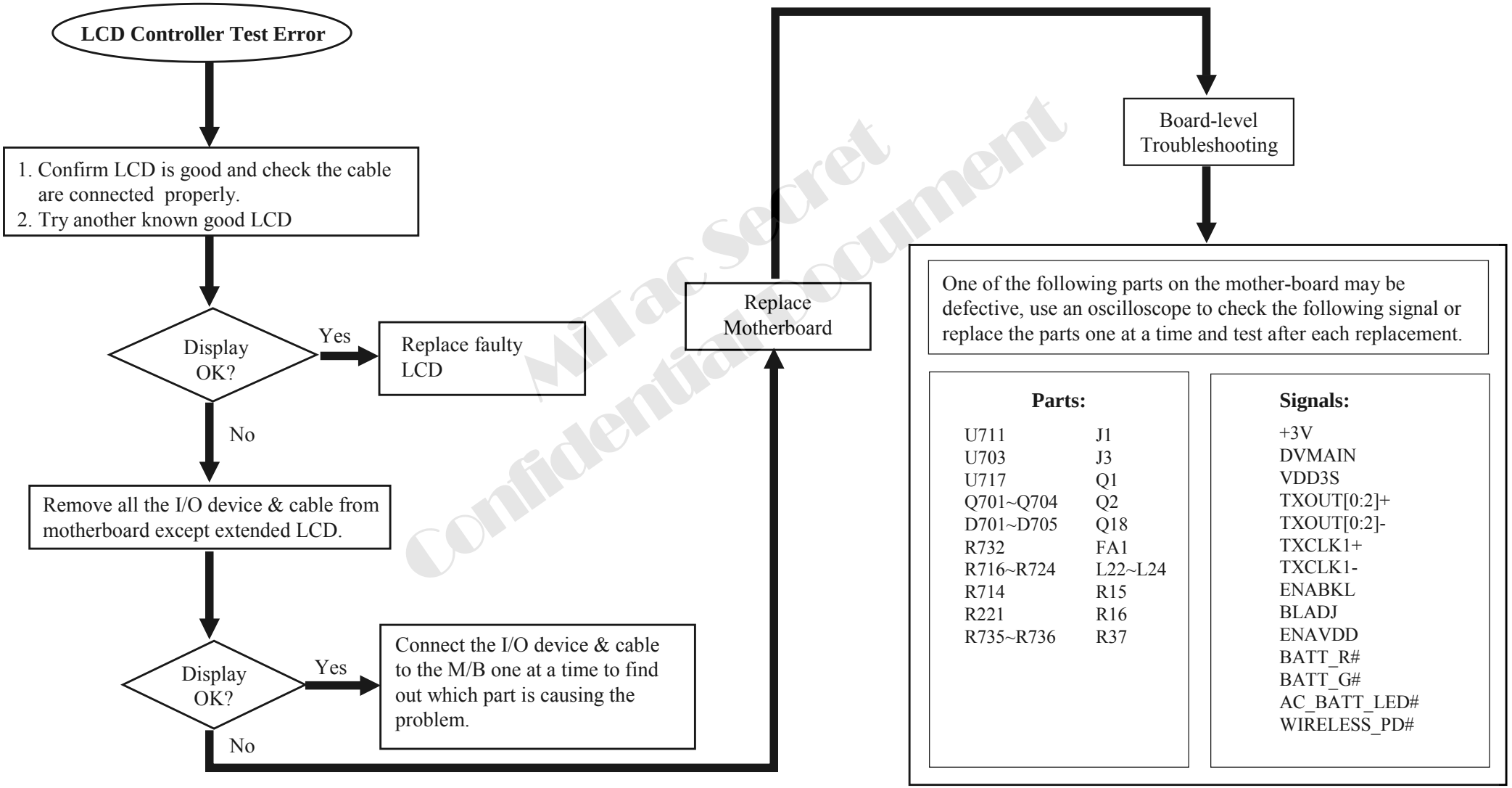
	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU (MHz)	AGPCLK (MHz)	PCICLK (MHz)
FSB 400 MHz →	1	1	0	1	100.00	66.60	33.30
FSB 533 MHz →	1	1	1	1	133.30	66.60	33.30

8.2 No Display (3)



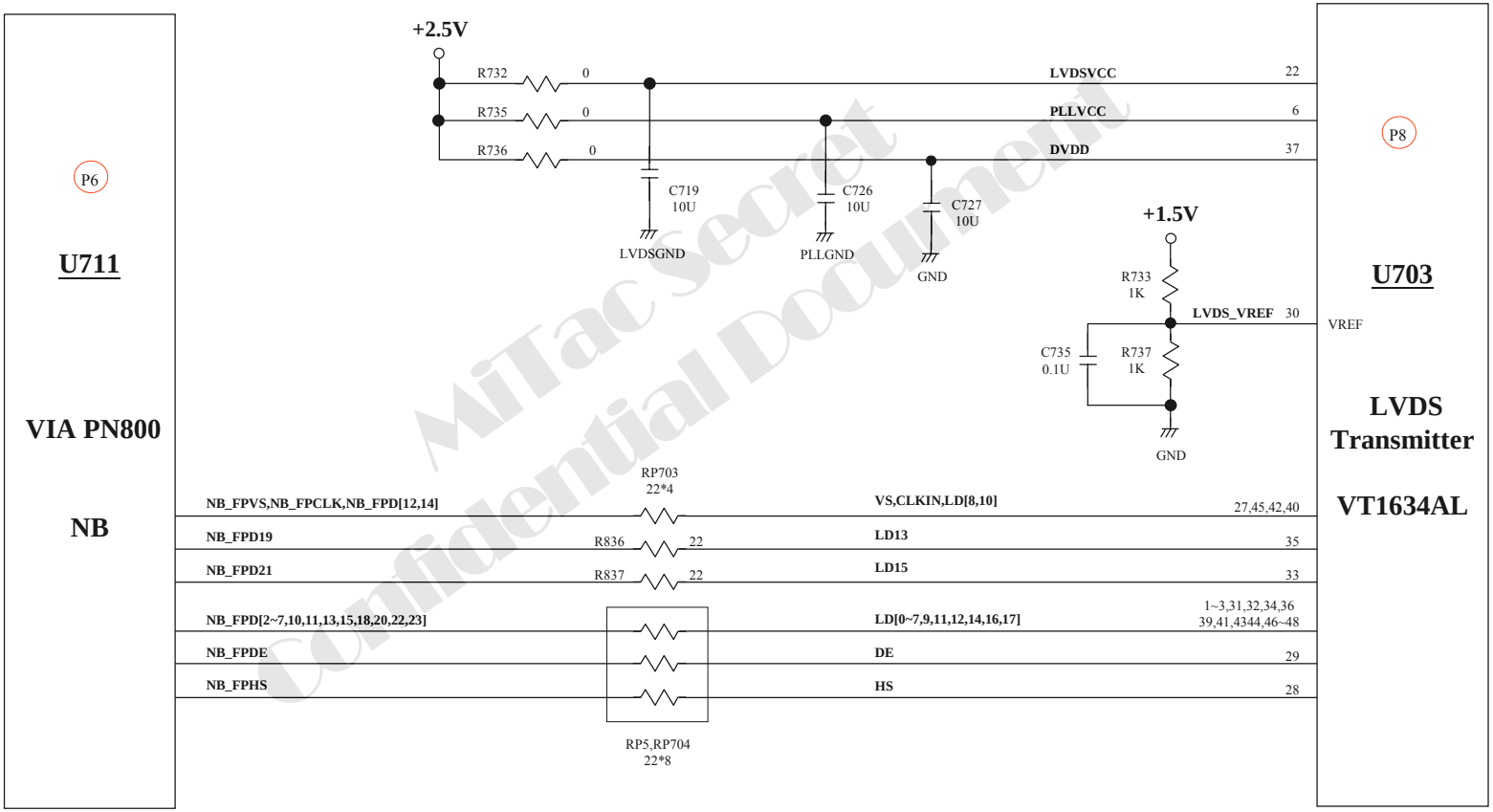
8.3 LCD No Display or Picture Abnormal (1)

There is no display or picture abnormal on LCD or monitor.



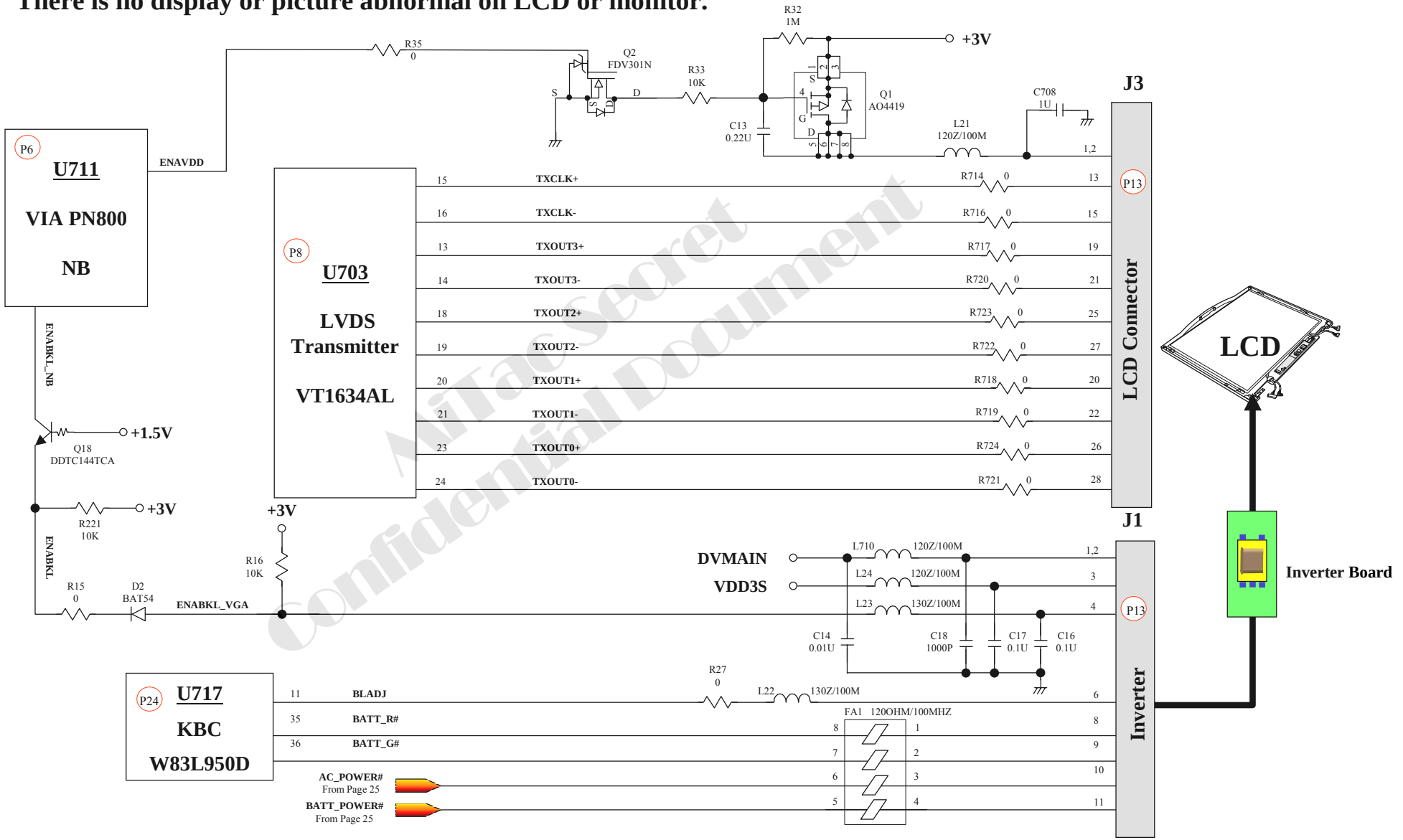
8.3 LCD No Display or Picture Abnormal (2)

There is no display or picture abnormal on LCD or monitor.



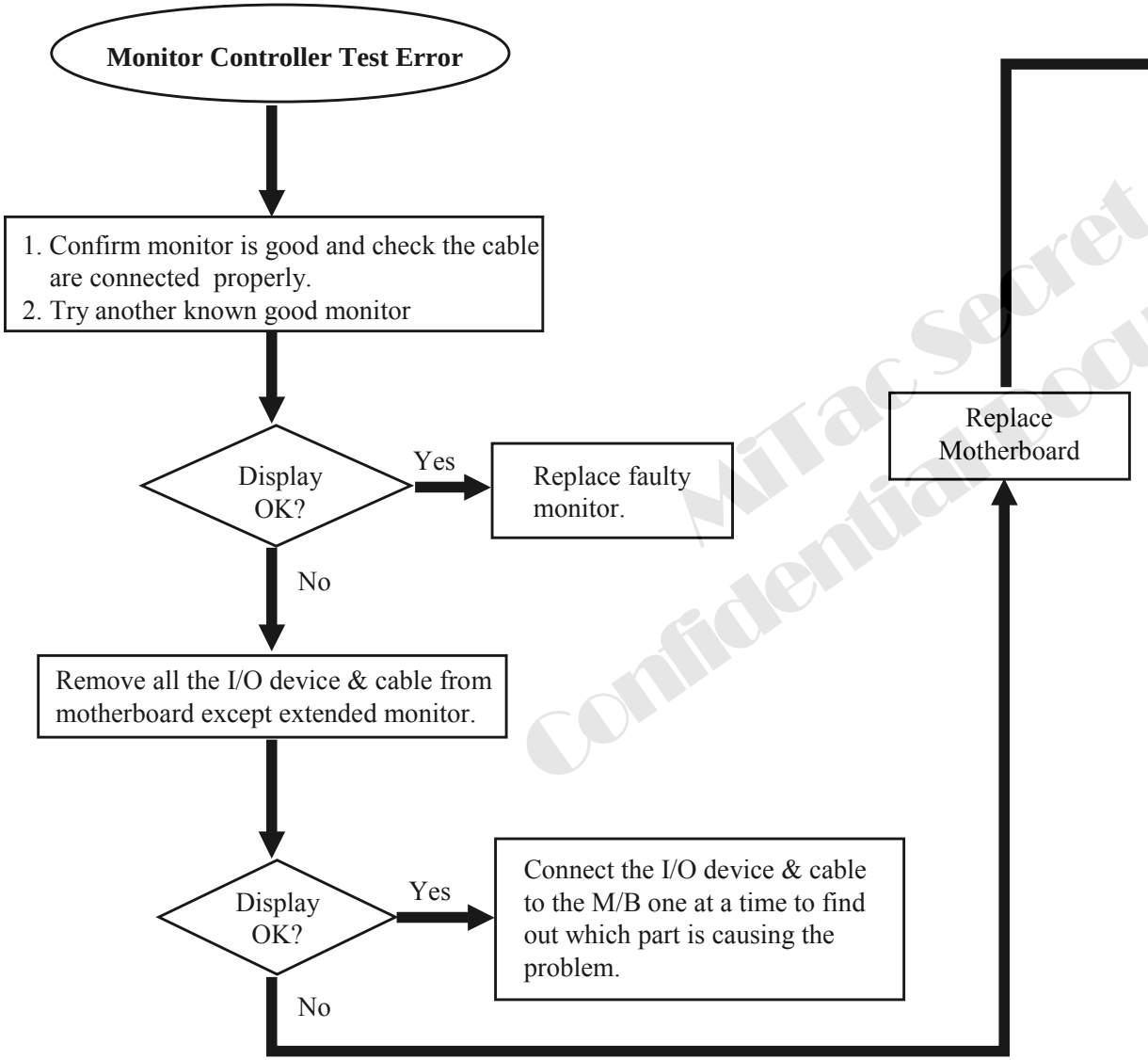
8.3 LCD No Display or Picture Abnormal (3)

There is no display or picture abnormal on LCD or monitor.



8.4 External Monitor No Display or Color Abnormal (1)

There is no display or picture abnormal on monitor.



Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

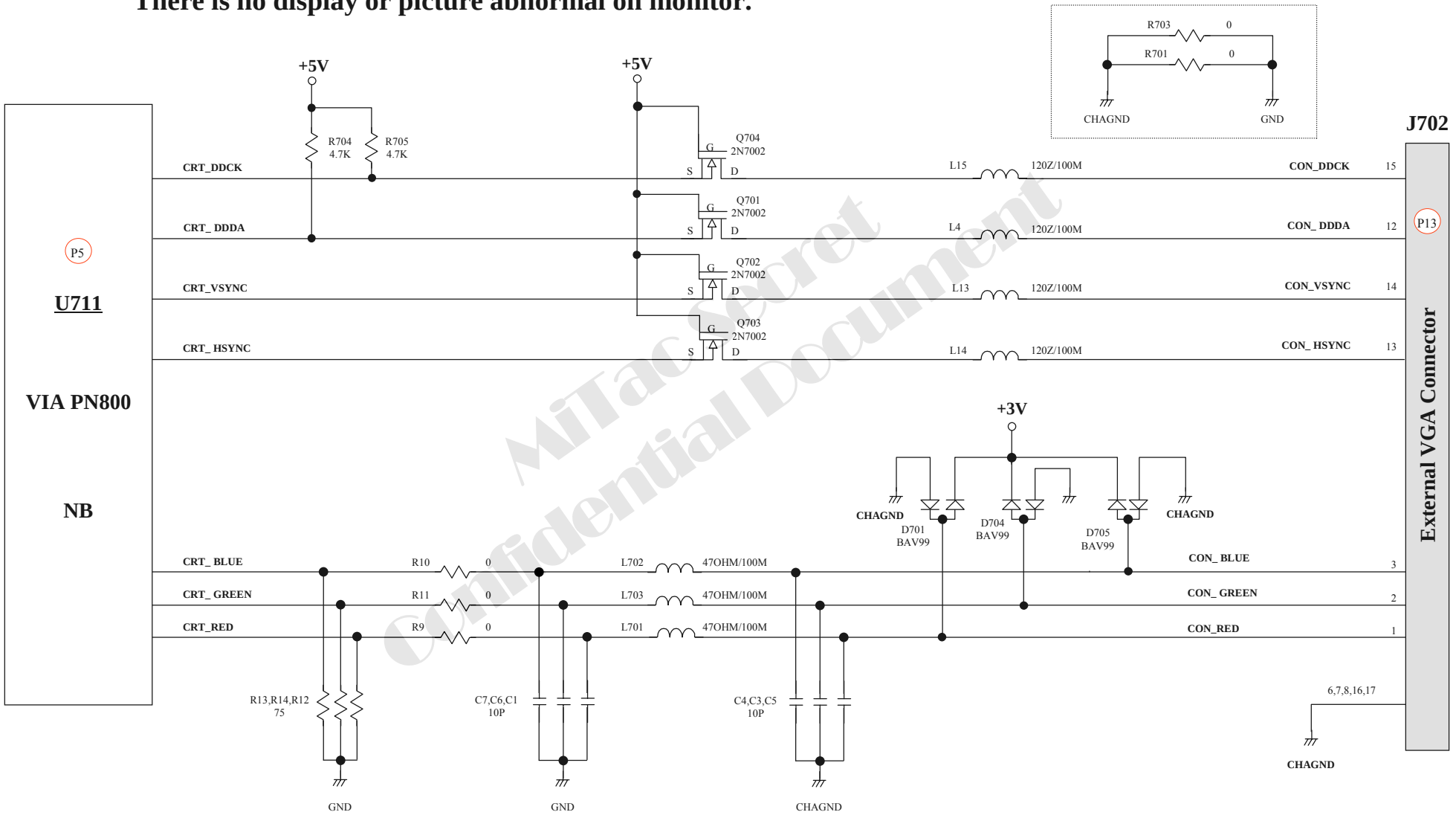
U711
J702
L4
L13~15
R12~14
Q701~704
R12~14
D701
D704
D705

Signals:

+5V	CHAGND
CRT_RED	CON_RED
CRT_GREEN	CON_GREEN
CRT_BLUE	CON_BLUE
CRT_DDCK	CON_DDDA
CRT_DDDA	CON_HSYNC
CRT_HSYNC	CON_VSYNC
CRT_VSYNC	CON_DDCK

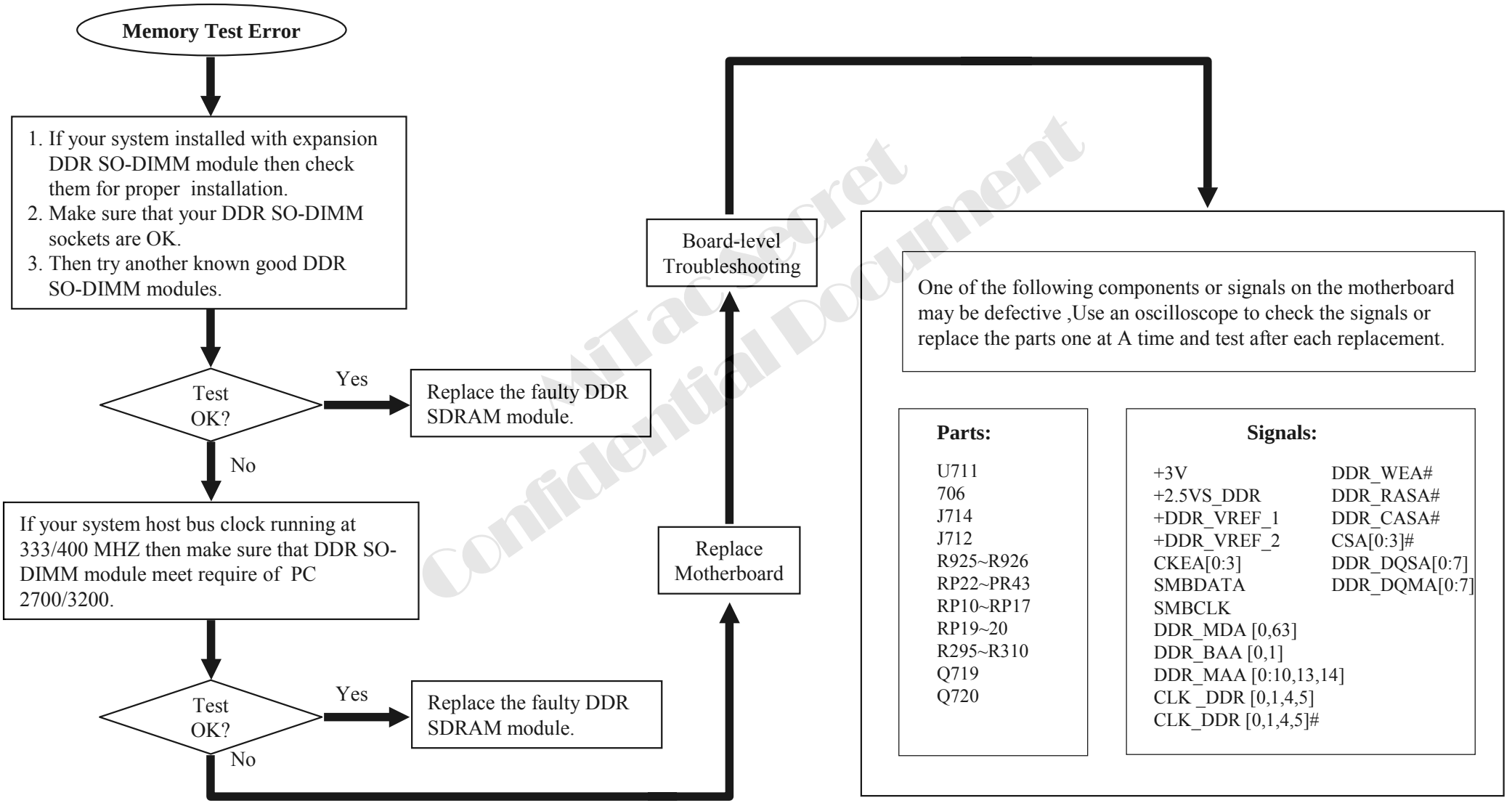
8.4 External Monitor No Display or Color Abnormal (2)

There is no display or picture abnormal on monitor.



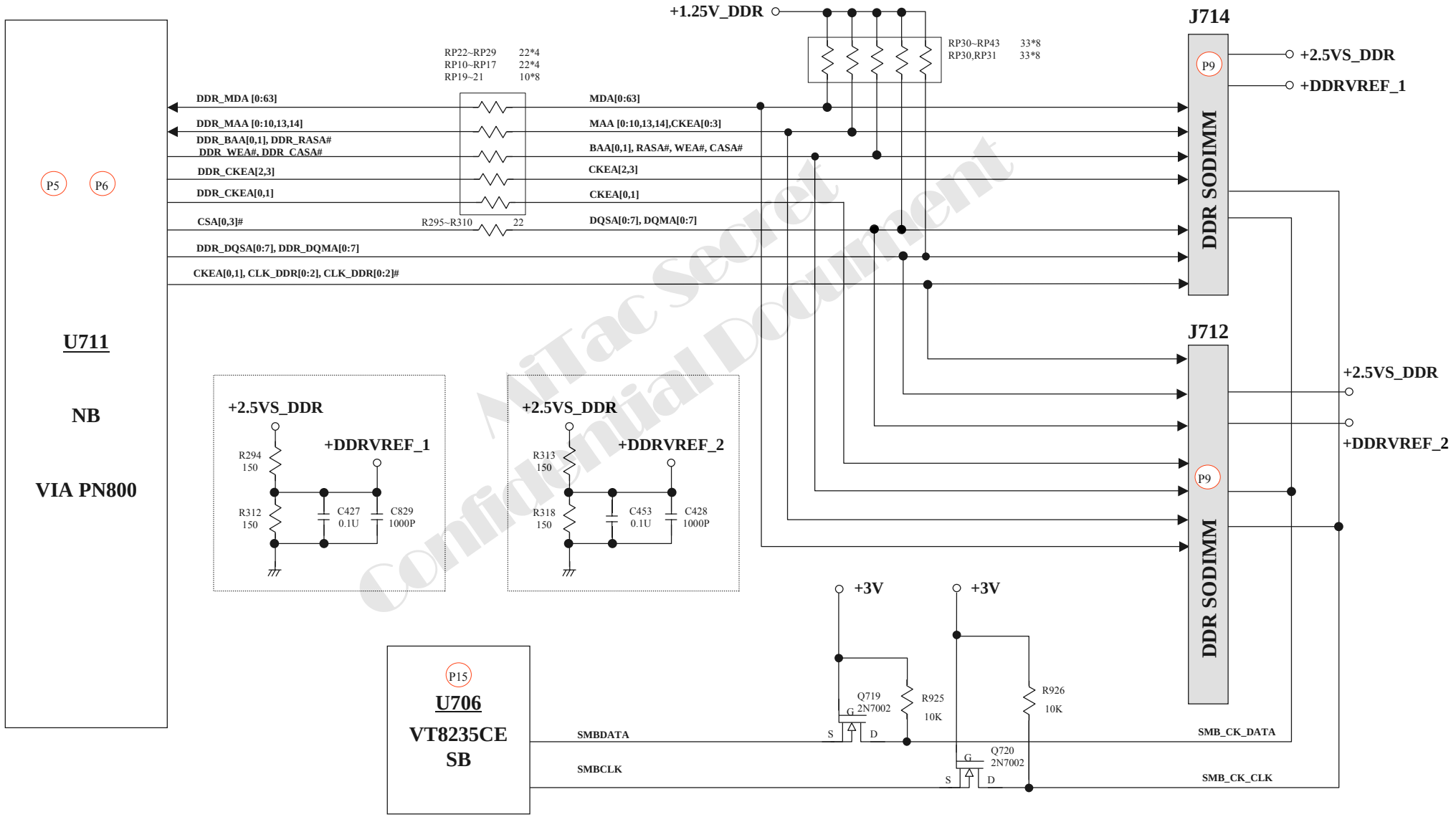
8.5 Memory Test Error (1)

Extend DDRAM tests error or system hangs up.



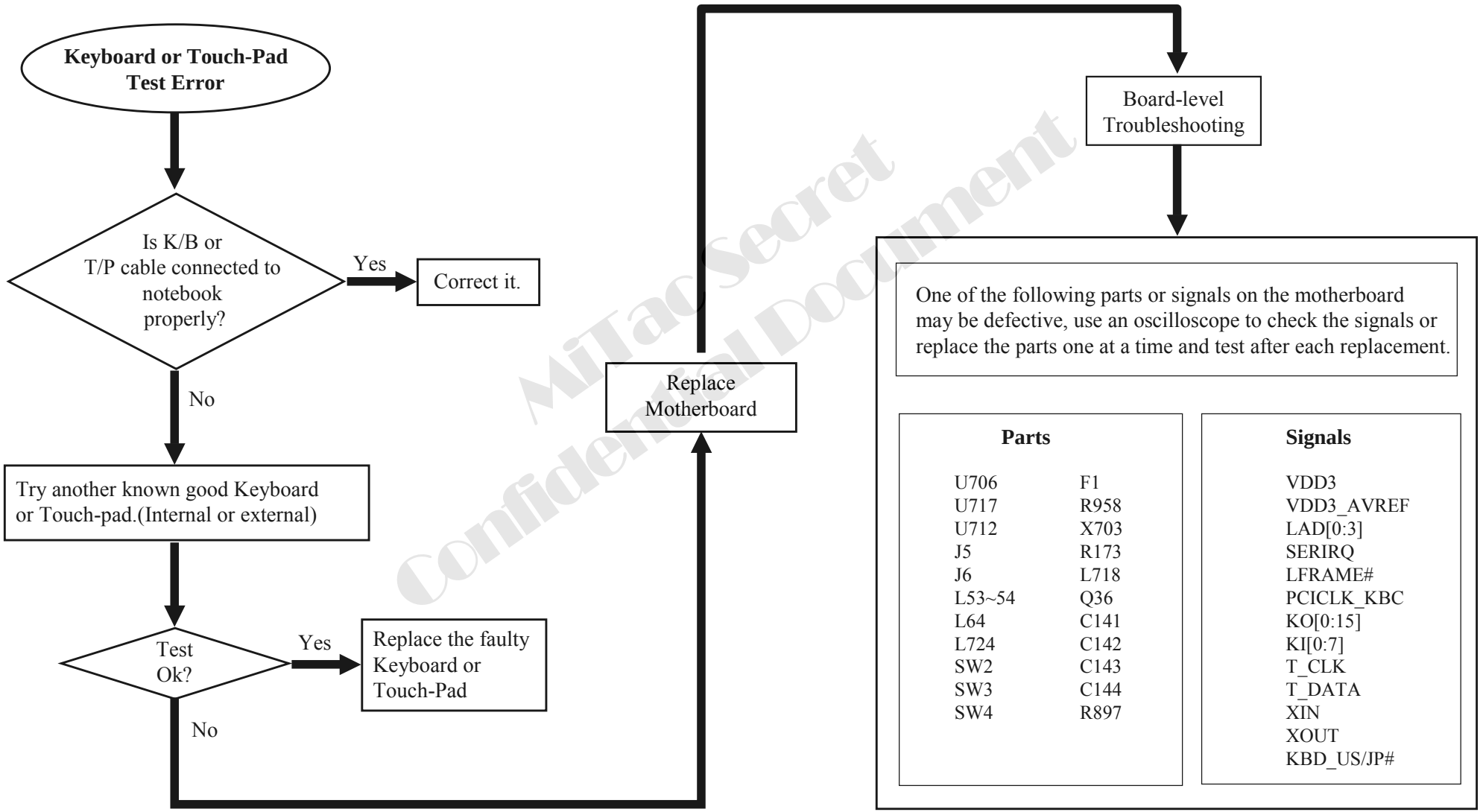
8.5 Memory Test Error (2)

Extend DDRAM tests error or system hangs up.



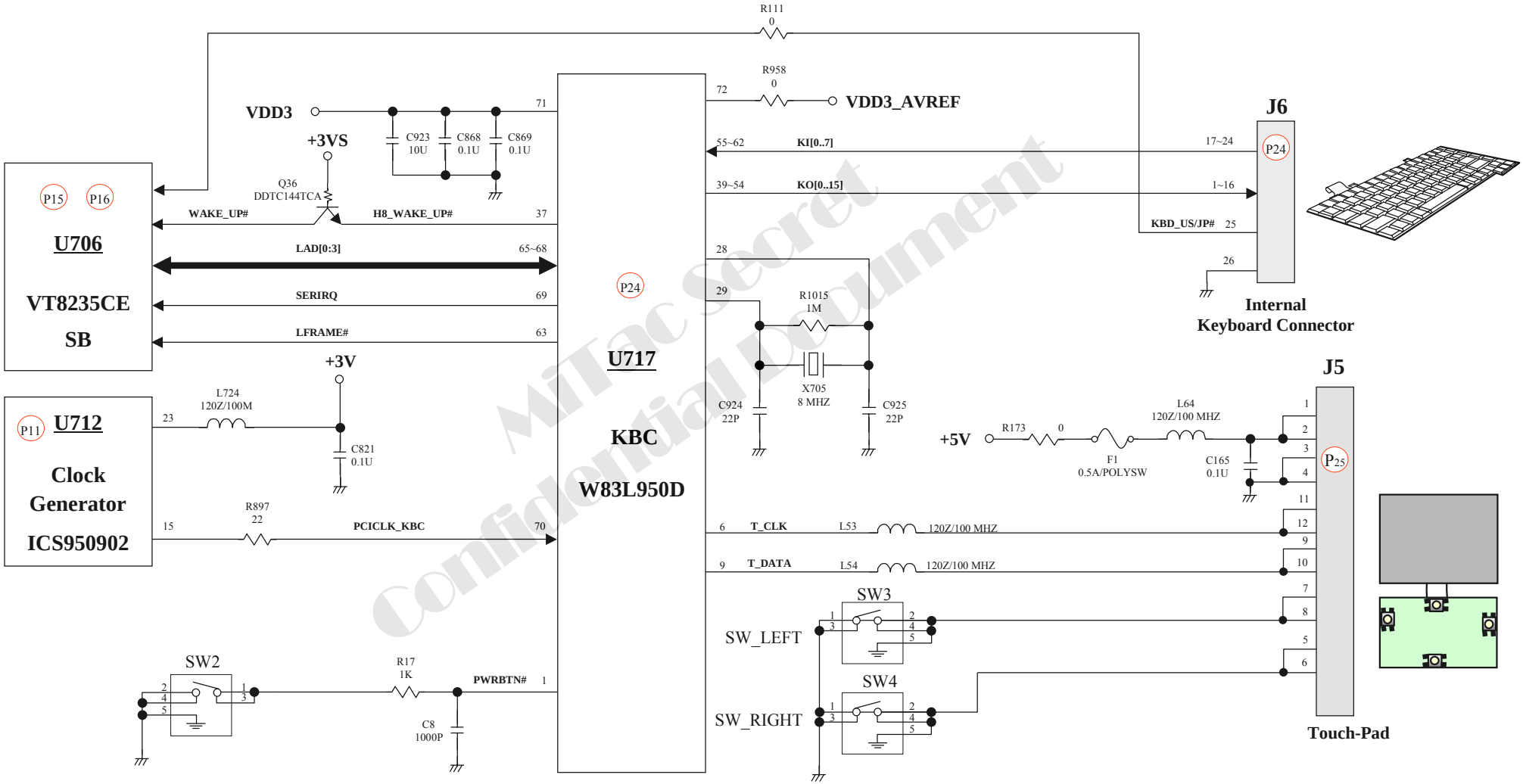
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

Error message of keyboard or touch-pad is shown or any key does not work.



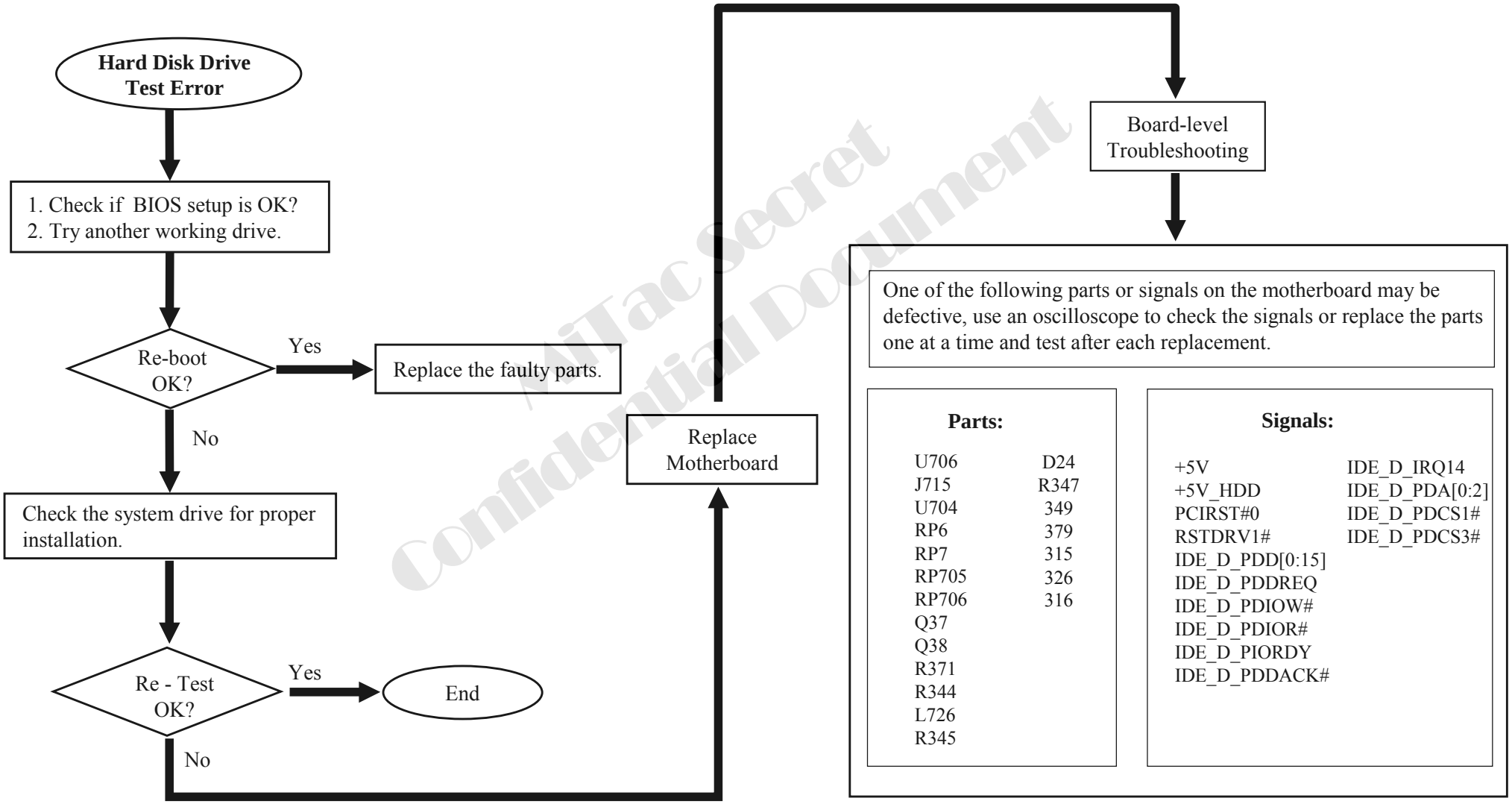
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

keyboard or touch-pad error is shown or any key does not work.



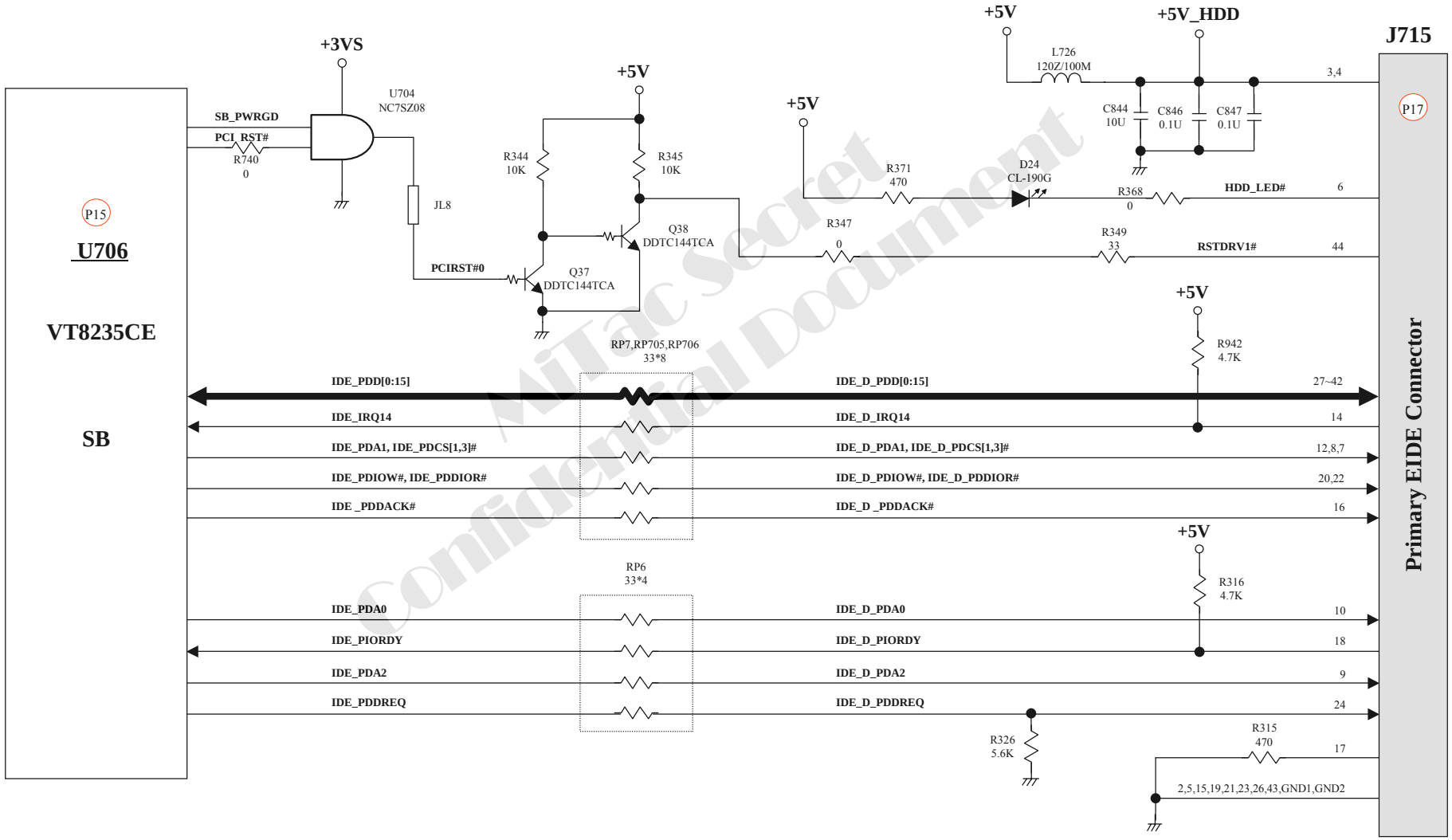
8.7 Hard Disk Drive Test Error (1)

Either an error message is shown, or the driver motor continues spinning, while reading data from or writing data to hard disk drive.



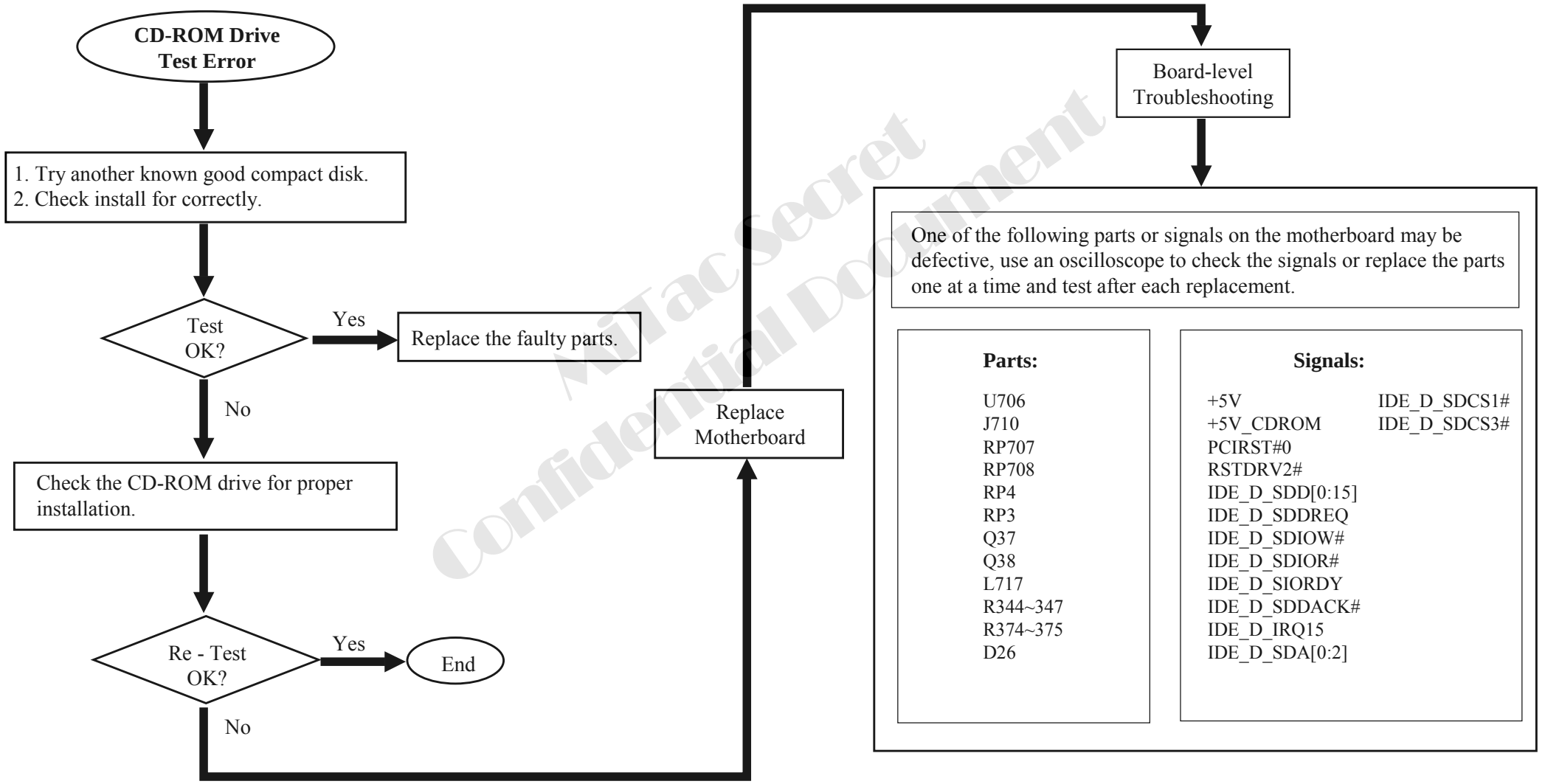
8.7 Hard Disk Drive Test Error (2)

Either an error message is shown, or the driver motor continues spinning, while reading data from or writing data to hard disk drive.



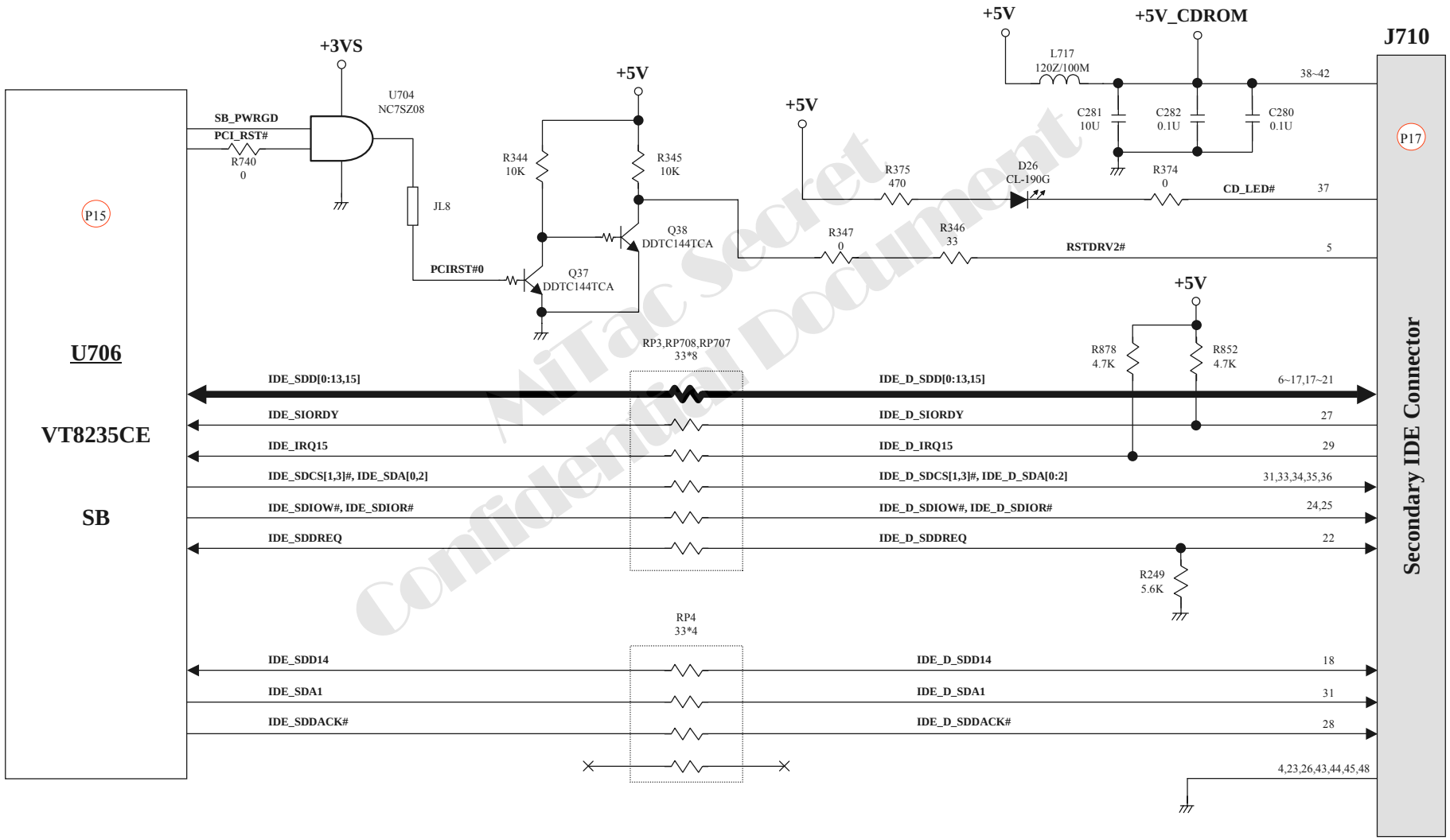
8.8 CD-ROM Drive Test Error (1)

An error message is shown when reading data from CD-ROM drive.



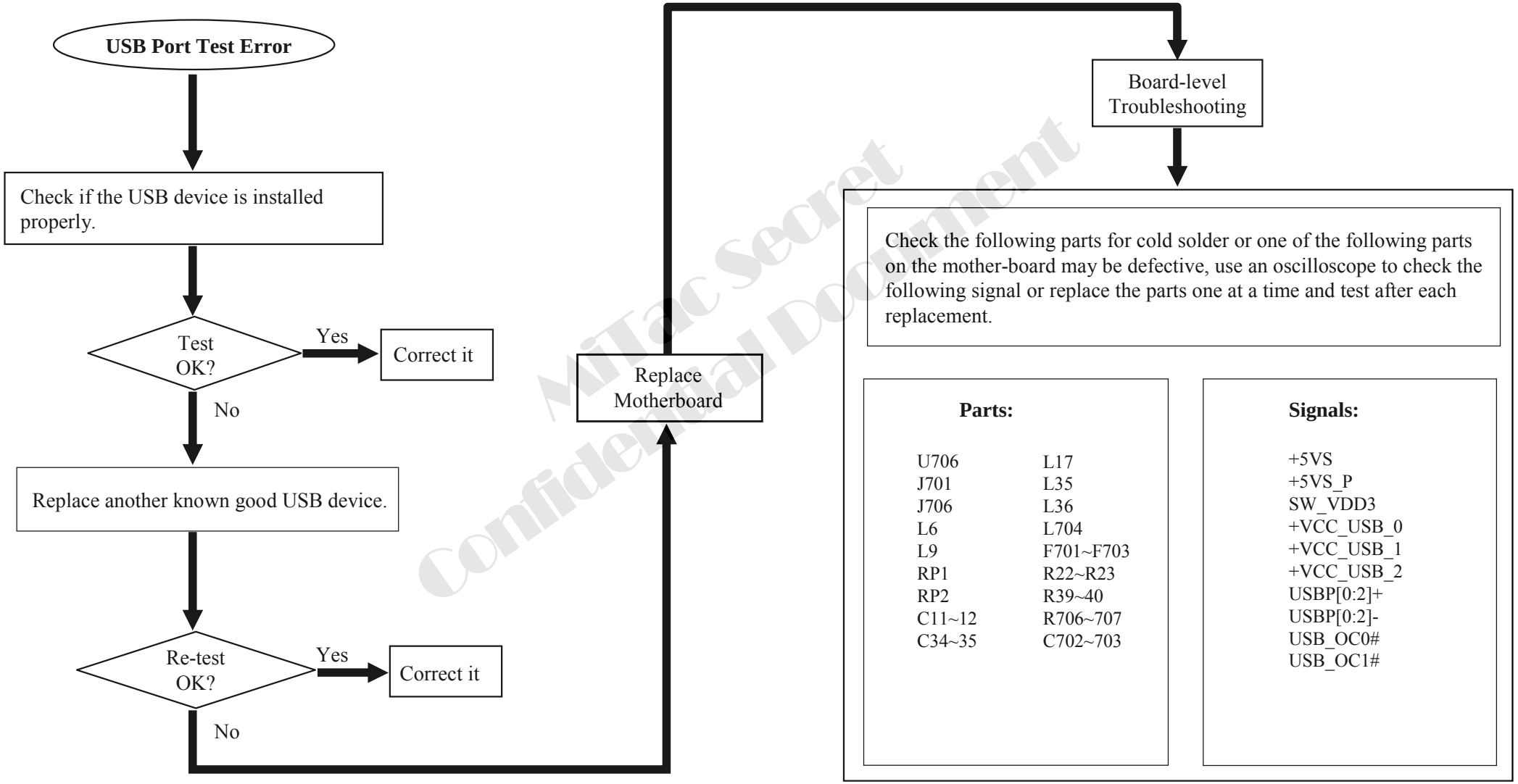
8.8 CD-ROM Drive Test Error (2)

An error message is shown when reading data from CD-ROM drive.



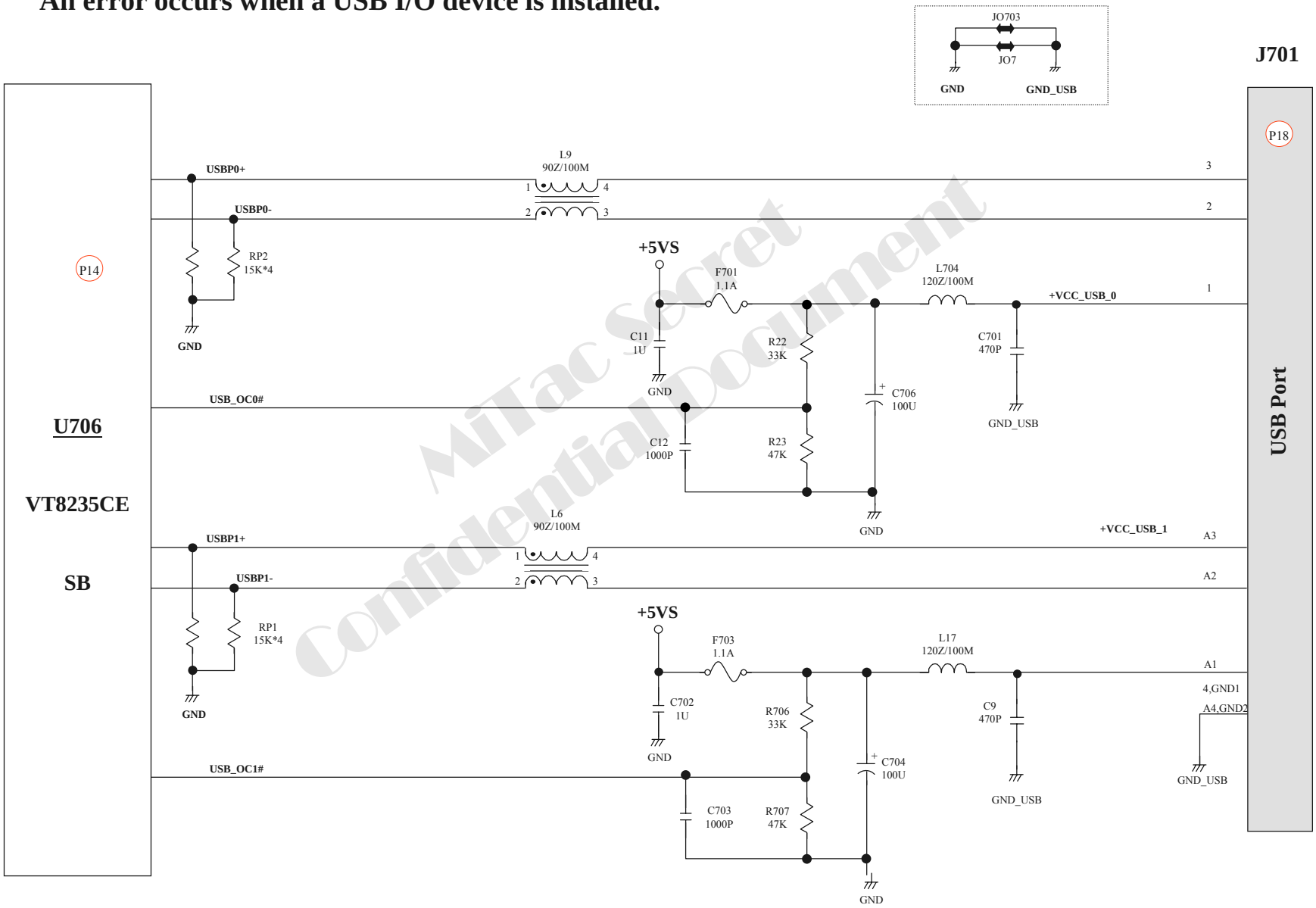
8.9 USB Port Test Error (1)

An error occurs when a USB I/O device is installed.



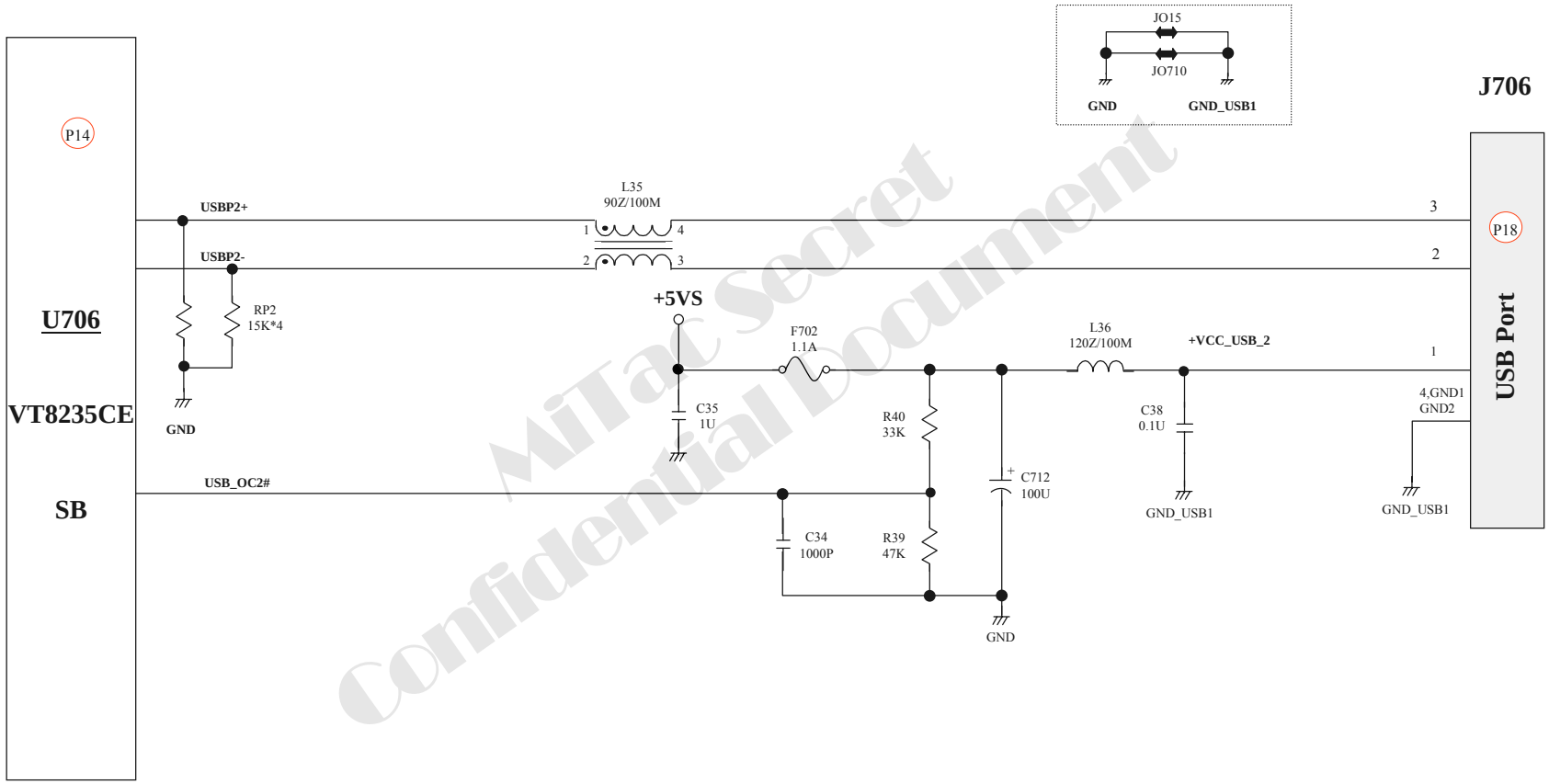
8.9 USB Port Test Error (2)

An error occurs when a USB I/O device is installed.



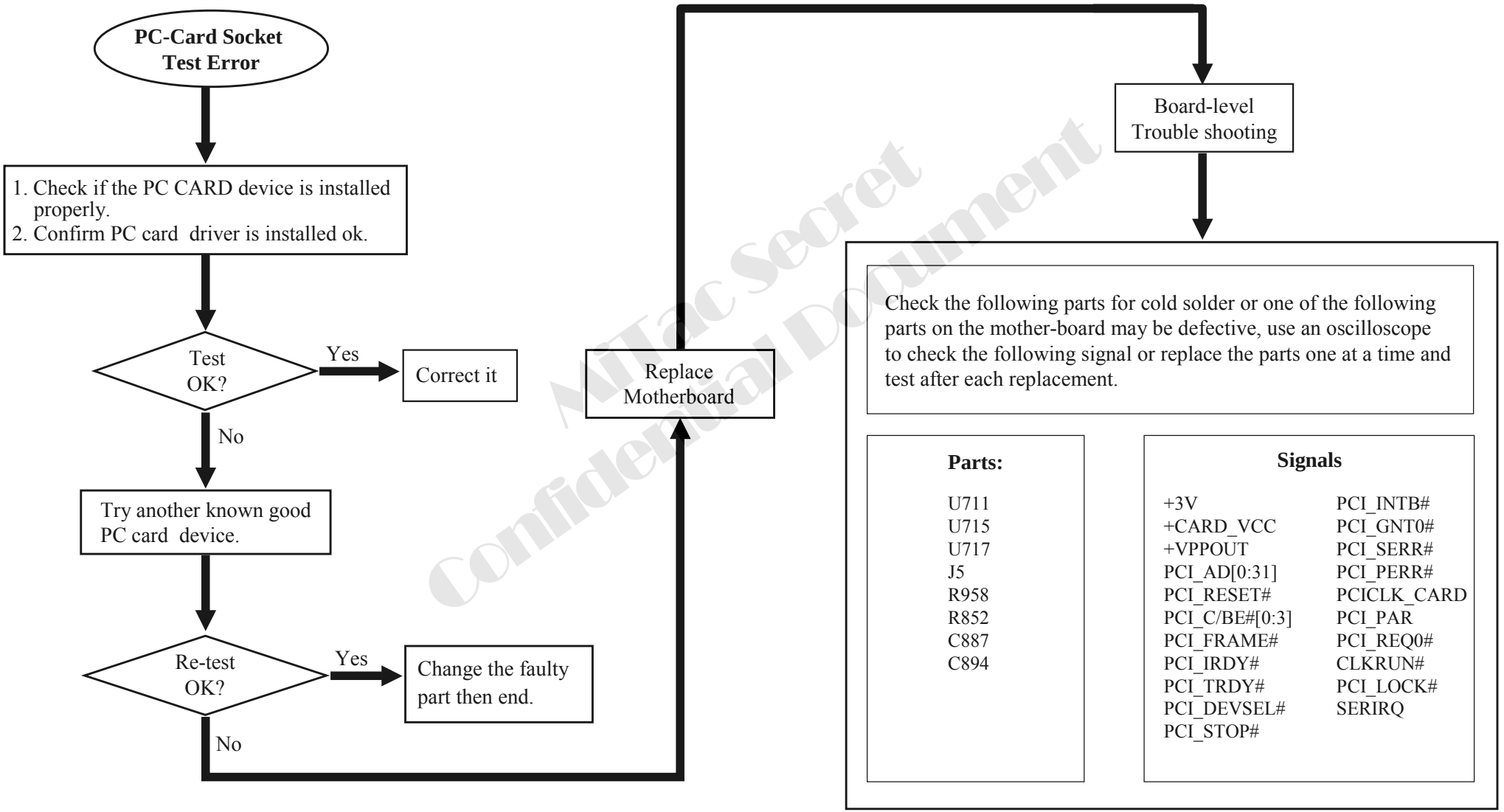
8.9 USB Port Test Error (3)

An error occurs when a USB I/O device is installed.



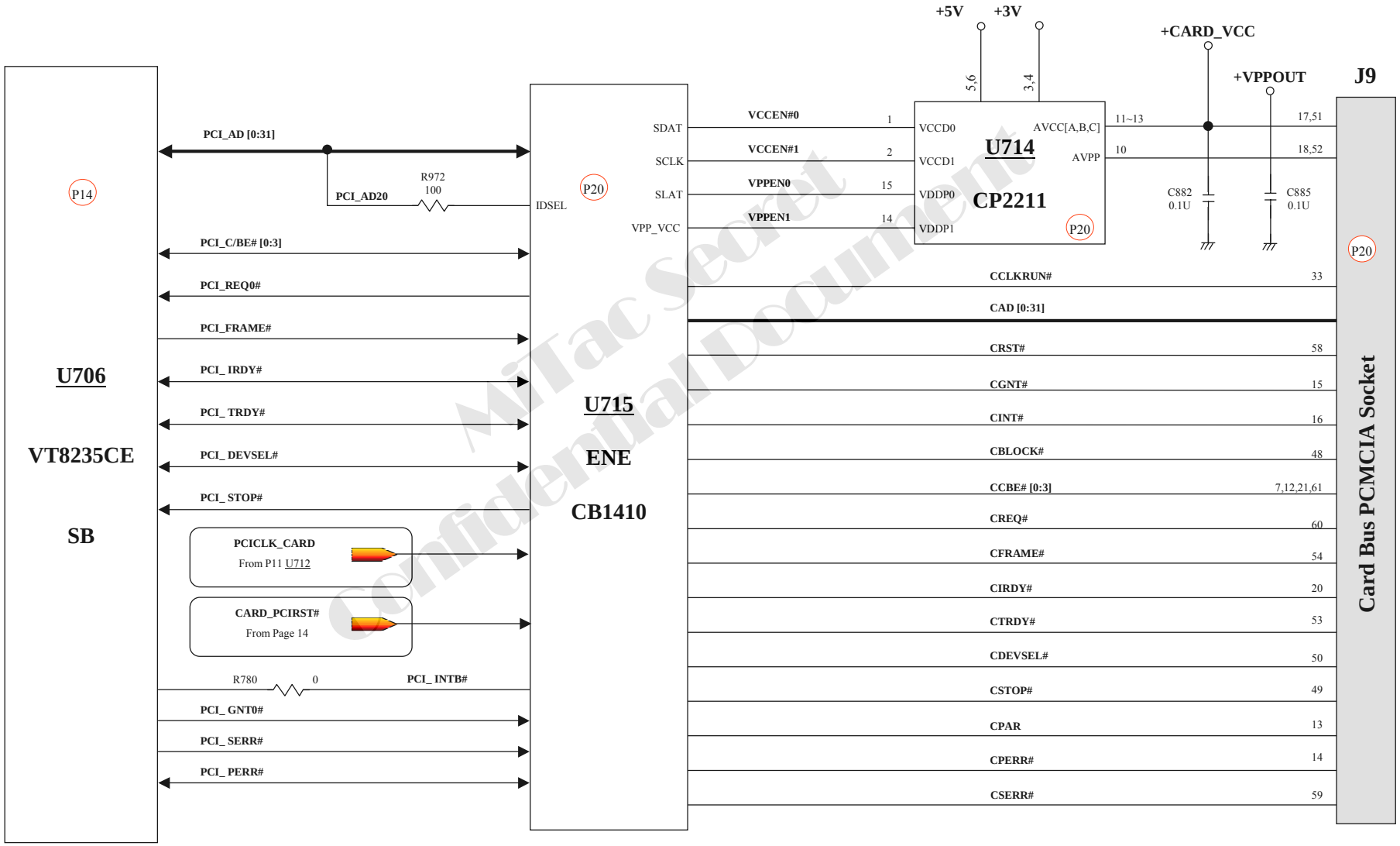
8.10 PC-Card Socket Test Error (1)

An error occurs when a PC card device is installed.



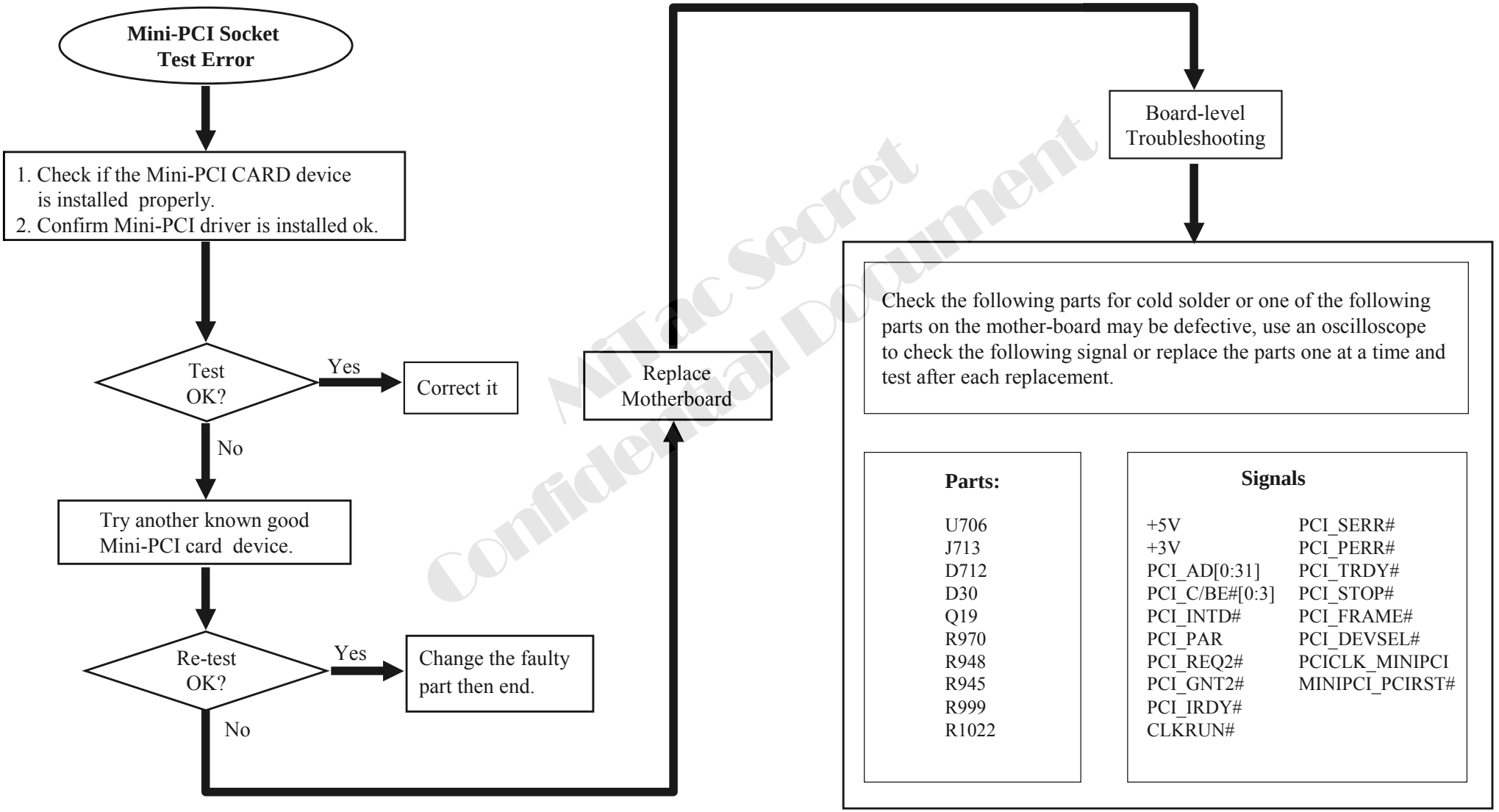
8.10 PC-Card Socket Test Error (2)

An error occurs when a PC card device is installed.



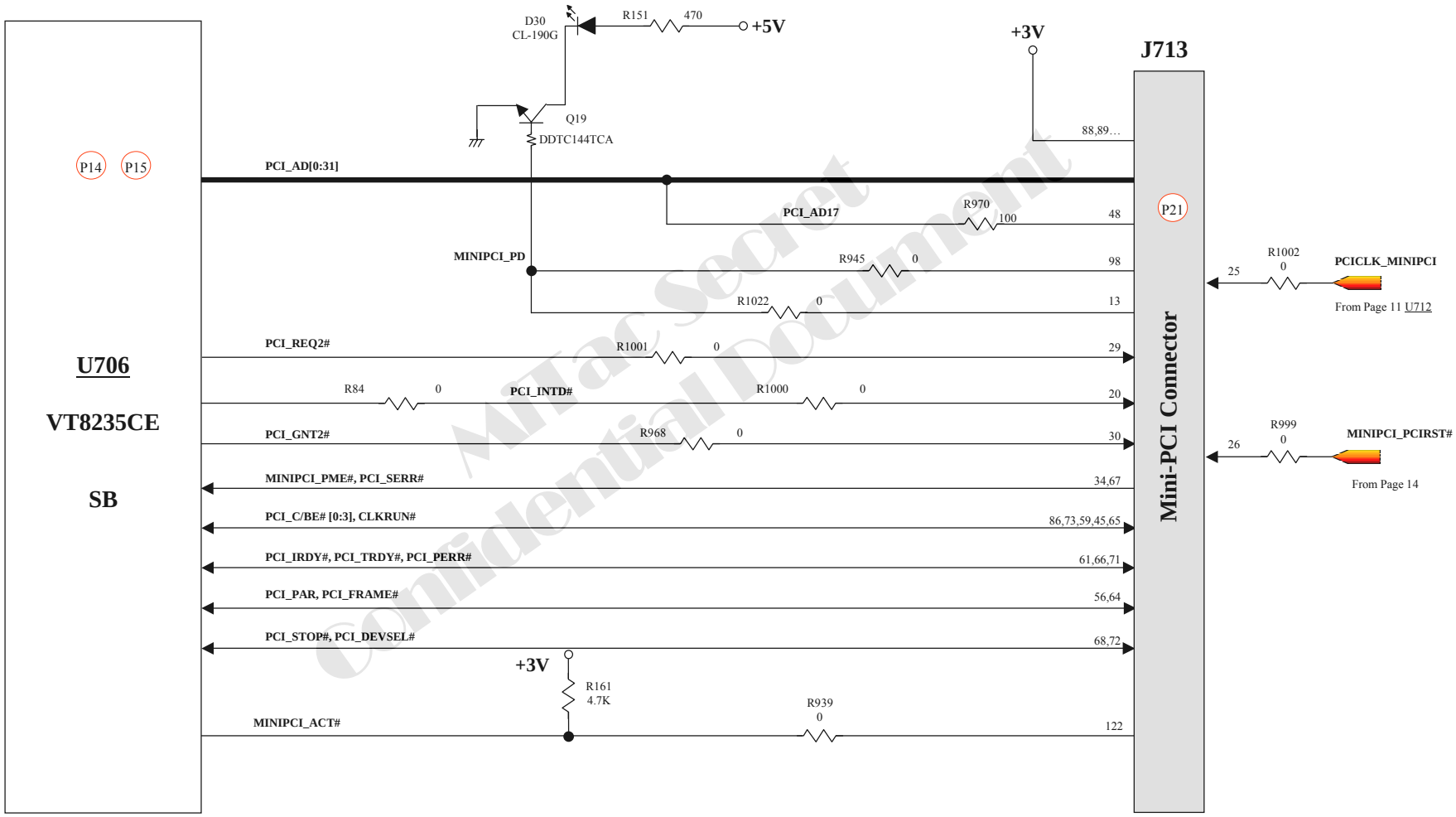
8.11 Mini-PCI Socket Test Error (1)

An error occurs when a Mini-PCI card device is installed.



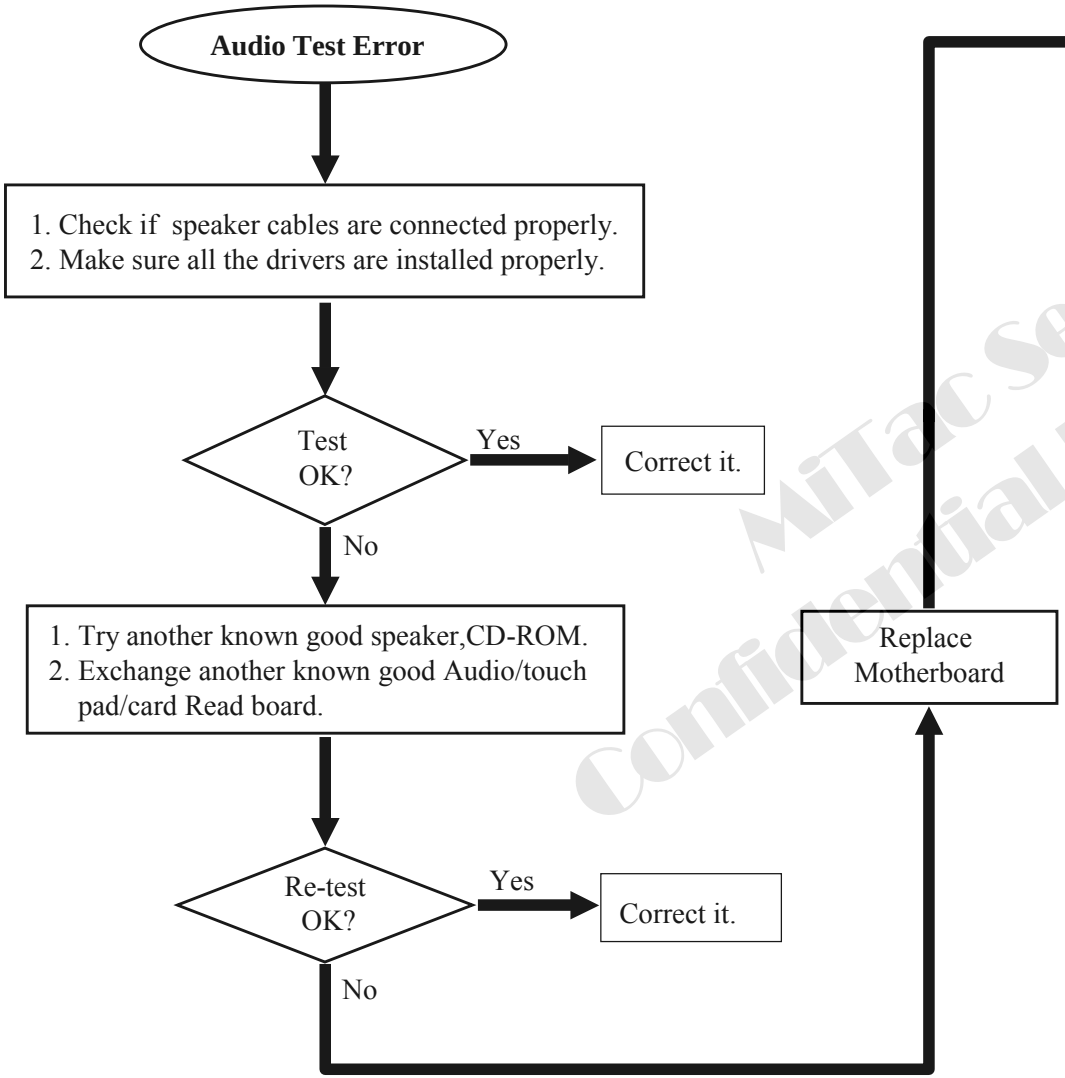
8.11 Mini-PCI Socket Test Error (2)

An error occurs when a Mini-PCI card device is installed.



8.12 Audio Test Error (1)

No sound from speaker after audio driver is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

Parts:

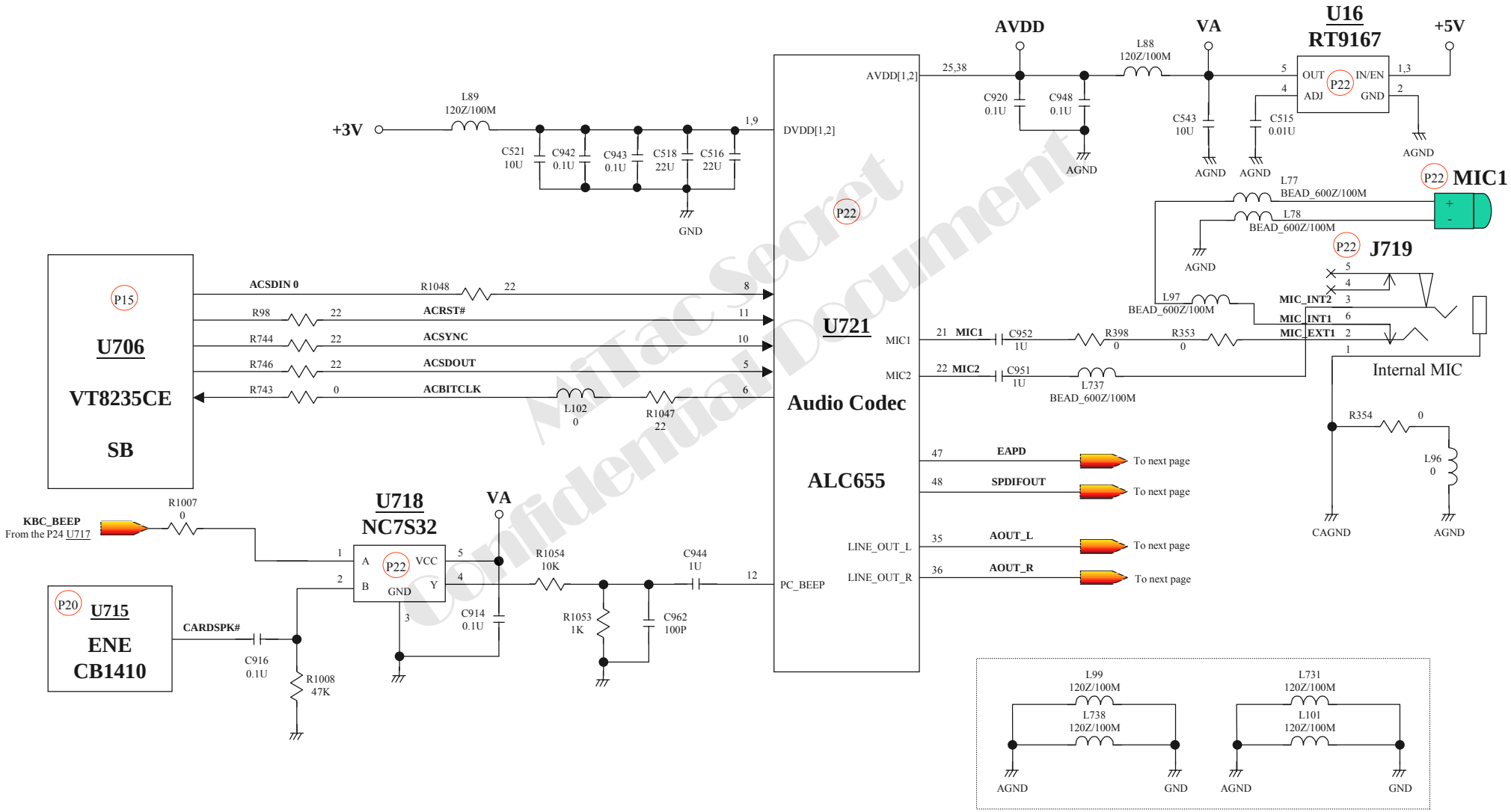
U706	D21
U16	J7
U715	J2
J719	J717
U721	L86
U718	L90~92
L96	MIC1
L77	U15
L78	Q28
L88	Q35
Q39	L19~L20
Q40	R330

Signals

+5V	AMPVDD
VA	DEVICE_DECT#
AVDD[1,2]	SPK_OFF#
DVDD[1,2]	DECT_HP#OPT
AOUT_R	SPDIFOUT
AOUT_L	MIC_INT1
ACRST#	MIC_INT2
ACSDOUT	ACBITCLK
ACSDIN0	PC_BEEP
ACSYNC	

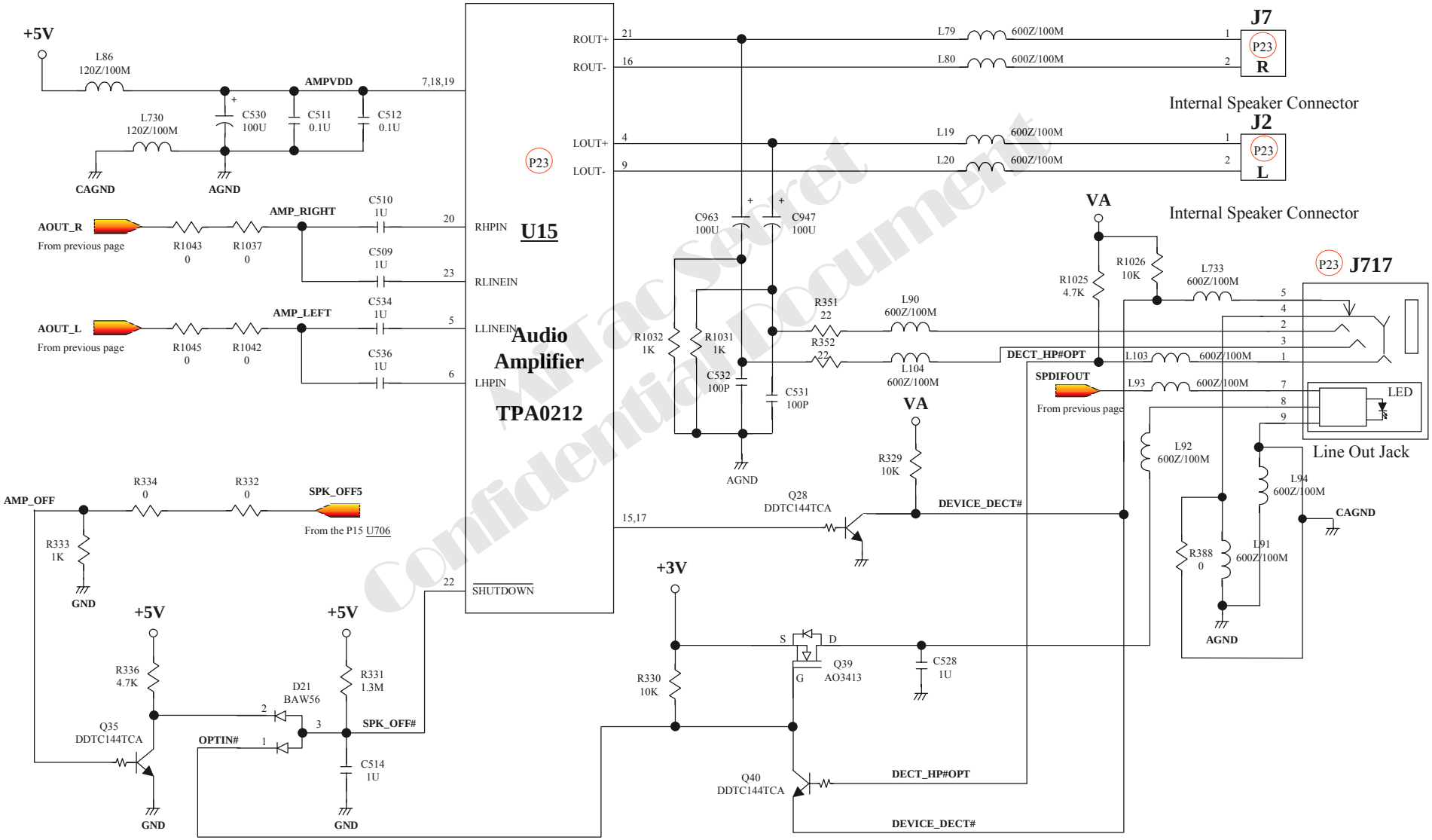
8.12 Audio Test Error (2) – Audio IN

No sound from speaker after audio driver is installed.



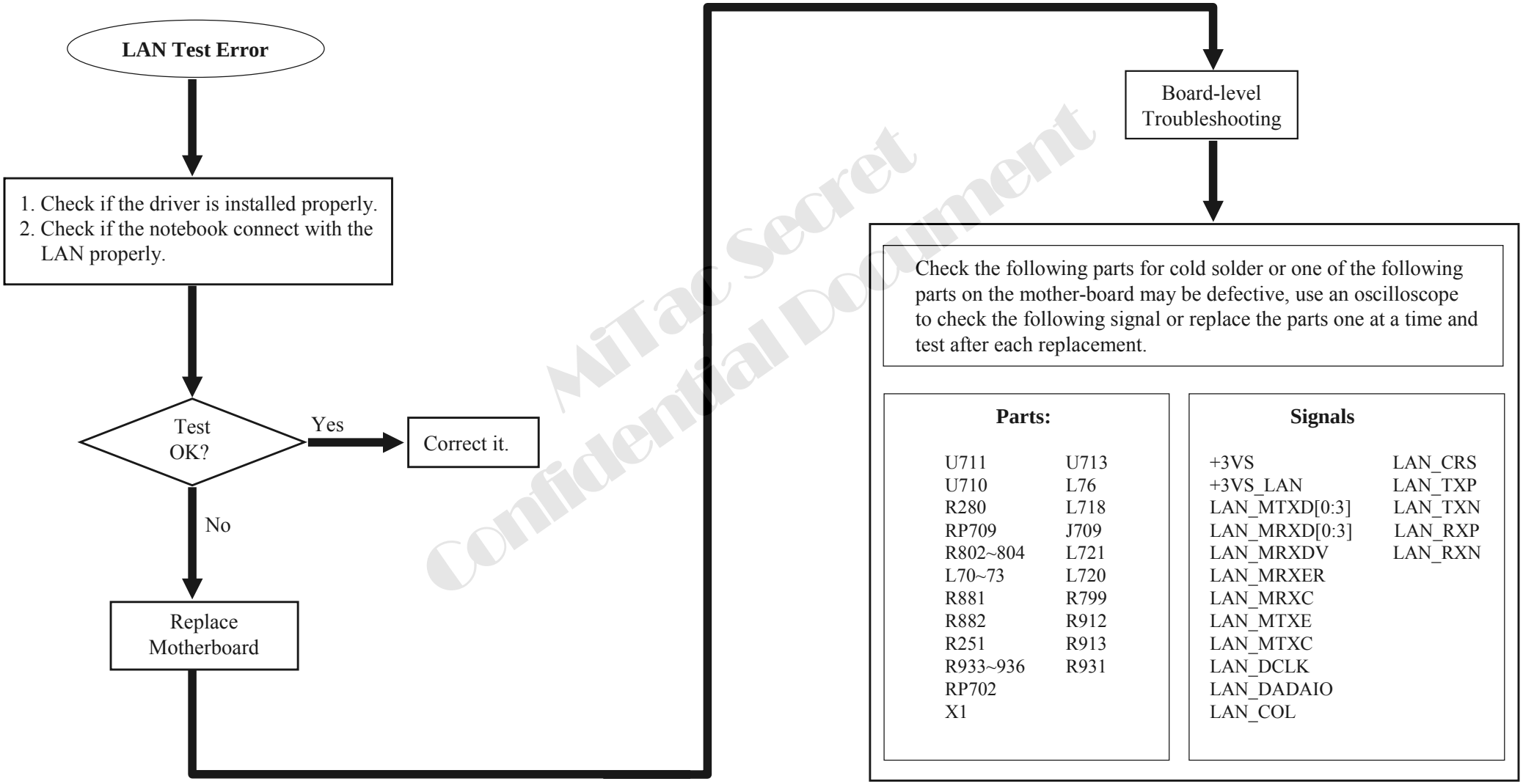
8.12 Audio Test Error (3) – Audio OUT

No sound from speaker after audio driver is installed.



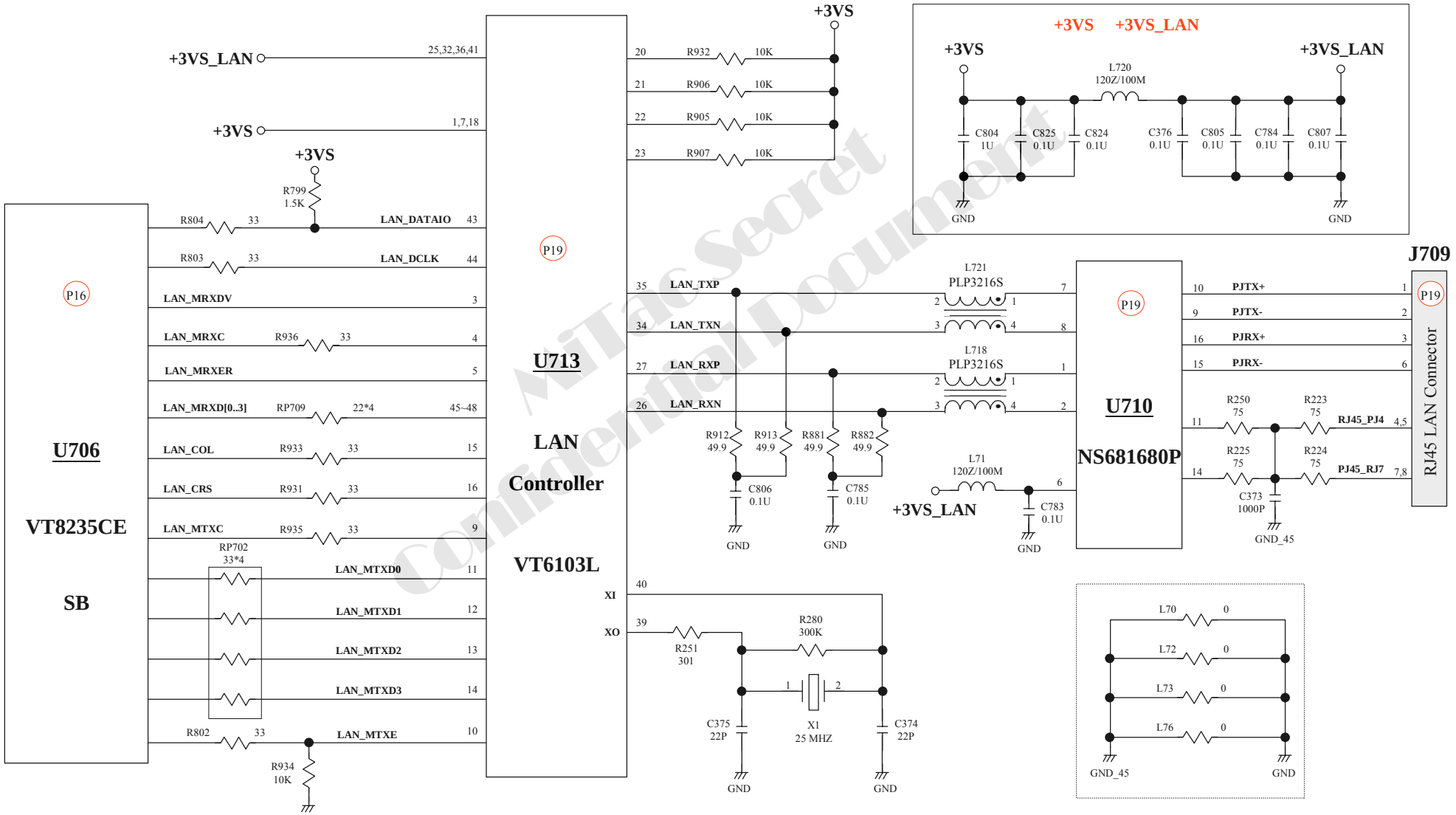
8.13 LAN Test Error (1)

An error occurs when a LAN device is installed.



8.13 LAN Test Error (2)

An error occurs when a LAN device is installed.



9. Spare Part List - 1

Part Number	Description	Location(S)
526280280003	LTXXNON;8650 ID1/W5A6/0E40H/1XUI	
416280280003	TF041-LT PF;CLAA154WA05,8650 ID1	
340802800012	TF041-HOUSING ASSY;LCD,8650	
340802800010	TF041-COVER ASSY;LCD,8650	
342803300002	TF041-HINGE;R,ZEUSTF041-HINGE;R,ZEUS	
342803300003	TF041-HINGE;L,ZEUSTF041-HINGE;L,ZEUS	
422802800007	TF041-WIRE ASSY;LCD,8650	
346803300008	TF041-INSULATOR;INVERTER LCD,ZEU	
422802800004	TF041-WIRE ASSY;INVERTER,COMAX,8	
421803300003	TF041-ANTENNA ;LCD,ZEUS	
371102010263	TF041-SCREW;M2L2.5,K-HD(+1),D4.0	
370102010415	TF041-SPC-SCREW;M2L4,K-HD(t0.3),	
370102611602	TF041-SPC-SCREW;M2.6L16,K-HD,NIW	
370102610408	TF041-SPC-SCREW;M2.6L4,NIW,K-HD,	
346802800008	TF041-CONDUCTIVE-TYPE;LCD,8650	
346802800016	TF041-MYLAR;COVER,LCD,8650	
242664800093	TF041-LABEL;CAUTION,INVERT BD,PI	
345802800008	TF041-INSULATOR;LENS,LCD,8650	
413000021142	TFT LCD;CLAA154WA05,15.4"WXGA,CP	
412681300004	TF041-PCB ASSY;D/A BD,DA-1A08-A1	
225680920001	TF041-TAPE;3M,1350F,W6,YELLOW,66	
346680900029	TF041-THERMAL PAD;L17*W10,T=0.5M	
346680900030	TF041-INSULATOR;L16W8.5T0.05MM,D	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/CU0.	
411681300014	TF041-PWA;PWA-INVERTER BD,SMT,DA	

Part Number	Description	Location(S)
271071102313	TF041-TH-RES;1K ,1/16W,5% ,060	R11
271071103310	TF041-TH-RES;10K ,1/16W,5% ,060	R2
271071122105	TF041-TH-RES;1.2K ,1/16W,1% ,060	R14B
271071151107	TF041-TH-RES;150 ,1/16W,1% ,060	R14A
271071152305	TF041-TH-RES;1.5K ,1/16W,5% ,060	R17
271071202305	TF041-TH-RES;2K ,1/16W,5% ,0603,	R12
271071304103	TF041-TH-RES;301K ,1/16W,1% ,060	R13,R3
271071331306	TF041-TH-RES;330 ,1/16W,5% ,060	R16,R21,R22
271071470103	TF041-TH-RES;4.32K,1/16W,1% ,060	R10
271072433101	TF041-TH-RES;43.2K,1/10W,1% ,060	R1
271072474102	TF041-TH-RES;470K ,1/10W,1% ,060	R5
272010560303	TF041-TH-CAP;56P,2KV,5%,1206,NPO	C18
272012016401	TF041-TH-CAP;1U,CR,16V,10%,1206,	C14A,C14B
272023475402	TF041-TH-CAP;4.7U ,25V ,10%,1210	C1
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10%,0	C17
272072823404	TF041-TH-CAP;.082U ,16V ,10%,060	C16
272075103415	TF041-TH-CAP;0.01U ,50V,10%,060	C13,C8
272075472703	TF041-TH-CAP;4700P,50V ,+ -20%,0	C15A
272990100302	TF041-TH-CAP;10P,3000V,+- 5%,NPO	C19
273001050217	TF041-TH-XFMR;CI8.5,25T/2150T,29	T1
291000020229	TF041-TH-CON;HDR,MA,2P*1,3.5MM,R	J2
291000021109	TF041-TH-CON;HDR,MA,11P*1,ACES,8	CN1
294011200511	TF041-TH-LED;RE/GR,H0.8,L1.9,W1.	LED1
294011200512	TF041-TH-LED;GREEN,19-21VGC/TR8,	LED4,LED5PAGE: 2
361200003064	TF041-SOLDER PASTE;SN96.5/AG3.0/	

9. Spare Part List - 2

Part Number	Description	Location(S)
271071104310	TF041-TH-RES;100K ,1/16W,5% ,060	R7
271071152305	TF041-TH-RES;1.5K ,1/16W,5% ,060	R19
271071331306	TF041-TH-RES;330 ,1/16W,5% ,060	R18,R20,R23
271071563102	TF041-TH-RES;56K ,1/16W,1% ,060	R6
271071753302	TF041-TH-RES;75K ,1/16W,5% ,060	R8
271072474102	TF041-TH-RES;470K ,1/10W,1% ,060	R4
272071105411	TF041-TH-CAP;1U ,10V ,10%,0603,X	C10,C4
272071334404	TF041-TH-CAP;0.33U ,10V ,10%,060	C2
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10%,0	C12,C6
272073104712	TF041-TH-CAP;0.1U,25V,10%,0603,X	C22,C7
272073223408	TF041-TH-CAP;0.022U,CR,25V ,10%,	C9
272075101408	TF041-TH-CAP;100P ,50V ,10%,0603	C20,C21
272075103415	TF041-TH-CAP;0.01U ,50V,10%,060	C11,C3
272075222407	TF041-TH-CAP;2200P,50V ,10%,0603	C5
281101015002	TF041-TH-IC;MP1015EM-Z-LF,CCFL C	U1
294011200511	TF041-TH-LED;RE/GR,H0.8,L1.9,W1.	LED2
294011200512	TF041-TH-LED;GREEN,19-21VGC/TR8,	LED3,LED6
295000010218	TF041-TH-FUSE;FAST,2A,63VDC,1206	F1
316686300003	TF041-PCB;PWA-INVERTER BD (DA-1A	R0A
242683200024	TF041-LABEL;5*20,BLANK,COMMON	
422802800006	TF041-CABLE;FFC,TP,8650	
340803300008	TF041-SPEAKER ASSY;L,ZEUS	
340803300009	TF041-SPEAKER ASSY;R,ZEUS	
340802800017	TF041-COVER ASSY;DDR,8650	
340802800018	TF041-HOUSING ASSY;8650	

Part Number	Description	Location(S)
340802800008	TF041-BRACKET ASSY;SYSTEM,8650	
340803300011	TF041-BRACKET ASSY;TP,ZEUS	
340802800009	TF041-COVER ASSY;HDD,8650	
341800200006	TF041-SPC SCREW;#4-1/4,POLARIS	
344802800017	TF041-COVER;REAR,R,8650	
344802800016	TF041-COVER;REAR,L,8650	
344802800015	TF041-COVER;HINGE,R,8650	
344802800010	TF041-COVER;CPU,8650TF041-COVER;CPU,8650	
340802800019	TF041-COVER ASSY;8650TF041-COVER ASSY;8650	
344802800003	TF041-DUMMY CARD;PCMCIA,8650	
344802800014	TF041-COVER;HINGE,L,8650	
370102010314	TF041-SPC-SCREW;M2L3,K-HD(+1),NI	
370102010415	TF041-SPC-SCREW;M2L4,K-HD(t0.3),	
370102030304	TF041-SPC-SCREW;M2L3,K-HD(+1)D3.	
370102610408	TF041-SPC-SCREW;M2.6L4,NIW,K-HD,	
370102611602	TF041-SPC-SCREW;M2.6L16,K-HD,NIW	
371102010263	TF041-SCREW;M2L2.5,K-HD(+1),D4.0	
422802800005	TF041-WIRE ASSY;MDC,8650	
340802800011	TF041-COVER ASSY;MINIPCI,8650	
340802800016	TF041-SHIELDING ASSY;COVER,8650	
345802800009	TF041-SPONGE;HEATSINK,SIDE,CPU,8	
370102631204	TF041-SPC-SCREW;M2.6L6,K-HD,NIW/	
411802800018	TF041-PWA;PWA-8650,MOTHER BD	PAGE: 3
411802800020	TF041-PWA;PWA-8650,MOTHER BD,SMT	
271002000312	TF041-TH-RES;0 ,1/10W,5% ,080	L101,L731,L736,L738

9. Spare Part List - 3

Part Number	Description	Location(S)
271002102312	TF041-TH-RES;1K ,1/10W,5% ,080	R38,R49
271002472304	TF041-TH-RES;4.7K ,1/10W,5% ,080	PR704,PR705
271012000308	TF041-TH-RES;0 ,1/8W,5% ,1206	PR753
271013221302	TF041-TH-RES;220 ,1/4W,5% ,1206	PR709,PR710,PR771
271045087104	TF041-TH-RES;.008 ,1W ,1% ,2512,	PR715
271045107104	TF041-TH-RES;.01 ,1W ,1% ,2512	PR701
271045127103	TF041-TH-RES;.012,1W,1%,2512,SMT	PR738
271046029102	TF041-TH-RES;.02 ,2W,1%,2512,SMT	PR721
271061000003	TF041-TH-RES;0 ,1/16W,0402,SM	PR10,PR11,PR12,PR13
271061100312	TF041-TH-RES;10 ,1/16W,5% ,040	R895
271061101109	TF041-TH-RES;100 ,1/16W,1% ,040	R214,R216,R244,R970
271061102113	TF041-TH-RES;1K ,1/16W,1% ,040	R207,R733,R737
271061102310	TF041-TH-RES;1K ,1/16W,5% ,040	R1031,R1032,R1053,R7
271061103307	TF041-TH-RES;10K ,1/16W,5% ,040	R1004,R1005,R102,R126
271061104108	TF041-TH-RES;100K ,1/16W,1% ,040	PR826,PR833
271061104306	TF041-TH-RES;100K ,1/16W,5% ,040	R1012,R355,R357,R46
271061105307	TF041-TH-RES;1M ,1/16W,5% ,040	R1015,R32,R66
271061106308	TF041-TH-RES;10M ,1/16W,5% ,040	R784
271061135102	TF041-TH-RES;1.3M,1/16W,1%,0402,	R331
271061151110	TF041-TH-RES;150 ,1/16W, 1%,040	R231
271061152502	TF041-TH-RES;1.5K ,1/16W,5% ,040	R799,R835
271061153110	TF041-TH-RES;15K ,1/16W,1% ,040	R136,R137,R61,R805
271061184304	TF041-TH-RES;180K ,1/16W, 5%,04	R65
271061201107	TF041-TH-RES;200 ,1/16W, 1%,040	R209,R211,R228,R234
271061203112	TF041-TH-RES;20K ,1/16W,1% ,040	R791

Part Number	Description	Location(S)
271061220308	TF041-TH-RES;22 ,1/16W,5% ,040	R1047,R1048,R189,R10
271061221318	TF041-TH-RES;220 ,1/16W, 5%,040	R378,R383,R385
271061222308	TF041-TH-RES;2.2K ,1/16W,5% ,040	R101,R711,R748,R750
271061223105	TF041-TH-RES;22K,1/16W,1% ,0402,	R1027,R1029
271061244101	TF041-TH-RES;249K,1/16W,1%,0402,	PR832
271061270104	TF041-TH-RES;27.4 ,1/16W, 1%,04	R187,R212,R253
271061272105	TF041-TH-RES;2.7K ,1/16W,1% ,040	PAGE: 5R163,R171,R172
271061273308	TF041-TH-RES;27K,1/16W,5%,0402,S	R769,R794
271061301121	TF041-TH-RES;301,1/16W,1%,0402,S	R251
271061302104	TF041-TH-RES;3K,1/16W,1%,0402,SM	R208
271061330311	TF041-TH-RES;33 ,1/16W,5% ,040	R122,R205,R346,R349
271061332317	TF041-TH-RES;3.3K ,1/16W,5% ,040	R165
271061333304	TF041-TH-RES;33K ,1/16W,5% ,0402	R22,R40,R706
271061361104	TF041-TH-RES;360 ,1/16W,1% ,040	R159,R206
271061390309	TF041-TH-RES;39, 1/16W, 5%,0402	R230
271061471308	TF041-TH-RES;470 ,1/16W,5% ,040	R151,R315,R371,R375
271061472104	TF041-TH-RES;4.7K ,1/16W,1% ,040	R158
271061472312	TF041-TH-RES;4.7K ,1/16W,5% ,040	R100,R1025,R106,R11
271061473502	TF041-TH-RES;47K ,1/16W,5% ,040	R1006,R1008,R23,R39
271061474304	TF041-TH-RES;470K ,1/16W,5% ,040	R5
271061490102	TF041-TH-RES;49.9 ,1/16W,1% ,040	R213,R217,R218,R856
271061510306	TF041-TH-RES;51, 1/16W, 5%,0402	R237,R262,R266,R28
271061540102	TF041-TH-RES;54.9 ,1/16W,1% ,040	R186,R239,R252
271061562107	TF041-TH-RES;5.6K ,1/16W, 1%,04	R198,R249,R326,R83
271061563103	TF041-TH-RES;56K,1/16W,1%,0402,S	R56

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Part Number	Description	Location(S)
271061608101	TF041-TH-RES;60.4,1/16W,1%,0402,	R202,R832
271061642102	TF041-TH-RES;6.49K,1/16W,1% ,040	R909
271061681308	TF041-TH-RES;680 ,1/16W,5% ,040	R232
271061682304	TF041-TH-RES;6.8K ,1/16W,5% ,04	R1055,R1078,R399,R4
271061750105	TF041-TH-RES;75,1/16W,1%,0402,SM	R12,R13,R14,R223,R24
271061800101	TF041-TH-RES;80.6,1/16W,1%,0402,	R193
271061822307	TF041-TH-RES;8.2K ,1/16W,5% ,040	R768,R793,R848
271071000312	TF041-TH-RES;0 ,1/16W,5% ,060	L102,L70,L72,L73,L70
271071100103	TF041-TH-RES;10 ,1/16W,1% ,060	PR1
271071100312	TF041-TH-RES;10 ,1/16W,5% ,060	PR5,PR727,PR816
271071101107	TF041-TH-RES;100 ,1/16W,1% ,060	R175
271071102107	TF041-TH-RES;1K ,1/16W,1% ,060	PR724,PR732,PR765
271071103108	TF041-TH-RES;10K ,1/16W,1% ,060	PR722,PR783,PR820
271071103310	TF041-TH-RES;10K ,1/16W,5% ,060	PR815
271071104108	TF041-TH-RES;100K ,1/16W,1% ,060	PR703,PR713,PR720
271071104110	TF041-TH-RES;107K ,1/16W,1% ,060	PR733
271071105312	TF041-TH-RES;1M ,1/16W,5% ,060	PR2,PR760,PR768,PR73
271071113114	TF041-TH-RES;11K ,1/16W,1% ,060	PR823
271071122105	TF041-TH-RES;1.2K ,1/16W,1% ,060	PR729
271071124117	TF041-TH-RES;124K ,1/16W,1% ,060	PR782
271071133114	TF041-TH-RES;13.7K,1/16W,.1%,060	PR745
271071151107	TF041-TH-RES;150 ,1/16W,1% ,060	R245,R246,R294,R312
271071151309	TF041-TH-RES;150 ,1/16W,5% ,060	R240,R241,R242,R243
271071182216	TF041-TH-RES;18.2K,1/16W,1%,0603	PR786
271071196213	TF041-TH-RES;19.6K,1/16W,1% ,060	PR734

Part Number	Description	Location(S)
271071203106	TF041-TH-RES;20K ,1/16W,1% ,060	PR708,PR716,PR770
271071203107	TF041-TH-RES;20K ,1/16W,.1%,060	PR744
271071204104	TF041-TH-RES;200K ,1/16W,1% ,060	PR730,PR763,PR764
271071221105	TF041-TH-RES;220,1/16W,1% ,0603,	R839
271071221312	TF041-TH-RES;220 ,1/16W,5% ,060	R258PAGE: 7
271071224102	TF041-TH-RES;226K ,1/16W,1% ,060	PR739
271071228306	TF041-TH-RES;2.2 ,1/16W,5% ,060	PR735,PR736,PR754
271071237212	TF041-TH-RES;23.7K,1/16W,1% ,060	PR834
271071242104	TF041-TH-RES;2.49K,1/16W,1% ,060	PR781
271071264101	TF041-TH-RES;267K ,1/16W,1% ,06	PR836
271071270102	TF041-TH-RES;27.4 ,1/16W,1% ,060	R215
271071333102	TF041-TH-RES;33K ,1/16W,1% ,060	PR741
271071357113	TF041-TH-RES;3.57K,1/16W,1% ,060	PR718
271071413101	TF041-TH-RES;41.2K,1/16W,1% ,060	PR818
271071433303	TF041-TH-RES;43K ,1/16W,5% ,060	R974
271071453212	TF041-TH-RES;45.3K,1/16W,1% ,060	PR756
271071471105	TF041-TH-RES;475 ,1/16W,1% ,040	R923
271071471308	TF041-TH-RES;470 ,1/16W,5% ,060	PR769,PR807
271071472309	TF041-TH-RES;4.7K ,1/16W,5% ,060	PR750,PR751,R396
271071478102	TF041-TH-RES;4.7,1/16W,1%,0603,S	PR792,PR806
271071490101	TF041-TH-RES;49.9 ,1/16W,1% ,060	R174
271071492102	TF041-TH-RES;4.99K,1/16W,1% ,060	PR707
271071494101	TF041-TH-RES;499K ,1/16W,1% ,060	PR719
271071549213	TF041-TH-RES;54.9K,1/16W,1% ,060	PR757
271071612101	TF041-TH-RES;6.19K,1/16W,1% ,060	PR780

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Part Number	Description	Location(S)
271071634212	TF041-TH-RES;63.4K,1/16W,1% ,060	PR737
271071642101	TF041-TH-RES;6.49K,1/16W,1% ,060	PR803
271071661101	TF041-TH-RES;665 ,1/16W,1% ,060	R182
271071681103	TF041-TH-RES;680 ,1/16W,1% ,060	PR726
271071752105	TF041-TH-RES;7.5K,1/16W,1%,0603,	PR749
271071753302	TF041-TH-RES;75K ,1/16W,5% ,060	PR755
271071754102	TF041-TH-RES;750K,1/16W,1% ,0603	PR776
271072124104	TF041-TH-RES;121K ,1/10W,1% ,060	PR758
271072142102	TF041-TH-RES;1.4K,1/10W,1% ,0603	PR791,PR797
271072263101	TF041-TH-RES;26.7K,1/10W,1% ,060	PR788
271072300331	TF041-TH-RES;300K ,1/10W,5% ,060	R280
271072372101	TF041-TH-RES;37.4K ,1/10W,1% ,06	PR802
271072394102	TF041-TH-RES;392K ,1/10W,1% ,060	PR743
271072474102	TF041-TH-RES;470K ,1/10W,1% ,060	PR702
271072562104	TF041-TH-RES;5.6K ,1/10W,1% ,060	R840
271571100303	TF041-TH-RP;10*8 ,16P ,1/16W,5%	RP19,RP20,RP21
271571220302	TF041-TH-RP;22*8 ,16P ,1/16W,5%	RP5,RP704
271571330303	TF041-TH-RP;33*8 ,16P ,1/16W,5%	RP3,RP32,RP33,RP34
271591220304	TF041-TH-RP;22*4,8P,1/16W,5%,080	RP10,RP11,RP12,RP13
271591330310	TF041-TH-RP;33*4,8P,1/16W,5%,080	RP30,RP31,RP4,RP6
271611103305	TF041-TH-RP;10K*4 ,8P ,1/16W,5%	RP8PAGE: 8
271611153304	TF041-TH-RP;15K*4 ,8P ,1/16W,5%	RP1,RP2
271611220305	TF041-TH-RP;22*4 ,8P ,1/16W,5%	RP703,RP709
271611330305	TF041-TH-RP;33*4 ,8P ,1/16W,5%	RP702,RP710
271621103306	TF041-TH-RP;10K*8 ,10P,1/32W,5%	RP45

Part Number	Description	Location(S)
271621222101	TF041-TH-RP;2.2K*8,10P,1/16W,5%,	RP701
271621472306	TF041-TH-RP;4.7K*8,10P,1/32W,5%	RP44
272001105410	TF041-TH-CAP;1U ,10%,10V ,0805	PC3,PC780,PC801
272001106404	TF041-TH-CAP;10U,6.3V ,10%,0805,	PC722,PC800,PC838
272001106514	TF041-TH-CAP;10U,6.3V,+- 20%,080	C115,C117,C119,C159
272001106709	TF041-TH-CAP;10U,10V,+80-20%,080	C104,C111,C123,C129
272001475704	TF041-TH-CAP;4.7U ,CR,10V ,+80-2	C335,C353,C432,C433
272002225705	TF041-TH-CAP;2.2U ,CR,16V ,+80-2	C164,C33,C852
272003105708	TF041-TH-CAP;1U ,CR,25V ,+80%-	PC1,PC741
272005105402	TF041-TH-CAP;0.1U,CR,50V,10%,X7R	PC750,PC754,PC769
272011226509	TF041-TH-CAP;22U,6.3V,+-20%,1206	C368
272013106504	TF041-TH-CAP;10U,25V,+/-20%,1206	PC732,PC760,PC761
272013475403	TF041-TH-CAP;4.7U ,25V ,10%,1206	PC719,PC725,PC726
272030102411	TF041-TH-CAP;1000P,2KV,10%,1808,	C204,C205,C373
272071225406	TF041-TH-CAP;2.2U ,CR,6.3V ,10%,	C175,C379,C383,C435
272071475403	TF041-TH-CAP;4.7U,6.3V,10%,0603,	C127,C132,C137,C58,70
272072105403	TF041-TH-CAP;0.1U ,CR,16V,10%,0	PC708,PC724,PC756
272072153405	TF041-TH-CAP;0.015U ,CR,16V,10%,	PC743
272075101313	TF041-TH-CAP;100P ,CR,50V,5%,060	PC831
272075101411	TF041-TH-CAP;560P ,CR,50V ,10%,0	PC771
272075102419	TF041-TH-CAP;1000P,CR,50V,10%,06	PC6,PC702,PC705,PC72
272075103414	TF041-TH-CAP;0.01U ,CR,50V ,10%,	PC2,PC4,PC5,PC701
272075104710	TF041-TH-CAP;0.1U ,50V,+80-20%,	PC713,PC730,PC736
272075120306	TF041-TH-CAP;12P ,CR,50V ,5% ,0	C744,C745
272075152405	TF041-TH-CAP;1500P,CR,50V,10%,06	PC716,PC772

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Part Number	Description	Location(S)
272075181308	TF041-TH-CAP;180P ,50V ,5% ,0603	PC773,PC775
272075470315	TF041-TH-CAP;47P ,CR,50V ,5%,060	PC752,PC774
272075472703	TF041-TH-CAP;4700P,50V ,+ -20%,0	PC749
272075562404	TF041-TH-CAP;5600P,CR,50V ,10%,0	PC755
272075680307	TF041-TH-CAP;68P ,50V ,5% ,0603	C417
272101015402	TF041-TH-CAP;1U,6.3V,+-10%,0402,	C146,C147,C151,C153
272101104415	TF041-TH-CAP;0.1U ,CR,10V,10%,0	C124,C161,C36,C388
272101105705	TF041-TH-CAP;1U ,CR,6.3V ,80-2	C11,C135,C167,C192
272101224702	TF041-TH-CAP;0.22U ,10V ,+80-20%	C13,C954
272101473407	TF041-TH-CAP;0.047U,10V,10%,0402	C43,C747
272102104708	TF041-TH-CAP;0.1U ,16V,+80-20%,	C102,C103,C106,C108
272103103407	TF041-TH-CAP;0.01U ,CR,25V ,10%,	C100,C101,C105,C107
272103330403	TF041-TH-CAP;33P ,25V ,+/-10%,0	C369,C370,C371,C390
272105100307	TF041-TH-CAP;10P ,CR,50V ,5%,04	C1,C3,C4,C5,C6,C7,C79
272105101404	TF041-TH-CAP;100P ,50V ,+ -10%,0	C182,C531,C532,C927
272105102421	TF041-TH-CAP;1000P,CR,50V,10%,04	C178,C179,C184,C185
272105102503	TF041-TH-CAP;1000P,50V ,+/-20%,0	C12,C18,C189,C191,C94
272105120310	TF041-TH-CAP;12P ,CR,50V ,5% ,0	C557,C558,C559,C56
272105220404	TF041-TH-CAP;22P ,50V ,+ -10%,0	C171,C211,C212,C286
272105221410	TF041-TH-CAP;220P ,CR,50V ,10%,0	C169,C170
272105222503	TF041-TH-CAP;2200P,50V ,+/-20%,0	C546,C766,C796
272105270305	TF041-TH-CAP;27P ,50V ,5%,0402,	C423,C431,C437,C55
272105470403	TF041-TH-CAP;47P ,50V ,+ -10%,0	C141,C142,C143,C14
272105471408	TF041-TH-CAP;470P ,50V,10%,0402,	C701,C9
272430227501	TF041-TH-CAP;220uF,2V,±20%,15mo	PC807,PC810,PC839

Part Number	Description	Location(S)
272431227006	TF041-TH-CAP;220uF,4V,7343,25moh	PC820,PC830
272431337102	TF041-TH-CAP;330U,2V,-35/+10%,H1	C765,PC805,PC813,PC18
272601107521	TF041-TH-EC;100U,6.3V,+-20%,9.3*	C530
272602107516	TF041-TH-EC;100U,16V,M,6.3*5.5,-	C704,C706,C712,C947
272603276502	TF041-TH-EC;27U,23V,+/-20%,H5.7,	PC768
273000136023	TF041-TH-FERRITE CHIP;47OHM/100M	L701,L702,L703
273000500184	TF041-TH-FERRITE CHIP;600OHM/100	L103,L104,L19,L20,L27
273000500185	TF041-TH-FERRITE CHIP;130OHM/100	L13,L14,L22,L23,L71
273000500189	TF041-TH-CHOKE COIL;90OHM/100MHZ	L35,L6,L9
273000500232	TF041-TH-CHOKE COIL;SPC-10039P-4	PL716,PL717
273000500233	TF041-TH-CHOKE COIL;SPC-10039P-3	PL711
273000500267	TF041-TH-CHOKE COIL;400uH MIN,12	L715
273000500288	TF041-TH-CHOCK COIL; 3.0UH,29mOH	PL710PAGE: 13
273000501272	TF041-TH-CHOCK COIL; 3.0UH,14mOH	PL719
273000501273	TF041-TH-CHOCK COIL; 0.68UH,1.7m	PL713
273000610037	TF041-TH,FERRITE CHIP;120OHM/100	PL1,PL2,PL701,PL705
273000610041	TF041-TH,FERRITE CHIP;120OHM/100	L15,L17,L21,L24,L31
273000610048	TF041-TH,FERRITE ARRAY;120OHM/10	FA1
273000990289	TF041-TH-INDUCTOR;10UH,30%,SPC-1	PL702,PL704
273001050272	TF041-TH-TRANSFORMER;10/100 BASE	U710
274011431454	TF041-TH-XTAL;14.318MHZ,32PF,50P	X703
274013275401	TF041-TH-XTAL;32.768KHZ,20PPM,12	X702
274018000304	TF041-TH-XTAL;8Mhz,30PPM,16PF,8*	X705
281307076001	TF041-TH-IC;NC7WZ07P6X,D-BUFFER,	U13
281307085005	TF041-TH-IC;NC7SZ08P5,2-INPUT &	U704,U705

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Part Number	Description	Location(S)
282574014007	TF041-TH-IC;74AHC14,HEX INVERTER	U8
282574132012	TF041-TH-IC;74AHCT1G32,SINGLE OR	U718
283468470002	TF041-TH-IC;EEPROM,M93C46-WMN6T,	U707
284500655005	TF041-TH-IC;ALC655,AUDIO CODEC,L	U721
284500800004	TF041-TH-IC;PN800G CD,NORTH BRID	U711
284501634003	TF041-TH-IC;VT1634AL,LVDS TRANS	U703
284506103012	TF041-TH-IC;VT6103GL,LAN-PHY,LQF	U713
284507460004	TF041-TH-IC;ADT7460,TEMPERATURE	U708
284508235010	TF041-TH-IC;VT8235GCE,SOUTH BRID	U706
284595090205	TF041-TH-IC;ICS950902DFLF,CLOCK	U712
286100212002	TF041-TH-IC;TPA0212,AMPLIFIER,TS	U15
286100393013	TF041-TH-IC;LMV393,DUAL COMPARTO	PU706
286104173002	TF041-TH-IC;MAX4173F,I-SENSE AMP	PU1
286300594004	TF041-TH-IC;TL594C,PWM CONTROL,S	PU707
286301410005	TF041-TH-IC;CB1410FB0,PCI/CARDBU	U715
286301470002	TF041-TH-IC;SC1470,PWM CTRL,TSSO	PU716
286302211010	TF041-TH-IC;CP2211,POWER DISTRI	U714
286302996002	TF041-TH-IC;G2996P1U,DDR,GMT,SOP	PU717
286303107003	TF041-TH-IC;AMS3107C,3.3V,1%,VOL	U716
286303728003	TF041-TH-IC;LTC3728LXCUH,PWM CTR	PU705
286304315001	TF041-TH-IC;SC431LCSK-.5,.5%,ADJ	PQ716
286306227003	TF041-TH-IC;ISL6227CAZ, PWM CONT	PU711
286308800032	TF041-TH-IC;AME8800MEFTZ,0.3A,1.	U11
286308800033	TF041-TH-IC;AME8800,0.3A,1.5V,RE	U9
286369229003	TF041-TH-IC;G692L293Tf,RESET CIR	U17

Part Number	Description	Location(S)
286391674003	TF041-TH-IC;RT9167-47PB,LDO,SOT2	U16PAGE: 14
286406218001	TF041-TH-IC;ISL6218CVZ, PWM CONT	PU704
288100032014	TF041-TH-DIODE;BAS32L,VRRM75V,ME	D18,D19,D711,PD713
288100034012	TF041-TH-DIODE;SSA34,40V,3A,SMA	PD709,PD711,PD715
288100054034	TF041-TH-DIODE;BAT54,30V,200mA,S	D2,D3,D9
288100056022	TF041-TH-DIODE;BAW56,70V,215mA,S	D21,PD707,PD716
288100099018	TF041-TH-DIODE;BAV99,70V,450MA,S	D701,D704,D705,PD2
288100140012	TF041-TH-DIODE;SCS140PL,40V,1A,S	PD714
288100541004	TF041-TH-DIODE;BAT54ALT1,COM. AN	D710,D712,D8
288100701003	TF041-TH-DIODE;BAV70LT1,70V,225M	D13,D713,PD701,PD70
288101040012	TF041-TH-DIODE;PDS1040,10A SCHOT	PD704
288105520002	TF041-TH-DIODE;BZV55-C20,ZENER,5	PD708
288105524005	TF041-TH-DIODE;BZV55-C2V4,ZENER,	PD717
288105524006	TF041-TH-DIODE;BZV55-C24,ZENER,5	PD1
288200114014	TF041-TH-TRANS;DDTC114TCA-F,NPN,	Q11,Q12,Q705
288200144027	TF041-TH-TRANS;DDTC144WCA,NPN,SO	PQ704,Q728
288200144028	TF041-TH-TRANS;DDTC144TCA,NPN,SO	Q10,Q13,Q18,Q19,Q20
288200144044	TF041-TH-TRANS;DDTA144WCA-F,PNP,	PQ718
288200301017	TF041-TH-TRANS;FDV301N_NL,N-CHAN	Q2,Q27
288200436004	TF041-TH-TRANS;AOD436,N-MOS,85A,	PU708
288202222021	TF041-TH-TRANS;PMBT2222A,NPN,SOT	PQ710,Q707,Q708,Q71
288203413002	TF041-TH-TRANS;AO3413,P-MOSFET,S	Q14,Q17,Q39,Q717,Q72
288203414002	TF041-TH-IC;TRANS;AO3414,N-CHANN	Q3,Q5
288204407002	TF041-TH-TRANS;AO4407,P-MOS,.01O	PQ701,PQ707,PQ708
288204419002	TF041-TH-TRANS;AO4419,P-MOSFET,9	Q1,U6,U7

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Part Number	Description	Location(S)
288204422002	TF041-TH-TRANS;AO4422,24mOHM,N-M	PU701,PU715
288204702004	TF041-TH-TRANS;AO4702, N-MOSFET,	PU702,PU714
288204914002	TF041-TH-TRANS;AO4914,DUAL N-MOS	PU703,PU712,PU713
288227002024	TF041-TH-TRANS;2N7002LT1,N-CHANN	PQ2,PQ730,Q706,Q715
288227002025	TF041-TH-TRANS;2N7002LT1,N-CHANN	PQ1,PQ702,PQ703,PQ75
291000000618	TF041-TH-CON;STEREO JACK,6P,W9.5	J718,J719
291000000716	TF041-TH-CON;BATTERY,7P,MA,2.5MM	J704
291000003008	TF041-TH-CON;HDR,FM,15P*2,0.8MM.	J716
291000006803	TF041-TH-CON;IC CARD,68P,9291000	J9
291000010229	TF041-TH-CON;HDR,MA,2P*1,1.25MM,	J711
291000010318	TF041-TH-CON;HDR,MA,3P*1,1.25MM,	J707
291000011231	TF041-TH-CON;FPC/FFC,12P,88241-1	J5
291000012612	TF041-TL-CON;HDR,ACES,85202-2602	J6
291000013044	TF041-TH-CON;HDR,MA,15P*2,88107-	J3
291000020001	TF041-TH-CON;HDR,1.25MM,85204-04	J708
291000020227	TF041-TH-CON;HDR,MA,2P*1,1.25MM,	J2,J7
291000021109	TF041-TH-CON;HDR,MA,11P*1,ACES,8	J1
291000611262	TF041-TH-CON;MINIPCI SOCKET,R/A,	J713
291000614798	TF041-TH-IC SOCKET;UPGA479M,479P	U709
291000810003	TF041-TH-CON;PHONE JACK,2 IN 1,7	J709
294011200510	TF041-TH-LED;GREEN,H0.8,0603,CL-	D24,D26,D27,D28,D29
295000010207	TF041-TH-FUSE;FAST,3A,32V,1206,S	PF704
295000010209	TF041-TH-FUSE;1A,NORMAL,1206,SMT	F4
295000010213	TF041-TH-FUSE;0.14A/60V,POLY SWI	F3
295000010214	TF041-TH-FUSE;0.5A/15V,POLY SWIT	F1

Part Number	Description	Location(S)
295000010243	TF041-TH-FUSE;NANO,10A/125V,R451	PF703
295000010247	TF041-TH-FUSE;FAST,7A/24V,1206,S	PF701
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,	SW2,SW3,SW4
312374706131	TF041-TH-EC;470U,6.3V,20%,D8.0,L	PC709
331000008119	TF041-TH-CON;USB,4P*2,020122MR00	J701
331040044028	TF041-TH-CON;HDR,R/A,2.0MM,H04@1	J715
331040050033	TF041-TH-CON;HDR,BTB R/A,0.8MM,K	J710
331660020022	TF041-TH-CON;DIMM SOCKET;DDR SOD	J714
331660020023	TF041-TH-CON;DIMM SOCKET;DDR SOD	J712
331710015018	TF041-TH-CON;D,FM,15P,3ROW,SUYIN	J702
331840010019	TF041-TH-CON;STEREO JACK,10P,W/S	J717
342686000023	TF041-SMT SCREW;A40M20-50AS,HOOK	MTG701,MTG702
342687600009	TF041-TH,FINGER;EMI GROUNDING SM	TP4,TP42,TP43,TP46
481802800003	TF041-F/W ASSY;KBC,8650	U717
242600000561	TF041-LABEL;10*10,BLANK,COMMON	
284583950003	TF041-TH-IC;W83L950G-Ver.C,LPC_K	
361200003064	TF041-SOLDER PASTE;SN96.5/AG3.0/	
242600000632	TF041-LABEL;27*7MM,XF-5811;POLYI	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000001	LABEL;PAL,20*5MM,COMMON	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
272401227001	TF041-TH-CAP;220U,4V,EEFCX0G221Y	PC841
316802800002	TF041-TH-PCB;PWA-8650/M BD	R01

9. Spare Part List - 9

Part Number	Description	Location(S)
273000500182	TF041-TH-CHOKE COIL;120OHM/100MH	L718,L721
274012500452	TF041-TH-XTAL;25MHZ,20PF,30PPM,8	X1PAGE: 16
295000010271	TF041-TH-FUSE;1.1A/6V,POLY SWITC	F701,F702,F703
342687600011	TF041-TH,FINGER;EMI GROUNDING SM	TP47,TP49,TP50,TP51
481802800004	TF041-F/W ASSY;BIOS,8650	U14
288208896012	TF041-TH-TRANS;FDD8896_NL,N-MOS,	PU709,PU710
297140200010	TF041-SW;COVER SWITCH,0.1A,30V,4	SW1
331000004118	TF041-TH-CON;USB,4P,020173MR004S	J706
331910002016	TF041-TH-CON;DC POWER JACK,2P,20	PJ701
339115000074	TF041-MICROPHONE;-62dB+-2dB,D6.0	MIC1
422802800003	TF041-WIRE ASSY;BATT TO MB,MOLEX	J711
365350000004	SOLDER WIRE;LEAD_FREE,ECO,RMA98S	
345802800006	TF041-SPONGE;RTC,8650	
340880370001	TF041-TH-HOLDER;PCMCIA,933100000	
346802800018	TF041-INSULATOR;DDR,MINIPCI,8650	
370102010509	TF041-SPC-SCREW;M2L5,K-HD(+1),NI	
370102030304	TF041-SPC-SCREW;M2L3,K-HD(+1)D3.	
348105030025	TF041-GASKET;1,05,030,025	
348110010010	TF041-GASKET;1,10,010,010	
348105040015	TF041-GASKET;1,05,040,015	
346802800013	TF041-INSULATOR;PCMCIA,8650	
348108040008	TF041-GASKET;1,08,040,008	
346802800019	TF041-INSULATOR;MB,8650	
346802800015	TF041-INSULATOR;RJ11,BACK,8650	
346802800014	TF041-INSULATOR;PCMCIA_AL,8650	

Part Number	Description	Location(S)
348105025024	TF041-GASKET;1,05,025,024	
348210005010	TF041-GASKET;2,10,005,010	
343802800001	TF041-HEATSINK;NORTH BRIDGE,CHEE	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
412600000035	TF041-PCB ASSY;FAX MODEM 56K,MDC	
442600000077	TF041-TOUCHPAD MODULE;TM61PDM1G2	
324180787252	IC,CPU,Celeron-M 370,1.5GHZ(Doth	
340803300015	TF041-SHIELDING ASSY;HDD,ZEUS	
370103011402	TF041-SPC-SCREW;M3L3,NIW,K-HD(+)	
523402259026	HDD DRIVE,40GB,2.5",SAMSUNG MP04	
370102010207	TF041-SPC-SCREW;M2L2,NIW/NLK,K-H	
342672200010	TF041-BRACKET;CD-ROM,8500	
523430061040	8X Dual DVD R9 DEVICE;SDVD8431,W	
340802800020	TF041-BEZEL ASSY;D-D+R9,UJ840,86	
323780280001	DDR SO-DIMM;HYMD532M646CP6-J,DDR	
531020237777	KBD;88,UI,K011818A1,8050,BK	
442687900004	AC ADPT ASSY;19V,3.42A,Delta 65W	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	PAGE: 17
411802800017	TF041-BATT ASSY;LI-ION,14.8V/2.0	
222687630001	TF041-PE BUBBLE BAG;BATTERY,GRAM	
225686920001	TF041-TAPE;INSULATING,POLYESTER	
225686920002	TF041-TAPE;ADHENSIVE,DOUBLE-FACE	
242683200024	TF041-LABEL;5*20,BLANK,COMMON	

9. Spare Part List - 10

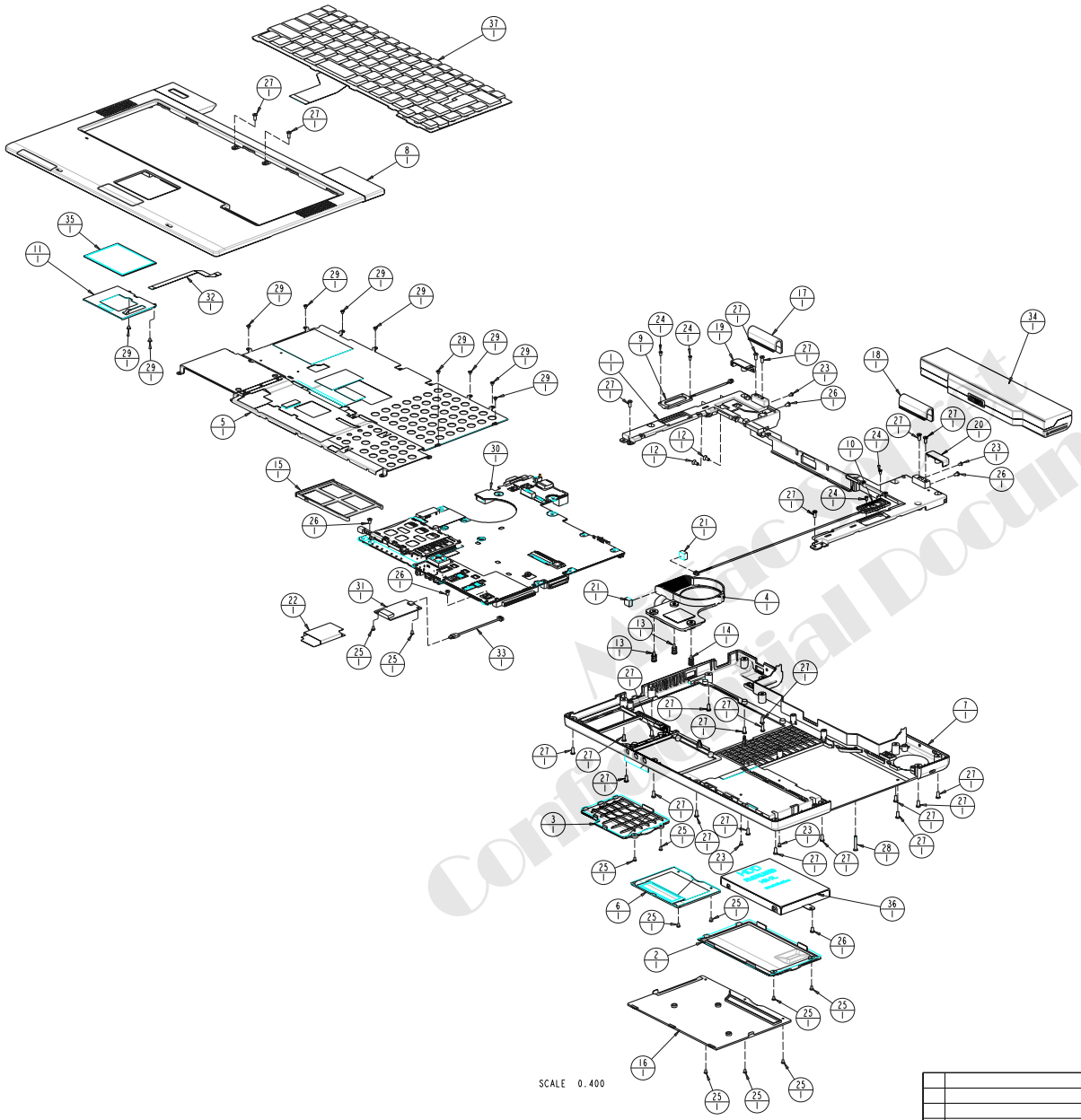
Part Number	Description	Location(S)
242686000009	TF041-LABEL;LOT NUMBER,HOOK	
242686000010	TF041-LABLE;40*6mm,BLANK, WHITE,	
242686500007	TF041-LABEL;BATTERY TRANSPORTATI	
242802800008	TF041-LABEL;BATT,LI-ION,14.8V/2.	
333025000015	TF041-SHRINK TUBE;300V,125,I.D=2	
335152000148	TF041-FUSE;20V/100A,LR4-550,POLY	
338536010061	TF041-BATTERY;LI,3.6V/2.0AH,1865	
342680600001	TF041-CONTACT PLATE;W5L24T0.13,7	
342686000017	TF041-TH-CONTACT PLATE;W4L30T0.1	
342687600003	TF041-CONTACT PLATE;W5L9T0.13,PW	
344686500034	TF041-DUMMY;PVC,D18L31.5,BATTERY	
344802800007	TF041-COVER;BATTERY,8650	
344802800008	TF041-HOUSING;BATTERY,8650	
346671600025	TF041-INSULATOR;BATT ASSY,W7L13,	
346678500024	TF041-INSULATOR;PE,MID ADHESIVE,	
346686000021	TF041-INSULATOR;BATT ASSY,L22R9.	
346686500032	TF041-INSULATOR;FIBRE,129*12,T=0	
346686500033	TF041-INSULATOR;FIBRE,106.4*13.4	
346801200006	TF041-INSULATOR;FIBRE,2CELL,DOUB	
361400004013	TF041-ADHESIVE;ABS+PC PACK,G485,	
361400004017	TF041-ADHESIVE;HEAT,TRANSFER,ES2	
365350000009	LF-SOLDER WIRE;SN96.5/AG3.0/CU0.	
310111103044	TF041-THERMISTOR;10K,1%,103AT-4-	RT1
331000007063	TF041-CONNECTOR;7 PIN,DIP,ALLTOP	CON1
332100020030	TF041-WIRE;#20,UL1007,57mm,RED,P	CN1

Part Number	Description	Location(S)
332100020031	TF041-WIRE;#20,UL1007,117mm,BLAC	CN5
332100026011	TF041-WIRE;#26,UL1007,60MM,BLUE,	CN4
332100026026	TF041-WIRE;#26,UL1007,105MM,YELL	CN2
332100026034	TF041-WIRE;#26,UL1007,35mm,WHITE	CN3
335152000131	TF041-FUSE; VS19, DC-7A/50V 139	F1
411802800034	TF041-PWA;PWA-8650/BATT,LI,4CELL	
271002102109	TF041-TH-RES;1K ,1/8W,1% ,0805,S	R10A
271002201103	TF041-TH-RES;200 ,1/10W,1% ,080	R24,R25
271006159301	TF041-TH-RES;.015 ,2W ,5% ,2512,	RM
271013101303	TF041-TH-RES;100 ,1/4W,5% ,1206,	R21,R23
271047407102	TF041-TH-RES;0.040,3W, 1%,2512,S	RS1
271071000312	TF041-TH-RES;0 ,1/16W,5% ,060	R10
271071101309	TF041-TH-RES;100 ,1/16W,5% ,060	R20,R22,R5,R6,R7,R
271071103310	TF041-TH-RES;10K ,1/16W,5% ,060	R13,R14,R3
271071104108	TF041-TH-RES;100K ,1/16W,1% ,060	R12,R15,R16,R17
271071105312	TF041-TH-RES;1M ,1/16W,5% ,060	R18,R19,R2,R4
271071224305	TF041-TH-RES;220K ,1/16W,5% ,060	R1
271071331306	TF041-TH-RES;330 ,1/16W,5% ,060	R11A
271071332313	TF041-TH-RES;332K ,1/16W,1% ,060	R11
271071364103	TF041-TH-RES;365K ,1/16W,1% ,060	R26PAGE: 18
272003105402	TF041-TH-CAP;1U ,CR,25V ,10%,0	C18,C21
272075102424	TF041-TH-CAP ;0.1U CR 50V 10% 06	C12,C13,C15,C19,C3,C5
272075224001	TF041-TH-CAP;0.22U,CR,50V,Y5V ,0	C1,C10B,C11B,C14A
272075470407	TF041-TH-CAP; 0.0047U CR 50V 10%	C20
272075471415	TF041-TH-CAP;470P ,50V,10%,0603,	C4

9. Spare Part List - 11

Part Number	Description	Location(S)
283240260001	TF041-TH-IC;EEPROM,M24C02-WMN6T,	IC2
286002040002	TF041-TH-IC;BQ2040,GAS GAUGE,SO,	IC4
286301414005	TF041-TH-IC;MM1414,PROTECTION,TS	IC1
286400812001	TF041-TH-IC;S-812C,DECECTOR,SOT-	IC3
288100056026	TF041-TH-DIODE;UDZ5V6B-F,ZENER,U	ZD1,ZD2
288100717001	TF041-TH-DIODE;SDMG0340LA,SCHOTT	SD1
288104148022	TF041-TH-DIODE;1N4148WS,75V,200m	D2
288111544002	TF041-TH-DIODE;S1G-F,400V,1.0A,S	D1
288200144035	TF041-TH-TRANS;DDTA144EKA,PNP,SM	Q1
288204409003	TF041-TH-TRANS;AO4409,P-MOSFET,S	Q2,Q3
316686500005	TF041-PCB;PWA-COUGAR A/4S1P,BATT	R0A
361200003064	TF041-SOLDER PASTE;SN96.5/AG3.0/	
335152000126	TF041-TH-CFM-BAT;FUSE,THERMAL,NE	
221802820001	TF041-CARTON;EZ PACKING,8650	
221802850004	TF041-CARD BOARD;TOP/BTM,8650	
221802850001	TF041-CARD BOARD;FRAME,8650	
221802850002	TF041-PARTITION;EZ IN CARTON,865	
224685330001	TF041-PALLET;1250*1080*130,3D-Ar	
227802800001	TF041-END CAP;R/L,8650	
222667220005	TF041-PE BAG;L560XW345,CERES	
222802810001	TF041-PROTECTING CLOTH;LCD/KB,86	
242600000559	TF041-LABEL;BAR CODE,125*65,COMM	
221802850003	TF041-PARTITION;PALLET,8650	
222685320003	TF041-PE BAG;120x170MM,W/SEAL,3D	
222300820002	TF041-PE BAG;50*70MM,W/SEAL,COMM	

Part Number	Description	Location(S)
222680830001	TF041-PE BUBBLE BAG;300X150mm,25	
222672730003	TF041-PE BUBBLE BAG;250*240mm,AM	
340802800014	TF041-HEAT SINK ASSY;MPT,FORCECON	
242803300001	TF041-BFM-SHARP;LABEL,WINXP,17x2	
242600000651	TF041-LABEL;25*10MM,3020F	
242802800012	TF041-LABEL;RATING,FUJITSU,AMILO	
		P/N 526280280003



SCALE 0.400

ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340802800008	TF041-BRACKET ASSY;SYSTEM,8650	1	ASSEMBLY	
2	340802800009	TF041-COVER ASSY;HDD,8650	1	ASSEMBLY	
3	340802800011	TF041-COVER ASSY;MINIPCI,8650	1	ASSEMBLY	
4	340802800013	TF041-HEATSINK ASSY;ALRO,8650	1	ASSEMBLY	
5	340802800016	TF041-SHIELDING ASSY;COVER,8650	1	ASSEMBLY	
6	340802800017	TF041-COVER ASSY;DDR,8650	1	ASSEMBLY	
7	340802800018	TF041-HOUSING ASSY;8650	1	ASSEMBLY	
8	340802800019	TF041-COVER ASSY;8650	1	ASSEMBLY	
9	340803300008	TF041-SPEAKER ASSY;L,ZEUS	1	ASSEMBLY	
10	340803300009	TF041-SPEAKER ASSY;R,ZEUS	1	ASSEMBLY	
11	340803300011	TF041-BRACKET ASSY;TP,ZEUS	1	ASSEMBLY	
12	341800200006	TF041-SPC SCREW;#4-1/4,POLARIS	2	PART	
13	341800200007	TF041-SPRING-SCREW-HEATSINK-POLA	2	PART	
14	341802800001	TF041-SPRING SCREW;HEATSINK,8650	1	PART	
15	344802800003	TF041-DUMMY CARD;PCMCIA,8650	1	PART	IN
16	344802800010	TF041-COVER;CPU,8650	1	PART	
17	344802800014	TF041-COVER;HINGE,L,8650	1	PART	
18	344802800015	TF041-COVER;HINGE,R,8650	1	PART	
19	344802800016	TF041-COVER;REAR,L,8650	1	PART	
20	344802800017	TF041-COVER;REAR,R,8650	1	PART	
21	345802800009	TF041-SPONGE;HEATSINK,SIDE,CPU,8	2	PART	
22	346802800012	TF041-INSULATOR;MDC,8650	1	PART	
⚠ 23	370102010314	TF041-SPC-SCREW; M2L3,K-HD(+I),N	4	PART	
⚠ 24	370102010354	TF041-SPC-SCREW;M2L3.5,K-HD(T0.3	4	PART	
25	370102030304	TF041-SPC-SCREW; M2L3,K-HD,ZnB/N	11	PART	
⚠ 26	370102610409	TF041-SPC-SCREW;M2.6L4,NIW,K-HD,	5	PART	
⚠ 27	370102610604	TF041-SPC-SCREW;M2.6L6,K-HD(+I)D	25	PART	IN
⚠ 28	370102611605	TF041-SPC-SCREW;M2.6L16,K-HD,ZNB	1	PART	IN
29	371102010263	TF041-SCREW;M2L2.5,K-HEAD(+I),NI	10	PART	
30	411802800018	TF041-PWA;PWA-8650,MOTHER BD	1	ASSEMBLY	
31	412600000035	TF041-PCB ASSY;FAX MODEM 56K,MDC	1	PART	
32	422802800006	TF041-CABLE;FFC,TP,8650	1	PART	
33	422802800010	TF041-WIRE ASSY;MDC,ISMT,8650	1	ASSEMBLY	
34	441802800045	TF041-BATT ASSY;LI-ION,11.1V/4.4	1	ASSEMBLY	
35	442600000077	TF041-TOUCHPAD MODULE;TM61PDW1G2	1	PART	
36	451802800004	TF041-HDD ME KIT;8650	1	ASSEMBLY	
37	53106809090I	KBD OPTION;UI,BK,8050	1	PART	

ITEM	CONTENTS OF CHANGE	BVS	CHK	APV	M/D/Y
⚠	ECR:G226945425/G226945932				09/10/05

TOL: RANGE	Plo	Met	Tes	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

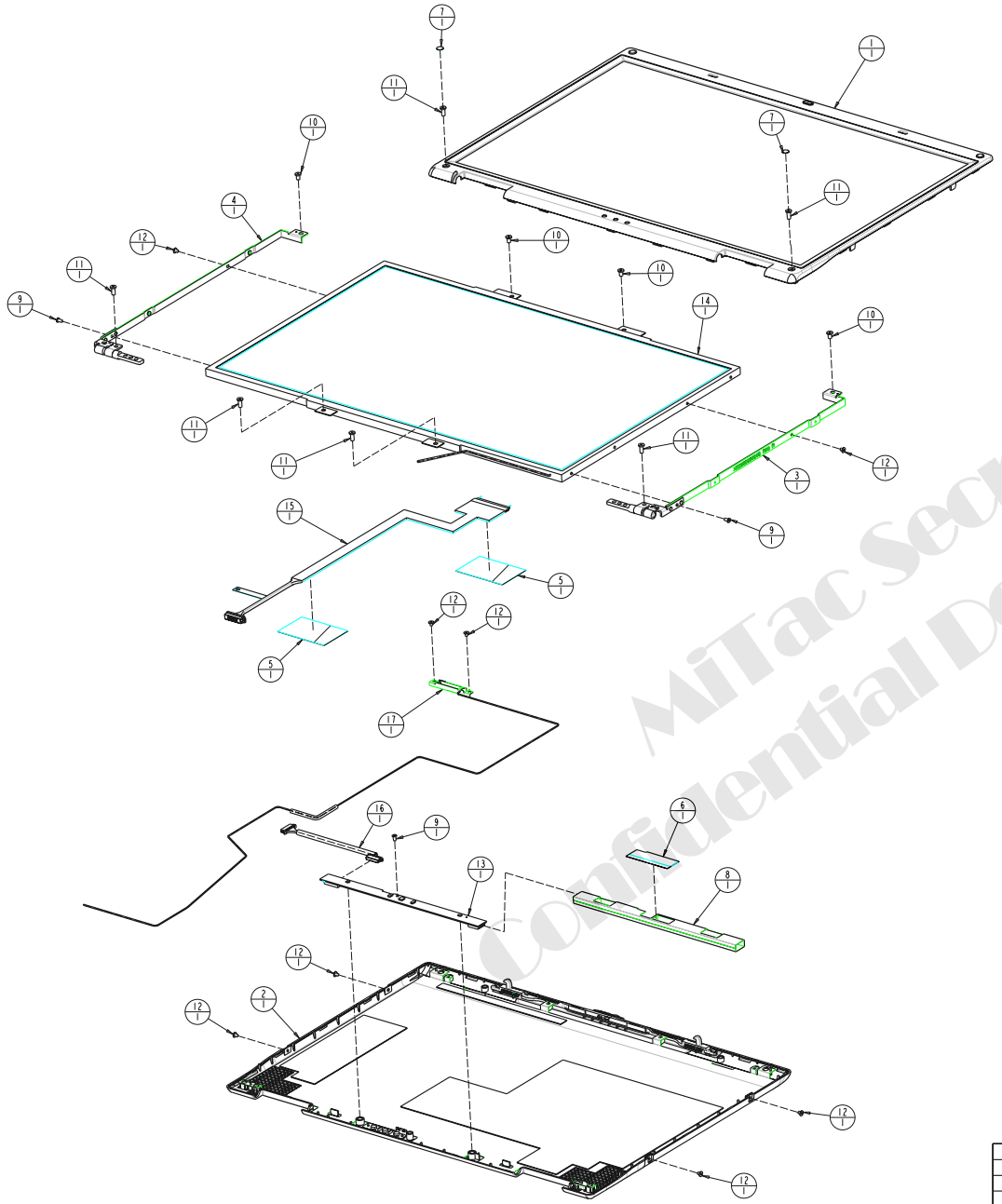
DATE	15-Sep-05	MATERIAL	SEE NOTES	TREATMENT	
UNIT	MM	SCALE	0.10	DRAWING NAME	TF041-HOUSING KIT;ID1/ID3,8650
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 802 800072 R 01

REMARK

MiTAC Technology Corp.

model name:STRU-8650 | file name:HOUSING-KIT-8650

SHEET NO. 1 of 1



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340802800010	TF041-COVER ASSY;LCD,8650	1	ASSEMBLY	
2	340802800012	TF041-HOUSING ASSY;LCD,8650	1	ASSEMBLY	
3	342803300002	TF041-HINGE;R,ZEUS	1	ASSEMBLY	
4	342803300003	TF041-HINGE;L,ZEUS	1	ASSEMBLY	
5	345802800008	TF041-CONDUCTIVE TAPE;LCD,8650	2	PART	
6	345802800008	TF041-INSULATOR;LENS,LCD,8650	1	PART	
7	346802800016	TF041-MYLAR;COVER,LCD,8650	2	PART	
8	346802800025	TF041-INSULATOR;INVERTER,LCD,865	1	PART	
9	370102010416	TF041-SPC-SCREW;M2L4,K-HD(10.3),	3	PART	
10	370102610409	TF041-SPC-SCREW;M2.6L4,NIW,K-HD,	4	PART	
11	370102610604	TF041-SPC-SCREW;M2.6L6,K-HD(+I)D	6	PART	IN
12	371102010263	TF041-SCREW;M2L2.5,K-HEAD(+I),NI	8	PART	
13	412681300004	TF041-PCB ASSY;D/A BD,DA-1A08-A,	1	ASSEMBLY	
14	413000021124	TFT LCD;CLAA154WA05,15.4" WXGA C	1	PART	
15	422802800008	TF041-WIRE_ASSY-LCD_15-ISMT-8650	1	ASSEMBLY	
16	422802800009	TF041-WIRE ASSY;INVERTER,ISMT,8650	1	ASSEMBLY	
17	422803300003	TF041-WIRE;ANTENNA,ASSY,L,ZEUS	1	ASSEMBLY	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

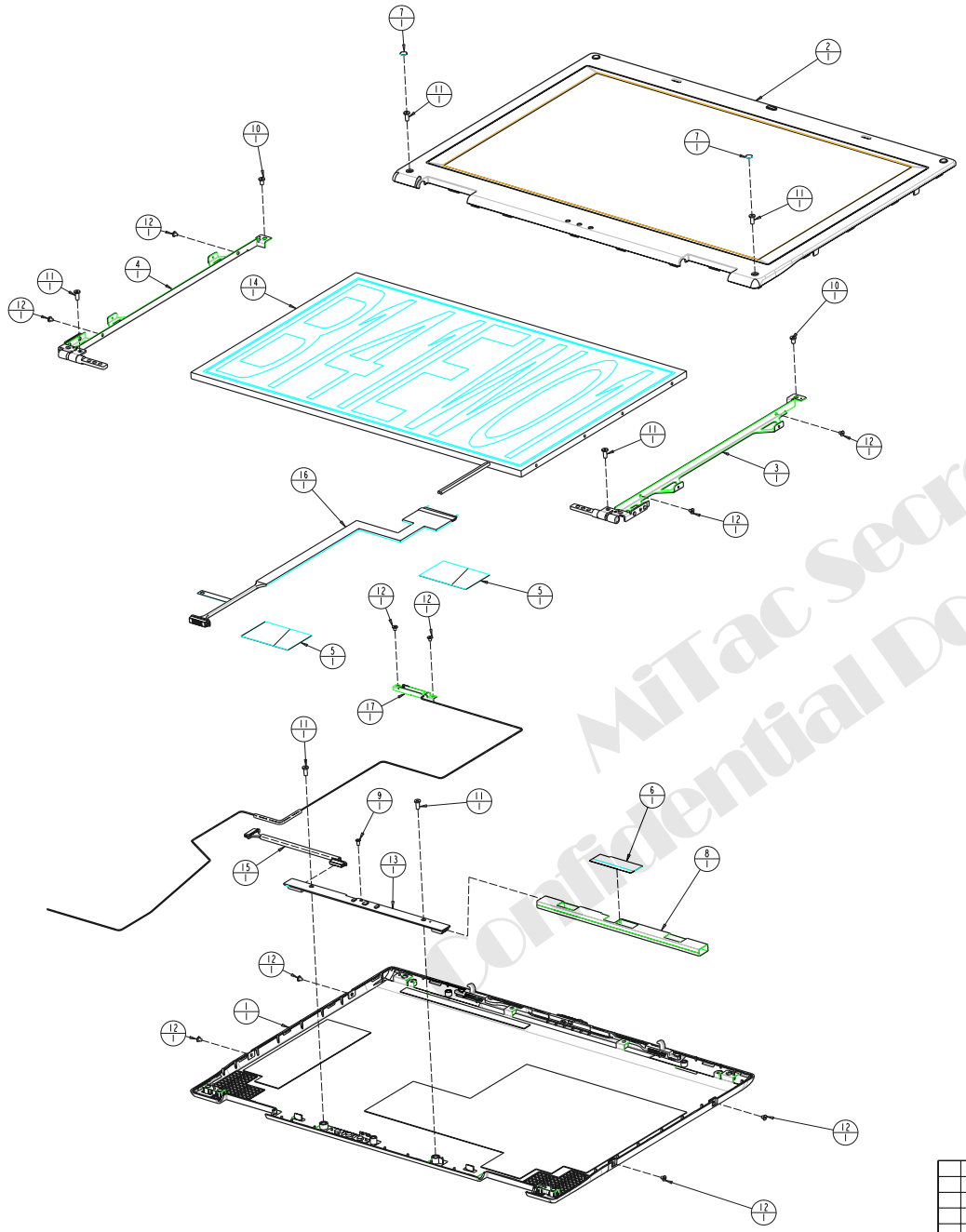
TOL ± RANGE	Pla	Met	Tes	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	05-Oct-05	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.55	DRAWING NAME	TF041-LCD ME KIT;CPT,1D1,8650		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 8028 00053 A 00		

MiTAC Technology Corp.

model name:LCD_ASSY-8650 | file name:LCD_ASSY-1D1-8650

SHEET NO. 1 of 1



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340802800012	TF041-HOUSING ASSY;LCD,8650	1	ASSEMBLY	
2	340802820001	TF041-COVER ASSY;LCD,14",ID3,865	1	ASSEMBLY	
3	342802820001	TF041-HINGE ;LCD,14",R,ID3,8650	1	ASSEMBLY	
4	342802820002	TF041-HINGE ;LCD,14",L,ID3,8650	1	ASSEMBLY	
5	345802800008	TF041-CONDUCTIVE TAPE;LCD,8650	2	PART	
6	345802800008	TF041-INSULATOR;LENS,LCD,8650	1	PART	
7	346802800016	TF041-MYLAR;COVER,LCD,8650	2	PART	
8	346802800025	TF041-INSULATOR;INVERTER,LCD,865	1	PART	
9	370102010416	TF041-SPC-SCREW;M2L4,K-HD(±0.3),	1	PART	
10	370102610409	TF041-SPC-SCREW;M2.6L4,NIW,K-HD,	2	PART	
11	370102610604	TF041-SPC-SCREW;M2.6L6,K-HD(+I)D	6	PART	IN
12	371102010263	TF041-SCREW;M2L2.5,K-HEAD(+I),NI	10	PART	
13	412681300004	TF041-PCB ASSY;D/A BD,DA-1A08-A,	1	ASSEMBLY	
14	413000021155	TFT LCD;B141EW01 V.1,14.1"WXGA,A	1	PART	
15	422802800009	TF041-WIRE ASSY;INVERTER,1SMT,8650	1	ASSEMBLY	
16	422802820002	TF041-WIRE ASSY;AU,LCD_14,1SMT,8650	1	ASSEMBLY	
17	422803300003	TF041-WIRE;ANTENNA,ASSY,L,ZEUS	1	ASSEMBLY	

ITEM	CONTENTS OF CHANGE	BVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL ± RANGE	Pla	Met	Tes	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	05-Oct-05	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.55	DRAWING NAME	TF041-LCD ME KIT;ID3,8650	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD 451 8028 20051 R 00	

MiTAC Technology Corp.

model name:LCD_ASSY-8650 | file name:LCD_ASSY-ID3-8650 | SHEET NO. 1 of 1

11. Reference Material

❖ Intel Banias CPU	Intel, INC
❖ VIA PN800 North Bridge	VIA, INC
❖ VIA VT8235CE South Bridge	VIA, INC
❖ Winbond W83L950D KBC	Winbond, INC
❖ 8650 Hardware Engineering Specification	Technology Corp/MITAC
❖ Explode Views	Technology Corp/MITAC

SERVICE MANUAL FOR 8650

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