SERVICE MANUAL FOR

8381

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MiTAC

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1. Hardware Engineering Specification

1.1 Introduction

The 8381 motherboard would support the AMD 35W Mobile Thoroughbred / Barton CPU with OPGA, 462 Socket, which will support different speeds up to 2200+ for Thoroughbred 35W (L2 cache 256K) and to 2500+ for Barton 35W(L2 cache 512K).

This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as Power indicator, HDD,CDROM, NUM LOCK, CAP LOCK, SCROLL LOCK,WIRELESS LAN and Battery charging status. It also equipped 4 USB ports.The memory subsystem supports 256MB on board DDR memory,One JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM) ,support PC2100.

Integrated VIA Apollo KN266 and S3 Graphics, ProSavage8 128-bit 2D/3D graphics controller with equivalent 8x AGP performance in a single chip, 64-bit Advanced Memory controller supporting PC2100/PC1600 DDR SDRAM. Combines with VIA VT8235 Vlink-LPC South Bridge with integrated audio, 4 USB ports, ATA100 IDE and LAN Mac.

To provide for the increasing number of multimedia applications, the AC97 CODEC CMI9738S is integrated onto the motherboard.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 2000 and Windows XP Home/Professional Edition to take full advantage of the hardware capabilities such as bus

mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

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1.2 System Hardware Parts

Item	System A	System B
CPU	AMD 35W Athlon XP CPU	AMD 35W Athlon XP CPU
Core logic	VIA KN266 (VT8372 +VT8235)	VIA KN266 (VT8372 +VT8235)
Memory on Board	DDRRAM:Samsung K4H561638D-TCB0	DDR RAM : Samsung K4H561638D-TCB0
AC Adapter	Delta:60W	FSP:90W FSP090-1ADC21
IDE External DVD-ROM Driver	8X DVD MKE: SR-8177(8X)	
IDE Internal Combo Drive		24*10*8*24 Combo(QSI:SBW-242)
USB External FDD driver	W/O Mitsumi ext. FDD	W/O Mitsumi ext. FDD
HDD	Fujitsu 20GB MHT2020AT	Fujitsu 40GB MHT2040T
TFT LCD Display	14.1”XGA QDI QD141*1LH12	14.1”XGA(CMO:N141X6-L01)
Video Controller	S3 ProSavage8	S3 ProSavage8
Pointing Device	SynapticsTM41PDM-311	SynapticsTM41PDM-311
FIR/ SIR	None	None
PCMCIA	TI PCI1510	TI PCI1510
Audio	CMI9783	CMI9783
I/O	None	None
Keyboard Controller	Hitachi H8/2140B	Hitachi H8/2140B
Fax Modem	Askey V1456VQL-P1(INT)	Askey 1456VQL4A(INT)
Battery	MSL 6 cells 2000mAH(Panasonic cell)	MSL 6 cells 2000mAH(sanyo cell)

1.2.1 The AMD Athlon XP processor model 8

The AMD Athlon XP processor model 8 is the latest member of the AMD Athlon family of processors designed to meet the computation-intensive requirements of cutting-edge software applications running on high-performance desktop systems. Delivered in an OPGA package, the AMD Athlon XP processor model 8 delivers the integer, floating-point, and 3D multimedia performance for highly demanding applications running on x86 system platforms.

The AMD Athlon XP processor model 8 delivers compelling performance for cutting-edge software applications that include high-speed Internet capability, digital content creation, digital photo editing, digital video, image compression, video encoding for streaming over the Internet, soft DVD, commercial 3D modeling, workstation-class Computer-Aided Design (CAD), commercial desktop publishing, and speech recognition. The AMD Athlon XP processor model 8 also offers the scalability and reliability that IT managers and business users require for enterprise computing.

The AMD Athlon XP processor model 8 features a seventh-generation micro architecture with an integrated, exclusive L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core of the AMD Athlon XP processor model 8 includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, an exclusive 256-Kbyte L2 cache, three independent integer pipelines, three address calculation pipelines, and a super scalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering outstanding performance on numerically complex applications.

The features of the AMD Athlon XP processor model 8 are Quaint Speed architecture, a high-performance full-speed cache, a 266-MHz, 2.1-Gigabyte per second system bus, and 3DNow! Professional technology. The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling to provide an extremely powerful, scalable bus for an x86 processor.

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The AMD Athlon XP processor model 8 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX, SSE, and 3DNow! technology. Using a data format and Single-Instruction Multiple-Data (SIMD) operations based on the MMX instruction model, the AMD Athlon XP processor model 8 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! Professional technology implemented in the AMD Athlon XP processor model 8 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for Digital Signal Processing (DSP) and communications applications.

The following features summarize the AMD Athlon XP processor model 8 QuantiSpeed architecture:

- An advanced nine-issue, super pipelined, super scalar x86 processor micro architecture designed for increased Instructions Per Cycle (IPC) and high clock frequencies
- Hardware data pre-fetch that increases and optimizes performance on high-end software applications utilizing high-bandwidth system capabilities
- Fully pipelined floating-point unit that executes all x87(floating-point), MMX, SSE and 3DNow! Instructions
- Advanced two-level Translation Look-aside Buffer (TLB) structures for both enhanced data and instruction address translation.

The AMD Athlon XP processor model 8 with QuantiSpeed architecture incorporates three TLB optimizations: the L1 DTLB increases from 32 to 40 entries, the L2 ITLB and L2 DTLB both use exclusive architecture, and the TLB entries can be speculatively loaded.

The AMD Athlon XP processor model 8 delivers excellent system performance in a cost-effective, industry-standard form factor. The AMD Athlon XP processor model 8 is compatible with motherboards based on Socket A.

1.2.2 System frequency

System frequency synthesizer ICS950902 pin configuration is suitable for VIA KN266 chipset with PC133 or DDR memory.

Output Features:

- 1 - Pair of differential CPU clocks @ 3.3V (CK408)/ 1 - Pair of differential open drain CPU clocks (K7)
- 1 - Pair of differential push pull CPU_PP clocks @ 2.5V
- 3 - AGP @ 3.3V
- 7 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz

Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.

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- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I 2 C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

- CPU_CS - CPUT/C: <250ps
- CPU_CS - AGP: <250ps
- CPU - DDR/SD: <250ps
- PCI - PCI: <500ps

1.2.3 Core Logic VIA KN266+ VIA 8235

1.2.3.1 VIA KN266 Chipset

Key Specifications:

- High Performance CPU Interface Socket-A support for AMD_ Athlon Processors.
- 266 or 200 MHz CPU Front Side Bus (FSB).
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions.
- Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch).
- Dynamic deferred transaction support.

High Bandwidth 266MB/sec 8-bit V-Link Host Controller:

- Supports 66 MHz V-Link Host interface with peak bandwidth of 266MB/sec.
- V-Link operates at 2X or 4X modes.
- Full-duplex commands with separate strobe / command.
- Request / Data split transaction.
- Configurable outstanding transaction queue for Host to V-Link Client accesses.

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- Supports Defer / Defer-Reply transactions.
- Transaction assurance for V-Link Host to Client access (eliminates V-Link Host-Client Retry cycles).
- Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency. All V-Link transactions (both Host and Client) have a consistent view of transaction data depth and buffer size to avoid data overflow .
- Highly efficient V-Link arbitration with minimum overhead. All V-Link transactions have predictable cycle length with known Command / Data duration .

Additional Features:

- 250 MHz RAMDAC with Gamma Correction.
- 12-bit interface to external TV encoder(No used).
- I2C Serial Bus and DDC Monitor Communications.
- 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O.
- 35 x 35mm HSBGA (Ball Grid Array with Heat Spreader) package with 552 balls.

Advanced High-Performance SDR / DDR DRAM Controller:

- DRAM interface synchronous with host CPU (100/133 MHz) for most flexible configuration.

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- DRAM interface may be faster than CPU by 33 MHz to allow use of 133 MHz memory with 100 MHz FSB.
- DRAM interface may be slower than CPU by 33 MHz to allow use of 100 MHz memory with 133 MHz FSB .
- Concurrent CPU, AGP, and V-Link access .
- Supports SDR and DDR SDRAM memory types.
- Clock Enable (CKE) control for SDRAM power reduction in high speed systems.
- Mixed 1M / 2M / 4M / 8M / 16M / 32M / 64MxN DRAMs.
- Supports 8 banks up to 4 GB DRAMs (512Mb x8/x16 DRAM technology) for registered SDR/DDR modules.
- Supports 6 banks up to 3 GB DRAMs (512Mb x8/x16 DRAM technology) for unbuffered SDR/DDR modules.
- Flexible row and column addresses. 64-bit data width only.
- LVTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM.
- Programmable I/O drive capability for MA, command, and MD signals.
- Dual copies of control signals for improved drive.
- Two-bank interleaving for 16Mbit SDRAM support.
- Two-bank and four bank interleaving for 64Mbit SDRAM support.
- Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU.

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- Seamless DRAM command scheduling for maximum DRAM bus utilization.
- Four cache lines (16 quadwords) of CPU to DRAM write buffers.
- Four cache lines of CPU to DRAM read prefetch buffers.
- Read around write capability for non-stalled CPU read.
- Speculative DRAM read before snoop result .
- Burst read and write operation .
- x-1-1-1-1-1-1-1 back-to-back accesses for SDR SDRAM .
- x-1/2-1/2-1/2-1-1/2-1/2-1/2 back-to-back accesses for DDR SDRAM .
- Supports DDR SDRAM CL 2/2.5/3 and 1T per command .
- Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh) .

Integrated ProSavage8 2D/3D/Video Accelerator:

- Optimized Shared Memory Architecture (SMA) .
- Equivalent 8x AGP internal performance .
- 8 / 16 / 32 MB frame buffer using system memory .
- Floating point triangle setup engine .

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- Single cycle 128-bit 3D architecture .
- 8M triangles/second setup engine .
- 140M pixels/second trilinear fill rate .
- Microsoft DirectX texture compression .
- Next generation, 128-bit 2D graphics engine .
- High quality DVD video playback .
- Flat panel monitor support .
- 2D/3D resolutions up to 1920x1440 .

3D Rendering Features:

- Single-pass multiple textures .
- Anisotropic filtering .
- 8-bit stencil buffer .
- 32-bit true color rendering .
- Specular lighting and diffuse shading .
- Alpha blending modes .

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- Massive 2K x 2K textures .
- MPEG-2 video textures .
- Vertex and table fog .
- 16 or 24-bit Z-buffering .
- Reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects .

2D Hardware Acceleration Features :

- ROP3 Ternary Raster Operation BitBLTs .
- 8, 16, and 32 bpp mode acceleration .

Motion Video Architecture :

- High quality up/down scaler .
- Planar to packed format conversion .
- Motion compensation for full speed DVD playback .
- Hardware subpicture blending and highlights .
- Multiple video windows for video conferencing .

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- Contrast, hue, saturation, brightness and gamma controls .
- Digital port for NTSC/PAL TV encoders .

Extensive LCD Support :

- Integrated 2-channel 110 MHz LVDS interface with 4-bit data path per channel .
- Support for all resolutions up to 1600x1200 .
- Panel power sequencing .
- Hardware Suspend/Standby control .

Flat Panel Monitor Support :

- 12-bit TFT flat panel interface to TMDS encoders .
- Digital Vis3ual Interface (DVI) 1.0 compliant .

Advanced System Power Management Support :

- Power down of SDRAM (CKE) .
- Independent clock stop controls for CPU / SDRAM and on-chip AGP bus .

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- Clock run and clock generator control for on-chip AGP bus .
- VTT suspend power plane preserves memory data .
- Suspend-to-DRAM and self-refresh power down .
- Low-leakage I/O pads .
- ACPI1.0B and PCIB us Power Management 1.1 compliant .

1.2.3.2 VIA VT8235 V-LINK CLIENT HIGHLY INTEGRATED SOUTH BRIGDE

High Bandwidth 533 MB/s 8-bit V-Link Client Controller :

- Supports 66 MHz V-Link Client interface with peak bandwidth of 533 MB/sec .
- V-Link operates in 2x, 4x, and 8x modes .
- Full duplex commands with separate Strobe / Command .
- Request / Data split transaction .
- Configurable outstanding transaction queue for V-Link Client accesses .
- Auto Client Retry to eliminate V-Link Host-Client Retry cycles .
- Auto connect / reconnect capability and dynamic stop for minimum power consumption .

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- Parity checking to insure correct data transfers .

Integrated Peripheral Controllers :

- Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability .
- Integrated USB 2.0 Controller with three root hubs and six function ports .
- Dual channel UltraDMA-133 / 100 / 66 / 33 master mode EIDE controller .
- AC-link interface for AC-97 audio codec and modem codec .
- HSP modem support .
- Integrated DirectSound compatible digital audio controller .
- LPC interface for Low Pin Count interface to Super-I/O or ROM .

Integrated Legacy Functions :

- Integrated Keyboard Controller with PS2 mouse support .
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI .
- Integrated DMA, timer, and interrupt controller.

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- Serial IRQ for docking and non-docking applications.
- Fast reset and Gate A20 operation.

Concurrent PCI Bus Controller :

- 33 MHz operation .
- Supports up to six PCI masters .
- Peer concurrency .
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time .
- Zero wait state PCI master and slave burst transfer rate .
- PCI to system memory data streaming up to 132Mbyte/sec (data sent to north bridge via high speed V-Link Interface) .
- PCI master snoop ahead and snoop filtering .
- Eight DW of CPU to PCI posted write buffers .
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities .
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM .

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- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters .
- Delay transaction from PCI master accessing DRAM .
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks) .
- Symmetric arbitration between Host/PCI bus for optimized system performance .
- Complete steerable PCI interrupts .
- PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs .

Fast Ethernet Controller :

- High performance PCI master interface with scatter / gather and bursting capability .
- Standard MII interface to external PHYceiver .
- 1 / 10 / 100 MHz full and half duplex operation .
- Independent 2K byte FIFOs for receive and transmit .
- Flexible dynamically loadable EEPROM algorithm .
- Physical, Broadcast, and Multicast address filtering using hashing function .
- Magic packet and wake-on-address filtering .
- Software controllable power down .

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UltraDMA-133 / 100 / 66 / 33 Master Mode EIDE Controller :

- Dual channel master mode hard disk controller supporting four Enhanced IDE devices .
- Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface .
- Increased reliability using UltraDMA-133/100/66 transfer protocols .
- Thirty-two levels (doublewords) of prefetch and write buffers .
- Dual DMA engine for concurrent dual channel operation .
- Bus master programming interface for SFF-8038i rev.1.0 .
- Windows-95com pliant .
- Full scatter gather capability .
- Support ATAPI compliant devices including DVD devices .
- Support PCI native and ATA compatibility modes .
- Complete software driver support .

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Direct Sound Ready AC97 Digital Audio Controller :

- AC-Link access to 4 CODECs (AC97 + AMC97 + MC97) .
- Multichannel Audio .
- Bus Master Scatter / Gather DMA .
- Dedicated read and write channels supporting simultaneous stereo playback and record .
- Dedicated read and write channels supporting simultaneous modem receive and transmit .
- 1 stereo DirectSound channel with source / volume control / mixer .
- 1 shared FM / SPDIF PCM read channel .
- 1 dedicated channel supporting multi-channel audio .
- 32-byte line-buffers for each SGD channel .
- Programmable 8bit / 16bit mono / stereo PCM data format support .
- AC97 2.1 compliant .

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System Management Bus Interface :

- Host interface for processor communications .
- Slave interface for external SMBus masters .

Universal Serial Bus Controller :

- USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible .
- USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible .
- Eighteen level (doublewords) data FIFO with full scatter and gather capability .
- Three root hubs and six function ports .
- Integrated physical layer transceivers with optional over-current detection status on USB inputs .
- Legacy keyboard and PS/2 mouse support .

Sophisticated PC2001-Compatible Mobile Power Management :

- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management .
- ACPI v1.0 Compliant .
- APM v1.2 Compliant .
- CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support .

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- PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control .
- Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options,suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up .
- Multiple suspend power plane controls and suspend status indicators .
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer .
- Normal, doze, sleep, suspend and conserve modes .
- Global and local device power control .
- System event monitoring with two event classes .
- Primary and secondary interrupt differentiation for individual channels .
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up .
- 32 general purpose input ports and 32 output ports .
- Multiple internal and external SMI sources for flexible power management models .
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field .
- Thermal alarm on external temperature sensing circuit .
- I/O pad leakage control .

Plug and Play Controller :

- PCI interrupts steerable to any interrupt channel .
- Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio .
- Microsoft Windows XPTM, Windows NTTM, Windows 2000TM, Windows 98TM and plug and play BIOS compliant .
- Built-in NAND-tree pin scan test capability .
- 22um, 2.5V, low power CMOS process .
- Single chip 27 x 27 mm, 1.0 mm ball pitch, 487 pin BGA .

1.2.4 Keyboard System: HITACHI 2140B Keyboard Controller

FEATURES :

- High-speed H8S/2000 central processing unit with an internal 16-bit architecture .
- Upward-compatible with H8/300 and H8/300H CPUs on an object level .
- Sixteen 16-bit general registers .
- 65 basic instructions .
- Various peripheral functions .

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- Data transfer controller (DTC) .
- 8-bit PWM timer (PWM) .
- 14-bit PWM timer (PWMX) .
- 16-bit free-running timer (FRT) .
- 8-bit timer (TMR) .
- Timer connection .
- Watchdog timer (WDT) .
- Asynchronous or clocked synchronous serial communication interface (SCI) .
- I2C bus interface (IIC) .
- Keyboard buffer controller .
- Host interface X-BUS interface (XBS) .
- Host interface LPC interface (LPC) .
- 8-bit D/A converter .
- 10-bit A/D converter .
- Clock pulse generator .

1.2.5 System Flash Memory (BIOS)

- 2 M (4M) bit Flash memory .
- Flashed by 3.3V only .
- User can upgrade the system BIOS in the future just running flash program .

1.2.6 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM) .
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components .
- 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD]) .
- VDD= VDDQ= +2.5V .
- VDDSPD = +2.2V to +5.5V .
- 5V I/O (SSTL_2 compatible) .
- Commands entered on each positive CK edge .
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs .

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- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle .
- Bi-directional data strobe (DQS) transmitted/received with data- i.e., source-synchronous data capture .
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.) .
- Four internal device banks for concurrent operation .
- Selectable burst lengths: 2, 4, or 8 .
- Auto pre-charge option .
- Auto Refresh and Self Refresh Modes .
- 15.6 μ s (MT4VDDT864H, MT8VDDT1664HD), 7.8125 μ s (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval .
- Serial Presence Detect (SPD) with EEPROM .
- Fast data transfer rates PC2100 or PC1600 .
- Selectable READ CAS latency for maximum compatibility .
- Gold-plated edge contacts .

1.2.7 VIA VT6103 Fast Ethernet 10/100 1-Port PHY / Transceiver

FEATURES :

- Single Chip 100Base-TX / 10Base-T Physical Layer Solution .
- Dual Speed - 100 / 10 Mbps .
- Half and Full Duplex .
- MII Interface to Ethernet Controller .
- MII Interface to Configuration & Status .
- Optional Repeater Interface .
- Auto Negotiation: 10 / 100, Full / Half Duplex .
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards .
- On Chip Wave Shaping - No External Filters Required .
- Adaptive Equalizer .
- Baseline Wander Correction .
- LED Outputs .
- Link Status .

- Duplex status
- Speed Status .
- Collision .
- 48 Pin SSOP Package .

1.2.8 PC Card Interface Controller: PCI 1510

The Texas Instruments PCI1510, a 144-terminal single-slot CardBus controller designed to meet the PCI Bus Power Management Interface Specification for PCI to CardBus Bridges, is an ultra low-power high-performance PCI-to-CardBus controller that supports a single PC card socket compliant with the PC Card Standard (rev. 7.2). The PCI1510 provides features that make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The PC Card Standard retains the 16-bit PC Card specification defined in the PCI Local Bus Specification and defines the 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1510 supports both 16-bit and CardBus PC Cards, powered at 5 V or 3.3 V, as required.The PCI1510 is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during CardBus PC Card bridging transactions. ThePCI1510 is also compliant with PCI Bus Power Management Interface Specification (rev. 1.1).

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1510 is register-compatible with the Intel 82365SL-DF and 82365SL ExCA controllers. The PCI1510 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1510 can also be programmed to accept fast posted writes to improve system-bus utilization.

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Multiple system-interrupt signaling options are provided, including parallel PCI,parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the PCI1510, such as a socket activity light-emitting diode (LED) outputs, are discussed in detail throughout this document. An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

The PCI1510 supports the following features:

- A 144-terminal low-profile QFP (PGE) or 144-terminal MicroStar BGA. ball-grid array (GGU) package .
- 2.5-V core logic and 3.3-V I/O with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments .
- Integrated low-dropout voltage regulator (LDO-VR) eliminates the need for an external 2.5-V power supply .
- Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards .
- A single PC Card or CardBus slot with hot insertion and removal .
- Parallel interface to TI TPS2211A single-slot PC Card power switch .
- Burst transfers to maximize data throughput with CardBus Cards .
- Interrupt configurations: parallel PCI, serialized PCI, parallel ISA, and serialized ISA .
- Serial EEPROM interface for loading subsystem ID, subsystem vendor ID, and other configuration registers

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- Pipelined architecture for greater than 130-Mbps throughput from CardBus-to-PCI and from PCI-to-CardBus .
- Up to five general-purpose I/Os .
- Programmable output select for CLKRUN .
- Five PCI memory windows and two I/O windows available for the 16-bit interface .
- Two I/O windows and two memory windows available to the CardBus socket .
- Exchangeable-card-architecture- (ExCA-) compatible registers are mapped in memory and I/O space .
- Intel. 82365SL-DF and 82365SL register compatible .
- Ring indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN .
- Socket activity LED terminal .
- PCI bus lock (LOCK) .
- Internal ring oscillator .

1.2.9 AC'97 AUDIO SYSTEM: CMI 9738S

VT8235 is an AC'97 2.1 compliant controller that communicates with companion Codecs through a digital serial link called the AC-link.

The CMI9738S is an AC97 2.2 compatible stereo audio codec designed for PC multimedia systems.The CMI9738S prives the way for PC98 and PC99-compliant desktop, portable, and entertainment PCs, where high-quality audio is required.

The CMI9738S AC'97 CODEC provides a complete high quality audio solution.

Features :

- Intel® AC’97(Rev 2.2) compatible, meeting Microsoft’s® PC2001 requirements .
- Built-in earphone buffer and internal PLL, the latter saving additional crystal.
- Line-in/rear out share the same jack.
- Digital S/PDIF IN/OUT support .
- 48 LQFP package.
- CRL® 3D: HRTF based DS3D compatible audio engine.
- EAX™ 1.0 & 2.0 compatible .
- Sensaura™ 3D audio enhancement (optional) .

- 18-20bit DAC interface for SPDIF I/O(ICH4) .

1.2.10 MDC: Billionton MDC56S-E Modem

Features :

- MDC (Mobile Daughter Card) 56Kbps modem card.
- Software modem & Fax. Line-in/rear out share the same jack.
- Supports V.92 and K56Flex modem function.
- Supports 14.4 Kbps Fax function.
- Supports TAPI & TAM telephony service.
- Supports ACPI Power Management and wake-up on ring.

Specification :

- Compliant to Intel Mobile Audio/Modem Daughter Card Specification 1.0.

Data Modem :

- 56 Kbps (K56Flex and V.90).
- V.34 (4.8 Kbps to 33.6 Kbps).

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- V.32 bis (4.8 Kbps to 14.4 Kbps).
- V.22 bis (50 bps to 2.4 Kbps).
- V21, Bell 103 / Bell 212.
- V.42 bis/MNP 5 data compression.
- V.42/MNP 2-4 error correction.
- Virtual Com port with a throughput of up to 460.8 Kbps.
- Hayes AT Command set.
- TIES escape code.
- Fax Modem Standard.
- Send and receive rates up to 14.4 kbps, V.17, V.29, V.27ter.
- Telephony Services .
- Country Select.

1.2.11 Audio Power Amplifier :TPA0212

Features :

- Compatible With PC 99 Desktop Line-Out Into 10-k ohm Load .
- Internal Gain Control, Which Eliminates .
- External Gain-Setting Resistors .
- 2-W/Ch Output Power Into 3-W Load .
- Input MUX Select Terminal .
- PC-Beep Input .
- Depop Circuitry .
- Stereo Input MUX .
- Fully Differential Input .
- Low Supply Current and Shutdown Current .
- Surface-Mount Power Packaging .
- 24-Pin TSSOP PowerPADE .

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Applications General Description :

The TPA0212 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2 W of continuous RMS power per channel into 3-W loads. This device minimizes the number of external components needed, simplifying the design, and freeing up board space for other features. When driving 1 W into 8-W speakers, the TPA0212 has less than 0.8% THD+N across its specified frequency range.

Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is internally configured and controlled by way of two terminals (GAIN0 and GAIN1). BTL gain settings of 2, 6, 12, and 24 V/V are provided, while SE gain is always configured as 1 V/V for headphone drive. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/LINE terminal allows the user to select which MUX input is active regardless of whether the amplifier is in SE or BTL mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0212 automatically switches into SE mode when the SE/BTL input is activated, and this reduces the gain to 1 V/V.

The TPA0212 consumes only 6 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to less than 150 mA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0212 to operate at full power into 8-W loads at an ambient temperature of 85°C.

1.2.12 Single-Slot PC Card Power Interface Switch: TPS2211

TPS2211 is a single slot PCMCIA and CardBus power switch. It integrates control logic, low switching resistance MOSFET, over current alarm and over temperature auto shutdown circuits. It can deliver 3.3V or 5V to PC Card xVCCOUT and 3.3V, 5V or 12V to PC Card xVPPOUT. The output current is up to 1A for xVCCOUT and 250mA for xVPPOUT. The power is controlled by 4-wire parallel data interface VCCD0Z, VCCD1Z, VPPD0 and VPPD1.Fully integrated Vcc and Vpp Switching for Single-Slot PC Card Interface Low Rds(on)(90-mohm 5-V Vcc Switch and 3.3-V Vcc Switch) Compatible with controllers from cirrus , Ricoh ,O2Micro , and Texas Instruments 3.3 -V Low -voltage Mode Meets PC Card Standards 12-V Supply Can BE Disable Except During 12-V Flash programming Short -Circuit and Thermal Protection Spacing-Saving 16-Pin SSOP(DB) Compatible with 3.3-V ,5-V and 12-v PC Cards Break-Before-Make Switching

1.3 OTHER FUNCTIONS

1.3.1 Hot Key Function (not confirmed with Sharp)

Keys Combination	Feature	Meaning
Fn + F1		
Fn + F2		
Fn + F3	Volume down	Audio Volume down
Fn + F4	Volume up	Audio Volume up
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F8	Max Brightness	Toggle Maximum brightness and last state
Fn + F9		
Fn + F10	Beep Off/ ON	Toggle Beep sound on/off
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power on/off/suspend/resume button

APM mode :

At APM mode, Power button is on/off system power.

ACPI mode :

At ACPI mode. Windows power management control panel set power button behavior.

You could set "standby", "power off" or "hibernate"(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None

2. Standby

3. Off

4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at the lower side of Panel cover and five in the front-left edge of the notebook .

Three LED indicators at the lower side of LCD Panel:

From left to right that indicate, POWER STATUS, BATTERY STATUS and WIRELESS LAN ANTENNA STATUS.

POWER STATUS: This LED lights green when system is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active .

BATTERY STATUS: When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged. When the battery capacity drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second.

Five LED indicators at front-left side of system:

From left to right that indicates CD-ROM activity, HARD DRIVE activity, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.3.5 Battery status

Battery Warning :

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds. nSystem will suspend to HDD after 2 Minutes to protect users data.

Battery Low State :

After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice per second.

Battery Dead State :

When the battery voltage level reaches 7.4 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan power on/off management

FAN is controlled by H8 embedded controller-using AD1032 to sense CPU temperature and H8/2140 PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

CR2032 3V 220mAh lithium battery

When AC in or system main battery inside, CMOS battery will consume no power.AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.Battery was put in battery holder, can be replaced.

1.3.8 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display .
- Supports four USB2.0 ports for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line.
- One RJ-45 for LAN.
- Headphone Out Jack.
- One Microphone Input Jack.

- One Card Bus Sockets for one type II PC card extension.
- One USB HDD connector.
- Low Supply Current and Shutdown Current .
- Surface-Mount Power Packaging .
- 24-Pin TSSOP PowerPADE .

1.3.9 Battery current limit and learning

Implanted H/W current limit and battery learning circuit to enhance the protection of battery.

1.3.10 NEC μPD720130 Hi-Speed USB 2.0 to IDE Bridge

The μPD720130 is designed to perform a bridge between USB 2.0 and ATA/ATAPI. The μPD720130 complies with the Universal Serial Bus Specification Revision 2.0 full-/high-speed signaling and works up to 480 Mbps. The μPD720130 is integrated CISC processor, ATA/ATAPI controller, endpoint controller (EPC), serial interface engine (SIE), and USB2.0 transceiver into a single chip. The USB2.0 protocol and class specific protocol (bulk only protocol) are handled by USB2.0 transceiver, SIE, and EPC. And the transport layer is performed by V30MZ CISC processor which is in the μPD720130. The software to control the μPD720130 is located in an embedded ROM. In the future, the μPD720130 will be released to support external Flash Memory / EEPROM™ option to update function by firmware.

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The μ PD720130 features:

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps) .
- Compliant with ATA/ATAPI-6 (LBA48, PIO Mode 0-4, Multi Word DMA Mode 0-2, Ultra DMA Mode 0-4) .
- USB2.0 high-speed bus powered device capability .
- Certified by USB implementers forum and granted with USB 2.0 high-speed Logo (TID :40320125) .
- One USB2.0 high-speed transceiver / receiver with full-speed transceiver / receiver .
- USB2.0 High-speed or Full-speed packet protocol sequencer (Serial Interface Engine) .
- Automatic chirp assertion and full-/high-speed mode change .
- USB Reset, Suspend and Resume signaling detection .
- Supports power control functionality for IDE device as CD-ROM and HDD .
- Supports set feature (TEST_MODE) functionality .
- System Clock is generated by 30 MHz X’tal .
- 2.5 V and 3.3 V power supply .

1.4 PERIPHERAL COMPONENTS

1.4.1 LCD PANEL

14" TFT XGA :

- QDI:QD141X1LH03-MP01 .
- CHI-mei : N141X6-L01 .
- AU :B141XN04-2(UB141X03) .

14" TFT XGA :

- Hannstar HSD121PX11 .
- Hyundai HT12X1215" TFT .
- Sanyo TM121XG-02L10 .

1.4.2 Ext.Floppy Disk Drive

Mitsumi D353FUE(3.5" 1.44MB /1.2 MB/720KB FDD) .

1.4.3 HDD

FUJITSUI : 40GB MHR2040AT

HITACHI : 30GB DK23EA-30 , 40GB DK23DA-40 , 60GB DK23DA-60

Toshiba : 60GB MK6021 .

1.4.4 DVD-ROM

QSI:SDR-083(8X)

1.4.5 Combo Driver

Quanta: DW242

Matsushita: UJDA 740SH1-A

Matsushita: UJDA810 .

1.4.6 CD-RW

Matsushita: CD-RW - UJDA 340 L-MT .

1.4.7 Keyboard

JME

OKI

1.4.8 Track Pad Synaptic

- Accurate positioning .
- Low fatigue pointing action .
- Low profile .
- No moving part, high reliability .
- Low power consumption .
- Environmentally sealed .
- Compact size .
- Software configurable .
- Low weight .
- Operating temperature: 0 to 60 degree C .

- Operating humidity: 5%-95% relative humidity, non condensing .
- Storage temperature: -40 to +65 degree C .
- ESD: 15KV applied to front surface SEE ESD Testing specification PN520-000270-01 .
- Power supply voltage: 5.0Voltage ±10% .
- Power supply current: 4.0mA max operating .

1.4.9 Fan

HY45J05-001

1.4.10 Memory (optional)

DDR SO-DIMM module 128/256 MB support PC2100 specification

1. Kingmax: MSDB62D-68KX2-MAA(256M), MSDA82D-68KX2-MAA (128M)
2. Apacer:77.10321.460 (128MB) ,77.10521.460 (128MB), 77.10620.110 (256MB)

1.4.11 Wireless LAN(optional)

MiTAC

Askey WLL030

Ambit

1.4.12 Modem MDC

Billionton MDC56S-1

AC97 Link: MDC (Mobile Daughter Card)Askey: V1456VQL-P1(INT)

1.5 POWER MANAGEMENT

The 8381system has built in several power saving modes to prolong the battery usage. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key).

Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

Full on mode :

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode :

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

Standby mode :

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

--CPU: Stop grant

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--LCD: backlight off

--HDD: spin down

Suspend to DRAM :

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

CPU: off

Twister K: Partial off

VGA: Suspend

PCMCIA: Suspend

Audio: off

SDRAM: self refresh

Suspend to HDD :

All devices are stopped clock and power-down

System status is saved in HDD

All system status will be restored when powered on again

1.5.2 Other power management functions

HDD & Video access :

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 APPENDIX 1: VT 8235 GPIO DEFINITIONS

The definition of VIA VT8235 GPIO :

GPIO	Multi-Function	Default	Selection function	Power plant	Comment
GPI0	GPI0	X	GPI0	RTC	4.7Kà +3V
GPI1	GPI1	X	GPI1	VSUS33	4.7Kà +3V
GPI2	EXTSMI#	X	EXTSMI#	VSUS33	
GPI3	RING#	X	WAKEUP#	VSUS33	
GPI4	LID	X	PME#	VSUS33	
GPI5	BATLOW#	X	GPI5	VSUS33	
GPI6	AGPBZ#	X	AGPBUSY#	MAIN	
GPI7	REQ5#	X	PCI_REQ5#	MAIN	
GPI***O*** 8	PCREQA/VGATE	X	CD_RST	MAIN	
GPI/O9	PCREQB		GPIO9	MAIN	
GPI/O10			GPIO10	MAIN	
GPI/***O*** 11			GPIO11	MAIN	
GPI/O12	INTE# / PCGNTA		MB_ID0	MAIN	
GPI/O13	INTF# / PCGNTB		MB_ID1	MAIN	
GPI/O14	INTG#	X	MPCI_ACT#	MAIN	
GPI/O15	INTH#		LCD_ID0	MAIN	

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The definition of VIA VT8235 GPIO :

GPIO	Multi-Function	Default	Selection function	Power plant	Comment
GPI16	INTRUDER#	X	GPI16	RTC	
GPI17	CPUMISS	X	CPUMISS#	MAIN	
GPI18	THRM# / AOLGPI	X	THRM#	MAIN	
GPI19	IORDY	X	IOCHRDY	MAIN	
GPI/O20	ACSDIN2/PCS0#	X	GPI20	MAIN	10K-> GND
GPI/O21	ACSDIN3 / PCS1# / SLPBTN#	X	GPI21	MAIN	10K -> GND
GPI/O22	GHI#	X	GHI	MAIN	10K-> +3VS
GPI/O23	DPSLP#	X	DPRSLP	MAIN	10K->+3VS
GP***I***/O24	GPIOA	X	KBD_US/JP#	MAIN	
GPI/***O*** 25	GPIOC	X	MINIPCI_PD	MAIN	
GPI/O26	SMBDT2	X	SMBCLK2	VSUS33	
GPI/O27	SMBCK2	X	SMBDATA2	VSUS33	
GPI/O28	VIDSEL	X	VIDSEL	MAIN	10K -> GND
GPI/O29	VRDSLP	X	LCD_ID0	MAIN	
GP***I***/O30	GPIOD	X	LCD_ID1	MAIN	
GP***I***/O31	GPIOE	X	LCD_ID2	MAIN	

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The definition of VIA VT8235 GPIO :

GPIO	Multi-Function	Default	Selection function	Power plant	Comment
GPO0		X	GPO0	VSUS33	4.7K-> +3V
GPO1	SUSA#	X	SUSA#	VSUS33	
GPO2	SUSB#	X	SUSB#	VSUS33	
GPO3	SUSST1#	X	SB_SUSST#	VSUS33	
GPO4	SUSCLK	X	SUSCLK#	VSUS33	
GPO5	CPUSTP#	X	CPU_STP#	MAIN	TP509
GPO6	PCISTP#		PCI_STP#	MAIN	
GPO7	GNT5#		PCI_GNT5#	MAIN	
GPIO16	SA16/STRAP		STRAP16	MAIN	10K-> +3VS
GPIO17	SA17/STRAP		STRAP17	MAIN	SBFEQ_SEL
GPIO18	SA18/STRAP		STRAP18	MAIN	LVSFID0
GPIO19	SA19/STRAP		STRAP19	MAIN	LVSFID1

1.7 Appendix 2: H8 Pins Definitions

Port/Pin	Pin Number	HIF disable	HIF enable	Flash Memory PROM Mode	Mitac definition function	During Reset	Normal Operation	Sleep Mode	Software Standby Mode
P1-0	79	P1-0		FA0	KO0	Tri-state	H/L	Prev.	Prev.
P1-1	78	P1-1		FA1	KO1	Tri-state	H/L	Prev.	Prev.
P1-2	77	P1-2		FA2	KO2	Tri-state	H/L	Prev.	Prev.
P1-3	76	P1-3		FA3	KO3	Tri-state	H/L	Prev.	Prev.
P1-4	75	P1-4		FA4	KO4	Tri-state	H/L	Prev.	Prev.
P1-5	74	P1-5		FA5	KO5	Tri-state	H/L	Prev.	Prev.
P1-6	73	P1-6		FA6	KO6	Tri-state	H/L	Prev.	Prev.
P1-7	72	P1-7		FA7	KO7	Tri-state	H/L	Prev.	Prev.
P2-0	67	P2-0		FA8	KO8	Tri-state	H/L	Prev.	Prev.
P2-1	66	P2-1		OE#	KO9	Tri-state	H/L	Prev.	Prev.
P2-2	65	P2-2		FA10	KO10	Tri-state	H/L	Prev.	Prev.
P2-3	64	P2-3		FA11	KO11	Tri-state	H/L	Prev.	Prev.
P2-4	63	P2-4		FA12	KO12	Tri-state	H/L	Prev.	Prev.
P2-5	62	P2-5		FA13	KO13	Tri-state	H/L	Prev.	Prev.
P2-6	61	P2-6		FA14	KO14	Tri-state	H/L	Prev.	Prev.
P2-7	60	P2-7		CE#	KO15	Tri-state	H/L	Prev.	Prev.
P3-0	82	P3-0	HDB0	FO0	LPC_AD0	Tri-state	H/L	Prev.	Prev.
P3-1	83	P3-1	HDB1	FO1	LPC_AD1	Tri-state	H/L	Prev.	Prev.
P3-2	84	P3-2	HDB2	FO2	LPC_AD2	Tri-state	H/L	Prev.	Prev.
P3-3	85	P3-3	HDB3	FO3	LPC_AD3	Tri-state	H/L	Prev.	Prev.

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Port/Pin	Pin Number	HIF disable	HIF enable	Flash Memory PROM Mode	Mitac definition function	During Reset	Normal Operation	Sleep Mode	Software Standby Mode
P3-4	86	P3-4	HDB4	FO4	LPC_FRAME#	Tri-state	H/L	Prev.	Prev.
P3-5	87	P3-5	HDB5	FO5	PCIRST#	Tri-state	H/L	Prev.	Prev.
P3-6	88	P3-6	HDB6	FO6	H8_CLK	Tri-state	H/L	Prev.	Prev.
P3-7	89	P3-7	HDB7	FO7	SERIRQ	Tri-state	H/L	Prev.	Prev.
P4-0	49				H8_PWRON	Tri-state	H/L	Prev.	Prev.
P4-1	50				H8_SPK_OFF#	Tri-state	H/L	Prev.	Prev.
P4-2	51				FAN_SWITCH	Tri-state	H/L	Prev.	Prev.
P4-3	52				FAN_SPD	Tri-state	H/L	Prev.	Prev.
P4-4	53				H8_MCLK_RST#	Tri-state	H/L	Prev.	Prev.
P4-5	54					Tri-state	H/L	Prev.	Prev.
P4-6	55				FAN_ON	Tri-state	H/L	Prev.	Prev.
P4-7	56				USB_LOW_POWER	Tri-state	H/L	Prev.	Prev.
P5-0	14				LED_DATA	Tri-state	H/L	Prev.	Prev.
P5-1	13				LED_CLK	Tri-state	H/L	Prev.	Prev.
P5-2	12				BAT_CLK	Tri-state	H/L	Prev.	Prev.
P6-0	26				KI0	Tri-state	H/L	Prev.	Prev.
P6-1	27				KI1	Tri-state	H/L	Prev.	Prev.
P6-2	28				KI2	Tri-state	H/L	Prev.	Prev.
P6-3	29				KI3	Tri-state	H/L	Prev.	Prev.
P6-4	32				KI4	Tri-state	H/L	Prev.	Prev.

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Port/Pin	Pin Number	HIF disable	HIF enable	Flash Memory PROM Mode	Mitac definition function	During Reset	Normal Operation	Sleep Mode	Software Standby Mode
P6-5	33				KI5	Tri-state	H/L	Prev.	Prev.
P6-6	34				KI6	Tri-state	H/L	Prev.	Prev.
P6-7	35				KI7	Tri-state	H/L	Prev.	Prev.
P7-0	38				BATT_T	Tri-state	H/L	Tri-state	Tri-state
P7-1	39				BATT_V	Tri-state	H/L	Tri-state	Tri-state
P7-2	40				+3V	Tri-state	H/L	Tri-state	Tri-state
P7-3	41				+2.5V	Tri-state	H/L	Tri-state	Tri-state
P7-4	42				+CPU_CORE	Tri-state	H/L	Tri-state	Tri-state
P7-5	43				D/CAP/I_LIMIT	Tri-state	H/L	Tri-state	Tri-state
P7-6	44				CHARGE_I_CTR	Tri-state	H/L	Tri-state	Tri-state
P7-7	45				BLADJ	Tri-state	H/L	Tri-state	Tri-state
P8-0	93				SW_VDD3	Tri-state	H/L	Prev.	Prev.
P8-1	94				H8_A20GATE	Tri-state	H/L	Prev.	Prev.
P8-2	95				CLKRUN#	Tri-state	H/L	Prev.	Prev.
P8-3	96				LPCPD#	Tri-state	H/L	Prev.	Prev.
P8-4	97				H8_WAKE_UP#	Tri-state	H/L	Prev.	Prev.
P8-5	98				H8_THRM#	Tri-state	H/L	Prev.	Prev.
P8-6	99					Tri-state	H/L	Prev.	Prev.
P9-0	25				H8_LIDSW#	Tri-state	H/L	Prev.	Prev.
P9-1	24				H8_SUSB	Tri-state	H/L	Prev.	Prev.

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Port/Pin	Pin Number	HIF disable	HIF enable	Flash Memory PROM Mode	Mitac definition function	During Reset	Normal Operation	Sleep Mode	Software Standby Mode
P9-3	22			WE#	H8_SB_PWRBTN	Tri-state	H/L	Prev.	Prev.
P9-4	19			FA15	H8_RCIN#	Tri-state	H/L	Prev.	Prev.
P9-5	18			FA16	H8_RSMRST#	Tri-state	H/L	Prev.	Prev.
P9-6	17				H8_SUSC	Tri-state	H/L	Tri-state/clocl output	Tri-state/clocl output
P9-7	16				BAT_DATA	Tri-state	H/L	Prev.	Prev.
PA-0	48				H8_ADEN#	Tri-state	H/L	Prev.	Prev.
PA-1	47				BATT_DEAD#	Tri-state	H/L	Prev.	Prev.
PA-2	31				CARD_RI#	Tri-state	H/L	Prev.	Prev.
PA-3	30				USBPWR_ON	Tri-state	H/L	Prev.	Prev.
PA-4	21					Tri-state	H/L	Prev.	Prev.
PA-5	20				KBD_US/JP#	Tri-state	H/L	Prev.	Prev.
PA-6	11				T_CLK	Tri-state	H/L	Prev.	Prev.
PA-7	10				T_DATA	Tri-state	H/L	Prev.	Prev.
PB-0	91				H8_SMI#	Tri-state	H/L	Prev.	Prev.
PB-1	90				H8_SCI	Tri-state	H/L	Prev.	Prev.
PB-2	81				PWRON_5V	Tri-state	H/L	Prev.	Prev.
PB-3	80				USB_HDD_IC_RST	Tri-state	H/L	Prev.	Prev.
PB-4	69				LEARNING	Tri-state	H/L	Prev.	Prev.

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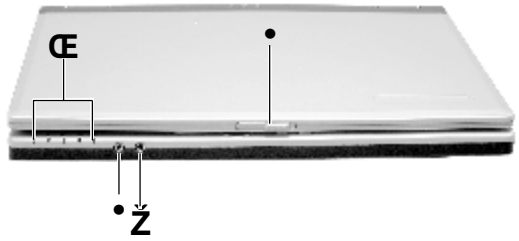
Port/Pin	Pin Number	HIF disable	HIF enable	Flash Memory PROM Mode	Mitac definition function	During Reset	Normal Operation	Sleep Mode	Software Standby Mode
PB-5	68				CHARGING	Tri-state	H/L	Prev.	Prev.
PB-6	58				USB_HDD_POWER	Tri-state	H/L	Prev.	Prev.
PB-7	57				USB_IC_POWER#	Tri-state	H/L	Prev.	Prev.
NMI#	7				H8_POWERBTN#				
STBY#	8				H8_STBY#				

2. System View and Disassembly

2.1 System View

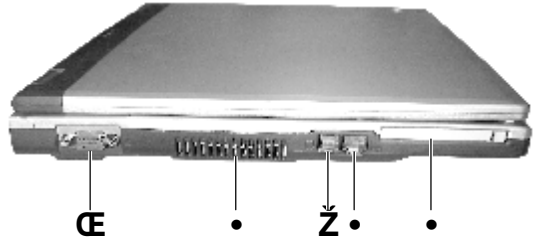
2.1.1 Front View

Œ Device LED indicator
• Line Out Phone Jack
Ž External Microphone Jack
• Top Cover Latch



2.1.2 Left-side View

Œ VGA Port
• Ventilation Openings
Ž RJ-11 Connector
• RJ-45 Connector
• PC Card Slot

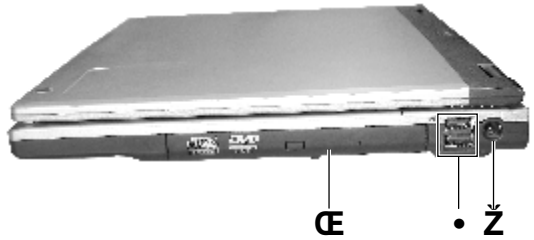


2.1.3 Right-side View

Œ CD-ROM/DVD-ROM Drive

• USB Ports *2

Ž Power Connector



2.1.4 Rear View

Œ USB Ports *2

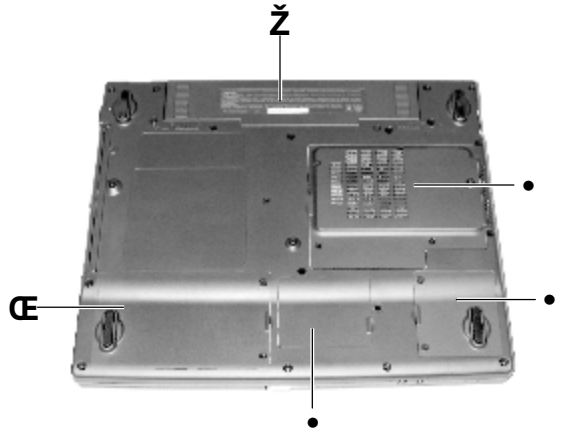
• Kensington Lock

8381 N/B Maintenance

2.1.5 Bottom View

Œ Hard Disk Drive
- Modem Card

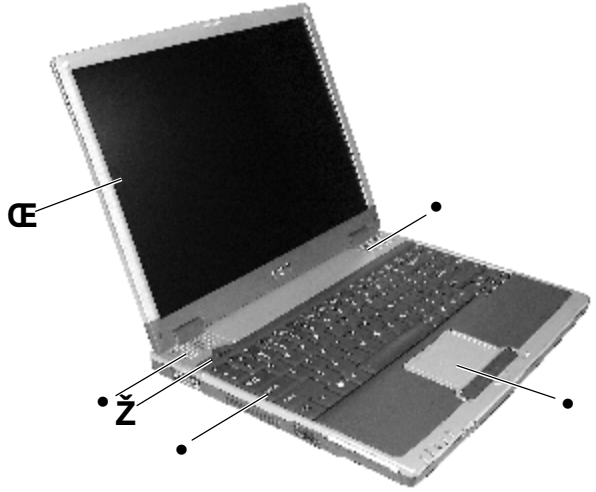
Ž Battery Park
- CPU
- Wireless Card



2.1.6 Top-open View

Œ LCD Screen
- Stereo Speaker Set

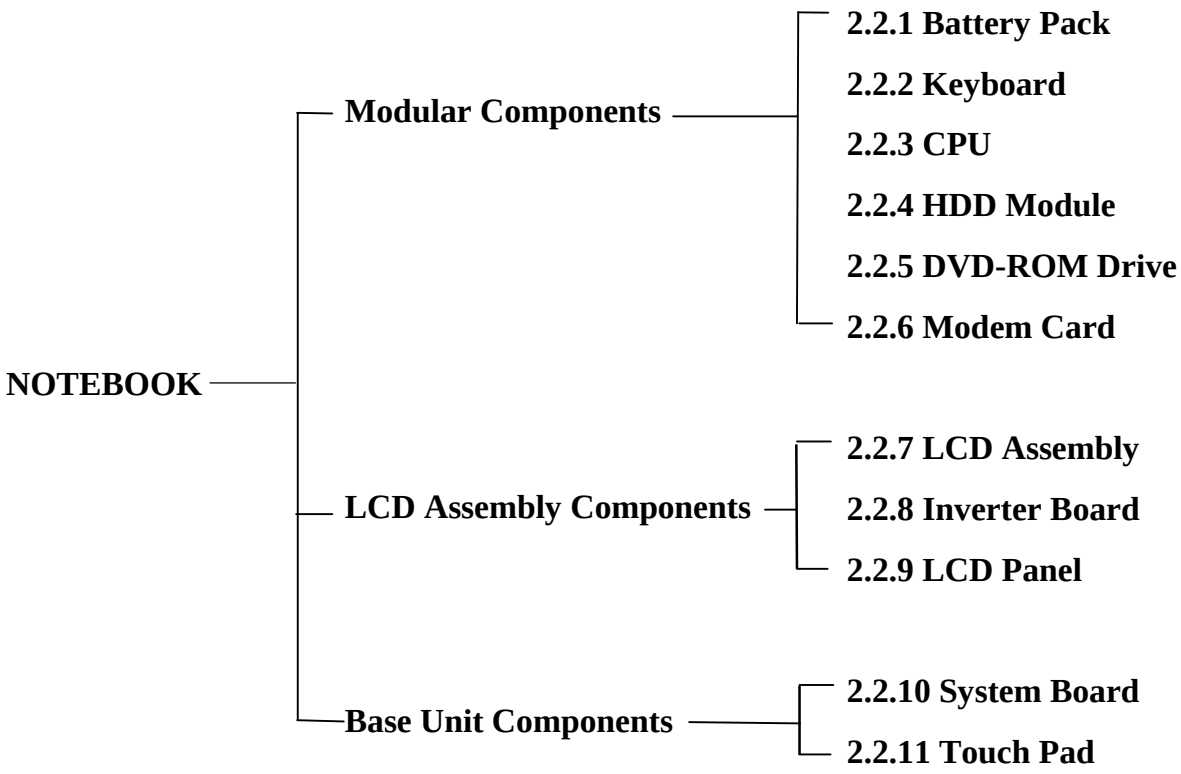
Ž Power Button
- Keyboard
- Touch Pad



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the left release lever to the "unlock" ( ) position (), then sliding and holding the right release lever outwards while take the battery pack out of the compartment (•). (Figure 2-1)

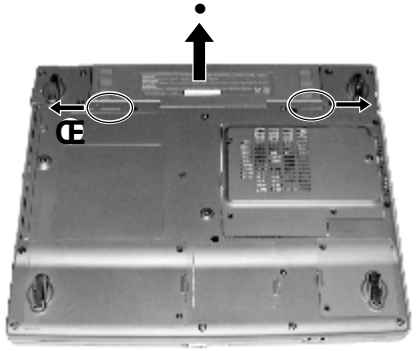


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove one screw and open the top cover.(Figure 2-2)
3. Remove the keyboard cover.(Figure 2-3)

Figure 2-2 Remove one screw

Figure 2-3 Remove the keyboard cover

4. Remove three screws that secure the keyboard cover and Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board to detach the keyboard. (Figure 2-5)

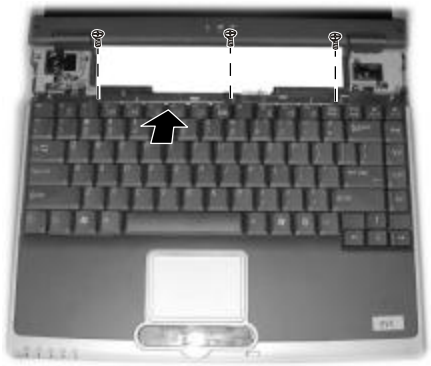


Figure 2-4 Remove three screws

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back.
2. Replace the keyboard into place with three screws.
3. Replace the keyboard cover into place with one screw.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove four screws fastening the heatsink cover. (Figure 2-6)
3. Remove four spring screws that secure the heatsink upon the CPU. (Figure 2-7)

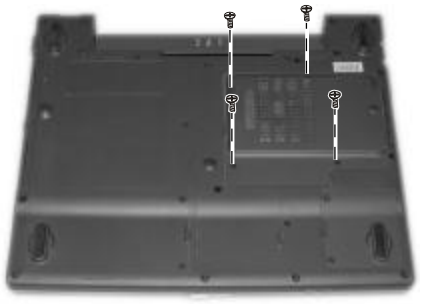


Figure 2-6 Remove four screws

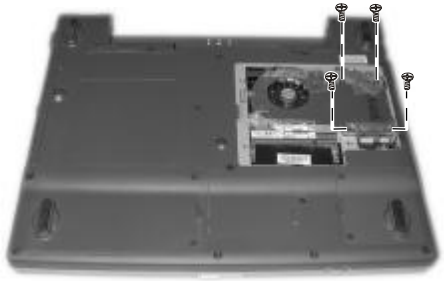


Figure 2-7 Remove four screws

4. Disconnect the fan's power cord from system board. (Figure 2-8)
5. Then insert a minus screwdriver 101 (JIS standard) into the "OPEN" hole of the socket, and push the screwdriver toward the CPU to free the CPU. Now you can take out the CPU from the socket. (Figure 2-9)

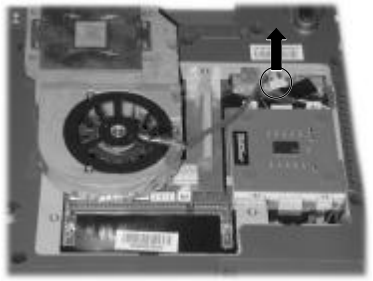


Figure 2-8 Remove the fan's power cord

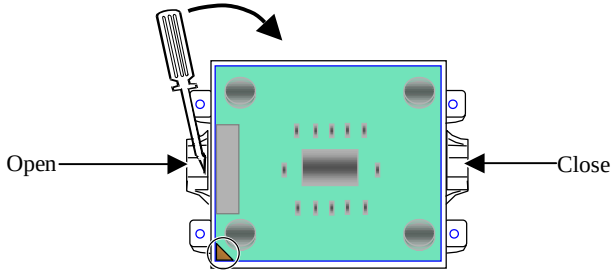


Figure 2-9 Remove the CPU socket

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket, and insert the CPU pins into the holes. Fit the CPU socket stopper. Insert the flat screwdriver into the "CLOSE" hole of the socket, and push the screwdriver toward the CPU to secure the CPU in place.
2. Reconnect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the CPU compartment cover and secure with four screws.
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-10)
3. Slide the HDD module out of the compartment. (Figure 2-11)

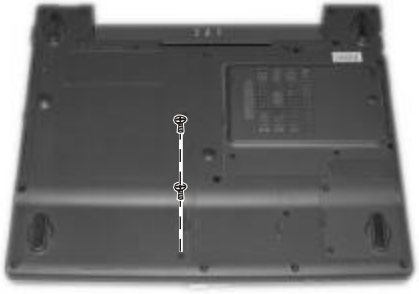


Figure 2-10 Remove the HDD compartment cover

Figure 2-11 Remove HDD module

4. Remove four screws to To separate the hard disk drive from the bracket, remove four screws. (Figure 2-12)

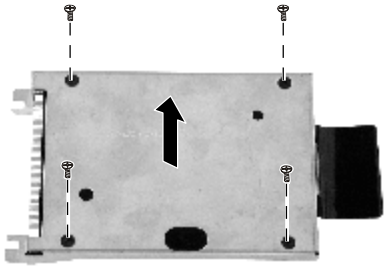


Figure 2-12 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the CD/DVD-ROM drive. (Figure 2-13)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (Œ) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(•). (Figure 2-14)

Figure 2-13 Remove two screws

Figure 2-14 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with two screws.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the modem card. (Figure 2-15)
3. Lift up the modem card and disconnect the cord. (Figure 2-16)

Figure 2-15 Remove two screws

Figure 2-16 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard, hard disk drive . (See sections 2.2.1,2.2.2 , 2.2.4 Disassembly)
2. Remove the twenty two screws fastening the housing. (Figure 2-17)
3. Remove the two screws fastening the Mini PCI compartment cover (Figure 2-18)

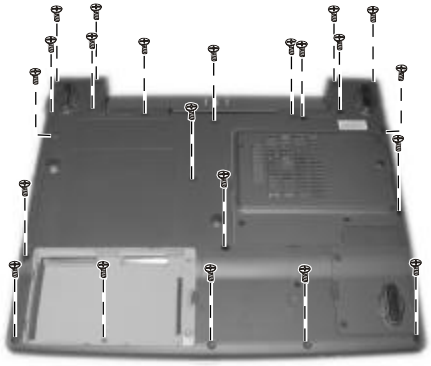


Figure 2-17 Remove twenty two screws

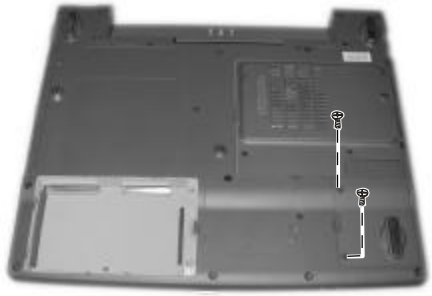


Figure 2-18 Remove two screws

4. Detach the antennae. (Figure 2-19)
5. Remove the two screws that secure the hinge cover (Figure 2-20)

Figure 2-19 Disconnect the antennae

Figure 2-20 Remove two screws

6. Remove the two rear covers. (Figure 2-21)
7. Remove three screws. And disconnect the touch pad's cable. Then separate the top cover. (Figure 2-22)

Figure 2-21 Remove two rear covers

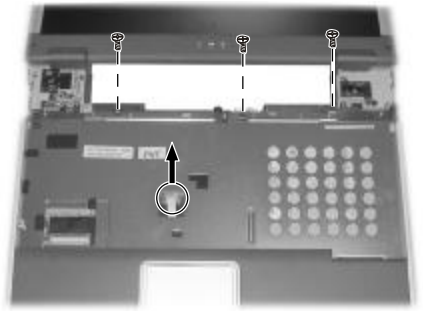


Figure 2-22 Remove the top cover

8. Remove the two hinge covers and disconnect two cables. (Figure 2-23)
9. Remove four screws. (Figure 2-24)

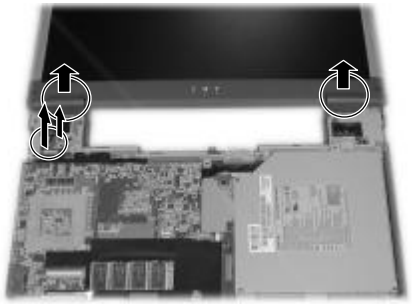


Figure 2-23 Remove two hinge covers

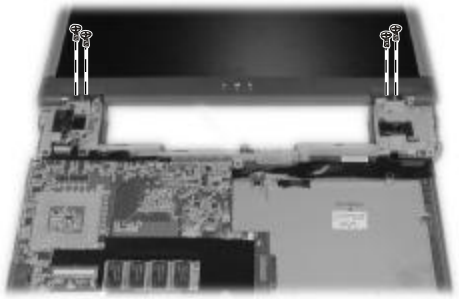


Figure 2-24 Remove four screws

10. Remove four screws fastening the system board into housing. Then lift up the system board. Peel off the antenna cord. Then detach the LCD ASSY. (Figure 2-25)

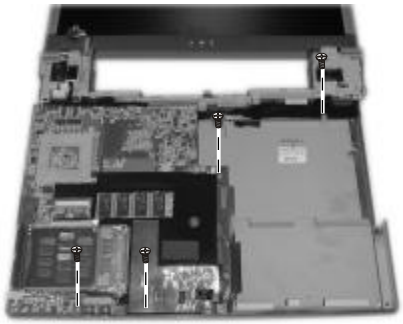


Figure 2-25 Remove four screws

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna cord.
3. Replace the system board into housing and secure with four screws.
4. Reconnect the two cables to the system board. Screw the hinge covers by two screws.
5. Replace the top cover and secure with three screws. And reconnect the touch pad's cable.
6. Replace the rear cover.
7. Upside down the notebook. The replace the housing and secure with twenty two screws.
8. Replace the antenna. And Secure the Mini PCI compartment cover by two screws.
9. Replace the ,CD/DVD-ROM drive, hard disk drive, keyboard and battery pack. (Refer to sections 2.2.5, 2.2.4, 2.2.2 and 2.2.1 Reassembly)

2.2.8 Inverter Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.2.1 2.2.2, 2.2.4, 2.2.5 and 2.2.7 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-26)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the two screws fastening the inverter board. (Figure 2-27)

Figure 2-26 Remove LCD cover

Figure 2-27 Remove the inverter board

5. To remove the inverter board on the lower part of the LCD housing , disconnect two cables. (Figure 2-28)

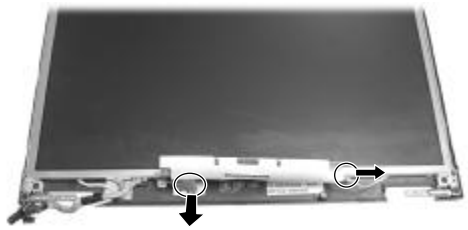


Figure 2-28 Remove the inverter board

Reassembly

1. Reconnect the cables. Fit the inverter board back into place and secure with two screw.
2. Replace the LCD cover and secure with two screws and rubber pads.
3. Replace the LCD assembly. (Refer to section 2.2.7 Reassembly)
4. Replace the CD/DVD-ROM drive, hard disk drive, keyboard and battery pack. (Refer to sections 2.2.5, 2.2.4, 2.2.2 and 2.2.1 Reassembly)

2.2.9 LCD Panel

Disassembly

1. Remove the battery, keyboard, hard disk drive ,CD/DVD-ROM drive and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.4, 2.2.5 and 2.2.7 Disassembly)
2. Remove the LCD cover. (Refer for two steps 2,3 of section 2.2.8 Disassembly)
3. Remove six screws fastening the LCD panel. And lift it up. (Figure 2-29)
4. To remove the inverter board on the lower part of the LCD housing , Detach two cables. (Figure 2-30)

Figure 2-29 Remove the LCD panel

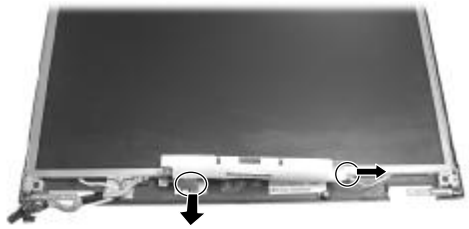


Figure 2-30 Remove the inverter board

5. Remove the four screws to free the LCD panel. (Figure 2-31)

Figure 2-31 Free the LCD panel

Reassembly

1. Attach the LCD panel's bracket back to LCD panel and secure with four screws.
2. Replace the LCD panel into place.
3. Reconnect two cables to inverter board and secure with two screws.
4. Fasten the LCD panel by six screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, CD/DVD-ROM drive, hard disk drive, keyboard, battery pack. (See sections 2.2.7 2.2.5, 2.2.4, 2.2.2 and 2.2.1 Reassembly)

2.2.10 System Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CPU, CD/DVD-ROM drive and modem card. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6 Disassembly)
2. Remove the top cover approach the system board. (Refer to steps 1-7 of section 2.2.7 Disassembly)
3. Remove four screws that secure the system board into housing. Then lift it up form the housing. (Figure 2-32)

Figure 2-32 Remove four screws

4. Remove two hex nuts and disconnect two speaker's cords from system board. Then separate the bracket.(Figure 2-33)
5. Carefully put the system board upside down. And remove one screw. (Figure 2-34)

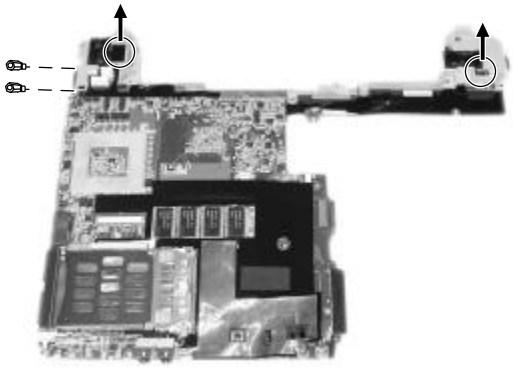


Figure 2-33 Remove two hex nuts

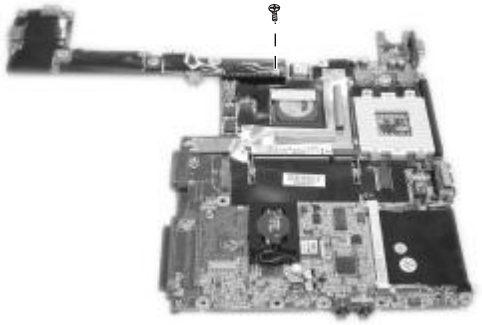


Figure 2-34 Remove the bracket

6. Separate the D/D board from system board. ((See the bracket (Figure2-33) Disassembly) Figure 2-35))

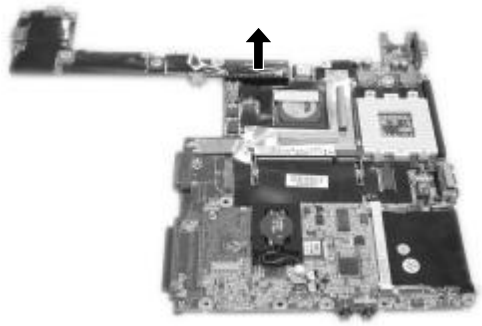


Figure 2-35 Free the system board

Reassembly

1. Replace the D/D board to the system board and secure with one screw.
2. Fit the bracket and secure with two hex nuts.
3. Turn over the system board. Reconnect the speaker’s cords.
4. Replace the system board back into the housing and secure with four screws .
5. Replace the LCD assembly, CD/DVD-ROM, HDD, keyboard and battery pack. (Refer to previous section Reassembly)

2.2.11 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, hard disk drive. (See sections 2.2.1,2.2.2 and 2.2.4 Disassembly)
2. Remove the top cover. (See steps 1-7 in section 2.2.7 Disassembly)
3. Disconnect the cable. (Figure 2-36)
4. Touch Pad can't be taken apart from Top Cover. It is necessary to replace the Top Cover, if defect.

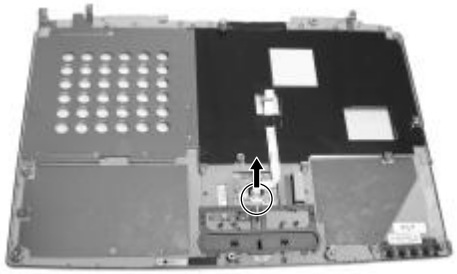


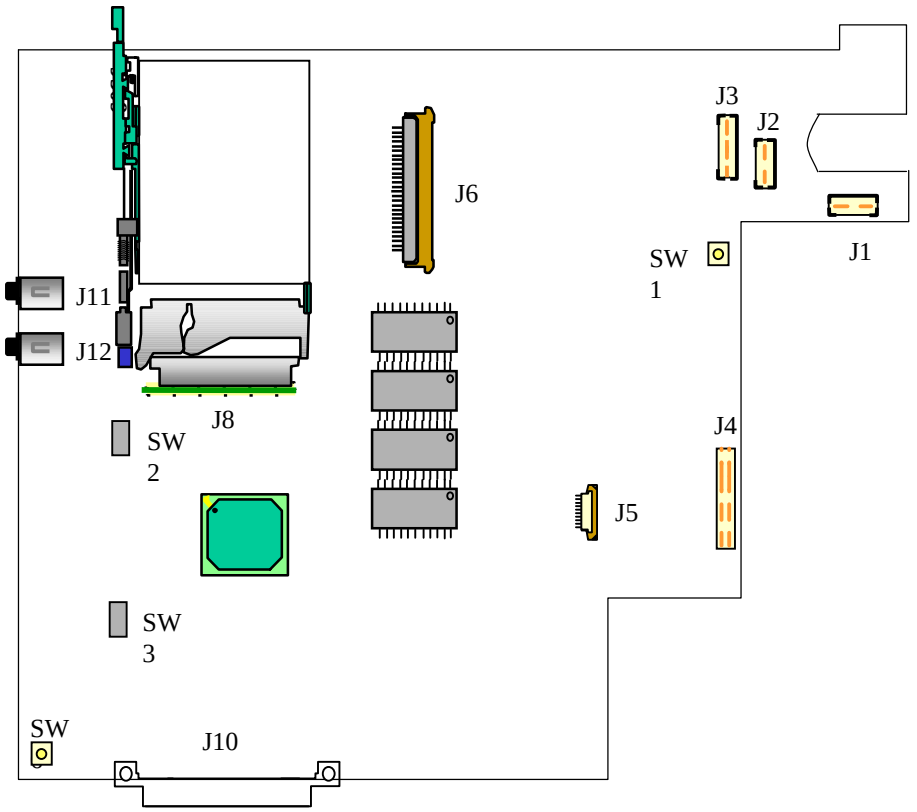
Figure 2-36 Disconnect the cable

Reassembly

1. Reconnect the cable.
2. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A

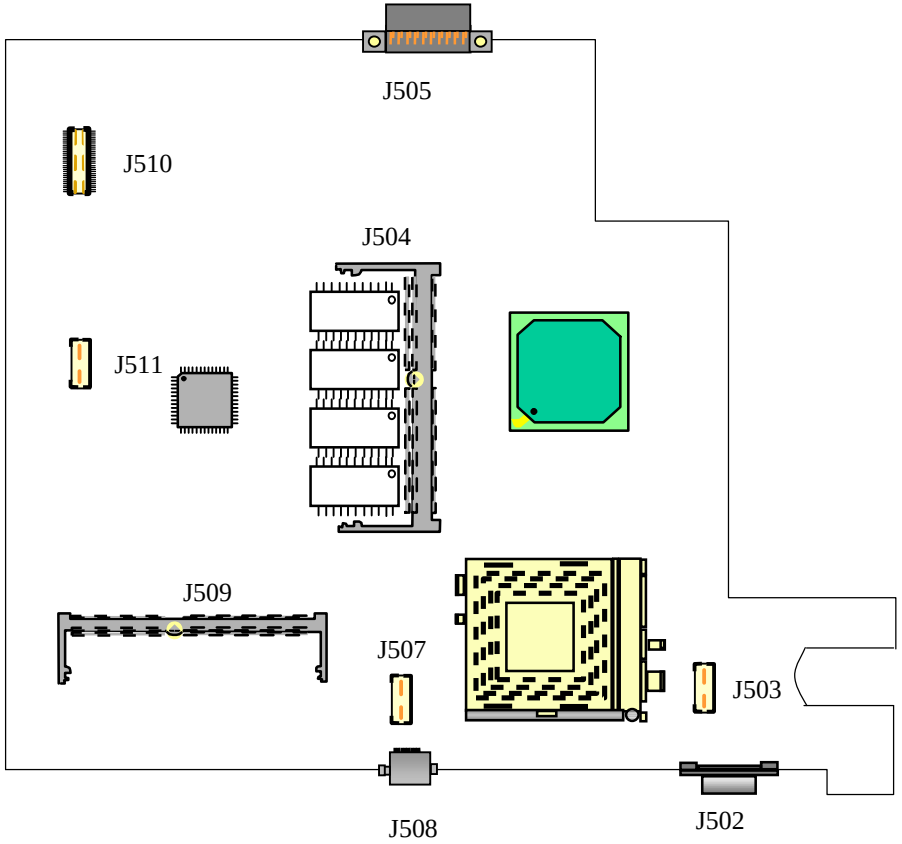


- J1 : Left Internal Speaker Connector
- J2 : LCD Inverter Board Connector
- J3 : LCD Connector
- J4 : D/D Board Connector
- J5 : Touch Pad Connector
- J6 : Key Board Connector
- J8 : PCMCIA Socket
- J10 : HDD Connector
- J11 : Line Out
- J12 : MIC In

- SW1 : Power Button
- SW2 : Touch Pad Left Button
- SW3 : Touch Pad Right Button
- SW6 : Cover Switch

3. Definition & Location of Connectors / Switches

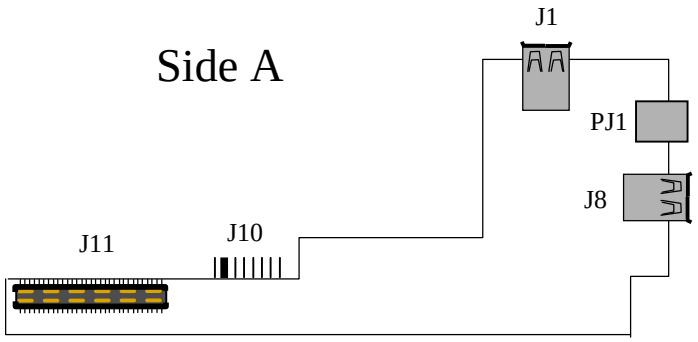
3.2 Mother Board-B



- **J502 : VGA Connector**
- **J503 : CPU FAN Connector**
- **J504 : Extended Memory Connector**
- **J505 : CDROM Connector**
- **J507 : MDC Jump wire Connector**
- **J508 : RJ45 & RJ11 Connector**
- **J509 : Mini PCI Connector**
- **J510 : Transform Board Connector(MDC)**
- **J511 : RTC Battery Connector**

3. Definition & Location of Connectors / Switches

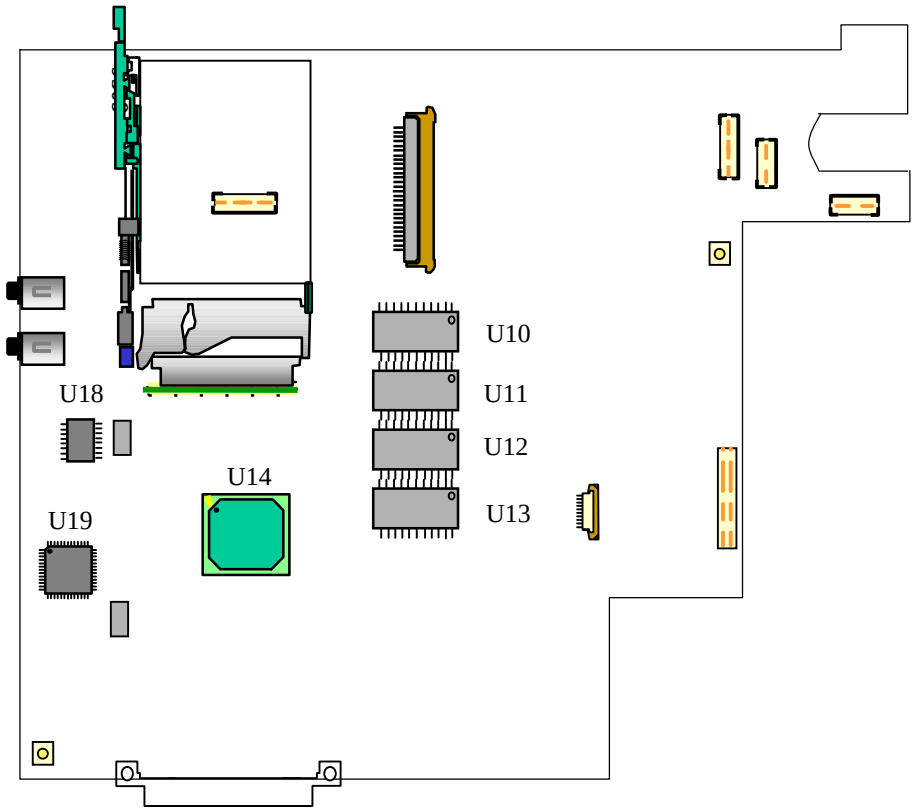
3.3 Charge Board



- **J1 ,J8 : USB Connector**
- **J10 : Battery Connector**
- **J11 : D/D Board to M/B Connector**
- **PJ1 : Power Jack**

4. Definition & Location of Major Components

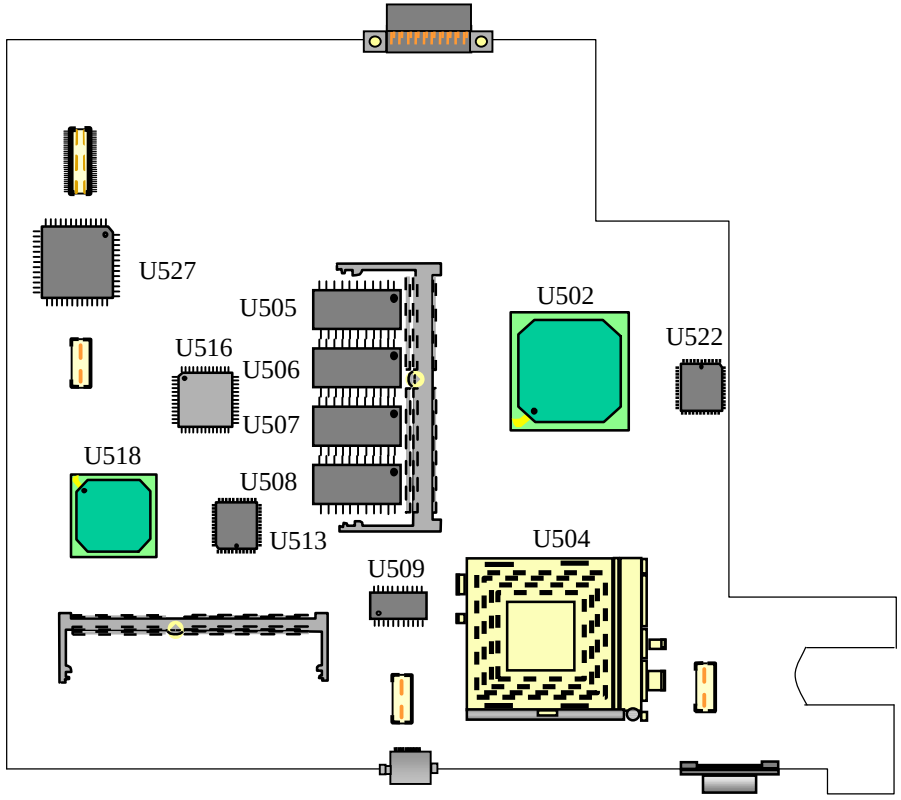
4.1 Mother Board-A



- **U10 : On Board DDR RAM**
- **U11 : On Board DDR RAM**
- **U12 : On Board DDR RAM**
- **U13 : On Board DDR RAM**
- **U14 : VT8235 (South Bridge)**
- **U18 : TPA0212 (Audio Amplifier)**
- **U19 : ALC201 (AC'97 CODEC)**

4. Definition & Location of Major Components

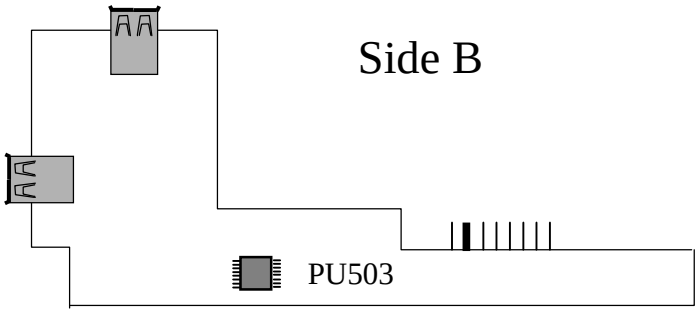
4.2 Mother Board-B



- **U502 : VT8372(North Bridge)**
- **U504 : CPU Socket (Mobile Athlon XP)**
- **U505 : On Board DDR RAM**
- **U506 : On Board DDR RAM**
- **U507 : On Board DDR RAM**
- **U508 : On Board DDR RAM**
- **U509 : ICS950902 (Clock Generator)**
- **U513 : VT6103 (LAN PHY)**
- **U516 : H82140B**
- **U518 : PCI1510 (Card Bus Controller)**
- **U522 : SYSTEM BIOS**
- **U527 : UPD720180 (USB HDD Controller)**

4. Definition & Location of Major Components

4.3 Charge Board



- **PU503 :TL594C Pulse-Width-Modulation Controller**

5. Pin Descriptions of Major Components

5.1 Mobile AMD Athlon XP Processor Model 8

Detailed Pin Descriptions

Name	Description
A20M# Pin	A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.
AMD Pin	AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.
AMD Athlon™ System Bus Pins	See the *AMD Athlon™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.
Analog Pin	Treat this pin as a NC.
APIC Pins, PICCLK, PICD[1:0]#	The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. The pin, PICCLK, must be driven with a valid clock input.
CLKFWDRST Pin	CLKFWDRST resets clock-forward circuitry for both the system and processor.
CLKIN, RSTCLK (SYSCLK) Pins	Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.
CONNECT Pin	CONNECT is an input from the system used for power management and clock-forward initialization at reset.
COREFB and COREFB# Pins	COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.
CPU_PRESENCE# Pin	CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.
DBRDY and DBREQ# Pins	DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.
FERR Pin	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

Detailed Pin Descriptions Cotinue

Name	Description
FLUSH# Pin	FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
IGNNE# Pin	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
INIT# Pin	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0_FFFF_FFF0h.
INTR Pin	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
JTAG Pins	TCK, TMS, TDI, TRST#, and TDO are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pull TDI, TCK, TMS, and TRST# up to VCC_CORE with pullup resistors.
K7CLKOUT and K7CLKOUT# Pins	K7CLKOUT and K7CLKOUT# are each run for two to three inches and then terminated with a resistor pair: 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.
Key Pins	These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.
NC Pins	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
NMI Pin	NMI is an input from the system that causes a non-maskable interrupt.
PGA Orientation Pins	No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.
PLL Bypass and Test Pins	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

5.1 Mobile AMD Athlon XP Processor Model 8

Detailed Pin Descriptions Cotinue

Name	Description
FID[3:0] Pins	FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio. **FID[3:0] Clock Multiplier Encodings** **FID[3:0][2] — Processor Clock to SYSCLK Frequency Ratio** 0000 — 11 0001 — 11.5 0010 — 12 0011 — ≥12.5[1] 0100 — 5 0101 — 5.5 0110 — 6 0111 — 6.5 1000 — 7 1001 — 7.5 1010 — 8 1011 — 8.5 1100 — 9 1101 — 9.5 1110 — 10 1111 — 10.5 ***Notes:*** *1. All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011b, which causesthe SIP configuration for all ratios of 12.5x or greater to be the same.* *2. BIOS initializes the CLK_Ctl MSR during the POST routine. This CLK_Ctl setting is used with all FID combinations and selects a Halt disconnect divisor and a Stop Grant disconnect divisor. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.* The FID[3:0] signals are open-drain processor outputs that are pulled High on the motherboard and sampled by the chipset to determine the SIP (Serialization Initialization Packet) that is sent to the processor. The FID[3:0] signals are valid after PWROK is asserted. The FID[3:0]signals must not be sampled until they become valid. See the *AMD Athlon™ System Bus Specification*, order# 21902 for more information about Serialization Initialization Packets and SIP protocol. The processor FID[3:0] outputs are open-drain and 2.5 V tolerant. To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor. For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

Detailed Pin Descriptions Cotinue

Name	Description
PLL Bypass and Test Pins	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.
PWROK Pin	The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.
SADDIN[1:0]# and SADDOUT[1:0]# Pins	The AMD Athlon XP processor model 8 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ System Bus Specification*, order# 21902.
Scan Pins	SCANSHIFTEN, SCANCLK1, SCANINTEVAL, and SCANCLK2 are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.
SMI# Pin	SMI# is an input that causes the processor to enter the system management mode.
STPCLK# Pin	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
SYSCLK and SYSCLK#	SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator.
THERMDA and THERMDC Pins	Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system.
VCCA Pin	VCCA is the processor PLL supply.
VREFSYS Pin	VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.
ZN and ZP Pins	ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z0 of the transmission line.

5.1 Mobile AMD Athlon XP Processor Model 8

Detailed Pin Descriptions Cotinue

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>VID[4:0] Pins</td><td>The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC_CORE DC/DC converter.
VID[4:0] Code to Voltage Definition
<table>
<tr><th>VID[4:0]</th><th>VCC_CORE (V)</th><th>VID[4:0]</th><th>VCC_CORE (V)</th></tr>
<tr><td>00000</td><td>1.850</td><td>10000</td><td>1.450</td></tr>
<tr><td>00001</td><td>1.825</td><td>10001</td><td>1.425</td></tr>
<tr><td>00010</td><td>1.800</td><td>10010</td><td>1.400</td></tr>
<tr><td>00011</td><td>1.775</td><td>10011</td><td>1.375</td></tr>
<tr><td>00100</td><td>1.750</td><td>10100</td><td>1.350</td></tr>
<tr><td>11101</td><td>1.725</td><td>10101</td><td>1.325</td></tr>
<tr><td>00111</td><td>1.675</td><td>10111</td><td>1.275</td></tr>
<tr><td>01000</td><td>1.650</td><td>11000</td><td>1.250</td></tr>
<tr><td>01001</td><td>1.625</td><td>11001</td><td>1.225</td></tr>
<tr><td>01010</td><td>1.600</td><td>11010</td><td>1.200</td></tr>
<tr><td>01011</td><td>1.575</td><td>11011</td><td>1.175</td></tr>
<tr><td>01100</td><td>1.550</td><td>11100</td><td>1.150</td></tr>
<tr><td>01101</td><td>1.525</td><td>11101</td><td>1.125</td></tr>
<tr><td>01110</td><td>1.500</td><td>11110</td><td>1.100</td></tr>
<tr><td>01111</td><td>1.475</td><td>11111</td><td>NO CPU</td></tr>
</table>
For more information, see the “Required Circuits” chapter of the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363.</td></tr>
</table>

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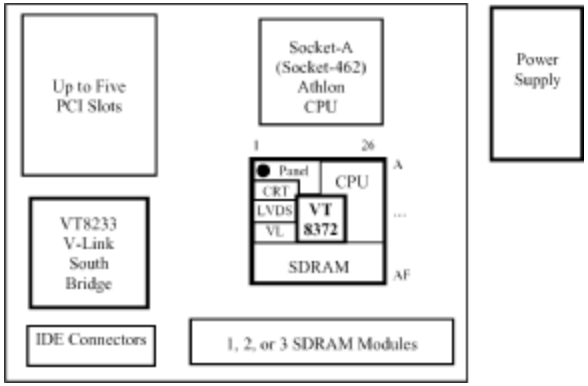
5.2 VIA VT8372 North Bridge with S3 ProSavage8 AGP8X

CPU Interface

Signal Name	Pin #	I/O	Signal Description
CFWDRST	D14	O	CLK Forward Reset.Reset the clock forward circuitry for the Athlon .interface.
CONNECT	C14	O	Connect.Used for power anagement and CLK-forward initialization at reset.
PROCRDY	E14	I	Processor Ready.Used for power anagement and clock-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	Host CPU Address /Command Output.Unidirectional syste address /com and interface to the processor from the system controller.It is used to transfer probes or data ovement com ands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]#is skew-aligned with the forward clock,AINCLK#
AINCLK#	B15	O	Host CPU Address Output Clock.Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the syste controller.Both rising and falling edges are used to transfer addresses or com ands to the processor.
AOUT[14-2]#	(see pin list)	I	Host CPU Address Input.Unidirectional system address /command interface from the processor to the system controller.It is used to transfer processor com ands or probes responses to the syste controller.AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	R25	I	Host CPU Address Input Clock.Single-ended forwarded clock for the AOUT[14:bus that is driven by the processor.Both rising and falling edges are used to transfer com ands or probe responses.
D[63-0]#	see pin list)	IO	Host CPU Data.Bi-directional interface between the processor and the system controller for data movement. D[63:0]#bus is skew-aligned with either the DICLK[3:0]#or DOCLK[3:0]#forward clocks.
DICLK[3-0]#	L24,G23, A24,A19	O	Host CPU Data Input Clock. Single-ended forwarded clocks for the D[63:0]#bus, driven by the syste controller to the processor.Each 16-bit data word is skew-aligned with one of these clocks.Both rising and falling edges are used to transfer data to the pocessor.
DOCLK[3-0]#	L22,F23, B24,C19	I	Host CPU Data Output Clock.Single-ended forwarded clocks for the D[63:0]#bus, driven by the processor to the system controller.Each 16-bit data word is skew-aligned with one of these clocks.Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E13	O	HostCPUDataReadInVald.Driven by the syste controller to control the flow of data into the processor.DINVAL#can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7,	AC1	IO	Address/Data Bus. SB Strap Function Setting (L=strap low,H=strap high) Register Pin
VAD6 /strap	AB4	IO	VAD6 Auto-Configure L=Disable (use on-chip defaults) H=Enable (get from ROM) SDA2
VAD5 /strap,	Y2	IO	VAD5 CPU Clock Divide Bit-3 (see register description) Rx97[6] SDA1
VAD4 /strap,	AC2	IO	VAD4 CPU Clock Divide Bit-2 (see register description) Rx97[5] SDA0
VAD3 /strap,	Y1	IO	VAD3 CPU Clock Divide Bit-1 (see register description) Rx97[4] SA19
VAD2 /strap,	AA4	IO	VAD2 CPU Clock Divide Bit-0 (see register description) Rx97[3] SA18
VAD1 /strap,	W5	IO	VAD1 FSB Clock Speed Msb LL=66,LH=100, SA17
VAD0 /strap	W4	IO	VAD0 FSB Clock Speed Lsb HL=HH=133 MHz SA16
VBE#	Y3	IO	Byte Enable.
VUPCMD	Y4	I	Command from Client-to-Host.
VUPSTB	AA1	I	Strobe from Client-to-Host.
VUPSTB#	AA2	I	Complement Strobe from Client-to-Host.
VDNCMD	AB3	O	Command from Host-to-Client.
VDNSTB	AB1	O	Strobe from Host-to-Client.
VDNSTB#	AB2	O	Complement Strobe from Host-to-Client.

5.2 VIA VT8372 North Bridge with S3 ProSavage8 AGP8X

DRAM Interface

Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	IO	Memory Data.These signals are connected to the DRAM data bus. Output drive strength ay be set by Device 0 Rx6D[1-0].
MA[14:0]	AB19,AB18,AF17, AC9,AB10,AC17,A E17,AC18,AB15,AB 17,AB16,AB14,AC1 2,AB12,AC11	O	Memory Address.DRAM address lines.Output drive strength may be set by Device 0 Rx6C[7-6].
CS[5:0]#	AD5,AB7,AB6, AC6,AC5,AD6	O	Chip Select.Chip select of each bank.Output drive strength aybe set by Device 0 Rx6D[3-2].
DQM[7:0]	AF4,AB8,AF12, AE15,AF19,AD22,A D25,Y26	O	Data Mask.Data ask of each byte lane.Output drive strength may be set by Device 0 Rx6D[5-4].
DQS[7:0]#	AD4,AC8,AE12, AF15,AD19,AF22,A D26,Y24	IO	DDR Data Strobe.Data strobe of each byte lane.Output drive strength ay be set by Device 0 Rx6C[3-2].
SRASA#, SRASB#/CK E5, SRASC#/CK E4	AB11 AF24 AB20	O	Row Address Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
SCASA#, SCASB#/CK E3, SCASC#/CK E1	AD7 AC24 AD24	O	Column Address Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
SWEA#, SWEB#/CKE 2, SWEC#/CKE 0	AB9 AB22 AC21	O	Write Enable Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
CKE5 /SRASB#, CKE4 /SRASC#, CKE3 /SCASB#, CKE2 /SWEB#, CKE1 /SCASC#, CKE0 /SWEC#	AF24 AB20 AC24 AB22 AD24 AC21	O	Clock Enables.Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat /temperature in high-speed e ory systems. See Device 0 Rx6B[4].

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description
HCLK	G21	I	Host Clock. This pin receives the host CPU clock (100 /133 MHz).This clock is used by all TwisterK-DDR logic that is in the host CPU domain.
HCLK#	F22	I	Host Clock Complement. HCLK inverted. Used for Quad Data Transfer on host CPU bus.
MCLK	Y22	O	Memory (SDRAM)Clock. Output from internal clock generator to the external clock buffer.
MCLKFB	AA23	I	Memory (SDRAM)Clock Feedback. Input from the external clock buffer.
DCLKI	D5	I	Dot Clock (Pixel Clock)In. Used for external EMI reduction circuit if used. Loop back from DCLKO if external EMI reduction circuit not implemented.
DCLKO	C5	O	Dot Clock (Pixel Clock)Out. Used for external EMI reduction circuit if used. Loop back to DCLKI if external EMI reduction circuit not implemented.
GCLK	V5	I	Graphics Clock.
XIN	E6	I	Reference Frequency Input. An external 14.31818 MHz clock source is normally connected to this pin. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.
RESET#	AE1	I	Reset. Input from the South Bridge chip. When asserted, this signal resets Twister K-DDR and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD1	I	Power OK. Connect to South Bridge and Power Good circuitry.
SUSST#	AD2	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pull up to disable.
SUSPEND	B1	I	Suspend. Used to put the integrated graphics controller into suspend state.
STNDBY	E4	I	Standby. Used to put the integrated graphics controller into standby state.
GPOUT /STRW	E7	O	General Purpose Output. This pin reflects the state of SRD[0].
GOP0	D10	O	General Output Port. When SR1A[4]is cleared, this pin reflects the state of CR5C[0].
STRW /GPOUT	E7	O	
INTA#	F6	O	Interrupt. PCI interrupt output (handled by the interrupt controller in the South Bridge)

5.2 VIA VT8372 North Bridge with S3 ProSavage8 AGP8X

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test Continue

Signal Name	Pin #	I/O	Signal Description
BISTIN	A5	I	BIST In. This pin is used for testing and must be left unconnected or tied high on all board designs.
TESTIN	F12	I	Test In.
TEST[7:0]	E2,E1,D3,D2, D1,C2,C1,E3		Test Data.

LCD Panel /Flat Panel Monitor (DVI) Interface

Signal Name	Pin #	I/O	Signal Description
FPD11 /TVBL#, FPD10 /TVD10, FPD9 /TVD9, FPD8 /TVD8, FPD7/TVD7/strap, FPD6 /TVD6/strap, FPD5 /TVD5/strap, FPD4 /TVD4/strap, FPD3 /TVD3/strap, FPD2 /TVD2/strap, FPD1 /TVD1/strap, FPD0 /TVD0/strap	A7 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	Panel Data.Default output drive is 8 a.16 a ay be selected via SR3D[6]=1. Panel data is selected for output on these pins when SR31[4]=1.TV Encoder outputs are uxed on the FPD[11:0]pins (see the TV Encoder Interface pin list for details). FPD[7:0]are also used for power-up /reset straps for the internal graphics controller logic (see Table 10 in the Functional Description section of this data sheet for details). Internally pulled down during reset for strap default of 0. FPD0 /strap PCI Interrupt CR36[0] 1 =Enable FPD1 /strap IO Disable CR36[4] 1 =Enable FPD2 /strap PCI Base Address Mapping CRB0[7] 0 =Map1, 1 =Map0 FPD3 /strap -reserved- FPD4 /strap OEM Defined Panel Type bit-0 CRF0[0] FPD5 /strap OEM Defined Panel Type bit-1 CRF0[1] FPD6 /strap OEM Defined Panel Type bit- 2 CRF0[2] FPD7 /strap OEM Defined Panel Type bit-3 CRF0[3]
FPVS /TVVS	B11	O	Panel VSYNC. Internally pulled down.
FPHS /TVHS	B10	O	Panel HSYNC. Internally pulled down.
FPDE /TVCLKI	A10	O	Panel Data enable. Internally pulled down.
FPCLK /TVCLKO	D8	O	Panel Clock. Internally pulled down during reset.8Ma is the default.16Ma ay also be selected.
FPDET /TV11	A11	I	Panel Detect. If SR30[1]=0,SR30[2]will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
ENVDD	F3	O	Enable VDD. This signal is driven high to external logic to initiate a flat panel power up sequence.
ENVEE	F1	O	Enable VEE. This signal is driven high to a program able time after ENVDD is driven high during a flat panel power up sequence.

CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR	A3	A	Analog Red.Analog red output to the CRT onitor.
AB	B3	A	Analog Blue.Analog blue output to the CRT onitor.
AG	A2	A	Analog Green.Analog green output to the CRT onitor.
HSYNC	B6	O	Horizontal Sync.Output to CRT.
VSYNC	A6	O	Vertical Sync.Output to CRT.
RSET	B5	A	Reference Resistor.Tie to GNDRGB through an external 140 .resistor to control the RAMDAC full-scale current value.

TV Encoder Interface

Signal Name	Pin #	I/O	Signal Description
TVD11 /FPDET, TVD10 /FPD10, TVD9 /FPD9, TVD8 /FPD8, TVD7 /FPD7 /strap, TVD6 /FPD6 /strap, TVD5 /FPD5 /strap, TVD4 /FPD4 /strap, TVD3 /FPD3 /strap, TVD2 /FPD2 /strap, TVD1 /FPD1 /strap, TVD0 /FPD0 /strap	A11 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	TV Encoder Data.Internally pulled down during reset
TVCLKI /FPDE	A10	I	TV Encoder Clock In. Input clock from encoder. Internally pulled down.
TVCLKO /FPCLK	D8	O	TV Encoder Clock Out. Output clock to TV encoder. Internally pulled down.
TVHS /FPHS	B10	O	TV Encoder HSYNC. Internally pulled down during reset
TVVS /FPVS	B11	O	TV Encoder VSYNC. Internally pulled down during reset
TVBL#/FPD11	A7	O	TV Encoder Blanking. Internally pulled down during reset

5.2 VIA VT8372 North Bridge with S3 ProSavage8 AGP8X

Power,Ground,and Test

Signal Name	Pin #	I/O	Signal Description
VTT	J13-J18,K18,L18, M18,N18,P18,R18	P	Power for CPU I/O Interface Logic. Voltage is CPU dependent. See also VID (Voltage ID)pin.
VID#	E10v	I	Voltage ID.CPU FSB interface voltage select.0 =desktop,1=mobile.
VCCS2K	M21	P	S2K Bus Interface Power.(2.5V ±5%)
GNDS2K	K21	P	S2K Bus Ground. Connect to main ground plane.
S2KCOMP	L21	I	S2K Bus Compensation. Connect to 70 ？1%resistor to ground.
S2KVREF	F17,N21	P	S2K Bus Voltage Reference.碾TT derived using 100 ？1%+100 ？1% resistive voltage divider. See TwisterK-DDR Design Guide.
VCCM	T18,U18,V9-V18, AA7,AA17,AA21	P	Power for Memory I/O Interface Logic (2.5 ±5%).
MEMVREF	AA10,AA18	P	Memory Voltage Reference.
VCCVL	T9,U9,Y6,AA6	P	Power for V-Link I/O Interface Logic (2.5V ±5%).
VLCOMP	AB5	I	Vlink P-Channel Compensation. Connect 70 ？1%resistor to ground.
VLVREF	Y5	P	V-Link Voltage Reference.1.0V derived using a resistive voltage divider between VCC25 and ground (see Design Guide for details).
VCC33	(see pin list)	P	Power for Internal Logic (3.3V ±5%).
VCC25	(see pin list)	P	Power for Internal Logic (2.5V ±5%).
VSUS25	AD3	P	Suspend Power (2.5V ±5%).
VCCHCK	G22	P	Power for Host CPU Clock DLL (2.5V ±5%)
VCCMCK	AA22	P	Power for Memory Clock DLL (2.5V ±5%)
VCCMDLL	AA14	P	Power for Memory Strobe DLL (2.5V ±5%)
VCCFP	J10-J12	P	Power for Flat Panel /DVI Interface (3.3V ±5%).
VCCRGB	C3	P	Power for CRT RGB Outputs (2.5V ±5%).
VCCDAC	C4	P	Power for DAC Digital Logic (2.5V ±5%)
VCCPLL1	B4	P	Power for Graphics Controller PLL1 (2.5V ±5%).
VCCPLL2	A4	P	Power for Graphics Controller PLL2 (2.5V ±5%).
VCCLVDS	H1,W3	P	Digital Power for LVDS Circuitry (2.5V ±5%).
VCCALVDS	K2,N5,U4	P	Analog Power for LVDS Circuitry (3.3V ±5%).
VCCALPLL	H3	P	Analog Power for LVDS PLL (2.5V ±5%).
GND	(see pin table)	P	Ground. Connect to main ground plane.

Power,Ground,and Test Continue

Signal Name	Pin #	I/O	Signal Description
GNDHCK	F21	P	Ground for Host CPU Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDMCK	Y21	P	Ground for Memory Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDMDLL	AA13	P	Ground for Memory Strobe DLL Circuitry. Connect to main ground plane through a ferrite bead.
GNDRGB	A1	P	Connection Point for RGB Load Resistors.
GNDDAC	A1	P	Connection Point for RGB Load Resistors.
GNDDAC	B2	P	Ground for DAC Analog Circuitry.
GNDPLL1	E5	P	Ground for Graphics Controller PLL1.
GNDPLL2	D4	P	Ground for Graphics Controller PLL2.
GNDALPLL	H4,J3	P	Ground for LVDS PLL.
GNDALVDS	M5,R5,U5	P	Ground for LVDS Analog Circuitry.
GNDLVDS	H2,J1,J5,W2	P	Ground for LVDS Digital Circuitry.
NC	(see pin table)		No Connect.

LVDS Interface

Signal Name	Pin #	I/O	Signal Description
Y[3:0]+ Y[3:0] －	N4,T1,U3,U1 P3,T2,U2,V1	A A	LVDS Data Positive Output. LVDS Data Negative Output.
YC+ YC －	P4 P5	A A	LVDS Clock Posit ve Output. LVDS Clock Negative Output.nd
Z[3:0]+ Z[3:0] －	K3,L1,L4,N1 K1,L2,L3,N2	A A	2nd LVDS Data Positive Output. 2nd LVDS Data Negative Output.
ZC+ ZC －	K4 K5	A A	2nd LVDS Clock Positive Output. 2nd LVDS Clock Negative Output.

5.2 VIA VT8372 North Bridge with S3 ProSavage8 AGP8X

SMB /I2C Interface

Signal Name	Pin #	I/O	Signal Description
SPCLK[2:1]	C6,F7	IO	Serial Port (SMB/I2C)Clocks.These are the clocks for serial data transfer. SPCLK1 is typically used for I 2 C com unications.As an output,it is program ed via CRA0[0]. As an input,its status is read via CRA0[2].In either case the serial port ust be enabled by CRA0[4]=1.SPCLK2 is typically used for DDC onitor com unications.As an output,it is program ed via CRB1[0].As an input,its status is read via CRB1[2].The port is enabled via CRB1[4]=1.
SPDAT[2 :1]	D6,D7	IO	Serial Port (SMB/I2C)Data.These are the data signals used for serial data transfer.SPDAT1 is typically used for I^2C com unications.As an output,it is program ed via CRA0[1].As an input,its status is read via CRA0[3].In either case the serial port ust be enabled by CRA0[4]=1. SPDAT2 is typically used for DDC monitor communications. As an output,it is program ed via CRB1[1]. As an input,its status is read via CRB1[3].The port is enabled via CRB1[4]=1.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD[15:0]	K22,J22,G24,H22, G22,G23,F23,D25, K26,K24,E24,E26, J25,J26,F26,F25	IO	Address /Data Bus. Bits 0-7 are implemented and bits 8-15 are reserved for future use. VAD[6:0]are used to send strap information o he chipset north bridge. A power up VAD[6:4]reflect he state of straps on pins SDA[2:0] and VAD[3:0]reflect the state of straps on pins SA[19:16].The specific interpretation of these straps is north bridge chip design dependent.
VPAR	D26	IO	Parity. If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800,KT400).If VPAR is not implemented in the north bridge chip or is incompatible with he 8235 (4x V-Link north bridges) connect this pin to an 8.2K pull up to 2.5V (Pro266,Pro266T,KT266, KT266A, KT333, P4X266, PN266,KN266,KM266, P4M266, P4N266).See app note AN222 for details.
VBE[1:0]#	L26,F24	IO	Byte Enables.VBE0#is used with VAD[7-0]and VBE1# is used with VAD[15-8](VBE1#and VAD[15-8]are reserved for future use).
VCLK	L24	I	V-Link Clock.
UPCMD	K25	O	Command from Client-to-Host.
DNCMD	J24	I	Command from Host-to-Client.
UPSTB	H24	O	Strobe from Client-to-Host.
UPSTB#	H26	O	Complement Strobe from Client-to-Host.
DNSTB	G25	I	Strobe from Host-to-Client.
DNSTB#	G26	I	Complement Strobe from Host-to-Client.
VLVREF	J23	I	Voltage Reference.
VLCOMP	K23	I	V-Link Compensation.
VCCVK	(see pin list)	P	V-Link VK Power.

Advanced Programmable Interrupt Controller (APIC)Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	V23	O	Internal APIC Data 1.Function 0 Rx58[6]=1
APICD0	T22	O	Internal APIC Data 0.Function 0 Rx58[6]=1
APICCLK	U23	I	APIC Clock.

Straps

Signal Name	Pin #	I/O	Signal Description
Strap /SDCS3#	AD23	I	Strap. State reflected on VAD[7]at powerup. No internal function.
Strap /SDA2	AF23	I	Strap. State reflected on VAD[6]at powerup. No internal function.
Strap /SDA1	AC22	I	Strap. State reflected on VAD[5]at powerup. No internal function.
Strap /SDA0	AE23	I	Strap. State reflected on VAD[4]at powerup. No internal function.
Strap /SA19	AC11	I	Strap. State reflected on VAD[3]at powerup. No internal function.
Strap /SA18	AD11	I	Strap. State reflected on VAD[2]at powerup. No internal function.
Strap /SA17	AE11	I	Strap. State reflected on VAD[1]at powerup. No internal function.
Strap /SA16	AF11	I	Strap. State reflected on VAD[0]at powerup. No internal function.
Strap /SOE#	AD12	I	Strap. Strap low o enable (high o disable)auto reboot.
Strap /SPKR	AE9	I	Strap. Strap low o enable (high o disable)CPU frequency s rapping
Strap /ROMCS#/KBCS#	AF12	I	Strap. Strap high to enable LPCBIOSROM

5.3 VIA VT8235 BGA PCI-LPC South Bridge

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VGATE /GPIO8 /PCREQA	C8	I	Voltage Gate. Signal from he CPU voltage regulator. High indicates he voltage regulator output is stable. This pin performs he VGATE function if Device 17 Function 0 Rx53[7]=0,E5[4]=1 and E4[3]=0.
VIDSEL /GPIO28	P25	OD	Voltage Regulator ID Select. Connected o he CPU voltage regulator. Low selects the voltage ID from the CPU; high selects a different fixed voltage ID (the lower voltage used for CPU deep sleep mode). This pin performs the VIDSEL function if Function 0 RxE5[3]=0.
VRDSLP /GPIO29	P24	OD	Voltage Regulator Deep Sleep. Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This pin performs he VRDPSLP function if Function 0 RxE5[3]=0.
GHI#/GPIO22	R24	OD	CPU Speed Select. Connected o he CPU voltage regulator, used to select high speed (L) or low speed (H).This pin performs the GHI# function if Function 0 RxE5[3]=0.
DPSLP#/GPIO23	P26	OD	CPU Deep Sleep.
CPUMISS /GPI17	Y1	I	CPU Missing. Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of he CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ#/GPI6	A8	I	AGP Busy. Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if his input is asserted low).Connected to the AGP Bus AGPBZ# pin.

Summary of Internal Pull-Up /Pull-Down Resistor Implementation Internal Pullups are present on pins KBCK,KBDT,MSCK,MSDT,SERIRQ,LAD [3:0]Internal Pulldowns are present on pins SA [19-16] and all LAN pins

Low Pin Count (LPC)Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	AE7	IO		LPC Frame.
LREQ#	AD7	IO		LPC DMA /Bus Master Request.
LAD[3-0]	AF7,AD8,AE8, AF8	IO	PU	LPC Address /Data.

Note: Connect the LPC interface LPCRST#(LPC Reset)signal to PCIRST#

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	T25	OD	A20 Mask. Connect to A20 mask input of he CPU to control address bi -20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit -1 (Fast_A20).
FERR#	U26	I	Numerical Coprocessor Error. This signal is tied o he coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T26	OD	Ignore Numeric Error. This pin is connected to the CPU “ignore error” pin.
INIT#	R25	OD	Initialization. The VT8235 asserts INIT# if it detects a shut-down special cycle on he PCI bus or if a soft reset is initiated by he register
INTR	T23	OD	CPU Interrupt. INTR is driven by he VT8235 to signal he CPU hat an interrupt request is pending and needs service.
NMI	R23	OD	Non-Maskable Interrupt. NMI is used o force a non-maskable interrupt to the CPU. The VT8235 generates an NMI when PCI bus SERR# is asserted.
SLP#	U25	OD	Sleep. Used to put the CPU to sleep.
SMI#	T24	OD	System Management Interrupt. SMI# is asserted by he VT8235 o he CPU in response to different Power-Management events.
STPCLK#	R26	OD	Stop Clock. STPCLK# is asserted by he VT8235 to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 .pullup resistors to VCC_CMOS (see Design Guide).

Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	A13	O		Serial EEPROM Chip Select.
EECK	C14	O		Serial EEPROM Clock.
EEDO	A14	O		Serial EEPROM Data Output.
EEDI	B14	I		Serial EEPROM Data Input.

These pins are disabled if the SDCS1#pin is strapped low to enable serial EEPROM connection via the MII interface.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	see pin list)	IO	Address /Data Bus. Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	L1,A4, D1,F4	IO	Command /Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	B3	IO	Device Select. The VT8235 asserts his signal o claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	B4	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C4	IO	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	A3	IO	Target Ready. Asserted when the target is ready for data transfer.
STOP#	C3	IO	Stop. Asserted by the target to request the master to stop the current transaction.
SERR#	C1	I	System Error. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 can be programmed o generate an NMI to the CPU.
PAR	D3	IO	Parity. A single parity bi is provided over AD[31:0]and C/BE[3:0]#.
INTA# INTB# INTC# INTD# INTE# /GPIO12 /PCGNTA, INTF# /GPIO13 /PCGNTB, INTG# /GPIO14, INTH# /GPIO15	P1, P2, P3, R1 A7, B8, D8, C7	I	PCI Interrupt Request .The INTA# through INTD# pins are typically connected to the PCI bus INTA#-INTD# pins per the able below. INTE-H# are enabled by setting Device 17,Function 0 Rx5B[1]=1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#

PCI Bus Interface Continue

Signal Name	Pin #	I/O	Signal Description
REQ5#/GPI7, REQ4#, REQ3#, REQ2#, REQ1#, REQ0#	N4 L4 H4 D4 C5 D6	I	PCI Request. These signals connect to the VT8235 from each PCI slot (or each PCI master)o request he PCI bus. To use pin N4 as REQ5#, Function 0 RxE4 must be set to 1 otherwise his pin will function as General Purpose Input 7.
GNT5#/GPO 7, GNT4#, GNT3#, GNT2#, GNT1#, GNT0#	P4 M4 J4 E4 D5 E6	O	PCI Grant. These signals are driven by he VT8235 to grant PCI access to a specific PCI master. To use pin P4 as GNT5#,Function 0 RxE4 must be set to 1 otherwise this pin will function as General Purpose Output 7.
PCIRST#	R2	O	PCI Reset. This signal is used o reset devices attached to the PCI bus.
PCICLK	R22	I	PCI Clock. This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AF5	IO	PCI Bus Clock Run. This signal indicates whether he PCI clock is or will be stopped high) or running (low).The VT8235 drives his signal low when he PCI clock is running default on reset)and releases it when it stops the PCI clock. External devices may assert this signal low o request hat he PCI clock be restarted or prevent it from stopping. Connect his pin o ground using a 100 .resistor if he function is not used. Refer to the “PCI Mobile Design Guide” and he VIA “VT8633 Apollo Pro266 Design Guide” for more details.

PC /PCI DMA

Signal Name	Pin #	I/O	PU	Signal Description
PCREQA/GPIO8/VGATE	C8	I		PC /PCI Request A. Device 17 Function 0 Rx53[7]=1
PCREQB /GPIO9	B7	I		PC /PCI Request B. Device 17 Function 0 Rx53[7]=1
PCGNTA /GPIO12	A7	O		PC /PCI Grant A. Device 17 Function 0 Rx53[7]=1
PCGNTB /GPIO13	B8	O		PC /PCI Grant B. Device 17 Function 0 Rx53[7]=1

5.3 VIA VT8235 BGA PCI-LPC South Bridge

LAN Controller -Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	C13	I	*PD*	MII Collision Detect. From he external PHY.
MCRS	B13	I	*PD*	MII Carrier Sense. Asserted by the external PHY when the media is active.
MDCK	C9	O	*PD*	MII Management Data Clock. Sent to the external PHY as a timing reference for MDIO
MDIO	B9	IO	*PD*	MII Management Data I/O. Read from he MDI bit or written to the MDO bit.
MRXCLK	B10	I	*PD*	MII Receive Clock.2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	A9,D9,D10,E10	I	*PD*	MII Receive Data. Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	C10	I	*PD*	MII Receive Data Valid.
MRXERR	A10	I	*PD*	MII Receive Error. Asserted by the PHY when it detects a data decoding error.
MTXCLK	A12	I	*PD*	MII Transmit Clock. Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	C11,B11,A11, C12	O	*PD*	MII Transmit Data. Parallel transmit data lines synchronized to MTXCLK.
MTXENA	B12	O	*PD*	MII Transmit Enable. Signals that transmit is active from the MII port to the PHY.
MIIVCC	D11,D12,E11, E12	Power		MII Interface Power.3.3V ±5%.
MIIVCC25	D13,E13	Power		MII Suspend Power.2.5V ±5%.
RAMVCC	E7	Power		Power For Internal LAN RAM.2.5V ±5%.
RAMGND	E8	Power		Ground For Internal LAN RAM.

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	A21	IO	USB 2.0 Port 0 Data +
USBP0 –	B21	IO	USB 2.0 Port 0 Data –
USBP1+	E21	IO	USB 2.0 Port 1 Data +
USBP1 –	D21	IO	USB 2.0 Port 1 Data –
USBP2+	A19	IO	USB 2.0 Port 2 Data +
USBP2 –	B19	IO	USB 2.0 Port 2 Data –
USBP3+	E19	IO	USB 2.0 Port 3 Data +
USBP3 –	D19	IO	USB 2.0 Port 3 Data –
USBP4+	A17	IO	USB 2.0 Port 4 Data +
USBP4 –	B17	IO	USB 2.0 Port 4 Data –
USBP5+	E17	IO	USB 2.0 Port 5 Data +
USBP5 –	D17	IO	USB 2.0 Port 5 Data –
USBCLK	D23	I	USB 2.0 Clock.48MHz clock input for he USB interface
USBOC0#	A15	I	USB 2.0 Port 0 Over Current Detect. Port 0isdisablediflow.
USBOC1#	B15	I	USB 2.0 Port 1 Over Current Detect. Port1isdisablediflow.
USBOC2#	C15	I	USB 2.0 Port 2 Over Current Detect. Port2isdisablediflow.
USBOC3#	E15	I	USB 2.0 Port 3 Over Current Detect. Port 3isdisablediflow.
USBOC4#	D14	I	USB 2.0 Port 4 Over Current Detect. Port 4isdisablediflow.
USBOC5#	E14	I	USB 2.0 Port 5 Over Current Detect. Port 5isdisablediflow.
USBVCC	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Voltage.3.3V
USBGND	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Ground.
VSUSUSB	D15	Power	USB 2.0 Suspend Power.2.5V ±5%.
VCCUPLL	A23,D22	Power	USB 2.0 PLL Analog Voltage.2.5V ±5%.
GNDUPLL	B23,E22	Power	USB 2.0 PLL Analog Ground.

General Purpose I/O

Signal Name	Pin #	I/O	Signal Description
GPIOA /GPI24/GPO24	AE5	IO	**General Purpose I/O A /24**. RxE6[0]=1
GPIOC /GPI25/GPO25	AE6	IO	**General Purpose I/O C /25**.
GPIOD /GPI30/GPO30	AD6	IO	**General Purpose I/O D /30.**
GPIOE /GPI31/GPO31	AC6	IO	**General Purpose I/O E /31.**

The output type of he above pins may be selected as either OD or TTL (see Device 17 Function 0 RxE7)

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0#/GPIO20 /ACSDIN2	U2	O	Programmable Chip Select 0.RxE4[6]=1,E5[1]=1
PCS1#/GPIO21/ACSDIN3 /SLPBTN#	V1	O	Programmable Chip Select 1.RxE4[6]=1,E5[2]=1

5.3 VIA VT8235 BGA PCI-LPC South Bridge

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY / PDDMARDY / PDSTROBE	Y26	I	EIDE Mode: **Primary I/O Channel Ready.**Device read indicator UltraDMA Mode:**Primary Device DMA Ready** .Output flow control. The device may assert DDMARDY o pause output transfers **Primary Device Strobe** .Input data strobe (both edges).The device may s op DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	AD15	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready** .Output flow control. The device may assert DDMARDY to pause output transfers Secondary Device Strobe .Input data strobe (both edges).The device may stop DSTROBE o pause input data transfers
PDIOR#/ PHDMARDY / PHSTROBE	Y24	O	EIDE Mode: Primary Device I/O Read. Device read strobe UltraDMA Mode: Primary Host DMA Ready .Primary channel input flow control .The host may assert HDMARDY o pause input transfers Primary Host Strobe .Output data strobe (both edges).The host may stop HSTROBE o pause output data transfers
SDIOR#/ SHDMARDY / SHSTROBE	AF22	O	EIDE Mode: Secondary Device I/O Read. Device read strobe UltraDMA Mode: Secondary Host DMA Ready .Input flow control. The host may assert HDMARDY to pause input transfers Host Strobe B .Output strobe (both edges).The host may stop HSTROBE to pause output data transfers
PDIOW#/ PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device wri te strobe UltraDMA Mode: **Primary Stop.**Stop transfer: Asserted by the host prior to initiation an UltraDMA burst; negated by the host before data is transferred an UltraDMA burst. Assertion of STOP by he host during or after transfer in UltraDMA mode signals the nation of the burst
SDIOW#/ SSTOP	AC21		EIDE Mode: **Secondary Device I/O Write.**Device writ strobe UltraDMA Mode: **Secondary Stop** .Stop transfer Asserted by the host prior to initiation of an UltraDMA burst;negated by the host before data is transferted in an ULtraDMA burst Assert of Stop by the host during or after data transfer in ULtraDMA mode signals the termination of the burst

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface Continue

Signal Name	Pin #	I/O	Signal Description
PDDRQ	Y22	I	Primary Device DMA Request.Primary channel DMA request
SDDRQ	AE15	I	Secondary Device DMA Request.Secondary channel DMA request
PDDACK#	W26	O	Primary Device DMA Acknowledge.Primary channel DMA acknowledge
SDDACK#	AD22	O	Secondary Device DMA Acknowledge.Secondary channel DMA acknowledge
IRQ14	AE24	I	Primary Channel Interrupt Request.
IRQ15	AF24	I	Secondary Channel Interrupt Request.
PDCS1#	V24		Primary Master Chip Select.This signal corresponds toCS1FX#on the primary IDM connector
PDCS3#	W24		Primary Slave Chip Select.This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#/srap	AC23		Secondary Master Chip Select.This signal corresponds o CS17X# on he secondary IDE connector.S rap low (resistor o ground) to enable serial EEPROM interface via he MII bus (this disables the EExx pins).This pin has an internal pullup to default to serial EEPROM interface via the EEPROM interface via the Eexx pine
SDCS3#/s rap	AD23		Secondary Slave Chip Select. This signal corresponds toCS37X#on the secondary IDE connector. Strap information is communicated to the north bridge via VAD[7].
PDA[2-0]	V26,V25,Y23		Primary Disk Address. PDA[2:0]are used o indicate which by e in either the ATA command block or control block is being accessed.
SDA[2-0]/srap	AF23,AC22,AE23		Secondary Disk Address. SDA[2:0]are used o indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VAD[6:4].
PDD[15-0]	(see pin list)		Primary Disk Data.
SDD[15-0]/SA[15-0]	(see pin list)		Secondary Disk Data.
PDCOMP	W23		Primary Disk Compensation.
SDCOMP	AC15		Secondary Disk Compensation.

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AE10	I	Serial IRQ. This pin has an internal pull-up resistor.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 *(VBAT)*	AE3	I	**General Purpose Input 0**.Status on PMIO Rx20[0]
GPI1 *(VSUS33)*	AC3	I	**General Purpose Input 1**.Status on PMIO Rx20[1]
GPI2 /EXTSMI#*(VSUS33)*	AA1	I	**General Purpose Input 2**.Status on PMIO Rx20[4]
GPI3 /RING#*(VSUS33)*	Y2	I	**General Purpose Input 3**.Status on PMIO Rx20[8]
GPI4 /LID#*(VSUS33)*	AC1	I	**General Purpose Input 4**.Status on PMIO Rx20[11]
GPI5 /BATLOW#*(VSUS33)*	W4	I	**General Purpose Input 5**.Status on PMIO Rx20[12]
GPI6 /AGPBZ#	A8	I	**General Purpose Input 6**.Status on PMIO Rx20[5]
GPI7 /REQ5#	N4	I	**General Purpose Input 7**.RxE4[2]=0
GPI8 /GPO8 /PDREQA /VGATE	C8	I	**General Purpose Input8**. RxE4[3]=0, E5[4]=0, 53[7]=0
GPI9 /GPO9 /PDREQB	B7	I	**General Purpose Input 9**. RxE4[3]=0,53[7]=0
GPI10 /GPO10	D7	I	**General Purpose Input 10**.RxE4[3]=0
GPI11 /GPO11	A6	I	**General Purpose Input 11**.RxE4[3]=0
GPI12 /GPO12 /INTE#/PDGNTA	A7	I	**General Purpose Input 12**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI13 /GPO13 /INTF#/PDGNTB	B8	I	**General Purpose Input 13**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI14 /GPO14 /INTG#	D8	I	**General Purpose Input 14**.RxE4[4]=0,5B[1]=0
GPI15 /GPO15/INTH#	C7	I	**General Purpose Input 15**.RxE4[4]=0,5B[1]=0
GPI16 /INTRUDER#*(VBAT)*	AD3	I	**General Purpose Input 16**.Status on PMIO Rx20[6]
GPI17 /CPUMISS	Y1	I	**General Purpose Input 17**.Status on PMIO Rx20[5]
GPI18 /THRM#/AOLGPI	Y4	I	**General Purpose Input 18**.Rx8C[3]=0
GPI19 /IORDY	AD10	I	**General Purpose Input 19**.RxE5[0]=1
GPI20 /GPO20/ACSDIN2/PCS0#	U2	I	**General Purpose Input 20**.RxE4[6]=1,E5[1]=0, PMIO 4C[20]=1
GPI21 /GPO21/ACSDIN3/PCS1#/SLP BTN#	V1	I	**General Purpose Input 21**.RxE4[6]=1,E5[2]=0 PMIO 4C[21]=1
GPI22 /GPO22 /GHI#	R24	I	**General Purpose Input 22**.RxE5[3]=1,PMIO 4C[22]=1
GPI23 /GPO23 /DPSLP#	P26	I	**General Purpose Input 23**.RxE5[3]=1,PMIO 4C[23]=1
GPI24 /GPO24/GPIOA	AE5	I	**General Purpose Input 24**.RxE6[0]=0
GPI25 /GPO25/GPIOC	AE6	I	**General Purpose Input 25**.RxE6[1]=0
GPI26 /GPO26/SMBDT2 *(VSUS33)*	AD1	I	**General Purpose Input 26**.Rx95[2]=1,95[3]=0

General Purpose Inputs Continue

Signal Name	Pin #	I/O	Signal Description
GPI27 /GPO27 /SMBCK2 *(VSUS33)*	AE1	I	**General Purpose Input 27**.Rx95[2]=1,95[3]=0
GPI28 /GPO28 /VIDSEL	P25	I	**General Purpose Input 28**.RxE5[3]=1,PMIO 4C[28]=1
GPI29 /GPO29/VRDSLP	P24	I	**General Purpose Input 29**.RxE5[3]=1,PMIO 4C[29]=1
GPI30 /GPO30 /GPIOD	AD6	I	**General Purpose Input 30**.RxE6[6]=0
GPI31 /GPO31/GPIOE	AC6	I	**General Purpose Input 31**.RxE6[7]=0

Note:Defaul pin function is underlined in he signal name column above.
Note:Input pin s a us for he above GPI pins 31-0 is also available on PMIO Rx4B-48 [31-0]
Note:See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx4C.General purpose input pins 20-31 are shared with OD (open drain)general purpose output functions,so to use one of these pins as an input pin,a one must be written to the corresponding bit of PMIO Rx4C.

Resets,Clocks,and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	AF4	I	**Power Good.** Connected o he Power Good signal on he Power Supply. Internal logic powered by VBAT.
PWROK#	AE2	O	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	R2	O	**PCI Reset.** Active low reset signal for he PCI bus. The VT8235 will assert his pin during power-up or from he control register.
OSC	AC12	I	**Oscillator.**14.31818 MHz clock signal used by he in ernal Timer.
RTCX1	AD4	I	**RTC Crystal Input :**32.768 KHz crystal or oscilla or input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	AF3	O	**RTC Crystal Output :**32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	AF9	I	Test.
TPO	U24	O	**Test Pin Output.** Output pin for est mode.
NC	W22,AD17	-	**No Connect.** Reserved for future use,do not connect.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	AD2	I	**Power Button.**Used by the Power Management subsystem to monitor an external system on/off but on or switch. Internal logic powered by VSUS33.
SLPBTN#/GPIO21 /ACSDIN3 /PCS1#	V1	I	**Sleep Button.** Used by he Power Management subsystem to monitor an external sleep but on or switch.RxE4[6]=1,80[6]=1,E5[2]=0 and PMIO Rx4C[21]=1
RSMRST#	AD5	I	**Resume Reset.** Resets he internal logic connected o he VSUS33 power plane and also resets portions of he internal RTC logic. Internal logic powered by VBAT.
EXTSMI#/GPI2	AA1	IOD	**External System Management Interrupt.** When enabled o allow it ,a falling edge on this input causes an SMI# to be generated o he CPU o enter SMI mode.(10K PU to VSUS33 if not used)(3.3V only)
PME#	W3	I	**Power Management Event.**(10K PU o VSUS33 if not used)
SMBALRT#	AB2	I	**SMB Alert** .When programmed to allow it (SMB I/O Rx8[3]=1),assertion generates an IRQ, SMI,or power management event.(10K PU o VSUS33 if not used)
LID#/GPI4	AC1	I	**Notebook Computer Display Lid Open /Closed Monitor.** Used by he Power Management subsystem to monitor he opening and closing of the display lid of notebook computers. Can be used o detect either low-to-high or high-to-low transitions o generate an SMI#.(10K PU o VSUS33 if not used)
INTRUDER#/GPI16	AD3	I	Intrusion Indicator. The value of his bi may be read at PMIO Rx20[6]
THRM#/GPI18 /AOLGPI	Y4	I	**Thermal Alarm Monitor.**Rx8C[3]=1.Rising or falling edges (selectable by PMIO Rx2C[6])may be detected to status at used a PMIO Rx20[10].Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#)o automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-3]).
RING#/GPI3	Y2	I	**Ring Indicator.** May be connected to external modem circuitry to allow he system to be re-activated by a received phone call.(10K PU to VSUS33 if not used)
BATLOW#/GPI5	W4	I	**Battery Low Indicator.** (10K PU to VSUS33 if not used)(3.3V only)

Power Management and Event Detection Continue

Signal Name	Pin #	I/O	Signal Description
CPUSTP#/GPO5	AC7	O	**CPU Clock Stop** (RxE4[0]=0).Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP#/GPO6	AF6	O	**PCI Clock Stop** (RxE4[1]=0).Signals the system clock generator o disable he PCI clock outputs. Not connected if not used.
SUSA#/GPO1	AA2	O	**Suspend Plane A Control** (Rx94[2]=0).Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.(10K PU to VSUS33 if not used)
SUSB#/GPO2	AF2	O	**Suspend Plane B Control** (Rx94[3]=0).Asserted during power management STR and STD suspend states. Used o control he secondary power plane.(10K PU o VSUS33 if not used)
SUSC#	AF1	O	**Suspend Plane C Control**. Asserted during power management STD suspend state. Used to control he tertiary power plane. Also connected to ATX power-on circuitry. (10K PU o VSUS33 if not used)
SUSST1#/GPO3	Y3	O	**Suspend Status 1** (Rx94[4]=0).Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend statues. Connect 10K PU to VSUS33.
SUSCLK	AB1	O	**Suspend Clock.**32.768 KHz output clock for use by the North Bridge (e.g.,VT8633 or VT8366)for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS /GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to he CPUMISS pin of the CPU socket.The state of his pin may be read in the SMBus 2 registers.This pin may be used as CPUMISS and GPI17 a the same time.
AOLGPI /GPI18 /THRM#	R2	I	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pin may be used as AOLGPI, GPI18andTHRM#alla the same time.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK /IRQ1	W2	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Clock**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 1** .Interrupt input 1.
MSDT /IRQ12	W1	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Data**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK /KA20G	V3	IO /I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 Keyboard Clock. From internal keyboard controller Rx51[0]=0 Gate A20.Input from external keyboard controller.
KBDT /KBRC	V2	IO/I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data**. From internal keyboard controller. Rx51[0]=0 **Keyboard Rese**t. From external keyboard controller (KBC)for CPURST# generation
KBCS#/ROMCS#/srap	AF12	O/O		**Keyboard Chip Select** (Rx51[0]=0).To external keyboard controller chip. Strap high o enable LPC ROM:

Note: KBCK,KBDT,MSCK,and MSDT are powered by the VSUS33 suspend voltage plane.

AC97 Audio /Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	R3	O	AC97 Reset.
ACBTCK	T3	I	AC97 Bit Clock.
ACSYNC	T1	O	AC97 Sync.
ACSDO	U1	O	AC97 Serial Data Out.
ACSDIN0 (VSUS33)	T2	I	AC97 Serial Data In 0.
ACSDIN1 (VSUS33)	U3	I	AC97 Serial Data In 1.
ACSDIN2 /GPIO20 /PCS0#	U2	I	AC97 Serial Data In2.RxE4[6]=0,E5[1]=0,PMIO Rx4C[20]=1
ACSDIN3/GPIO21 /PCS1#/SLPBTN#	V1	I	AC97 Serial Data In 3.RxE4[6]=0,E5[2]=0,PMIO Rx4C[21]=1

The supply voltage for ACSDIN0-1 is VSUS33 so these inputs can support wake-up on modem ring

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)v	P	**I/O Power.**3.3V ±5%
VCC	(see pin list)	P	**Core Power.**2.5V ±5%.This supply is turned on only when he mechanical switch on the power supply is turned on and he PWRON signal is conditioned high . Note: The VT8235L core voltage is 2.5V so board designs that are intended t all w use of either VT8235 or VT8235L should take this difference into account and allow the core voltage to be selected as either 2.5V (for the VT8235)or 3.3V (for the VT8235L).
GND	(see pin list)	P	Ground. Connect o primary motherboard ground plane.
VSUS33	AA4,AB4, AC4,AC5	P	**Suspend Power.**3.3V ±5%.Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be Connected to VCC33.Signals powered by or referenced o this plane are:PWRGD, RSMRST#,PWRBTN#,SMBCK1/2, SMBDT1/2,GPO0,SUSA#/GPO1,SUSB#/ GPO2,SUSC#, SUSST1#/GPO3,SUSCLK /GPO4,GPI1,GPI2/EXTSMI#,GPI3 /RING#,GPI4 /LID,GPI5 /BATLOW#,GPI6 /PME#, SMBALRT#
VSUS25	T4,U4	P	**Suspend Power.**2.5V ±5%.
VSUSUSB	D15	P	**USB Suspend Power**.2.5V ±5%.
VBAT	AE4	P	**RTC Battery.** Battery input for internal RTC (RTCX1,RTCX2)
VLVREF	J23	P	**V-Link Voltage Reference.**0.9V ±5%.0.34 xVCC25to0.38 xVCC25.
VCCVK	(see pin list)	P	V-Link Compensation Circuit Voltage.2.5V ±5%
MIIVCC	D11,D12, E11,E12	P	**LAN MII Power.**3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY).Connect o VCC33 through a ferrite bead.
MIIVCC25	D13,E13	P	**LAN MII Suspend Power.**2.5V ±5%.
RAMVCC	E7	P	**LAN RAM Power.**2.5V ±5%.Power for LAN internal RAM. Connect to VCC through a ferrite bead.
RAMGND	E8	P	**LAN RAM Ground.** Connect o GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.**3.3V ±5%.Power for USB differential outputs (USBP0+,P0 –,P1+,P1 –,P2+, P2 –, P3+, P3 –,P4+,P4 –,P5+,P5 –).Connect o VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.

5.3 VIA VT8235 BGA PCI-LPC South Bridge

Power and Ground Continue

Signal Name	Pin #	I/O	Signal Description
VCCUPLL	A23,D22	P	**USB 2.0 PLL Analog Voltage**.2.5V ±5%.Connect to VCC through a ferrite bead.
GNDU PLL	B23,E22	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	P22	P	**PLL Analog Power.**2.5V ±5%.Connect to VCC through a ferrite bead.
PLLGND	P23	P	**PLL Analog Ground.** Connect o GND through a ferrite bead.

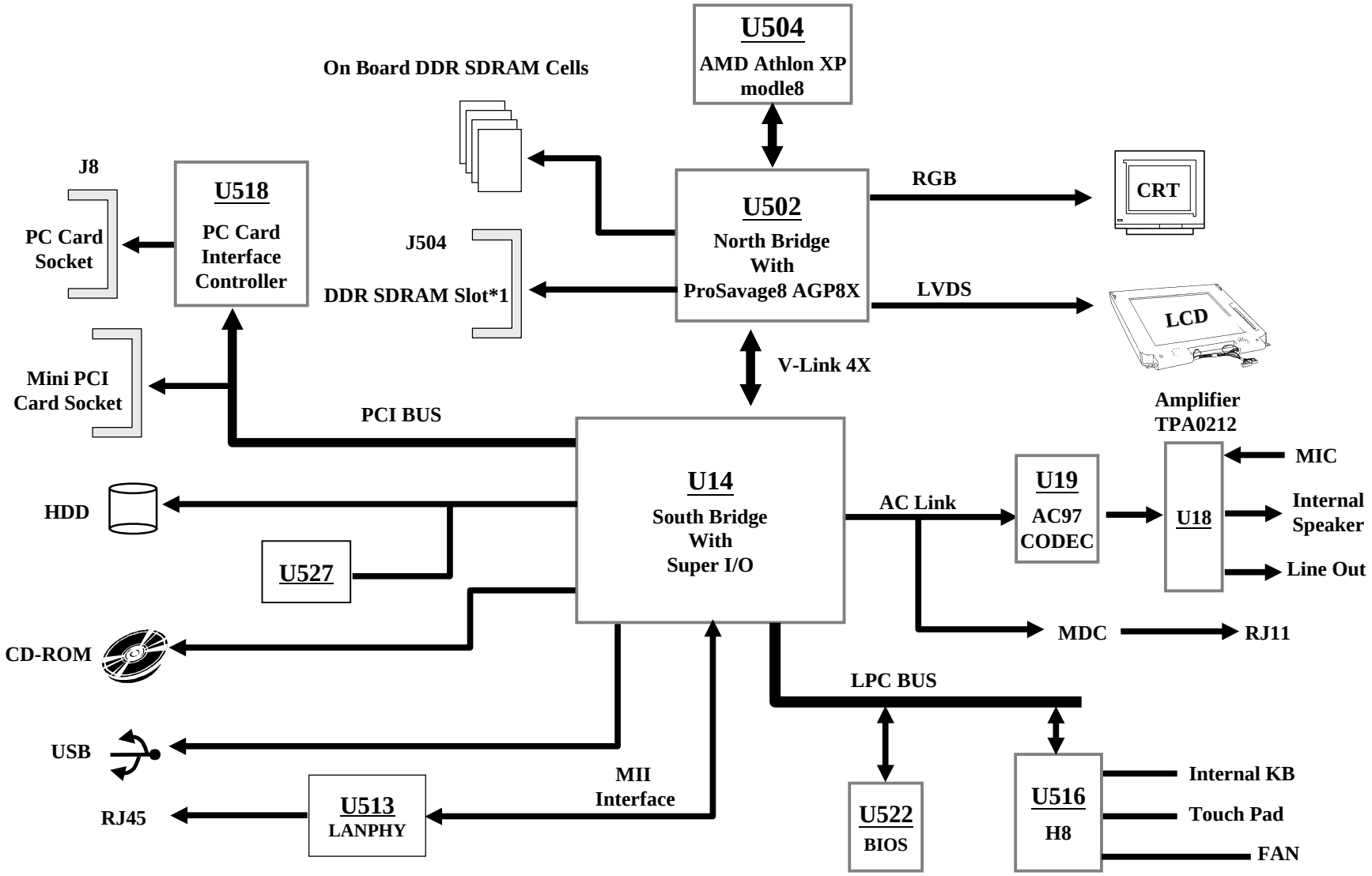
System Management Bus (SMB)Interface (I 2 CBus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AB3	IO	SMB /I^2 C Channel 1 Clock.
SMBCK2 /GPI27/GPO27	AE1	IO	SMB /I^2 C Channel 2 Clock.Rx95[2]=0
SMBDT1	AC2	IO	SMB /I^2C Channel 1 Data.
SMBDT2 /GPI26/GPO26	AD1	IO	SMB /I^3C Channel 2 Data.Rx95[2]=0
SMBALRT#	AB2	I	SMB Alert.(enabled by System Management Bus I/O space Rx08[1]When the chip is enabled to allow it, assertion generates an IRQ SMI interrupt or a power management resume event. Connect o a ohm pull up to VSUS33 if not used.

ISA Subset /Parallel BIOS ROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
ROMCS#/KBCS#/ strap	AF12	O		**ROM Chip Select** (Rx51[0]=1).Chip Select o the BIOS ROM. Strap high to enable LPCROM.
SPKR /srap	AE9	O		**Speaker**. Strap low to enable (high o disable)CPU frequency strapping.
MEMR#	AE12	O		**Memory Read.**
MEMW#	AF10	O		**Memory Write.**
IOR#	AC10	O		**I/O Read.**
IOW#	AD9	O		**I/O Write.**
IORDY /GPI19	AD10	I		**I/O Ready**. Used to insert wait states in I/O or memory cycles. RxE5[0]=0
SOE#/s rap	AD12	O		**XD Bus Tranceiver Output Enable**. Strap low to enable auto reboot.
XD[7-0]	AD13,AE 13, AF13,AD 14, AE14,AF 14, AC13,AC 14	IO		**XD Bus**. For input of BIOS ROM data or data from to her on-board I/O or memory devices.
SA[19-16]/GPO[19 -16] /sraps	AC11,AD 11, AE11,AF 11	O	*PD*	**System Address 19-16**.Strap states are passed to North Bridge via VAD[3-0].Functions as SA[19-16]if RxE4[5]=0.
SA[15-0]/SDD[15- 0]	(see pin lis)	O		**System Address 15-0**.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

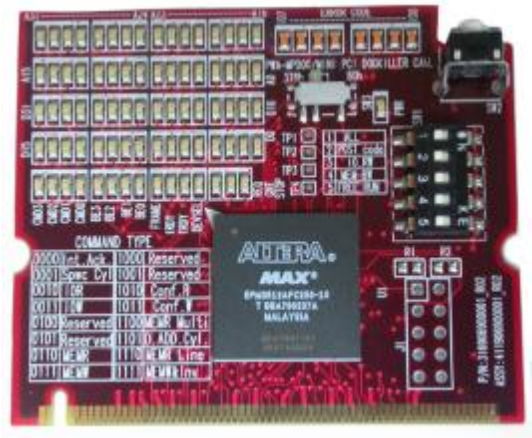
Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port by the debug card plug at MINI PCI slot.

7. Maintenance Diagnostics

7.1.1 Diagnostic Tool for Mini PCI Slot :

The Mini PCI DOGkiller card is a single-step debug tool which utilizes Mini PCI interface (Type III A) and is able to hold a PCI bus cycle so that address, data and control bus states on PCI bus can be inspected. Especially, the tool can help an engineer trace address/data bus for BIOS read cycles as soon as power on and debug open or short circuit problems easily. Usually, this sort of problem will make a PC motherboard fail to boot.



P/N:411906900001
Description: PWA; PWA-378 Port Debug BD
Note: Order it from MIC/TSSC

7.2 Error Codes - 1

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
10H	Some Type Of Long Reset
11H	Turn off FASTA20 for POST
12H	Signal Power On Reset
13H	Initialize the Chipset
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1
16H	user register configure through CMOS
17H	Size Memory
18H	Dispatch To RAM Test
19H	checksum the ROM
1AH	Reset PIC's
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Test Keyboard
21H	Test Keyboard Controller
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Int Vectors

POST (HEX)	DESCRIPTION
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Going To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter
2FH	Signon messages displayed
30H	special init of keyboard ctrl
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update OUTPUT port
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	test for RTC ticking
3CH	initialize the hardware vectors
3DH	Search and Init the Mouse

7.2 Error Codes - 2

Following is a list of error codes in sequent display on the debug board.

POST (HEX)	DESCRIPTION
3EH	Update NUMLOCK status
3FH	special init of COMM and LPT ports
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize option ROMs
44H	OEM's init of power management
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot
48H	Dispatch To Op. Sys. Boot
49H	Jump Into Bootstrap Code

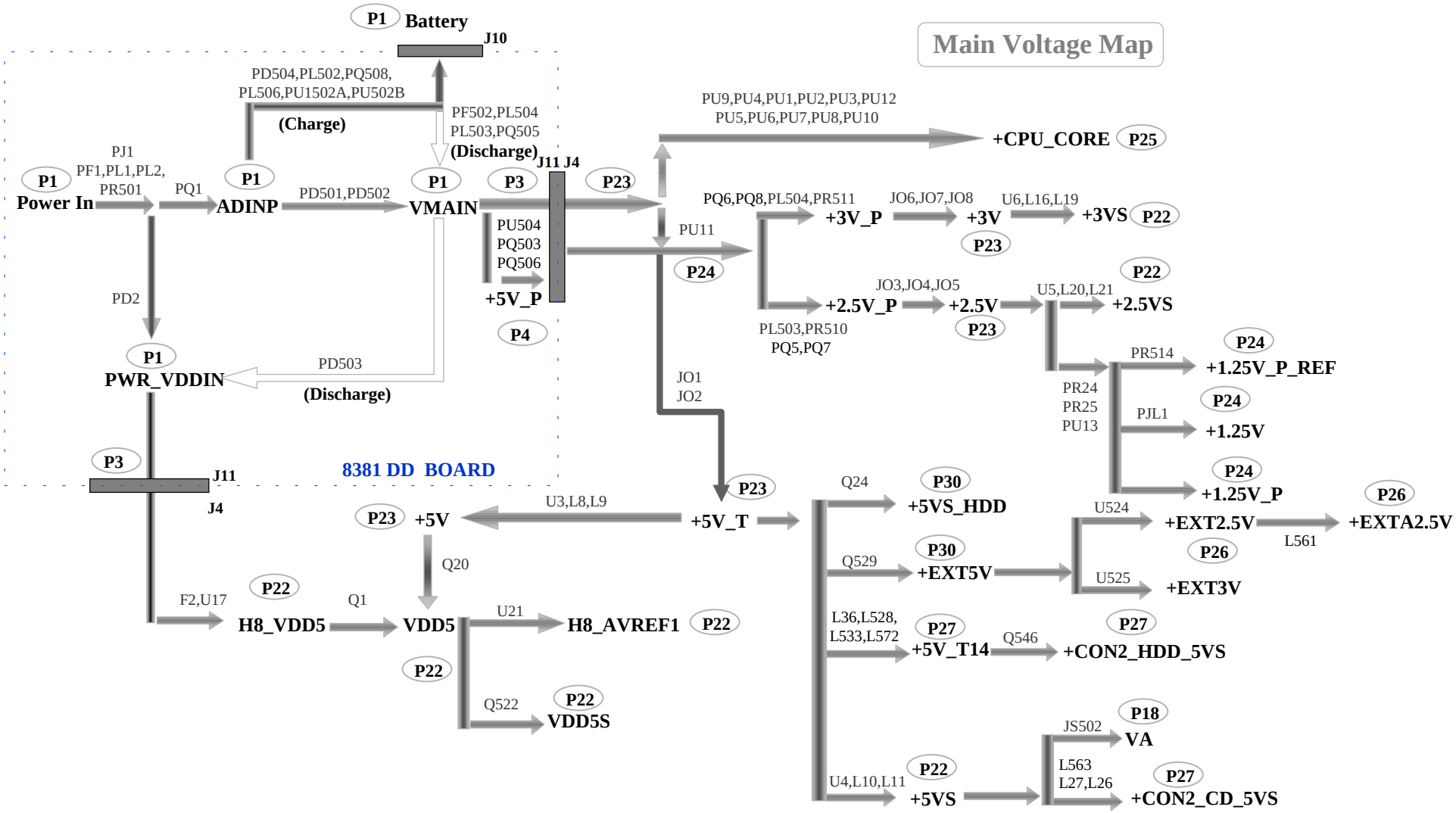
8. Trouble Shooting

- 8.1 No Power
- 8.2 Battery Can not Be Charged
- 8.3 No Display
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 Memory Test Error
- 8.7 Keyboard and Touch Pad Test Error
- 8.8 Hard Disk Drive Test Error
- 8.9 CD-ROM Drive Test Error
- 8.10 USB Port Test Error
- 8.11 PC Card Socket Test Error
- 8.12 LAN Test Error
- 8.13 Audio Failure
- 8.14 Mini PCI Test Error

8381 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens ,power indicator does not light up.



8381 N/B Maintenance

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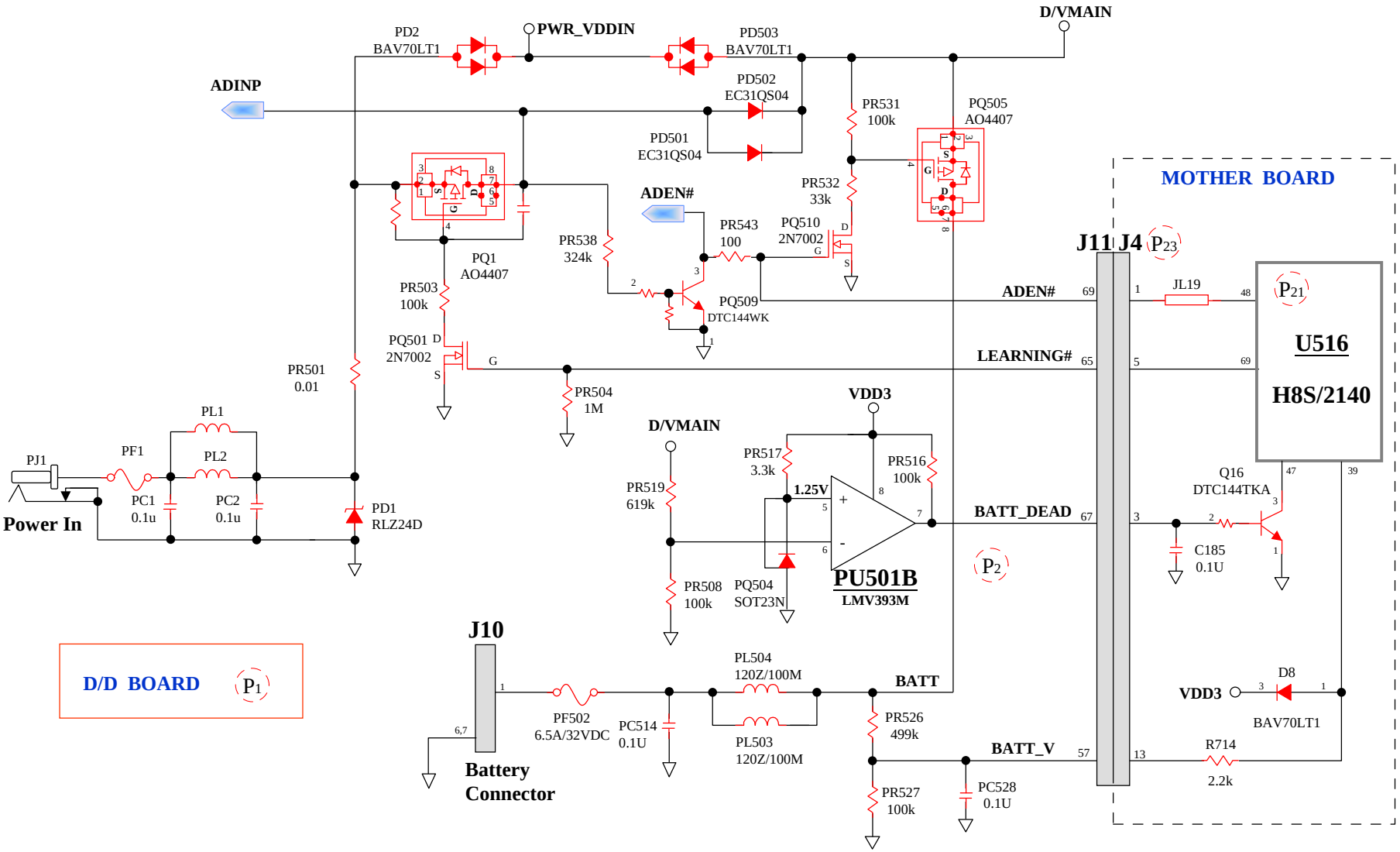

8381 N/B Maintenance

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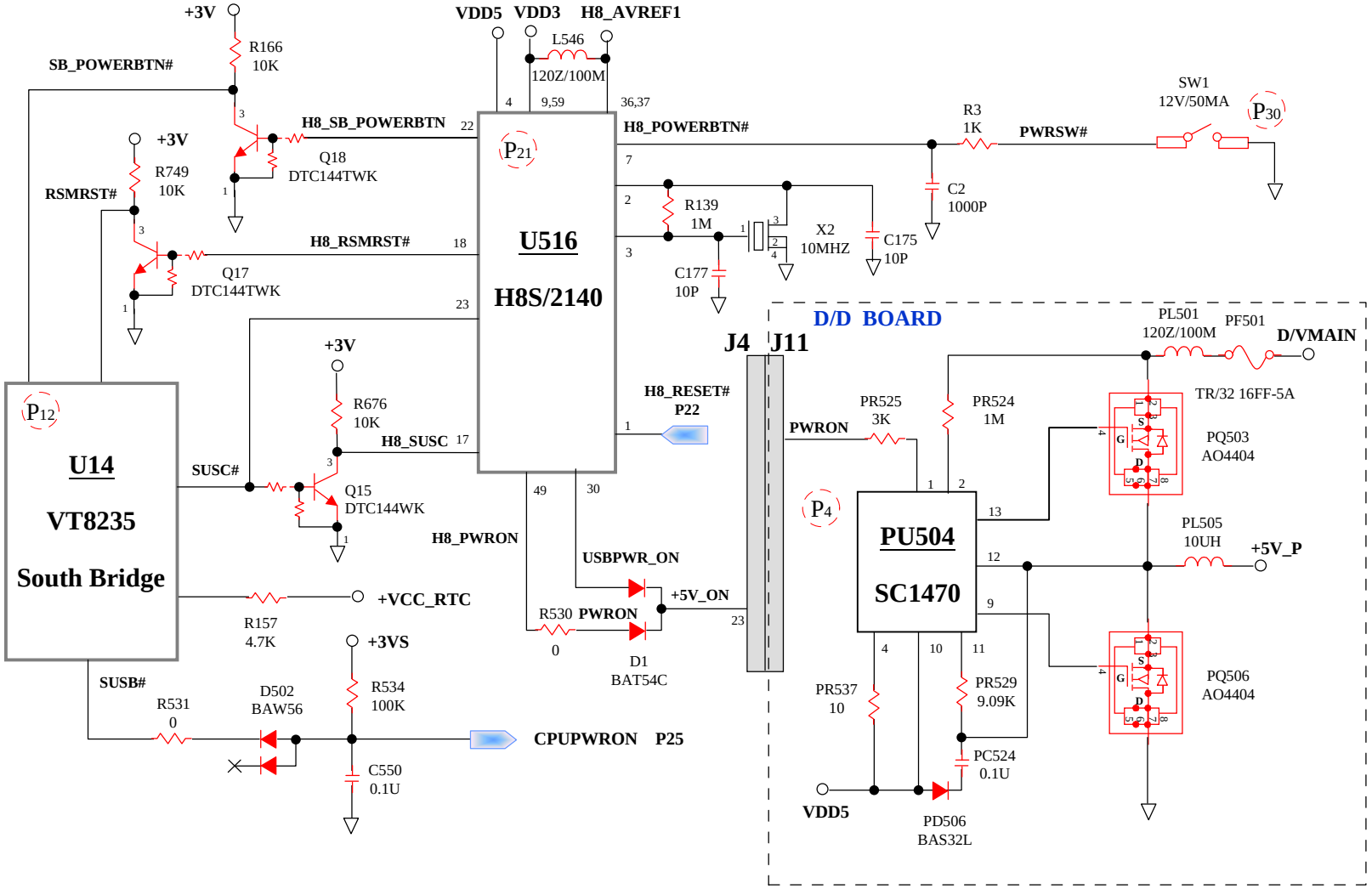

8381 N/B Maintenance

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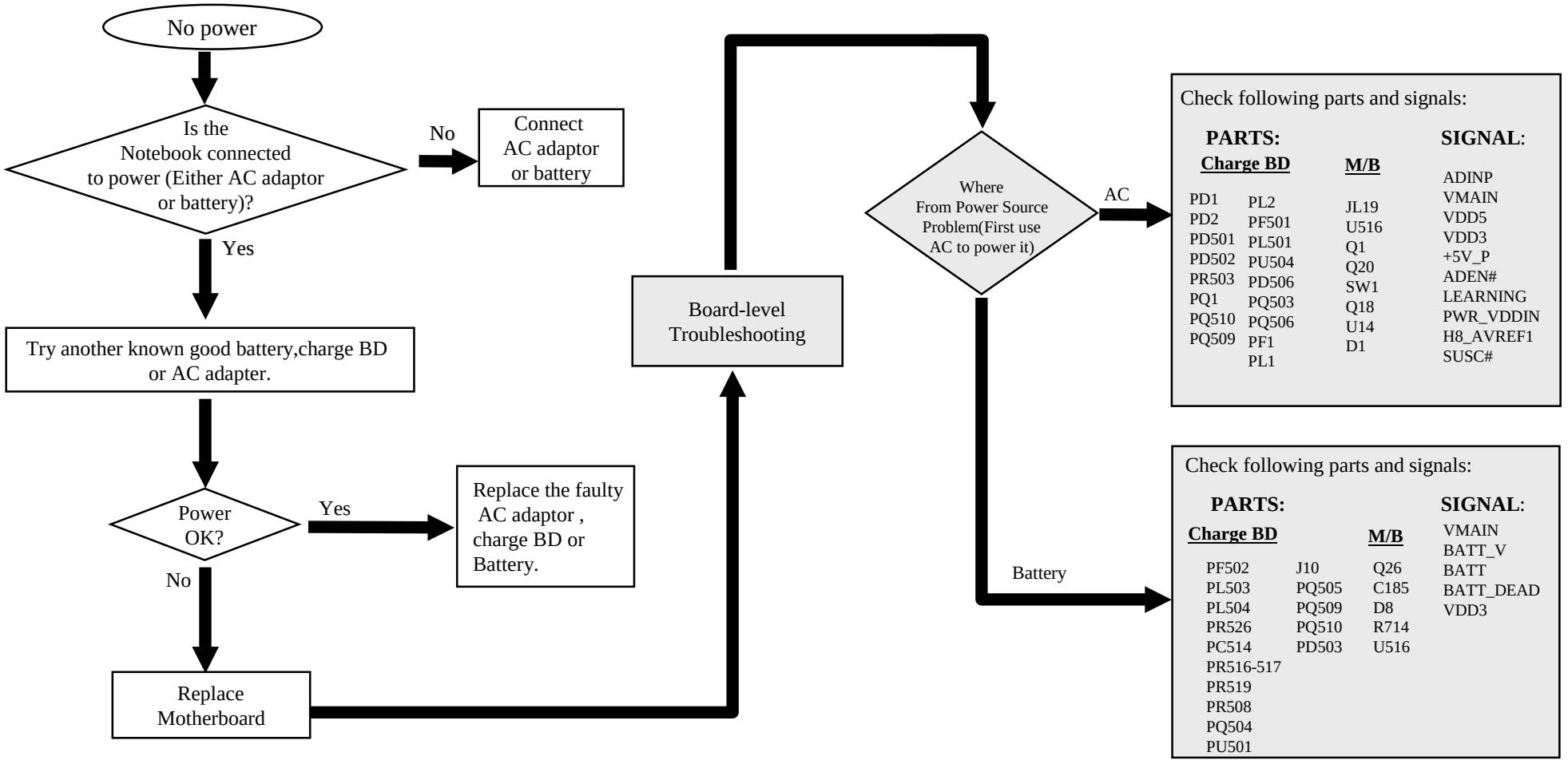
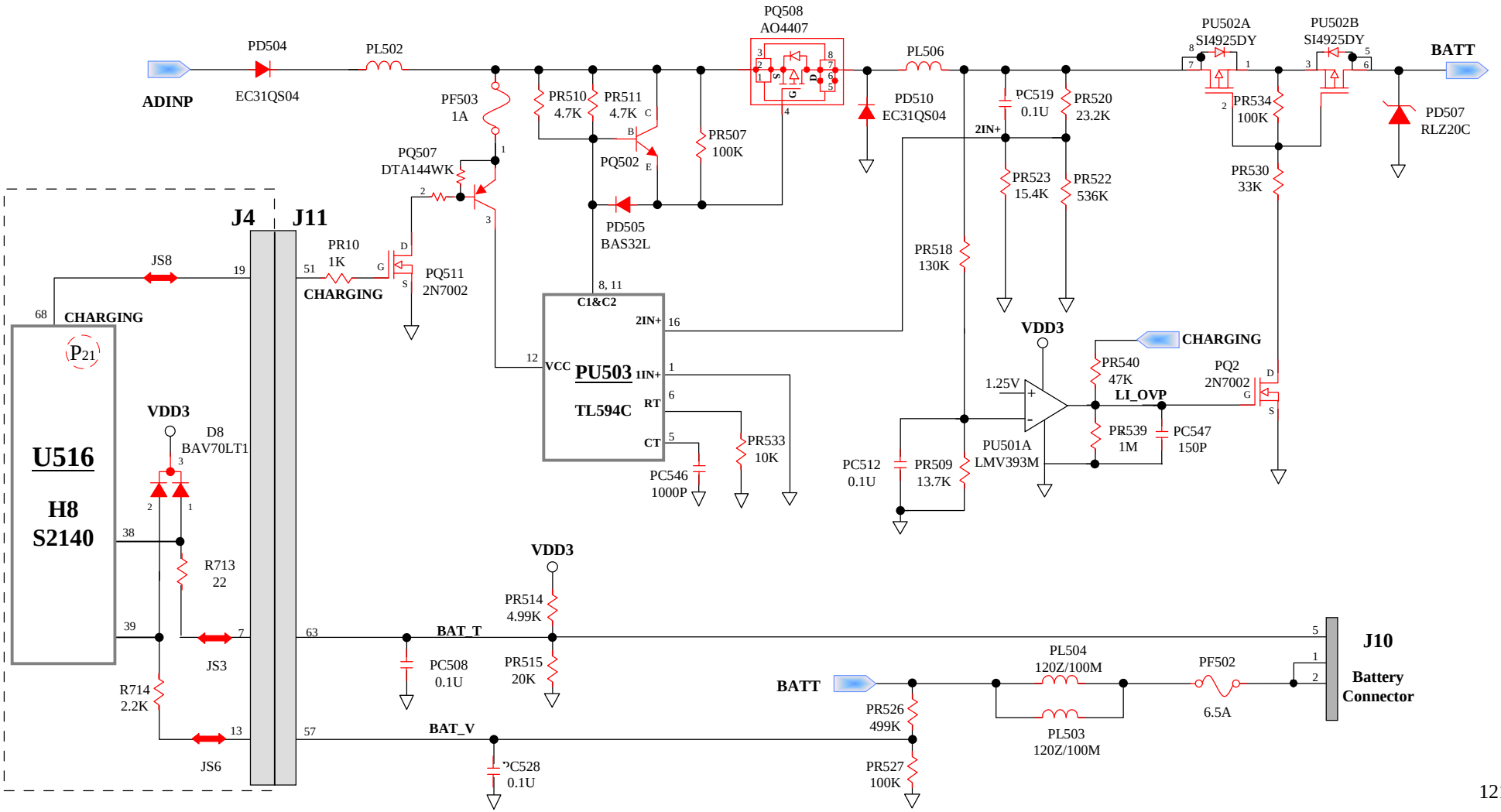


8.2 Battery Can not Be Charged

Symptom:

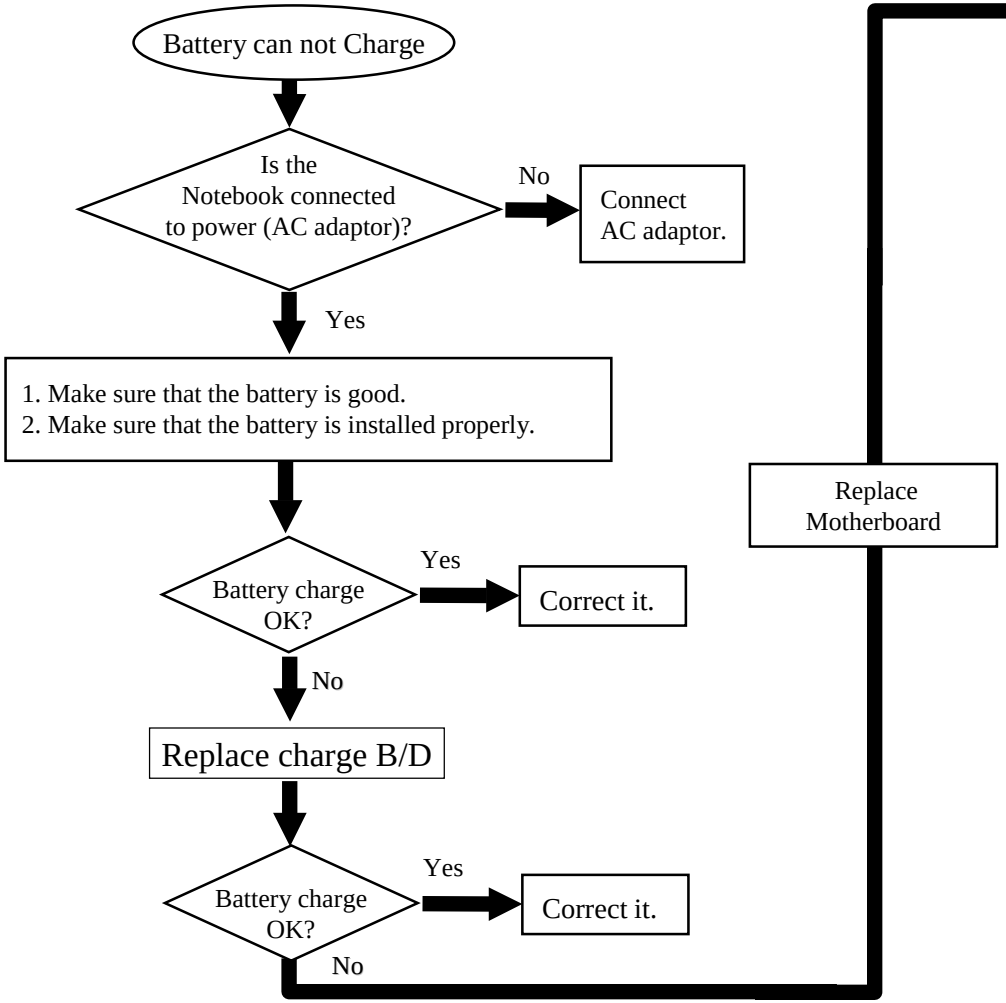
When the battery is installed but the battery status indicate LED display abnormal.



8.2 Battery Can not Be Charged

Symptom:

When the battery is installed but the battery status indicate LED display abnormal.



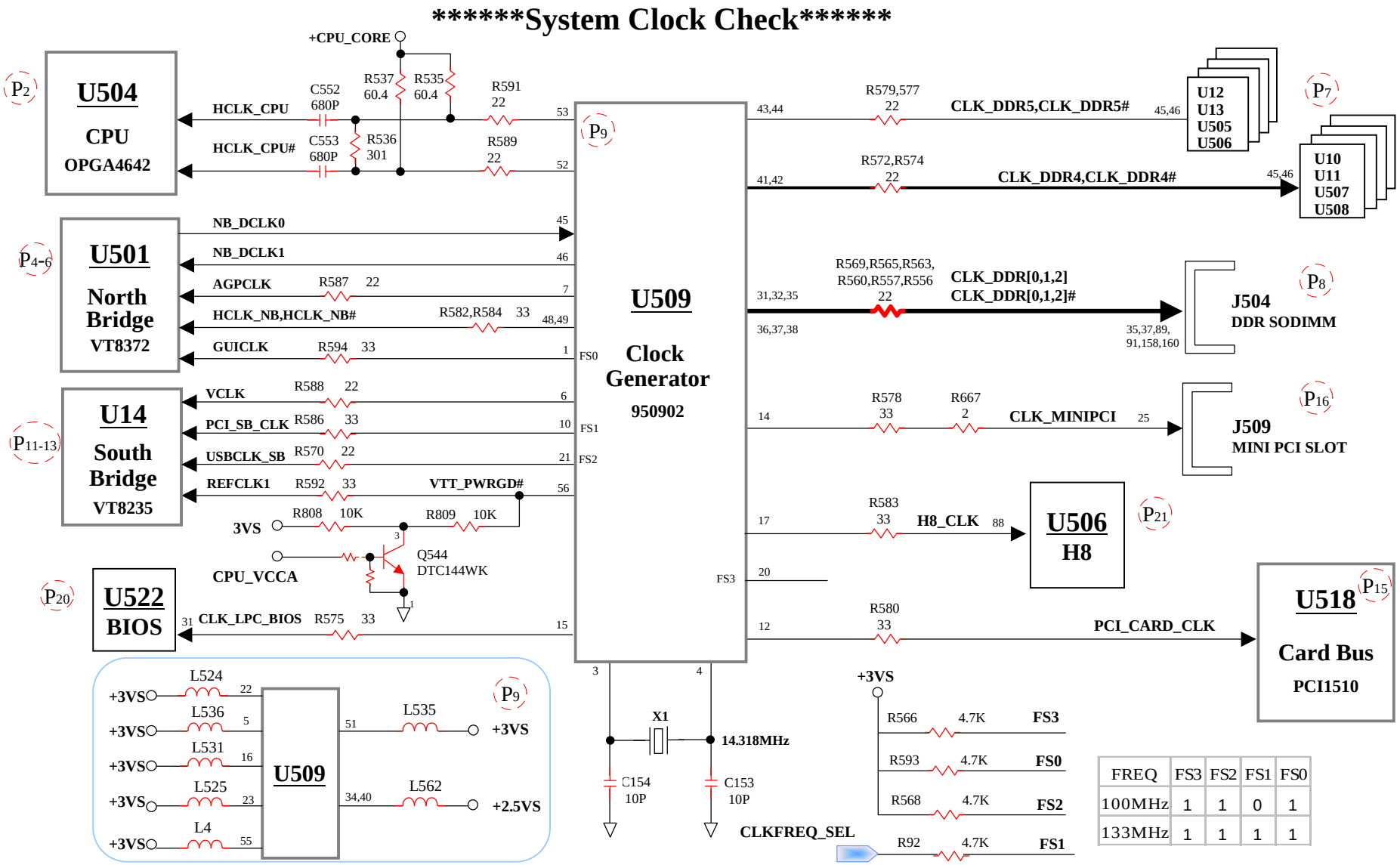
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the **mother-board** and **charge BD** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

PARTS			**SIGNAL**	
Charge BD		**M/B**	**Charge BD**	**M/B**
PD504	PQ2	Charge BD	BATT	VDD3
PD505	PQ508	D8	LI_OVP	CHARGING
PD507	PQ511	R713	ADINP	BAT_T
PD510	PU501	R714	CHARGING	BAT_V
PL502	PU502	U516	BAT_T	
PL503	PU503	J4	BAT_V	
PL506	PF502			
	PF503			

8381 N/B Maintenance

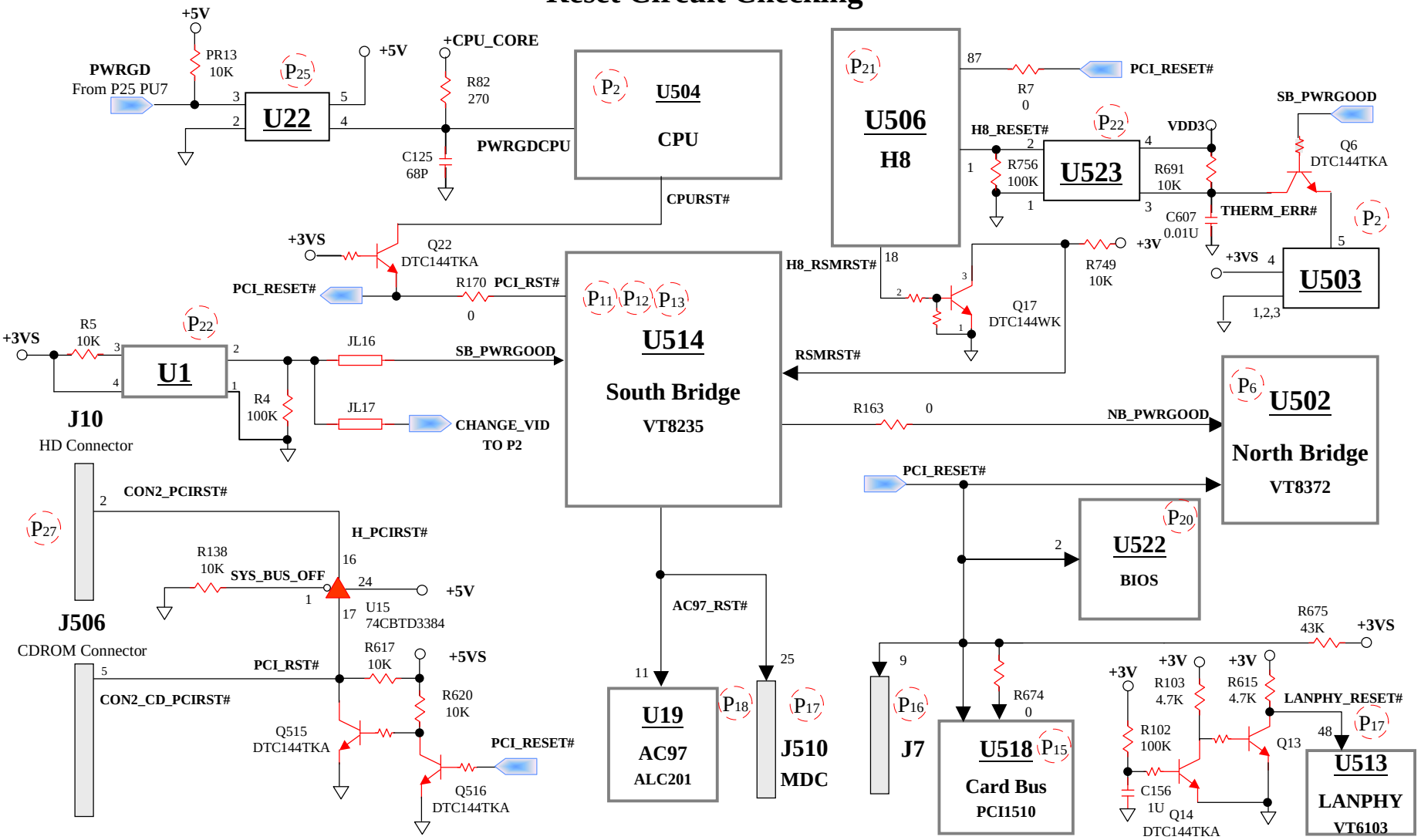
8.3 No Display (System Failure)



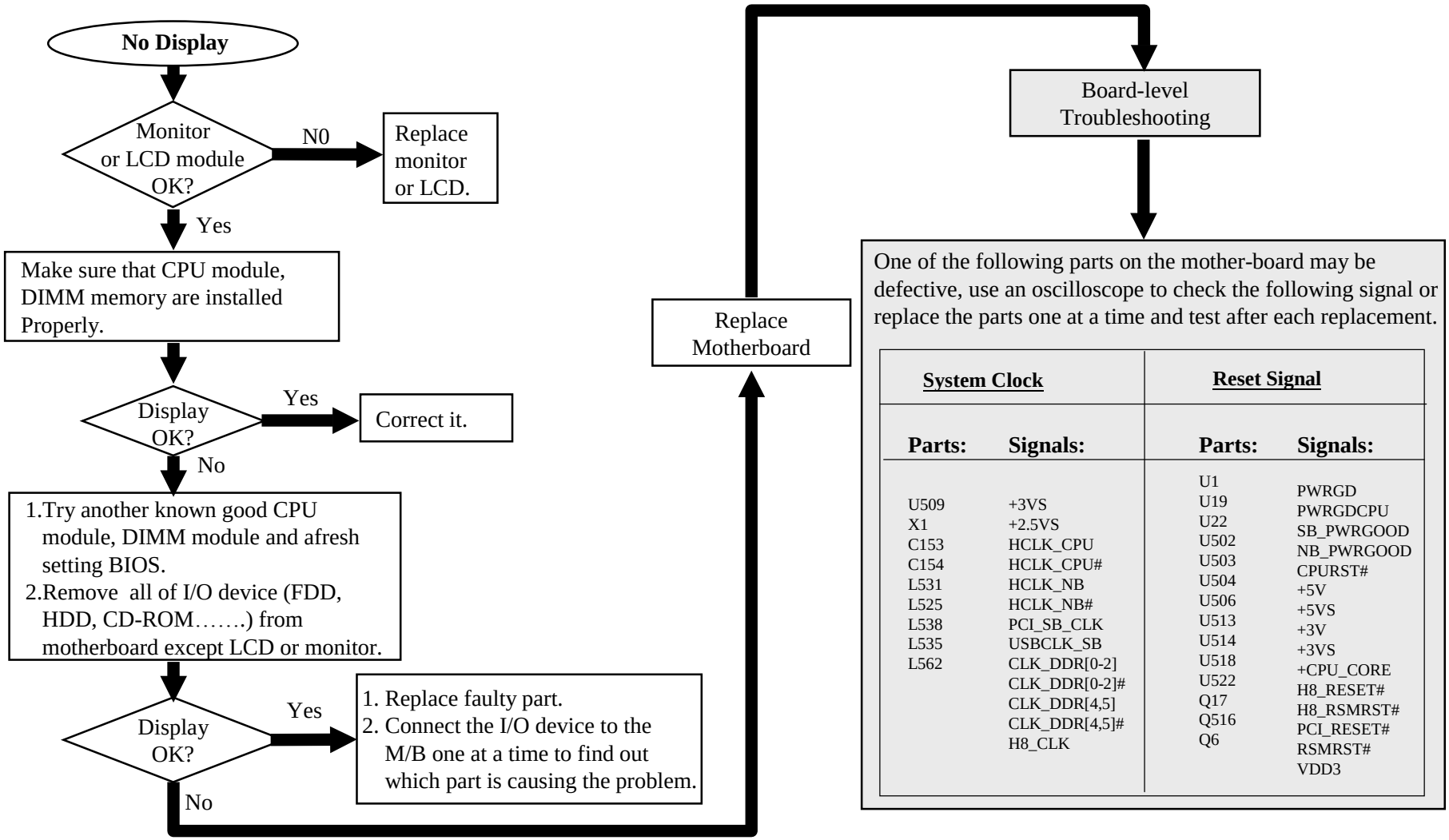
8381 N/B Maintenance

8.3 No Display (System Failure)

********Reset Circuit Checking********



8.3 No Display (System Failure)

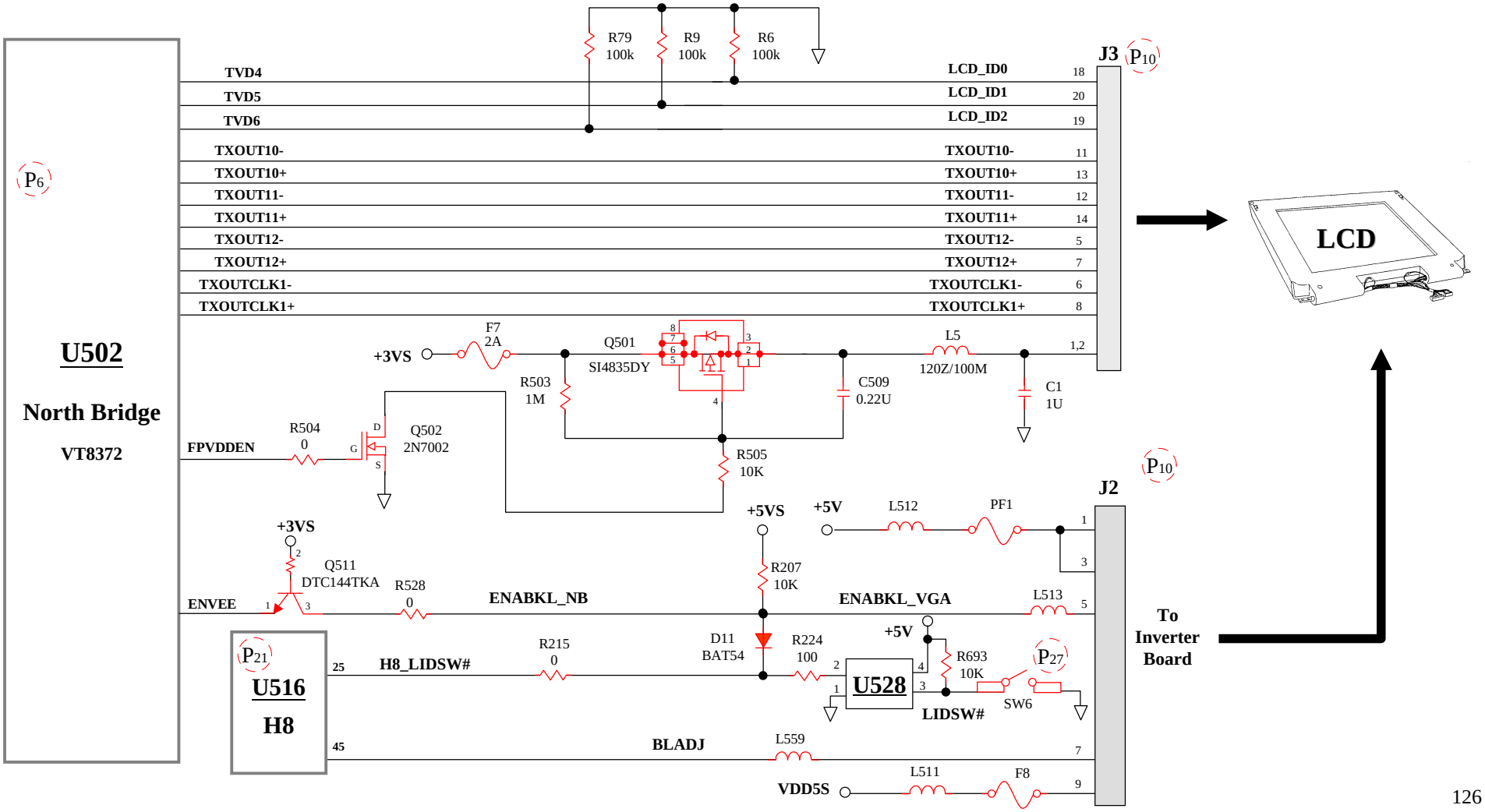


8381 N/B Maintenance

8.4 VGA Controller Failure LCD No Display

Symptom:

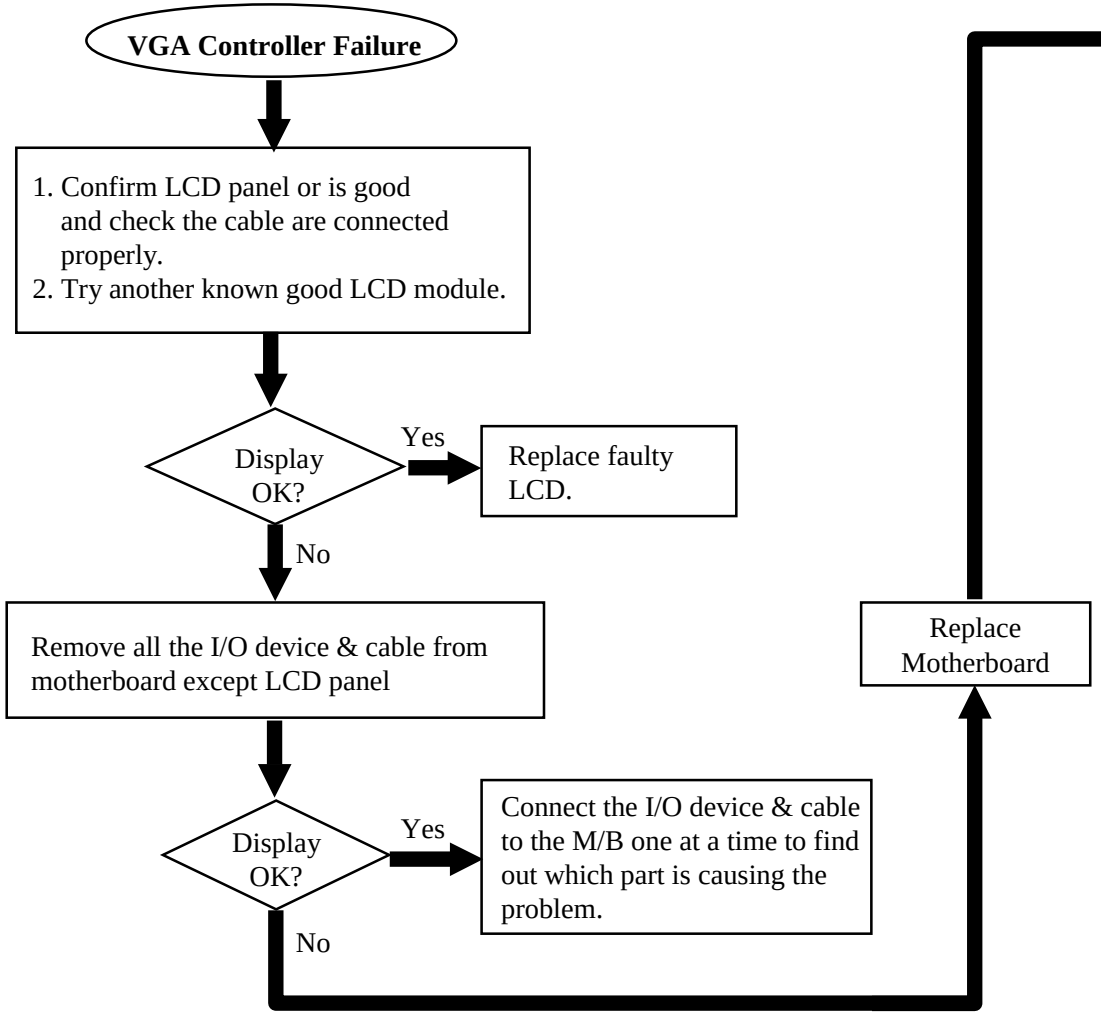
There is no display on LCD although power-on-self-test is passed.



8.4 VGA Controller Failure LCD No Display

Symptom:

There is no display on LCD although power-on-self-test is passed.



Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

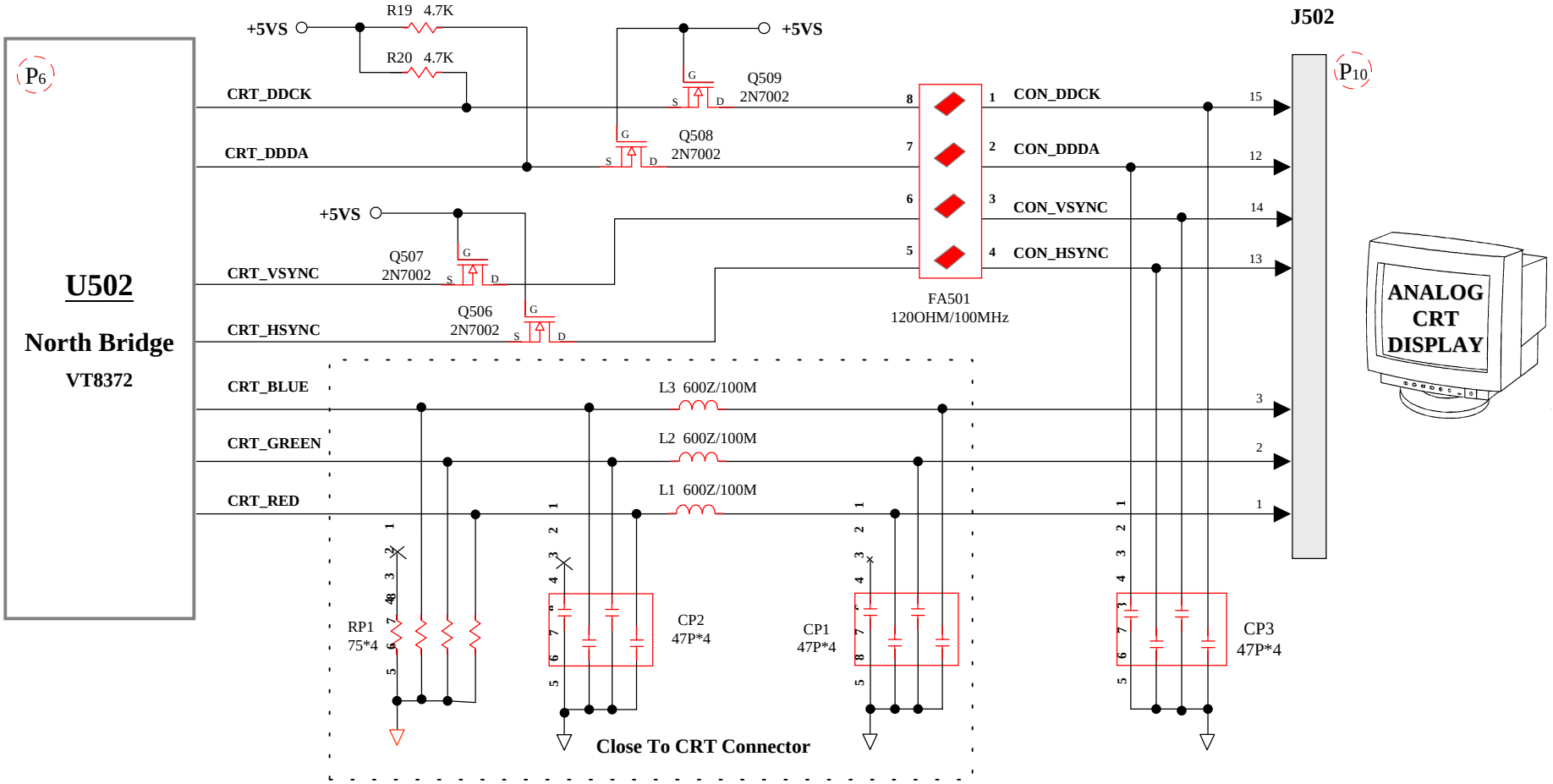
Parts:		**Signals:**	
U502	L513	TXOUTCLK1+	LCD-ID0
U506	L5	TXOUTCLK1-	LCD_ID1
Q501	F7	TXOUT10+	LCD_ID2
Q502	J2	TXOUT10-	H8_LIDSW#
Q511	J3	TXOUT11+	ENABKL_VGA
D11	PR529	TXOUT11-	BLADJ
L559	R224	TXOUT12+	
R208	R528	TXOUT12-	
PF1	R207	FPVDDEN	
F8		ENVEE	

8381 N/B Maintenance

8.5 External Monitor No Display

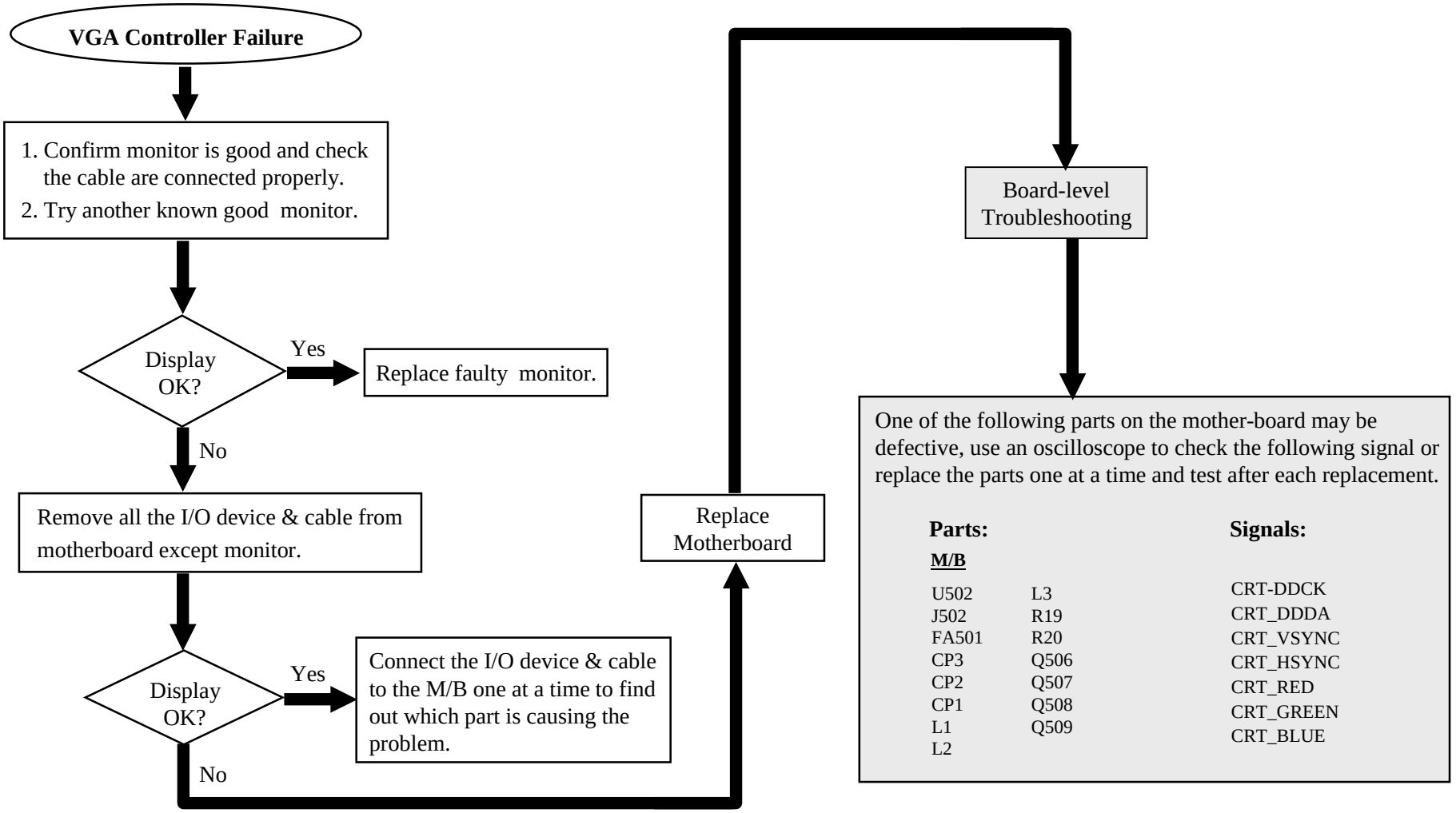
Symptom:

The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



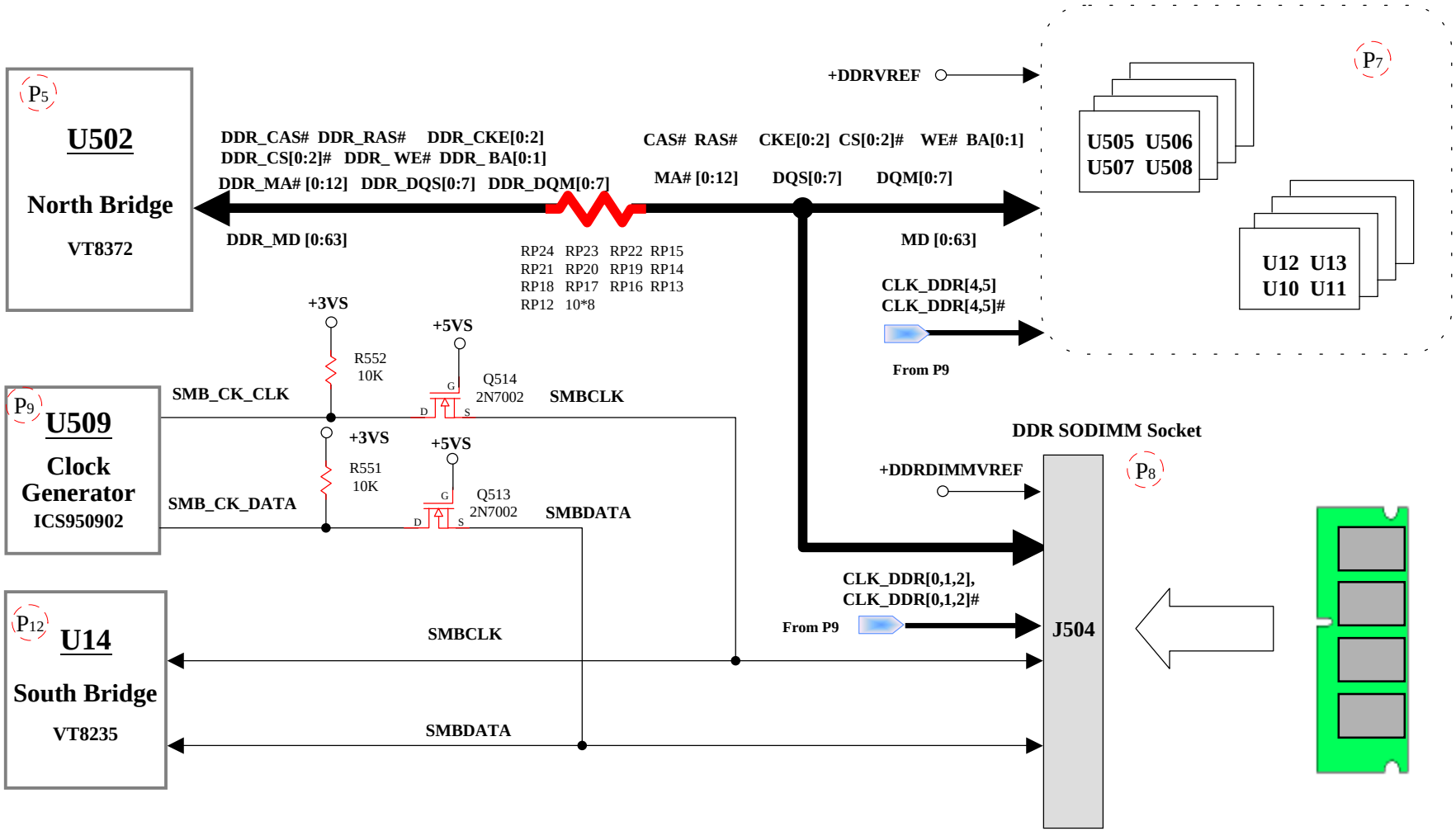
8.5 External Monitor No Display

Symptom:
The CRT monitor shows nothing or abnormal color, but it is OK for LCD.



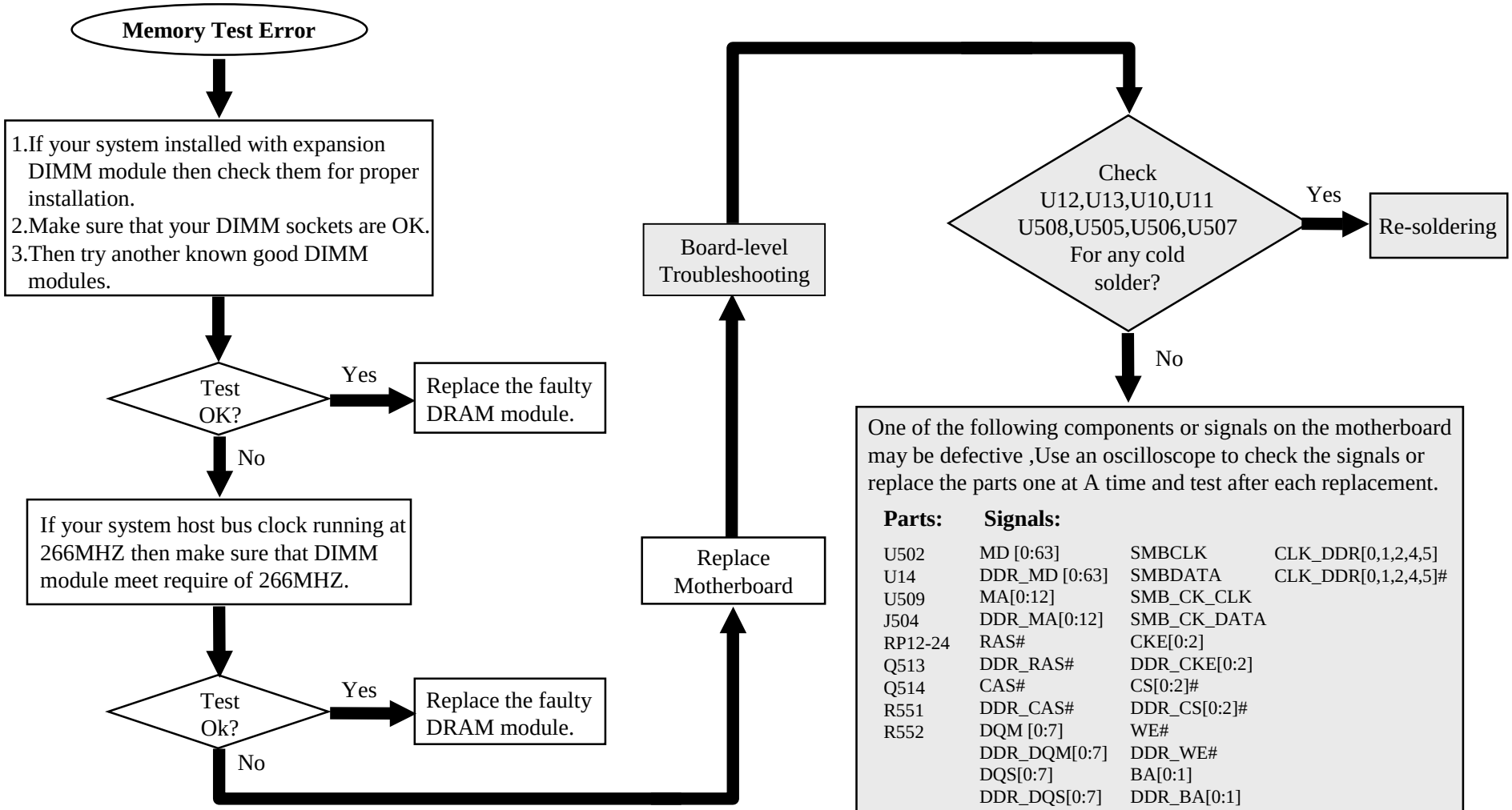
8.6 Memory Test Error

Symptom:
Either on board or extend DDR RAM is failure or system hangs up.



8.6 Memory Test Error

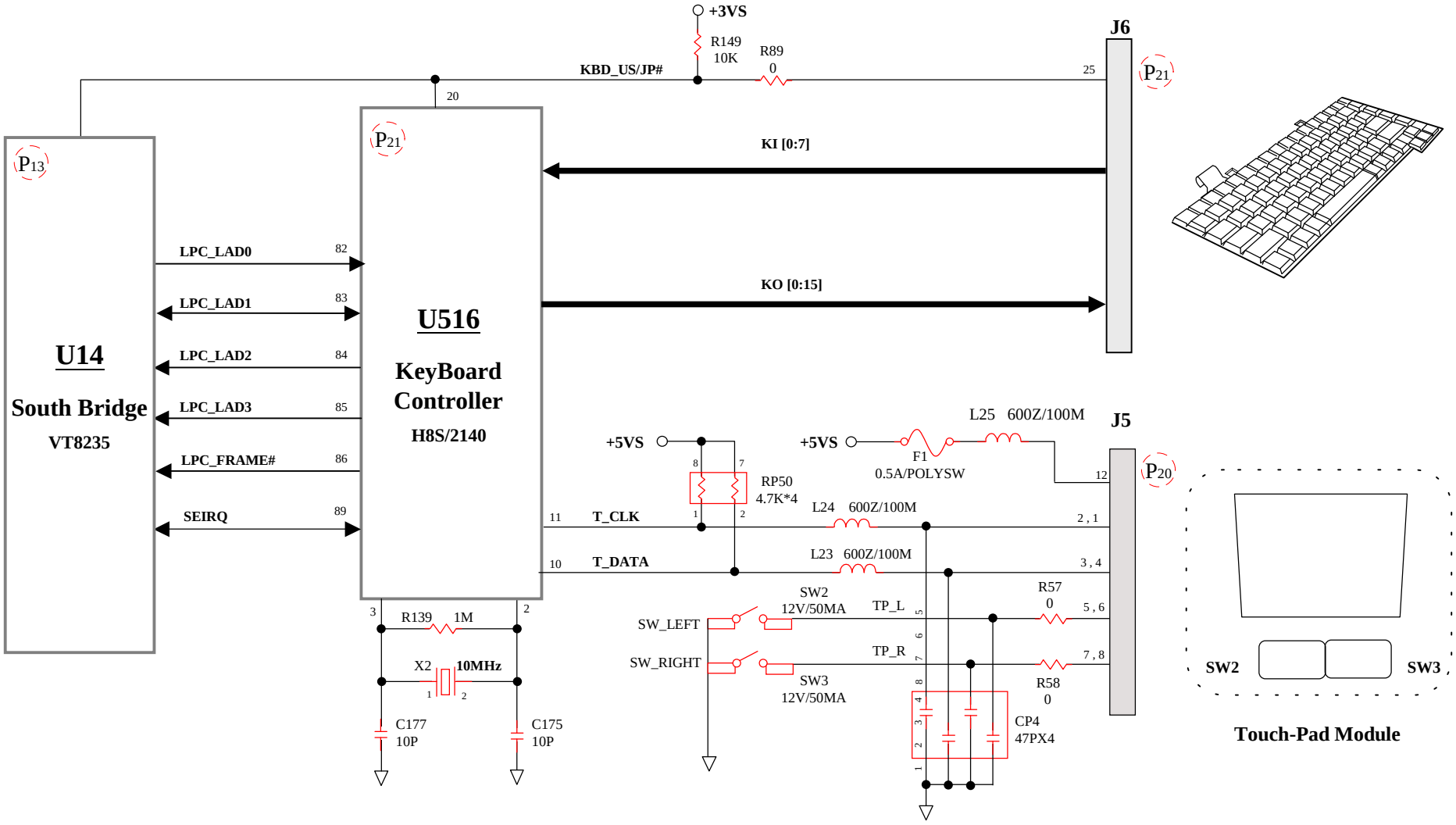
Symptom:
Either on board or extend DDR RAM is failure or system hangs up.



8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

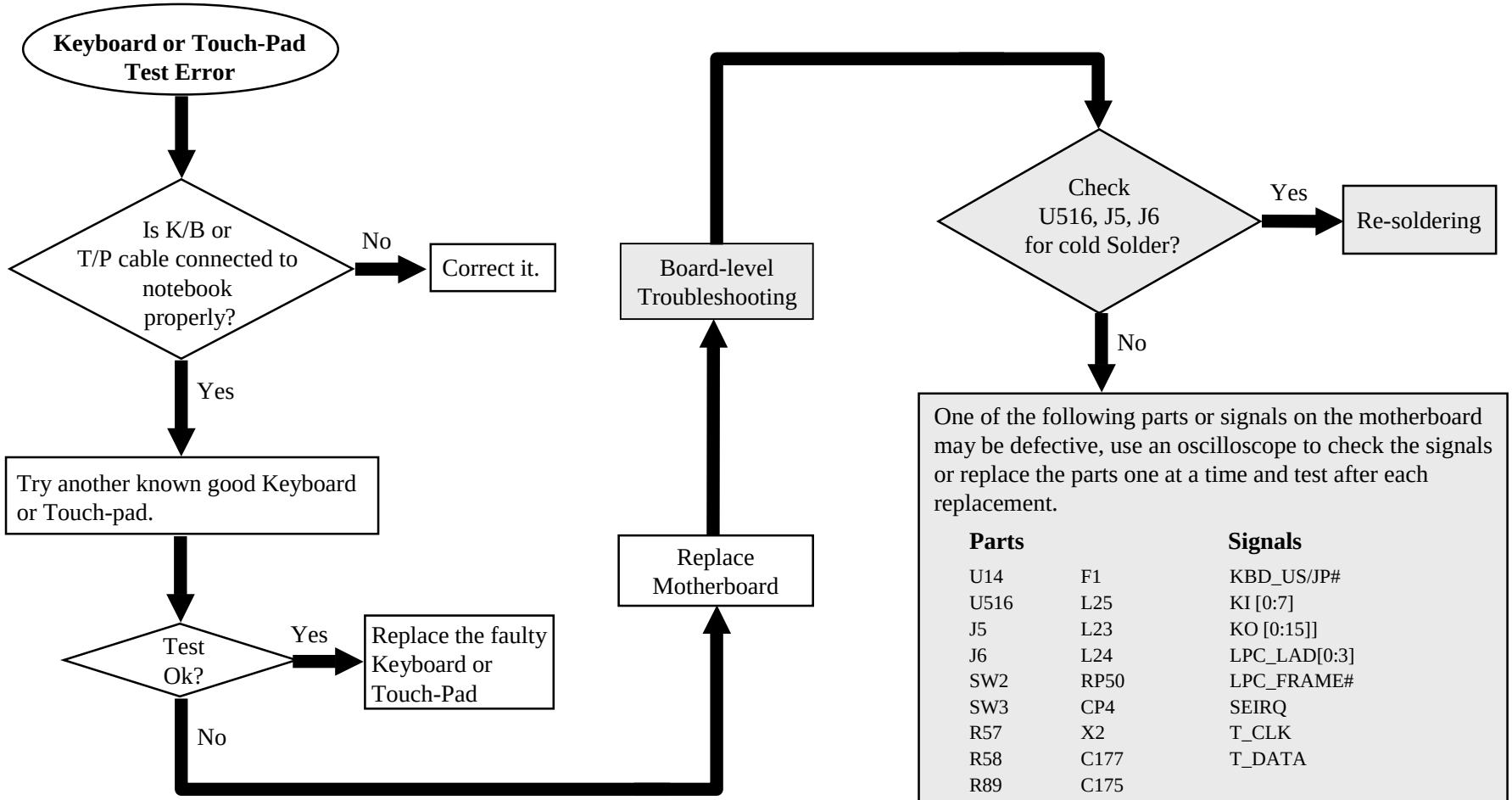
Symptom:

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Keyboard (K/B) Touch-Pad (T/P) Test Error

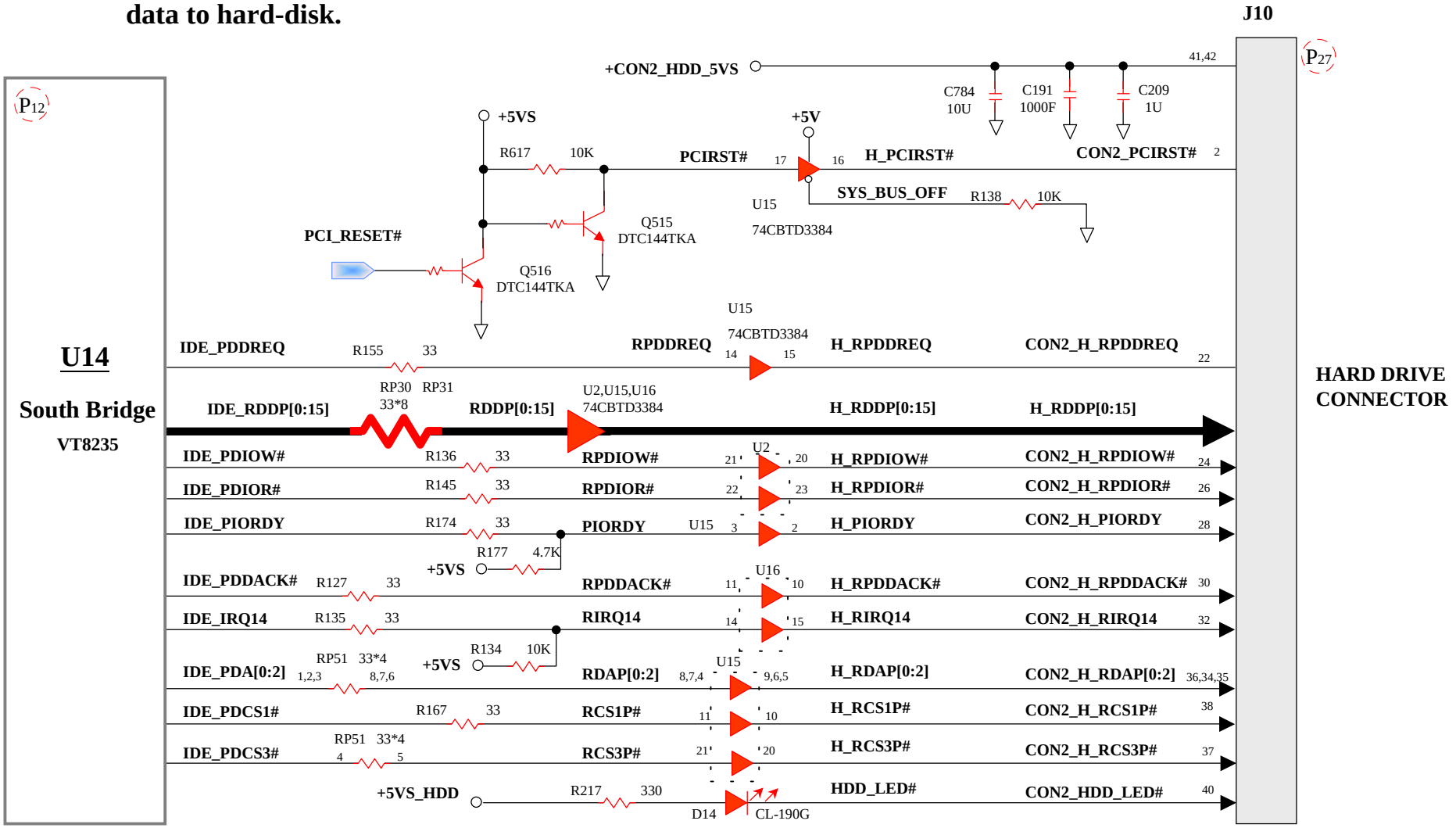
Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.8 Hard Disk Driver Test Error

Symptom:

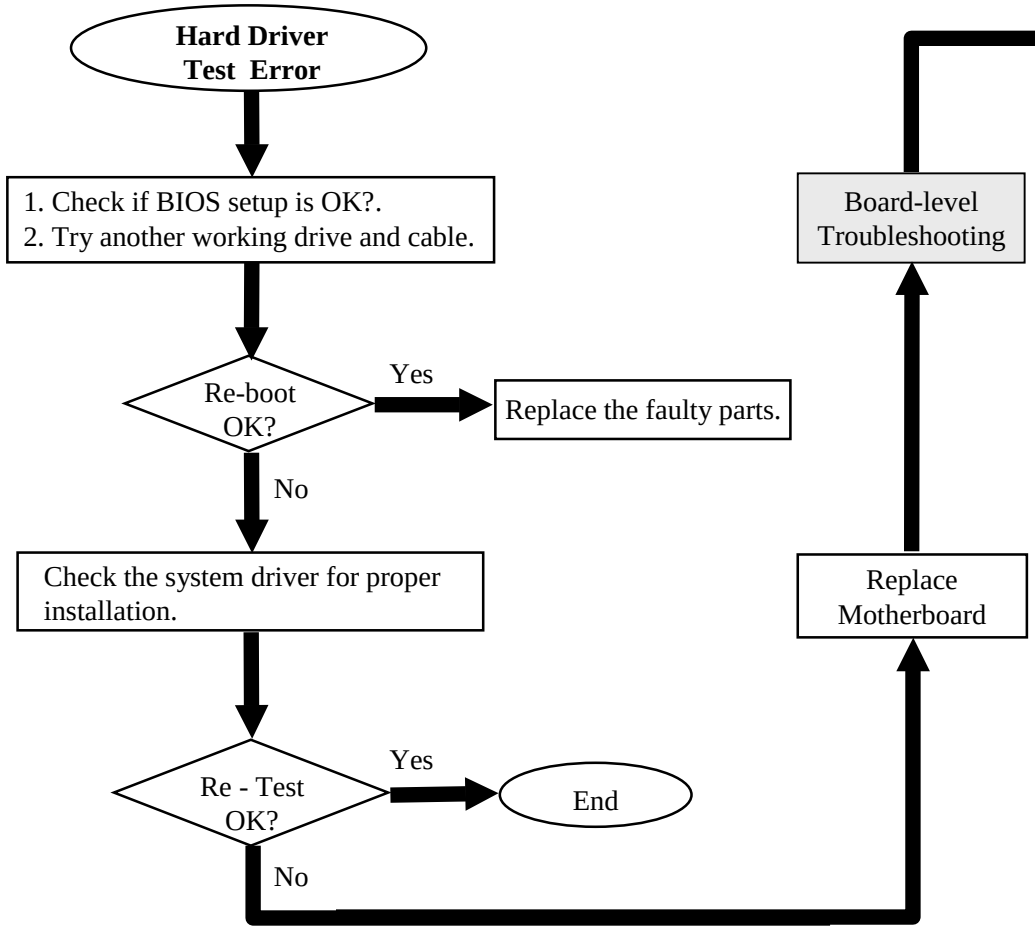
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



8.8 Hard Disk Driver Test Error

Symptom:

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:		SIGNALS:
U14	R217	H_RIRQ14
J10	D14	H_RPDDACK#
Q515	RP37	H_PIORDY
Q516	RP42	H_RPDLOW#
R617	RP45	H_RPDLOR#
R155	RP46	H_RPDDREQ
R136	RP531	H_RDDP[0:15]
R145	RP532	HDD_LED#
R174	U2	H_RCS3P#
R177	U15	H_RCS1P#
R127	U16	H_RDAP[0:2]
R135	R138	H_PCIRST#
RP51	Q546	USB+
R167		USB-
R134		

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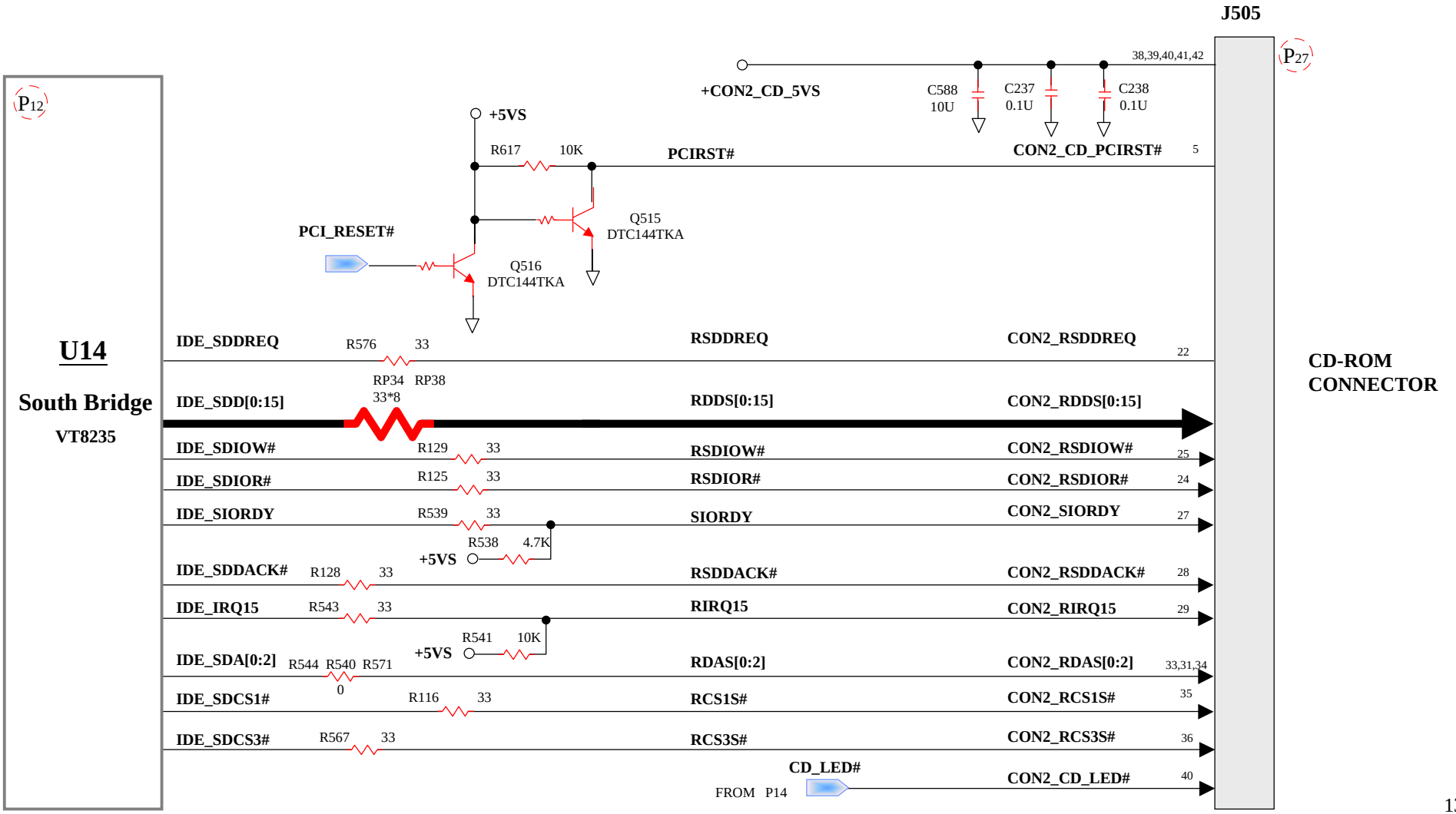
8.9 CD-ROM Driver Test Error

Symptom:

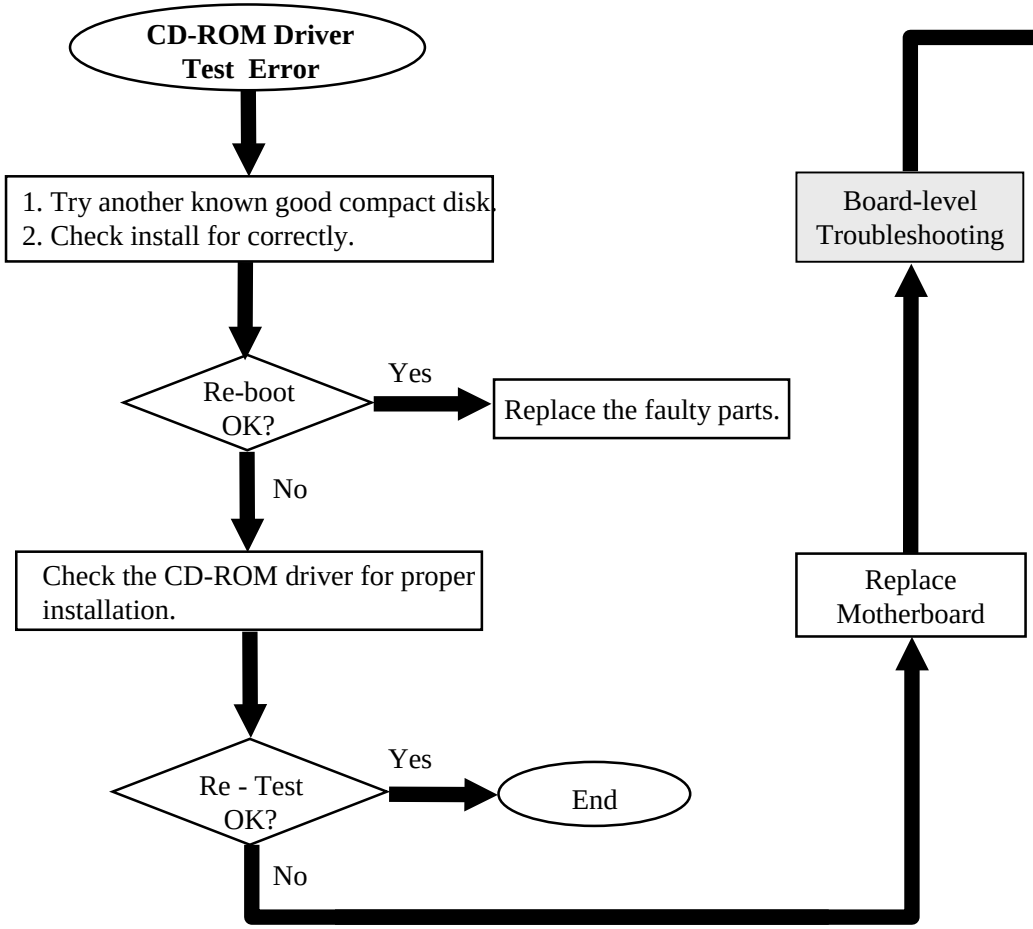
An error message is shown when reading data from CD-ROM drive.



8.9 CD-ROM Driver Test Error

Symptom:

An error message is shown when reading data from CD-ROM drive.

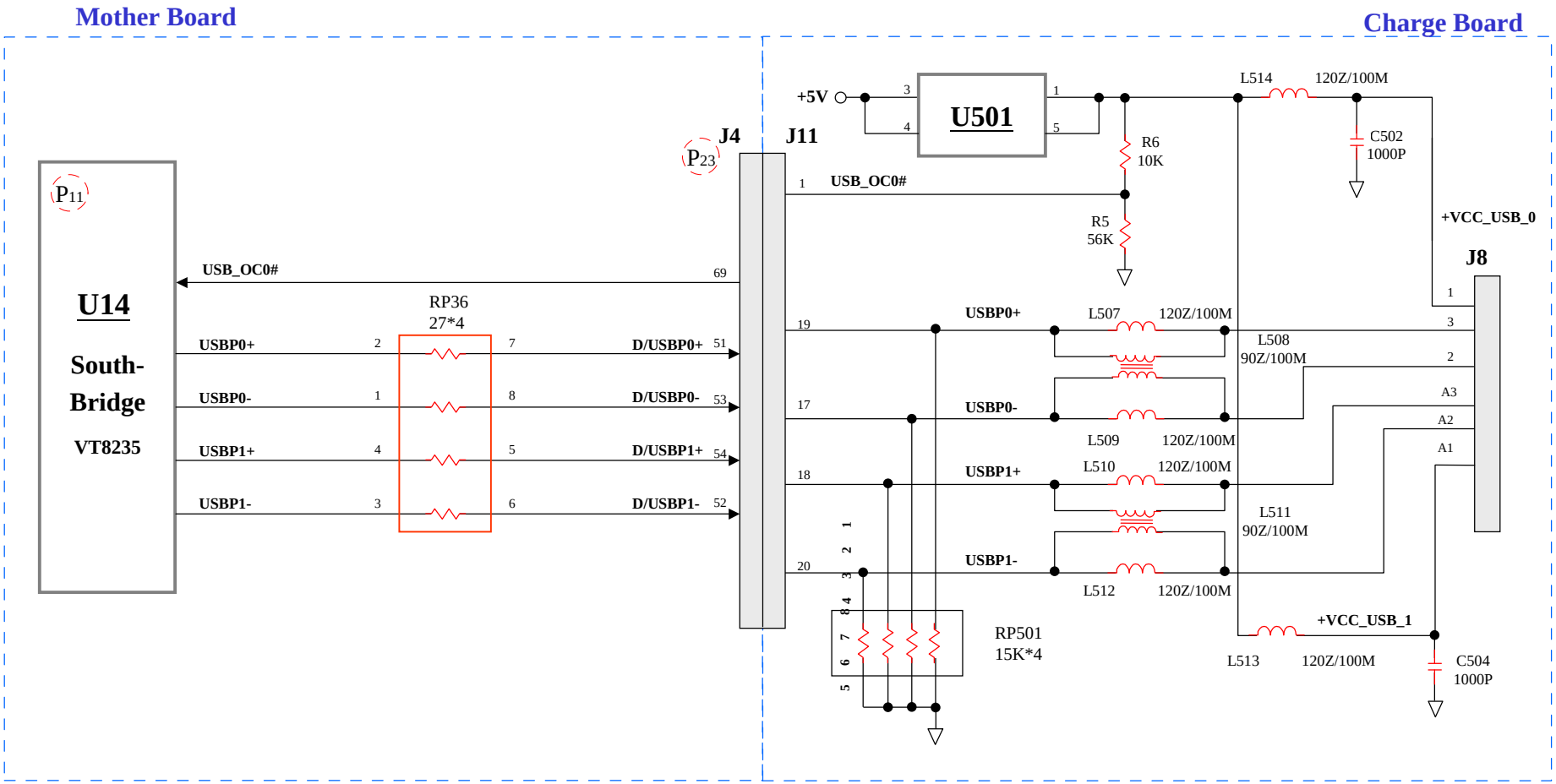


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

PARTS:		SIGNALS:
U14	R617	+CON2_CD_5VS
J505	R576	CON2_CD_PCIRST#
Q515	R129	CON2_RDDS[0:15]
Q516	R125	CON2_RSDIOW#
RP5	R539	CON2_SIORDY
RP34	R538	CON2_RIRQ15
RP38	R128	CON2_RDAS[0:2]
R116	R543	CON2_RCS1S#
R567	R541	CON2_RCS3S#
	R544	CON2_CD_LED#
	R540	CON2_RSDDACK#
	R571	CON2_RSDIOR#
		CON2_RSDDREQ

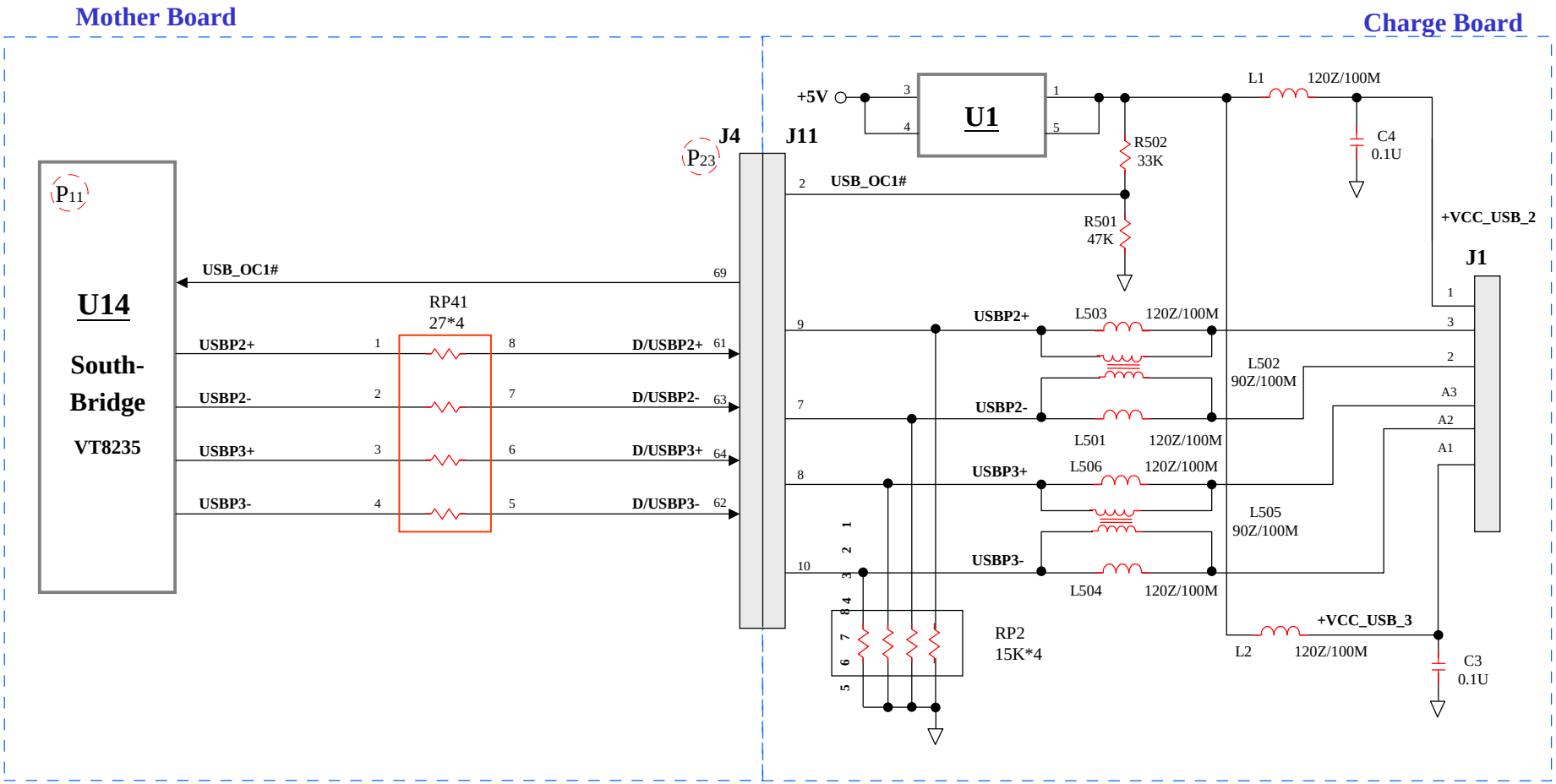
8.10 USB Test Error (1)

Symptom:
An error occurs when a USB I/O device is installed.



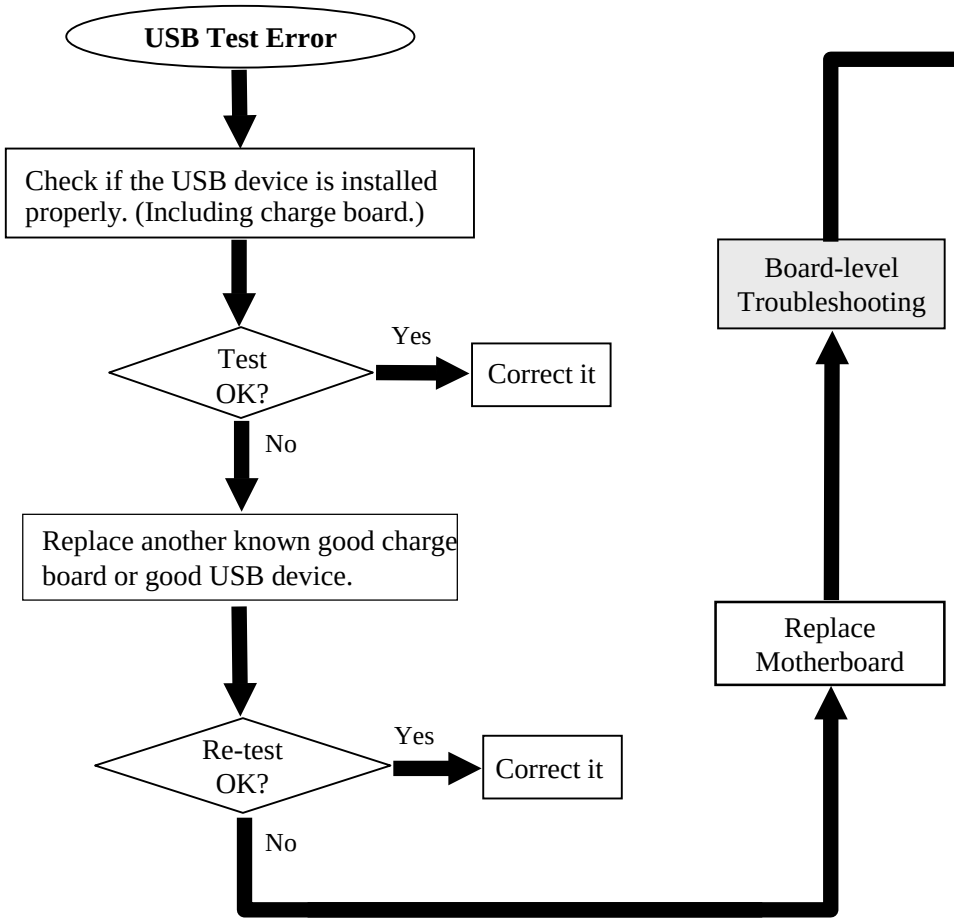
8.10 USB Test Error (2)

Symptom:
An error occurs when a USB I/O device is installed.



8.10 USB Test Error

Symptom:
An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the MB and Charge BD may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:			**Signals:**	
M/B	**Charge Board**			
U14 J4 RP36 RP41	J11 J1 J8 U501 U1 R5 R6 R501 R502	L1 L2 L501-514 C502 C504 C3 C4 RP2 RP501	USB_OC1# USB_OC0# USBP0+ USBP0- USBP1+ USBP1- D/USBP0+ D/USBP0- D/USBP1+ D/USBP1- +5V	USBP2+ USBP2- USBP3+ USBP3- D/USBP2+ D/USBP2- D/USBP3+ D/USBP3-

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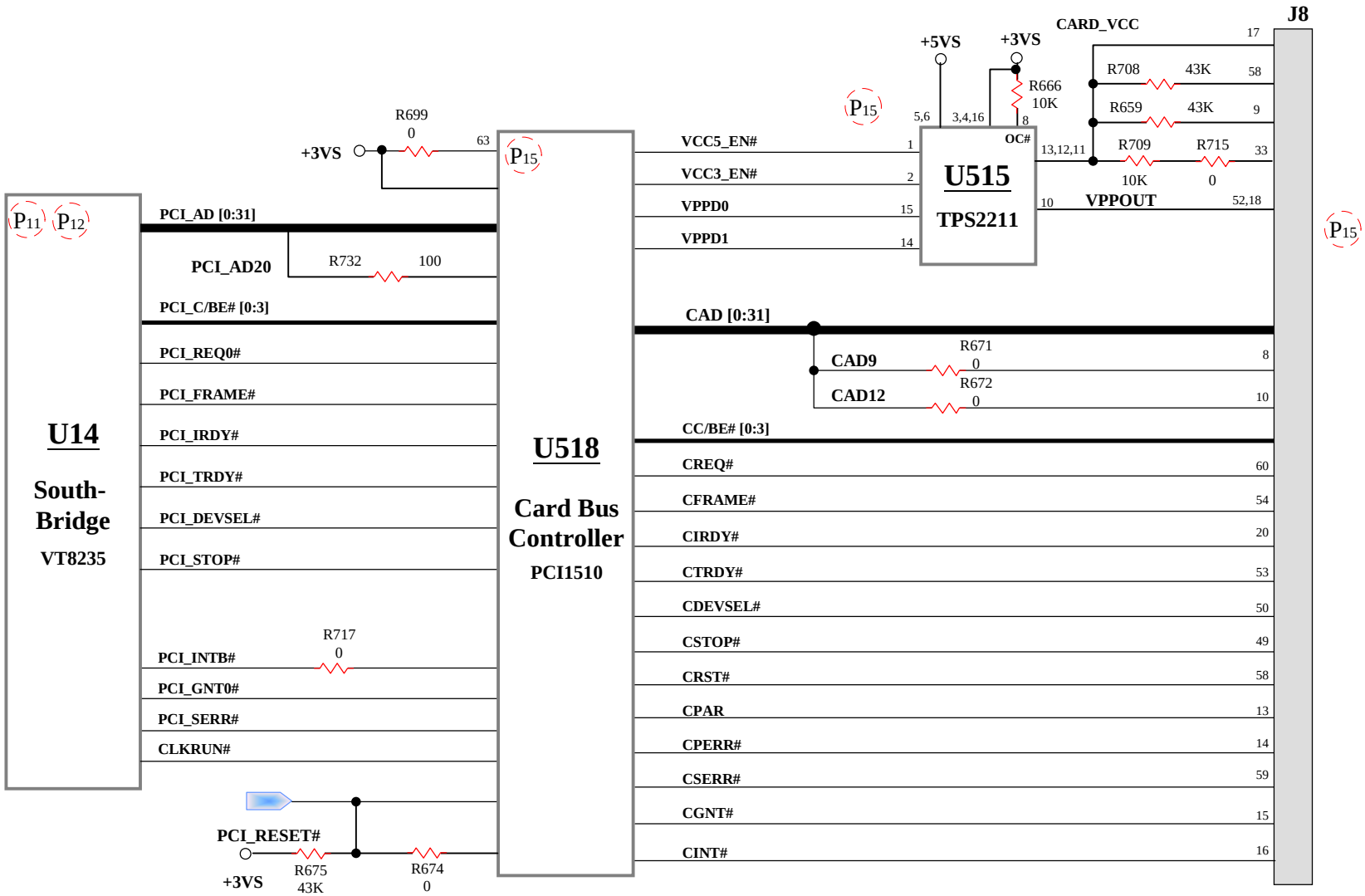
8.11 PC-Card Socket Failure

Symptom :

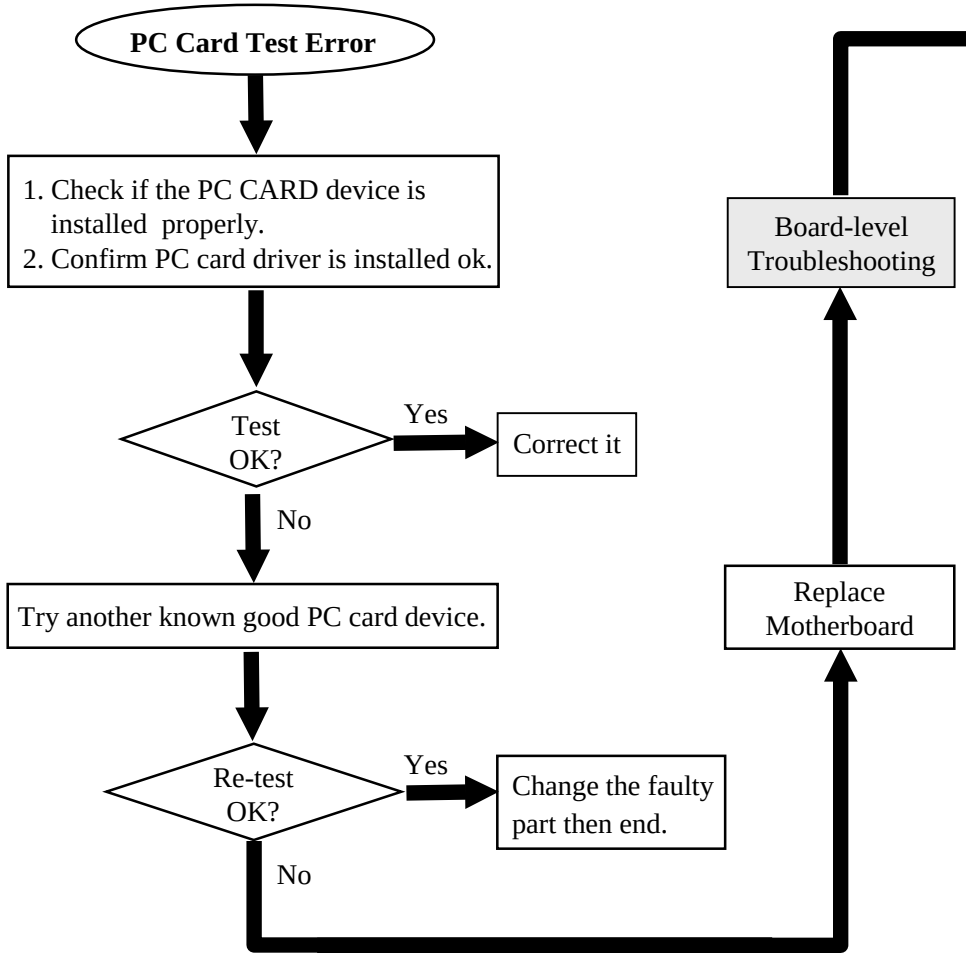
An error occurs when a PC card device is installed.



8.11 PC-Card Socket Failure

Symptom :

An error occurs when a PC card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U518
U14
U515
J8
R659
R708
R709
R666
R715
R671
R672
R674
R675
R717
R732

Signals

PCI_AD[0:31]	CAD[0:31]	VCC5-EN#
PCI_C/BE# [0:3]	CC/BE# [0:3]	VCC3-EN#
PCI_REQ0#	CREQ#	VPPD0
PCI_FRAME#	CFRAME#	VPPD1
PCI_IRDY#	CIRDY#	CARD-VCC
PCI_TRDY#	CTRDY#	VPPOUT
PCI_DEVSEL#	CDEVSEL#	
PCI_STOP#	CSTOP#	
PCI_INTB#	CGNT#	
PCI_RESET#	CRST#	
PCI_GNT0#	CSERR#	
PCI_SERR#	CPAR#	
CLKRUN#	CPERR#	

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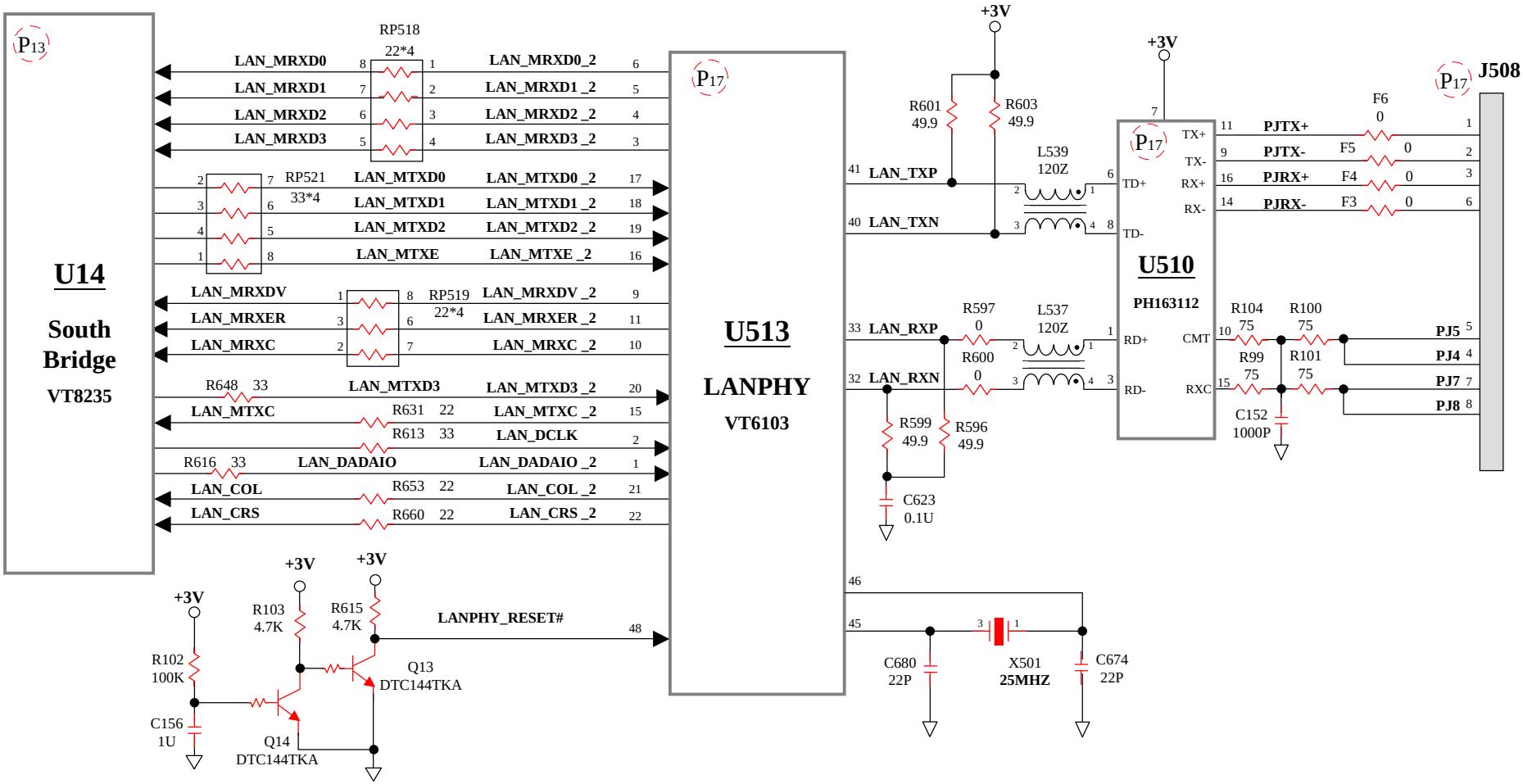
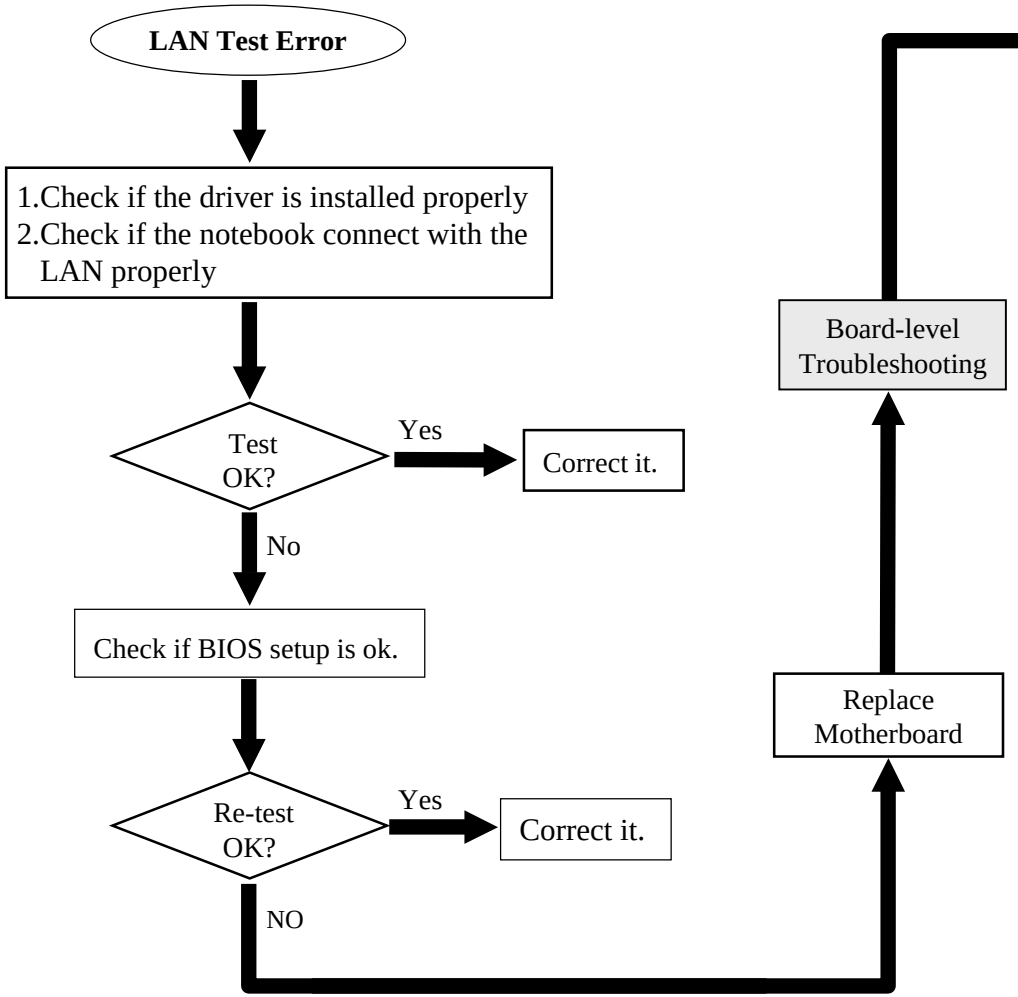
8.12 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



8.12 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



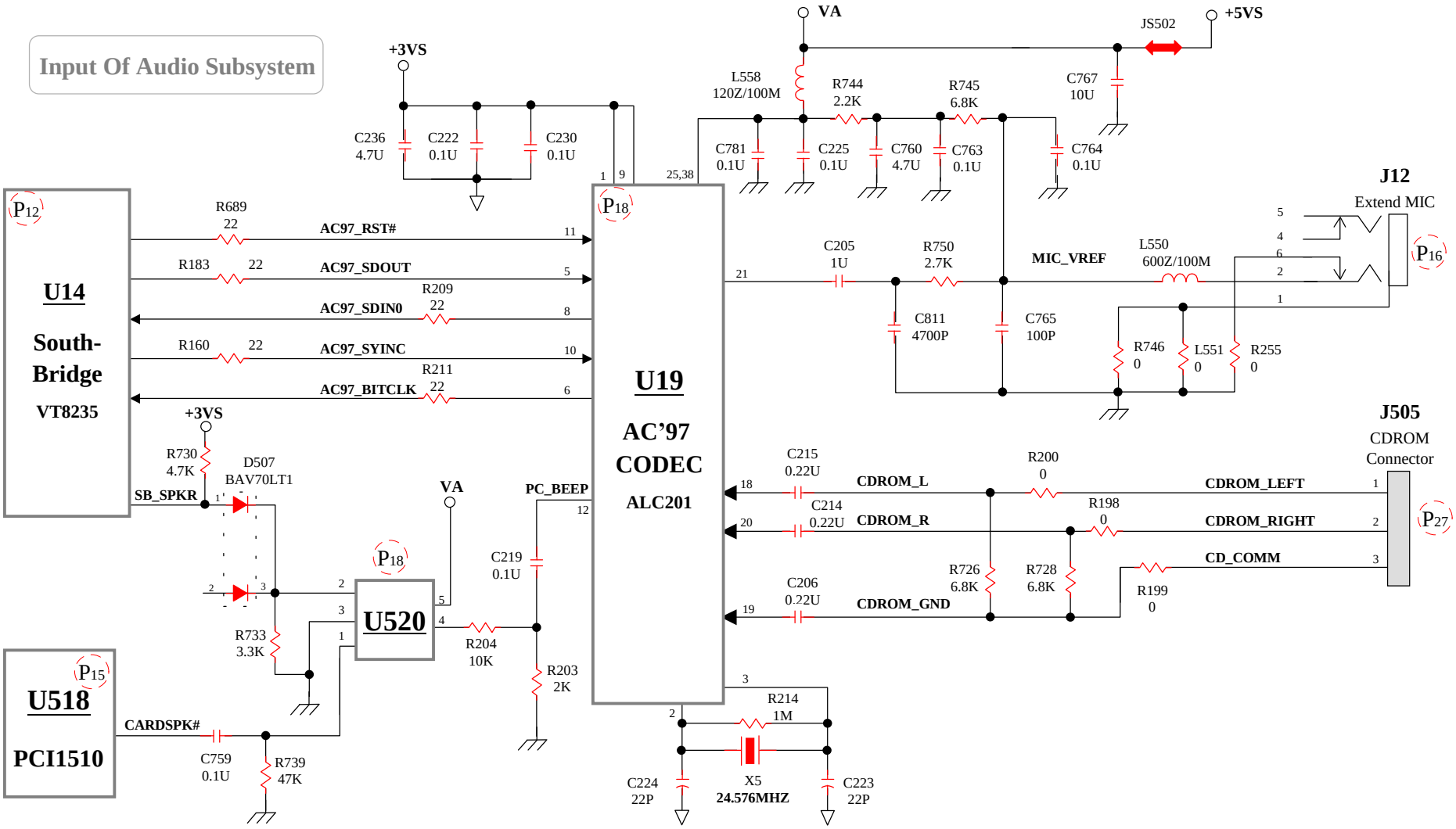
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals**	
U14	J508	LAN_MRXD0	LAN_TXP
U513	F[3-6]	LAN_MRXD1	LAN_TXN
U510	C152	LAN_MRXD2	LAN_RXP
X501	C674	LAN_MRXD3	LAN_RXN
RP518	C680	LAN_MRXDV	PJTX+
RP521		LAN_MRXER	PJTX-
RP519		LAN_MRXC	PJRX+
R[595-604]		LAN_MTXD0	PJRX-
R648		LAN_MTXD1	PJ5
R631		LAN_MTXD2	PJ4
R613		LAN_MTXD3	PJ7
R616		LAN_MTXE	PJ8
R653		LAN_MTXC	LAN_COL
R660		LAN_DCLK	LAN_CRS
R[99-101]			LAN_DATAIO
R104			LANPHY_RESET#

8.13 Audio Failure

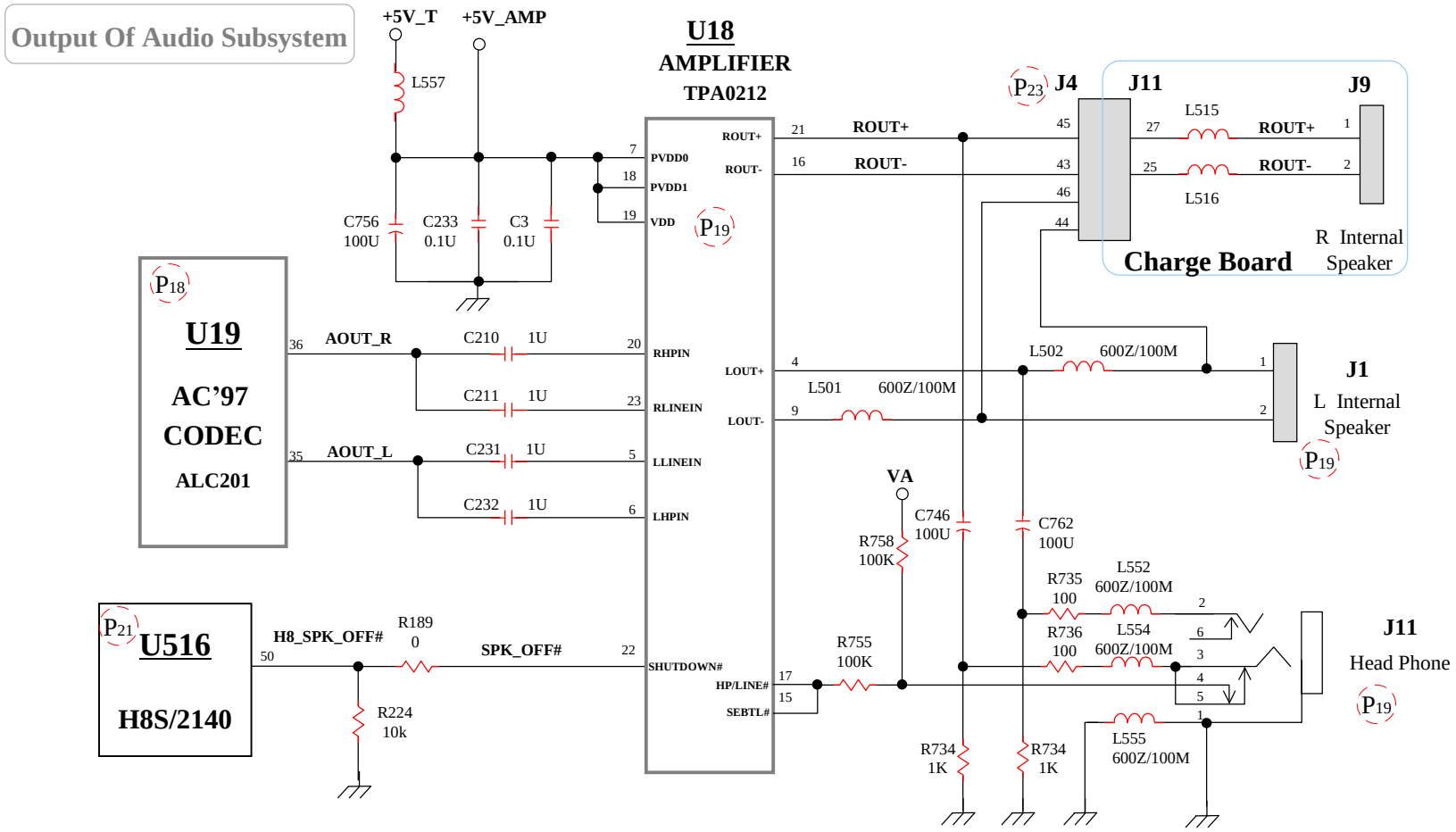
Symptom:

No sound from speaker after audio driver is installed.



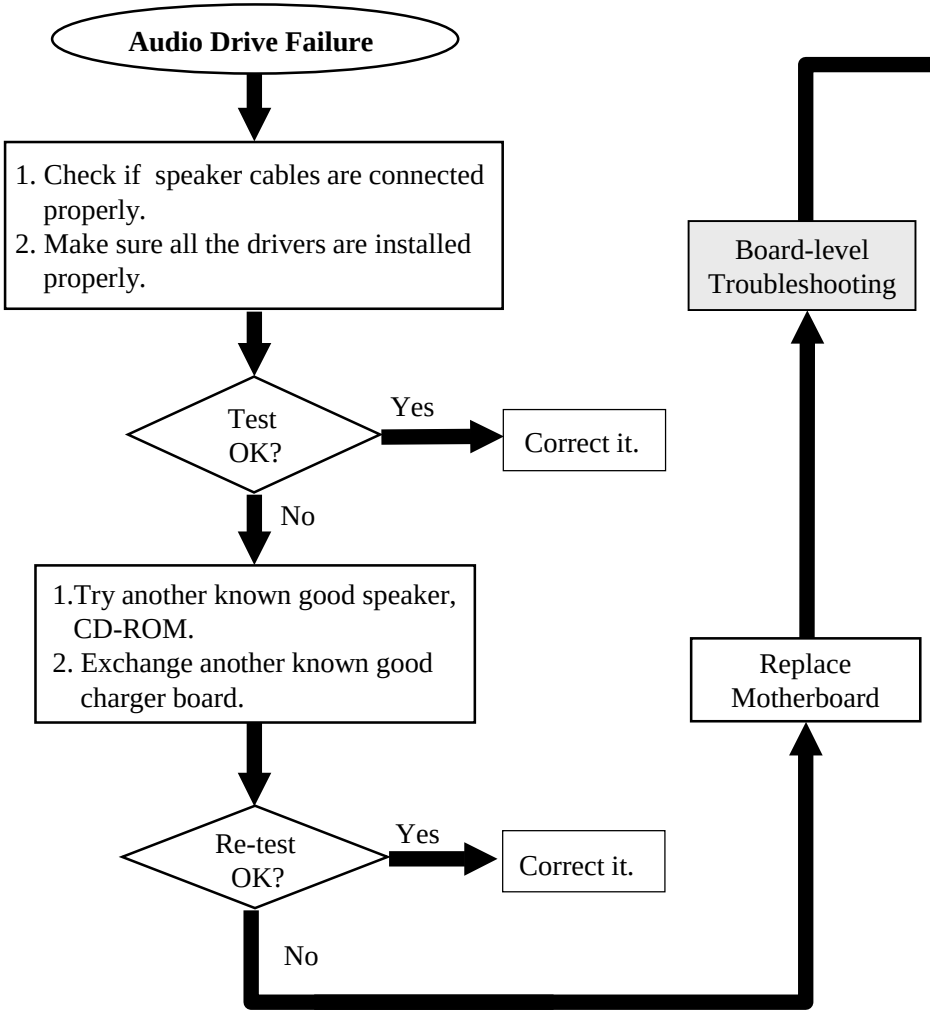
8.13 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



8.13 Audio Failure

Symptom:
No sound from speaker after audio driver is installed.



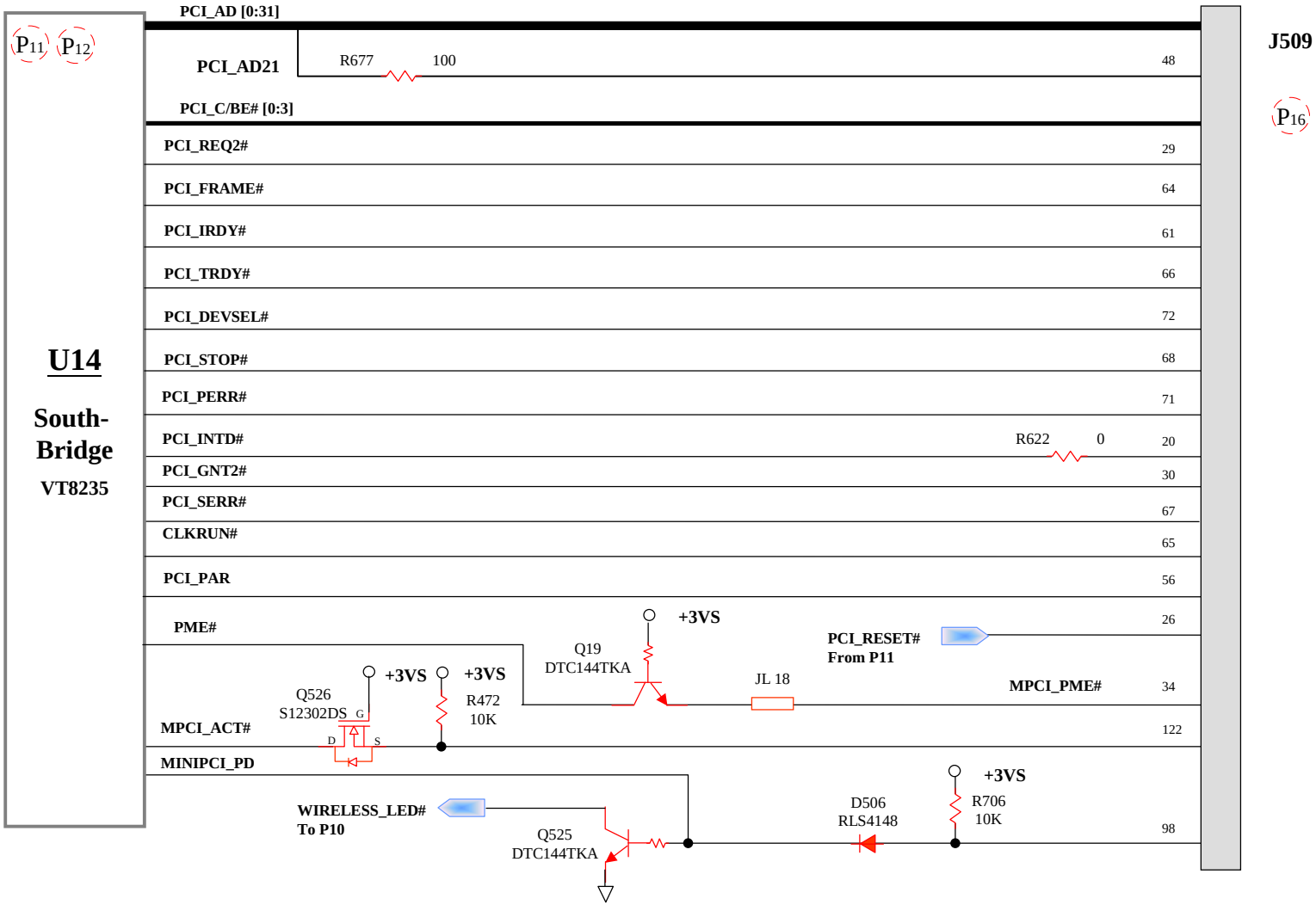
Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:		2. If no sound cause of MIC, check the following parts & signals:		3. If no sound cause of CD-ROM, check the following parts & signals:	
Parts:	**Signals:**	**Parts:**	**Signals:**	**Parts:**	**Signals:**
U14 C211 U19 C231 U518 C232 U516 U18 J4 R189 J1 R224 L501 J11 L502 L554 C210 L552 Charge BD	AOUT_R AOUT_L ROUT+ ROUT- LOUT+ LOUT- SPK_OFF# AC97_RESET	U19 C205 L550 R746 J12 X5	MIC_VREF	U14 U19 C206 C214 C215 R726 R728 RP28 R[198-200] J505	CDROM_L CDROM_R CDROM_GND CDROM_LEFT CDROM_RIGHT CD_COMM

8.14 Mini PCI Test Error

Symptom:

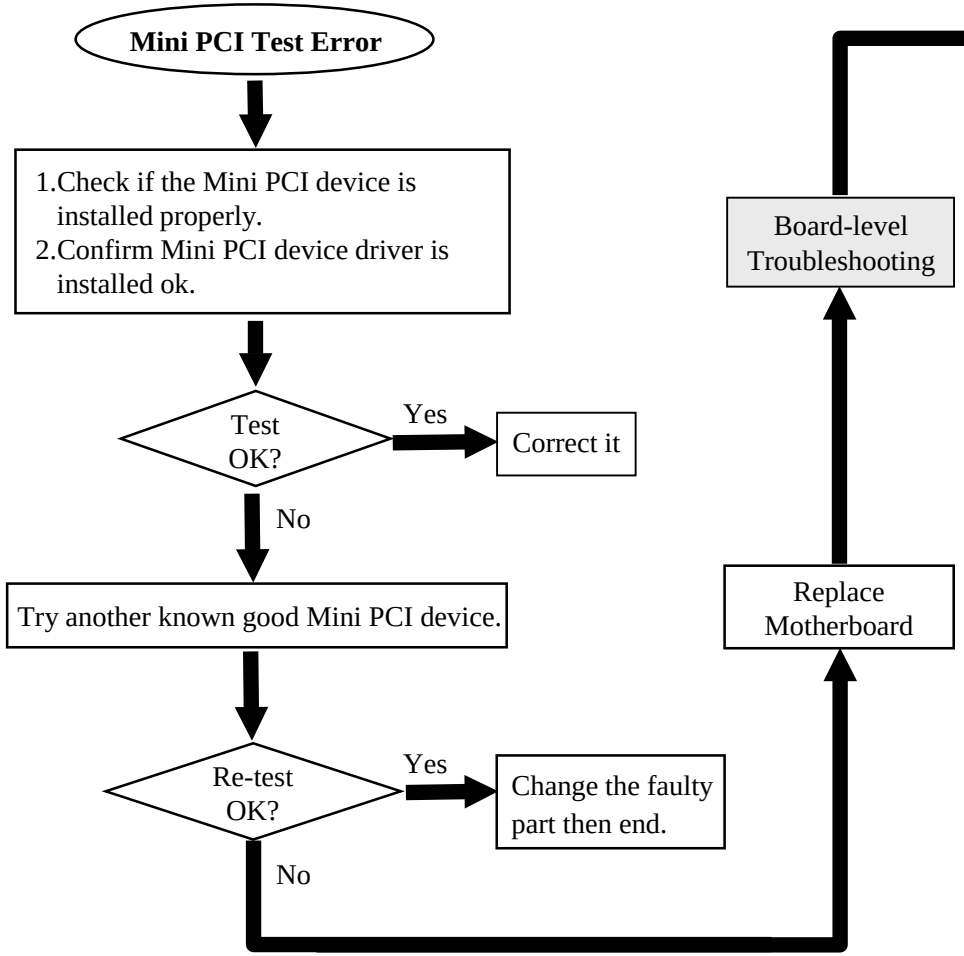
An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



8.14 Mini PCI Test Error

Symptom:

An error message is shown after Mini PCI device is installed or the Mini PCI device does't work.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U14	PCI_AD[0:31]	PCI_PERR#
J509	PCI_C/BE# [0:3]	PCI_PAR
R472	PCI_REQ2#	PME#
R622	PCI_FRAME#	MPCI_ACT#
R677	PCI_IRDY#	MINIPCI_PD
R706	PCI_TRDY#	
Q19	PCI_DEVSEL#	
Q525	PCI_STOP#	
Q526	PCI_INTD#	
D506	PCI_RESET#	
	PCI_GNT2#	
	PCI_SERR#	
	CLKRUN#	

9. 8381 Spare Part List-1

Part Number	Description	Location(S)
526267881002	AC ADPT ASSY;19V,4.74A,FSP FSP09	
324180786557	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
416267881005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
441678800005	AK;8381,UTILITY	
413000020323	AK;BOX,8381,UTILITY ONLY	
411677400001	AL-FOIL;LCD-LED,8081	
461677400001	AL-FOIL;T/P,8381	
600100010009	ANTENNA;LCD,8381	
411677400002	BATT ASS'Y;11.1V,4.0Ah,LI,BL3240	
242600000446	BATT ASSY;11.1V,4.0Ah,LI,CASE CL	
271071000002	BATT ASSY;11.1V,4.0Ah,LI,CORE PA	R7
271071102102	BATTERY;LI,3.6V/2.0AH,18650,SANY	R14
271071103101	BEZEL ASSY;COMBO,QSI,8081	R1,R10,R18
271071104101	BFM-WORLD MARK;WINXP,7521N	R13,R15
271071154101	BOX;AK,8080	R2
271071169211	BRACKET;CD-ROM,8500	R3
271071184101	BRACKET;I/O,8081	R6
271071203101	BRACKET;L,LCD,APOLLON	R29
271071303101	BRACKET;R,LCD,APOLLON	R5
271071305301	BRACKET;VGA,8081	R12,R20
271071473101	BRACKET-REAR,CDROM,APOLLON	R19
271071474301	CABLE ASSY;PHONE LINE,6P2C,W/Z C	R8
271071683101	CAP ;0.1U CR 50V 10% 0603 X7R S	R4
271071732011	CAP ;1U CR 50V +80-20% 0805 Y5V	R16
271071825211	CAP; 0.001U CR 50V 10% 0603 X7R	R11

Part Number	Description	Location(S)
272001105402	CAP; 0.0047U CR 50V 10% 0603 X7	C6
272001225401	CAP; 0.22U CR 50V +80-20% 0603	C5
272010101301	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C14
272011475501	CAP;.01U ,CR,25V ,10%,0603,X7R,S	C12
272030050301	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C13
272071105403	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C3
272072104402	CAP;.022U,CR,25V ,10%,0603,X7R,S	C11,C2
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C4,C8
272431476502	CAP;.1U ,16V,+80-20%,0603,Y5V,S	C1
273001050109	CAP;.1U ,50V,+80-20%,0603,Y5V,S	T1
286300965001	CAP;.1U ,50V,+80-20%,0603,Y5V,S	U1
288100099001	CAP;.1U ,CR,16V,10%,0603,X7R,SM	D1
288105230004	CAP;.1U ,CR,16V,10%,0603,X7R,SM	D2
288200301004	CAP;.1U ,CR,16V,10%,0603,X7R,SM	Q2,Q3
288203906018	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	Q1
291000000203	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	CN2
291000012411	CAP;.22U ,16V ,+80-20%,0603,Y5V,	CN1
294011200034	CAP;.22U ,16V ,10%,0603,X7R,SMT	LED3,LED4,LED5,LED6
294011200043	CAP;1000P,2KV,10%,1808,X7R,SMT	LED1,LED2
295000010140	CAP;1000P,50V ,+/-20%,0603,X7R,S	F1
316677400001	CAP;1000P,50V ,+/-20%,0603,X7R,S	R0D
361400003021	CAP;1000P,CR,50V,10%,0603,X7R,SM	
288204532001	CAP;1000P,CR,50V,10%,0603,X7R,SM	U2
271071220302	CAP;100P ,50V ,10%,0603,COG,SMT	R9
288114148004	CAP;100P ,50V ,10%,0603,COG,SMT	D3

9. 8381 Spare Part List-2

Part Number	Description	Location(S)
272075121301	CAP;100P,2KV,5%,1206,NPO,SMT,onl	C9
272075301302	CAP;10P ,50V ,+-10%,0603,NPO,SM	C10
272073103401	CAP;10P ,50V ,10%,0603,COG,SMT	C7
271071221301	CAP;10P ,CR,50V ,5%,0603,NPO,SM	R23,R26,R28
271071202102	CAP;10U ,10V ,20%,1210,X7R,SMT	R22,R24
271071331301	CAP;10U ,10V,+80-20%,1206,Y5V,1	R21,R25,R27
451678800076	CAP;10U ,16V,+80-20%,1210,Y5V,S	
342676400006	CAP;10U,16V,+/-10%,1206,X5R,SMT,	
342676400007	CAP;10U,16V,+/-10%,1206,X5R,SMT,	
340676400015	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	
340676400016	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	
345678500002	CAP;10U,6.3V,10%,1206,X7R,SMT	
421678500001	CAP;120P,CR,50V,5%,0603,NPO,SMT	
371102030303	CAP;120U,6.3V,+/-20%,H2.8,J121R,	
370102631202	CAP;120U,6.3V,+/-20%,H2.8,J121R,	
346676400006	CAP;1500P,CR,50V,10%,0603,X7R,SM	
340678800003	CAP;150P ,CR,25V,5% ,0603,NPO,SM	
340678500005	CAP;150U ,TPC,6.3V,20%,H1.9,7343	
370102610401	CAP;150U,4V,+/-20%,H2.8,G151R,73	
345678800011	CAP;15U ,TQC,25V,20%,H=1.9 ,7343	
346678500006	CAP;180P ,50V ,5% ,0603,NPO,SMT	
431678810001	CAP;18P ,50V ,5% ,0603,NPO,SMT	
411678800004	CAP;1U ,10%,10V ,0805,X7R,SMT	
345676400008	CAP;1U ,10%,10V ,0805,X7R,SMT	
346676400010	CAP;1U ,CR,10V ,80-20%,0603,Y5	

Part Number	Description	Location(S)
411678800005	CAP;1U ,CR,10V ,80-20%,0603,Y5	
271002472301	CAP;1U ,CR,10V,10%,0805,X5R,SM	PR505,PR506
271045107101	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PR501
271071000002	CAP;1U ,CR,16V ,-20+80%,0805,Y5	R2,R503,R504,R505
271071100302	CAP;1U ,10V ,10%,0603,X5R,SMT	PR1,PR537
271071101301	CAP;2.2U ,CR,10V ,10%,0805,X7R,S	PR542,PR543
271071102302	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	PR10
271071103101	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	PR4,PR533,PR535,PR541
271071104101	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	PR508,PR527
271071104302	CAP;2200P,50V ,+/-20%,0603,X7R,S	PR5,PR503,PR507,PR516,PR531,
271071105101	CAP;220U,2V,+/-20%,H2.8,D221R,73	PR524
271071105301	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PR504,PR539
271071134701	CAP;22P ,50V ,+ -10%,0603,NPO,S	PR518
271071137271	CAP;22P ,50V ,5% ,0603,COG,SMT	PR509
271071147311	CAP;22U ,10V,+80-20%,1210,Y5V,S	PR7
271071154201	CAP;300P,CR,50V,5%,0603,NPO,SMT	PR523
271071203101	CAP;330U,2.5V,TPB,H=3.1,7343	PR515
271071232271	CAP;33P ,50V,5% ,0603,NPO,SMT	PR520
271071302101	CAP;39P ,50V ,5% ,0603,NPO,SMT	PR6
271071324012	CAP;4.7U ,10%,10V ,1206,X7R,SMT	PR9
271071332302	CAP;4.7U ,10V,20%,1206,X5R,SMT	PR517
271071333301	CAP;4.7U ,CR,10V ,+80-20%,0805,S	PR530,PR532,R502,R6
271071472101	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	PR525
271071472302	CAP;4700P,50V ,+ -20%,0603,X7R,S	PR510,PR511
271071473301	CAP;47U ,6.3V,20%,SP-CAP,7343,S	PR540,R5,R501

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Part Number	Description	Location(S)
271071474301	CAP;5P ,CR,50V,+ -.5PF,0603,NP	PR502
271071499111	CAP;5P,3KV,5%,1808,NPO,SMT,only	PR514
271071499311	CAP;680P ,50V ,10%,0603,X7R,SMT	PR526
271071536311	CAP;68P ,50V ,5% ,0603,NPO,SMT	PR522
271071619111	CARD BOARD;FRAME,PALLET,8080	PR3
271071619311	CARD BOARD;TOP/BTM,PALLET,8080	PR519
271071909101	CARTON;BATTERY,CAIMAN,PWR	PR529
271586026101	CARTON;NON-BRAND,8080	PR2
271611153301	CASE KIT;M,8381	RP2,RP501
272001105403	CFM-BAT;FUSE,THERMAL,NEC,SF91E	PC501
272002105701	CFM-SUYIN,S-STANDOFF,#4-40H4.8,N	PC525
272002225701	CHOKE COIL;120OHM/100MHZ,20%,321	C2,C505
272005104402	CHOKE COIL;1UH,+-20%,24A,3.5MM,S	PC524
272011106408	CHOKE COIL;4.7uH,+/-20%,10A,3.5m	PC532,PC544
272071105701	CHOKE COIL;50UH(REF),D.4*2,5.5T,	C1,C6
272072104402	CHOKE COIL;90OHM/100MHZ,20%,2012	PC526
272073151301	CLEANNER;YC-336,LIQUID,STENCIL/P	PC547
272075101401	COMBO ASSY;Quanta,SBW-242,8381	PC521
272075102403	CON;BATTERY,7P,MA,2.5MM,R/A,C103	PC510,PC520,PC546
272075102701	CON;D,FM,15P,2.29,R/A,3ROW	PC506,PC509,PC535,PC536,PC54
272075103401	CON;FPC/FFC,12P,0.5MM,R/A,SMT	PC503,PC504,PC505,PC516,PC52
272075104701	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	C3,C4,C502,C504,PC1,PC2,PC3,P
272431127503	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	PC530,PC531
272431157507	CON;HDR,12P*1,1.25,ACES,SMT	C5,C503
272433156502	CON;HDR,BTB R/A,0.8MM,S-TECH1507	PC5,PC515,PC522

Part Number	Description	Location(S)
272993106001	CON;HDR,FM,35P*2,1.27,H2.2,CEN,S	PC4,PC507,PC513
273000130038	CON;HDR,MA,10P*2,1MM,H4.25,ST,SM	L515,L516
273000150013	CON;HDR,MA,12P,1MM,ACES1212,SMT	L1,L2,L513,L514,PL1,PL2,PL501
273000150313	CON;HDR,MA,22P*2,R/A,SUYIN,20038	L502,L505,L508,L511
273000500103	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	PL505
273000990021	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	PL506
286100393004	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	PU501
286104173001	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	PU1
286300431014	CON;HDR,MA,35P*2,1.27*1.27MM,CEN	PQ504
286300594003	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S	PU503
286301470001	CON;IC CARD,68P,0.635MM,62596-00	PU504
286309701001	CON;MINI PCI SOCKET,0.8MM,H4.0,S	U1,U501
288100032013	CON;PHONE JACK,2 IN 1,7.0MM,ALLT	PD505,PD506
288100099001	CON;POWER JACK,6P,D=2.5,H=7,W=9.	PD3,PD4
288100701002	CON;STEREO JACK,6P,W9.5,RC64-06G	PD2,PD503
288101004024	CON;USB,FM,H15.64,R/A,4P*2,2522A	PD508
288103104001	CONDUCTIVE TAPE;50*40,8381	PD501,PD502,PD504,PD510
288105520001	CONNECTOR;7 PIN,DIP,ALLTOP,C1034	PD507
288105524003	CONTACT PLATE ASSY;W4L27T0.15,S-	PD1
288105556001	CONTACT PLATE ASSY;W4L27T0.15FUS	PD509
288200144001	CONTACT PLATE;W4L27T0.15,7068	PQ509
288200144002	CONTACT PLATE;W4L27T0.15,7068	PQ507
288202222001	CONTACT PLATE;W4L63T0.15,1/4,T T	PQ502
288204404002	COVER ASSY,CPU,8081	PQ503
288204406001	COVER ASSY;HDD,8081	PQ506

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Part Number	Description	Location(S)
288204407001	COVER ASSY;LCD,8081	PQ1,PQ505,PQ508
288204807001	COVER ASSY;MINI-PCI,8081	PU502
288227002006	COVER ASSY;SPEAKER,8081	PQ2,PQ501,PQ510,PQ511
291000000706	COVER ASSY;TOP,8381	J10
291000010209	COVER;BATTERY,8081	J9
291000277002	COVER;HINGE;L,8081	J11
291000910601	COVER;HINGE;R,8081	
295000010016	COVER;MDC,8081	PF1,PF501,PF502
295000010105	COVER;REAR,L,8081	PF503
331000008033	COVER;REAR,R,8081	J1,J8
316678800002	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	R0A
242600000547	CU FOIL ASSY;SOUTH BRIDGE,APOLLO	
271071909211	DIMM SOCKET;DDR SODIMM200P,AMP13	PR528
361200003047	DIODE; 1SR-154-400 400V 1.0A	
361400003038	DIODE;1N4148WS,75V,200mW,SOD-323	
624200010140	DIODE;1SS355,80V,100mA,SOD-23,SM	
242600000452	DIODE;BAS32L,VRRM75V,MELF,SOD-80	
411678800001	DIODE;BAT54,30V,200mA,SOT-23	
242600000195	DIODE;BAT54C,SCHOTTKY DIODE,SOT2	
340676400018	DIODE;BAV70LT1,70V,225MW,SOT-23	
345676400006	DIODE;BAV70LT1,70V,225MW,SOT-23	
345676400011	DIODE;BAV99,70V,450MA,SOT-23	
345676400013	DIODE;BAV99,70V,450MA,SOT-23	
345676400023	DIODE;BAW56,70V,215mA,SOT-23	
345676400025	DIODE;BZM55B3V6,ZENER,3.6V,5mA,M	

Part Number	Description	Location(S)
345676400027	DIODE;BZV55-C20,ZENER,5%,SOD-80,	
346670500008	DIODE;BZV55-C24,ZENER,5%,SOD-80,	
346676400001	DIODE;BZV55-C2V4,ZENER,5%,SOD-80	
346676400003	DIODE;BZV55-C3V3,ZENER,5%,SOD-80	
346676400011	DIODE;BZV55-C4V3,ZENER,5%,SOD-80	
370102010502	DIODE;BZV55-C5V6,ZENER,5%,SOD-80	
411678800002	DIODE;EC10QS04,RECT,40V,1A,CHIP,	
242600000385	DIODE;EC31QS04-TE12L,40V,3A,SMT	
242600000452	DIODE;M1FM3,3A,30V,SHINDENGEN,SM	
291000024421	DIODE;RB717F,SCHOTTKY,40V,SOT323	J10
291000920602	DIODE;RLS4148,200MA,500MW,MELF,S	J11,J12
312271005357	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PC501,PC502,PC503,PC504
411678800003	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	
242600000001	DVD COMBO DRIVE;8X24X10X24X,SBW-	
242600000232	EC;100U,16V,M,6.3*5.5,-55+85'C,S	
242600000378	EC;10U,25V,20%,RA,6.3*6.8,+105℃	
242600000433	END CAP;LEFT,8081	
242600000452	END CAP;RIGHT,8081	
270140000003	F/W ASSY;KBD CTRL,8381	R88
271002000301	F/W ASSY;SYS/VGA BIOS,8381	L26,L27,L36,L528,L533,L563,L5
271002383011	FERRITE ARRAY;130OHM/100MHZ,3216	R637,R650
271071000002	FERRITE CHIP;120OHM/100MHZ,1608,	F3,F5,L551,PR11,PR12,PR21,PR2
271071101101	FERRITE CHIP;120OHM/100MHZ,2012,	R28,R31,R35,R36,R45,R46,R48,R4
271071101301	FERRITE CHIP;120OHM/100MHZ,2012,	R195,R732,R839
271071102102	FERRITE CHIP;130OHM/100MHZ,1608,	R126,R78,R83,R93,R98

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Part Number	Description	Location(S)
271071102172	FERRITE CHIP;600OHM/100MHZ,.2A,1	R625
271071102211	FERRITE CHIP;600OHM/100MHZ,1608,	R25
271071102302	FERRITE CHIP;600OHM/100MHZ,1608,	R181,R212,R3,R511,R626,R635,R
271071103302	FFC;TOUCH PAD,APOLLON	PR13,PR17,R106,R109,R110,R111
271071104302	FUSE; 128 DC-7A/50V 139℃only UC	PR10,PR5,R102,R152,R187,R213,
271071105301	FUSE;0.14A/60V,POLY SWITCH,PTC,S	PR2,R139,R214,R47,R503,R649
271071113113	FUSE;0.5A/15V,POLY SWITCH,SMD	R32,R638
271071121301	FUSE;1A,NORMAL,1206,SMT	R555,R561,R562,R564,R80,R81
271071122102	FUSE;1A,NORMAL,1206,SMT	PR6,PR7
271071147011	FUSE;2A,NORMAL,1206,SMT	R526
271071152101	FUSE;FAST,1A,32V,0603,SMT,THIN F	PR4
271071152302	FUSE;FAST,2A,63VDC,1206,SMT,0433	R608,R612
271071202102	FUSE;LR4-73X,POLY SWITCH,PWR	R203,R33,R639
271071203101	FUSE;NORMAL,2.5A/63VDC,3216,SMT	PR16,PR506
271071203302	FUSE;NORMAL,4A/32VDC,3216,SMT	R529
271071221301	FUSE;NORMAL,5A/32VDC,3216,SMT	R216,R217,R218,R219,R221
271071221302	FUSE;NORMAL,6.5A/32VDC,3216,SMT	R160,R183,R209,R211,R34,R556,
271071222302	GASKET;AUDIO,MB,APOLLON	R655,R696,R697,R714,R731,R744
271071224301	GASKET;BRACKET-IO,APOLLON	R656
271071271301	GASKET;CPU-MB,40*5*5,8381	R82
271071272101	GASKET;IO-BKT,20*4*4,8381	R117,R120,R121,R123,R750
271071301011	GASKET;MODEM,20*5*3.5,8381	R536
271071316211	GASKET;PCMCIA-1,APOLLON	PR18
271071330302	GASKET;PCMCIA-2,APOLLON	R116,R125,R127,R128,R129,R135
271071331301	GASKET;PCMCIA-3,APOLLON	R607,R611

Part Number	Description	Location(S)
271071332302	GLUE;TOSHIBA 3941	R733
271071361101	HD DRIVE,30GB,2.5",MHT2030AT,FUJ	R133,R609
271071392101	HDD ASSY;30GB,MHT2030AT,FUJITSU,	PR8
271071392301	HDD ME KIT;8381	R549,R554
271071402811	HEATSINK ASSY;8381	R62,R63
271071432211	HINGE,L,LCD,APOLLON	PR14
271071433301	HINGE;R,LCD,APOLLON	R659,R675,R682,R708,R725,R741
271071471302	HOLDER;PCMCIA FCI,APOLLON	R182
271071472101	HOUSING ASSY;CASE,8381	R623,R95,R96
271071472302	HOUSING ASSY;LCD,8381	R103,R141,R142,R143,R144,R147
271071473301	HOUSING KIT;M,8381	R165,R739
271071474301	HOUSING;BATTERY,8081	R74
271071475011	IC SOCKET;462P,ZIF,FOXCONN,PZ462	R558
271071475112	IC,H8S/2140B,KBD CTRL,TQFP,100P,	PR507
271071499311	IC;74AHC14,HEX INVERTER,TSSOP,14	PR29,PR3
271071499811	IC;74AHCT1G32,SINGLE OR GAT,SOT2	R596,R599,R601,R603
271071511301	IC;74CBTD3384,10 BIT BUS SW,TSSO	R73
271071560301	IC;74CBTH3383,BUS EXCHG SW,TSSOP	R56,R60
271071562301	IC;74VHC164,SIPO REGISTER,TSSOP,	R158,R573
271071563101	IC;ADM1032,TEMPERATURE MTR,SO8	PR9
271071604811	IC;AME8800,0.3A,1.5%,LDO,SOT89	R535,R537
271071634211	IC;BQ2040,GAS GAUGE,SO,16P,SMT	PR15
271071649111	IC;CMI9738-S,AC97 CODEC,LQFP,48P	R630
271071681301	IC;CPU,AMD-Athlon XP1800+,OPGA,3	R704
271071682101	IC;DDR SDRAM,32M*8-133,TSOP,66,H	R726,R728,R745

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Part Number	Description	Location(S)
271071690101	IC;EEPROM,9346,64*16 BITS,SO8,SM	R108,R38
271071750101	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	R100,R101,R104,R99
271071806112	IC;FLASH,256K*8,PLCC32,LPC,ST49L	PR508
271071820301	IC;G692L293T,RESET CIRCUIT,2.93V	R30
271071822301	IC;ICS950902,CLOCK GEN,SSOP56,56	R107,R522
271071866212	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PR27
271125008711	IC;ISL6223CA,PWM CONTROLLER SSOP	PR510,PR511
271571000301	IC;LMV393,DUAL COMPARTOR,SSOP,8P	RP17,RP18,RP19
271571100301	IC;LP2951ACM,VOLTAGE REGULATOR,S	RP12,RP13,RP14,RP15,RP16,RP2
271571330301	IC;LP2951CM-3.3,VOLTAGE REGULATO	RP30,RP31,RP34,RP38,RP505,RP
271611000301	IC;LP2996,DDR,NS,PSOP8,SMT	RP36,RP41
271611103301	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	RP44,RP49
271611152301	IC;MAX4173F,I-SENSE AMP,SOT23,6P	RP7
271611153301	IC;MAX6501_UKP95,TEMP MTR,SOT23-	RP522
271611220301	IC;MM1414,PROTECTION,TSOP-20A,PR	RP518,RP519,RP526
271611222301	IC;NC7WZ07P6X,D-BUFFER,SC-70,6P	RP47,RP48
271611330301	IC;OZ965R,CCFL CTRL,TSSOP16,O2	RP51,RP521
271611392311	IC;PCI1510,GGU,BGA144P	RP10,RP26,RP8
271611472301	IC;RT9701,POWER DISTRI SW,SOT23-	RP32,RP43,RP50,RP503,RP504,R
271611750301	IC;S-875061EUP VOLT DETECTOR S	RP1
271621103302	IC;SC1470,PWM CTRL,TSSOP,14P,SMT	RP39
271621471301	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	
271621473301	IC;TL594C,PWM CTRL,TSSOP16	RP524,RP527
271621820301	IC;TPA0212,AMPLIFIER,TSSOP,24P,S	RP11,RP6
271621820302	IC;TPS2211,POWER DISTRI SW,SSOP1	RP2,RP3

Part Number	Description	Location(S)
272001105403	IC;VT6103,LAN-PHY,SSOP,48P,SMT	PC29,PC39,PC4,PC507,PC9
272002105701	IC;VT8235,SOUTH BRIDGE,BGA,487P,	C1
272002225701	IC;VT8372,NORTH BRIDGE,HSBGA,552	C90
272002475701	INDUCTOR;10nH,10%,0805,SRF 2.1G,	C760
272005104402	INDUCTOR;10UH,CDRH104R,+/-30%,SU	C237,C238,PC11,PC13,PC16,PC8
272011106404	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	C103,C17,C20,C23,C36,C42,C45,C
272011106408	INSULATOR;5,BATTERY ASSY,7521Li	C197,C701,C755,PC508
272011106703	INSULATOR;AL-FOIL,PCMCIA,APOLLON	C108,C117,C15,C158,C159,C161,C
272011475401	INSULATOR;BATT ASSY,ONE ROUND,BL	C104,C106,C111,C88
272012225702	INSULATOR;D/D-B,APOLLON	C715,C766
272012475701	INSULATOR;FIBER,93.5x17.5,T=0.25	C193,C236,C699
272021106501	INSULATOR;FIBER,UL94V-0,195x15,T	C132,C149,C634,C635,PC30,PC52
272021226701	INSULATOR;FIBER,UL94V-0,35x15,T=	C774,PC531,PC535
272022106701	INSULATOR;FIBER,UL94V-0,D=17.5mm	C767
272030102401	INSULATOR;INVERTER,APOLLON	C133,C134,C142,C143,C152
272071105701	INSULATOR;M/B-1,APOLLON	C115,C120,C122,C156,C176,C180
272072104402	INSULATOR;MB,8381	C138,C139,C140,C141,C144,C145
272072104702	INSULATOR;MINI-PCI,APOLLON	C136,C683,C684,C71,C81
272072224402	KBD OPTION;US,8081	C206,C214,C215,C531,C532,C533
272072224701	KBD;86,US,3000160400,ZIPPY,8081	C509
272073223401	LABEL KIT;N-B,8381	PC6
272075100302	LABEL;10*10,BLANK,COMMON	C544,C617,C620,C74
272075100401	LABEL;10*10,BLANK,COMMON	C168,C32,C671
272075100701	LABEL;25*10MM,3020F	C175,C177,C178,C181,C187,C198
272075101401	LABEL;25*6,HI-TEMP,COMMON	C765,PC514,PC518

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Part Number	Description	Location(S)
272075102403	LABEL;27*10,LAN ID BAR CODE	C118
272075102701	LABEL;27*7MM,HI-TEMP 260'C	C12,C191,C2,C201,C226,C229,C2
272075103401	LABEL;5*20,BLANK,COMMON	PC10
272075103702	LABEL;5*20,BLANK,COMMON	C512,C513,C515,C6,C607,C7,C81
272075104701	LABEL;6*6MM,GAL,BLANK,COMMON	C101,C102,C109,C119,C121,C123
272075152401	LABEL;AGENCY-GLOBAL,8381	PC513
272075180304	LABEL;BAR CODE,(25*10MM)*12pcs,8	C153,C154
272075181301	LABEL;BAR CODE,125*65,COMMON	PC17,PC23
272075220301	LABEL;BATT,11.1V/4.0AH,LI,SAN,80	C674,C680
272075220701	LABEL;BLANK,11*5MM,COMMON	C220,C223,C224
272075222701	LABEL;BLANK,60*80MM,7170	C116,C164,C170,C18,C189,C22,C
272075330302	LABEL;BLANK,7*7MM,COMMON	C518,C519,C520
272075390301	LABEL;BLANK,7MM*7MM,PRC	C100,C105,C107,C110,C112,C113
272075472701	LABEL;BLANK,7MM*7MM,PRC	C811
272075509801	LABEL;BLANK,7MM*7MM,PRC	C521,C522,C530,C546
272075680302	LABEL;LOT NUMBER,RACE	C125
272075681401	LABEL;PAL,20*5MM,COMMON	C552,C553
272431127503	LABEL;RED ARROW HEAD,PRC	PC526,PC527
272431157513	LABEL;S/N,INVERTER,20MM*3MM,PRC	PC523,PC524
272431227402	LABEL;SOFTWARE,INSYDE BIOS-M	PC24,PC25,PC26,PC27,PC28,PC3
272431227531	LCD ASSY;14",XGA,AU,B141XN04,838	PC529,PC534
272431337001	LCD ME KIT;XGA,14",AU,B141XN04,8	C632
272602107501	LCD;B141XN04-2,TFT,14",LCDS,XGA,	C746,C756,C762
272625470401	LED;GREEN,H.8,0603,19-21VGC/TR,S	CP1,CP2,CP3,CP4
272993106001	LED;GREEN,H0.8,0603,CL-190G,SMT	PC505,PC515,PC516,PC517,PC54

Part Number	Description	Location(S)
273000111002	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	L537,L539
273000130001	LED;RE/GR,H0.8,L1.9,W1.6,19-22SR	L546
273000130038	LT PF;14",XGA,AU,B141XN04,M,8381	L501,L502,L550,L552,L554,L555
273000130039	LTXNX;8381M/4UCX/30M/1US1/L2D4A/	L1,L2,L23,L24,L3,L513,L559
273000150013	PACKING KIT;DA-1A05-A;PWR	L10,L11,L16,L19,L20,L21,L25,L5
273000150033	PACKING KIT;N-B,8381	L12,L13,L14,L15,L17,L18,L37,L3
273000150157	PAD;LCD/KB,ANIT-STATIC,8381	L514,L515,L516,L517,L520,L521
273000500015	PALLET;1250*1080*130,7521N	L530
273000500023	PARTITION;BATTERY,MARLIN,CAIMAN,	PL501,PL502
273000610019	PARTITION;PALLET,8080	FA1,FA501
273000990061	PARTITION;TOP/BTM,BATTERY,MARLIN	PL503,PL504
273001050028	PCB ASSY;FAX MODEM 56K,1456VQL4A	U510
274011000403	PCB;PWA-8381/DD BD	X2
274011431414	PCB;PWA-8381/M BD	X1
274012457406	PCB;PWA-APOLLON/BATT,BD,PWR	X5
274012500415	PCB;PWA-INVERTER BD (DA-1A05-A),	X501
274013276103	PE BABBLE BAG;300mm*260mm,8081	X3
281300707001	PE BAG;50*70MM,W/SEAL,COMMON	U22
282071338302	PE BAG;70X100MM,W/SEAL,COMMON	U9
282074338403	PE BAG;L560*W345,7521N	U15,U16,U2,U512
282574014004	PE BUBBLE BAG;160X270MM,ANTI-STA	U514
282574132001	PE BUBBLE BAG;BATTERY,GRAMPUS	U23,U520
282574164002	PE BUBBLE BAG;CD-ROM HOUSING,817	U20
283466570001	PHASEOUT;FERRITE CHIP,120OHM/100	U511
283767640002	PLATE;T/P,COVER,8081	U10,U11,U12,U13,U505,U506,U5

9. 8381 Spare Part List-8

Part Number	Description	Location(S)
284501032001	PLATE;T/P,GROUND,8081	U8
284501510002	PWA;PWA-8381,D/D BD,SMT	U518
284502996001	PWA;PWA-8381,D/D BD,T/U	PU13
284506103002	PWA;PWA-8381,MOTHER BD	U513
284506223001	PWA;PWA-8381,MOTHER BD,SMT	PU7
284508235002	PWA;PWA-8381,MOTHER BD,T/U	U14
284508372001	PWA;PWA-INVERTER BD,DA-1A05-A,PW	U502
284509738002	PWA;PWA-INVERTER BD,SMT,DA-1A05-	U19
284595090202	PWA-PWA-8X81/BATT BD;LI,4.0Ah,2P	U509
286100212001	PWA-PWA-8X81/BATT BD;SMT,BL3240G	U18
286302211001	PWR CORD;125V/7A,2P,BLACK,AMERIC	U515
286302951015	RES;.008,1W,1%,3720,SMT	U17
286303728002	RES;.01 ,1W ,1% ,2512,SMT	PU11
286306207001	RES;.02 ,2W,1%,2512,SMT	PU12,PU8
286308800001	RES;0 ,1/10W,5% ,0805,SMT	U7
286329510001	RES;0 ,1/16W,5% ,0603,SMT	U21
286369229301	RES;0 ,1/16W,5% ,0603,SMT	U1,U523
288100013006	RES;0 ,1/16W,5% ,0603,SMT	PD2,PD3
288100054001	RES;0.010,1.5W, 1%,2512,SMT;PWR	D11,D3,D503
288100054002	RES;0.050,1W, 1%,2512,SMT, only	D1,D4
288100056001	RES;1 ,1/10W,5% ,0805,SMT	D501,D6
288100056003	RES;1.02K,1/16W,1% ,0603,SMT	D502,PD501
288100701002	RES;1.13K,1/16W,1%,0603,SMT	D507,D8
288104148001	RES;1.2K ,1/16W,1% ,0603,SMT	D505,D506
288105524002	RES;1.5K ,1/16W,1% ,0603,SMT	PD6

Part Number	Description	Location(S)
288105533001	RES;1.5K ,1/16W,5% ,0603,SMT	PD502,PD503
288105543001	RES;10 ,1/16W,5% ,0603,SMT	PD5
288200114001	RES;10.2K,1/16W,1% ,0603,SMT	Q518,Q519
288200144001	RES;100 ,1/10W,5% ,0805,SMT	Q15,Q17,Q18,Q2,Q21,Q30,Q505,(
288200144003	RES;100 ,1/16W,1% ,0603,SMT	Q13,Q14,Q16,Q19,Q22,Q5,Q504,(
288202222001	RES;100 ,1/16W,5% ,0603,SMT	Q3,Q4
288202301001	RES;100 ,1/16W,5% ,0603,SMT	Q1,Q20,Q23,Q24,Q503,Q522,Q54
288202302001	RES;100 ,1/16W,5% ,0603,SMT	Q526
288203904010	RES;100K ,1/16W,1% ,0603,SMT	Q8
288204404002	RES;100K ,1/16W,1% ,0603,SMT	PQ5,PQ6
288204406001	RES;100K ,1/16W,1% ,0603,SMT	PQ7,PQ8,PU3,PU4,PU5,PU6
288204788001	RES;100K ,1/16W,5% ,0603,SMT	U3,U4,U5,U6
288204835001	RES;100K ,1/16W,5% ,0603,SMT	Q501
288227002006	RES;10K ,1/16W,1% ,0603,SMT	PQ1,PQ2,PQ3,PQ4,Q10,Q11,Q12,
291000000802	RES;10K ,1/16W,1% ,0603,SMT	J509
291000010209	RES;10K ,1/16W,5% ,0603,SMT	J1,J507
291000010303	RES;10K ,1/16W,5% ,0603,SMT	J503
291000012023	RES;120 ,1/16W,5% ,0603,SMT	J3
291000017012	RES;13.7K,1/16W,.1%,0603,SMT	J4
291000020206	RES;130K ,1/16W,0.1% ,0603,SMT	J511
291000021206	RES;147 ,1/16W,1% ,0603,SMT	J2
291000151201	RES;147K ,1/16W,1% ,0603,SMT	J5
291000152610	RES;15.4K,1/16W,.1%,0603,SMT	J6
291000153006	RES;150K ,1/16W,1% ,0603,SMT	J510
291000256827	RES;16.9K,1/16W,1% ,0603,SMT	J8

9. 8381 Spare Part List-9

Part Number	Description	Location(S)
291000614621	RES;180K ,1/16W,1% ,0603,SMT	U504
291000811008	RES;1K ,1/16W,1% ,0603,SMT	J508
294011200016	RES;1K ,1/16W,1% ,0603,SMT	D14,D15,D16,D17
294011200043	RES;1K ,1/16W,5% ,0603,SMT	D13
295000010009	RES;1K ,1/16W,5% ,0603,SMT	PF504
295000010028	RES;1M ,1/16W,1% ,0603,SMT	F502
295000010048	RES;1M ,1/16W,5% ,0603,SMT	F1
295000010105	RES;1M ,1/16W,5% ,0603,SMT	F2,F8
295000010106	RES;1M ,1/16W,5% ,0603,SMT	F7
295000010110	RES;2.2K ,1/16W,5% ,0603,SMT	PF1
295000010130	RES;2.7K ,1/16W,1% ,0603,SMT	PF501,PF502,PF503
295000010153	RES;20K ,1/16W,1% ,0603,SMT	F4,F6
297030105003	RES;20K ,1/16W,1% ,0603,SMT	SW6
297040100007	RES;20K ,1/16W,1% ,0603,SMT	SW1,SW4,SW5
316678800001	RES;20K ,1/16W,5% ,0603,SMT	R0B
331040050018	RES;22 ,1/16W,5% ,0603,SMT	J505
331660020002	RES;22 ,1/16W,5% ,0603,SMT,INT	J504
331720015006	RES;220 ,1/16W,5% ,0603,SMT	J502
342674500002	RES;220 ,1/16W,5% ,0603,SMT	MTG12,MTG13
342676400015	RES;220K ,1/16W,5% ,0603,SMT	MTG14
361200001018	RES;220K ,1/16W,5% ,0603,SMT	
361400003021	RES;23.2K,1/16W,.1%,0603,SMT	
481678800001	RES;270 ,1/16W,5% ,0603,SMT	
242600000145	RES;2K ,1/16W,1% ,0603,SMT	
283467640002	RES;2K ,1/16W,1% ,0603,SMT	U522

Part Number	Description	Location(S)
481678800002	RES;3.3K ,1/16W,5% ,0603,SMT	
242600000145	RES;3.3K ,1/16W,5% ,0603,SMT	
284582140002	RES;3.9K ,1/16W,1% ,0603,SMT	U516
284506501001	RES;3.9K ,1/16W,5% ,0603,SMT	U503
271002010301	RES;301 ,1/16W,1% ,0603,SMT	PR31,PR32
361400003037	RES;30K ,1/16W,1% ,0603,SMT	
288204410010	RES;31.6K,1/16W,1% ,0603,SMT	PU1,PU10,PU2,PU9
600100010003	RES;324K ,1/16W,1% ,0603,SMT	
422677000008	RES;33 ,1/16W,5% ,0603,SMT	
346678800001	RES;330 ,1/10W,5% ,0805,SMT	
345678800004	RES;330 ,1/16W,5% ,0603,SMT	
345678800008	RES;330 ,1/16W,5% ,0603,SMT	
442164900021	RES;33K ,1/16W,5% ,0603,SMT	
451678810001	RES;360 ,1/16W,1% ,0603,SMT	
412678800001	RES;383 ,1/10W,1% ,0805,SMT	
340678800002	RES;3K ,1/16W,1% ,0603,SMT	
340678800001	RES;3M ,1/16W,5% ,0603,SMT	
340678500003	RES;4.75K,1/16W,1% ,0603,SMT	
340678500006	RES;4.7K ,1/10W,5% ,0805,SMT	
340678500007	RES;4.7K ,1/16W,1% ,0603,SMT	
340678500008	RES;4.7K ,1/16W,1% ,0603,SMT	
344678500010	RES;4.7K ,1/16W,5% ,0603,SMT	
344678500012	RES;4.7K ,1/16W,5% ,0603,SMT	
344678500013	RES;4.99K,1/16W,1% ,0603,SMT	
344678500014	RES;40.2 ,1/16W,1% ,0603,SMT	

9. 8381 Spare Part List-10

Part Number	Description	Location(S)
344678500015	RES;43.2K,1/16W,1% ,0603,SMT	
340676400019	RES;43K ,1/16W,5% ,0603,SMT	
340676400009	RES;470 ,1/16W,5% ,0603,SMT	
341678500001	RES;470K ,1/16W,5% ,0603,SMT	
345678500001	RES;470K ,1/16W,5% ,0603,SMT	
370102010301	RES;470K ,1/16W,5% ,0603,SMT	
370102610401	RES;475 ,1/16W,1% ,0603,SMT	
370102610804	RES;47K ,1/16W,1% ,0603,SMT	
345676400016	RES;47K ,1/16W,5% ,0603,SMT	
421676400001	RES;47K ,1/16W,5% ,0603,SMT	
422676400001	RES;49.9 ,1/16W,1% ,0603,SMT	
345676400032	RES;499K ,1/16W,1% ,0603,SMT	
340678800004	RES;499K ,1/16W,1% ,0603,SMT	
370102010502	RES;499K ,1/16W,1% ,0603,SMT	
370102610603	RES;5.6K ,1/16W,5% ,0603,SMT	
370102611001	RES;510 ,1/16W,5% ,0603,SMT	
421678800001	RES;536K ,1/16W,1% ,0603,SMT	
345676400018	RES;56 ,1/16W,5% ,0603,SMT	
340676400025	RES;56K ,1/16W,1% ,0603,SMT	
370102010204	RES;6.19K,1/16W,1% ,0603,SMT	
342678500004	RES;6.49K,1/16W,1% ,0603,SMT	
342678500003	RES;6.8K ,1/16W,1% ,0603,SMT	
342665500010	RES;60.4 ,1/16W,1% ,0603,SMT	
345678800009	RES;619K ,1/16W,1% ,0603,SMT	
345678500002	RES;63.4K,1/16W,1% ,0603,SMT	

Part Number	Description	Location(S)
346678800002	RES;680 ,1/16W,5% ,0603,SMT	
523467880006	RES;68K ,1/16W,1% ,0603,SMT	
523402379037	RES;69.8,1/16W,1%,0603,SMT	
451678800001	RES;732 ,1/16W,1% ,0603,SMT	
370103010303	RES;75 ,1/16W,1% ,0603,SMT	
340678500021	RES;8.06K,1/16W,1%,0603,SMT	
523467880020	RES;8.2K ,1/16W,5% ,0603,SMT	
451678800031	RES;82 ,1/16W,5% ,0603,SMT	
342672200010	RES;82.5K,1/16W,1% ,0603,SMT	
342676400003	RES;86.6K,1/16W,1%,0603,SMT	
370102010204	RES;9.09K,1/16W,1% ,0603,SMT	
373101712351	RES;90.9K,1/16W,1% ,0603,SMT	
340678500014	ROM ME KIT;8381	
523408610080	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	
565167000013	RP;0*8 ,16P ,1/16W,5% ,1606,SM	
565180626001	RP;1.5K*4,8P ,1/16W,5% ,0612,SMT	
531067850001	RP;10*8 ,16P ,1/16W,5% ,1606,SM	
531017240176	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	
441677370001	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	
221600020252	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	
221600050218	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	
221600050219	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	
222503220001	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	
226600030332	RP;3.9K*4,8P,1/16W,5%,0612,SMT	
242678500003	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	

9. 8381 Spare Part List-11

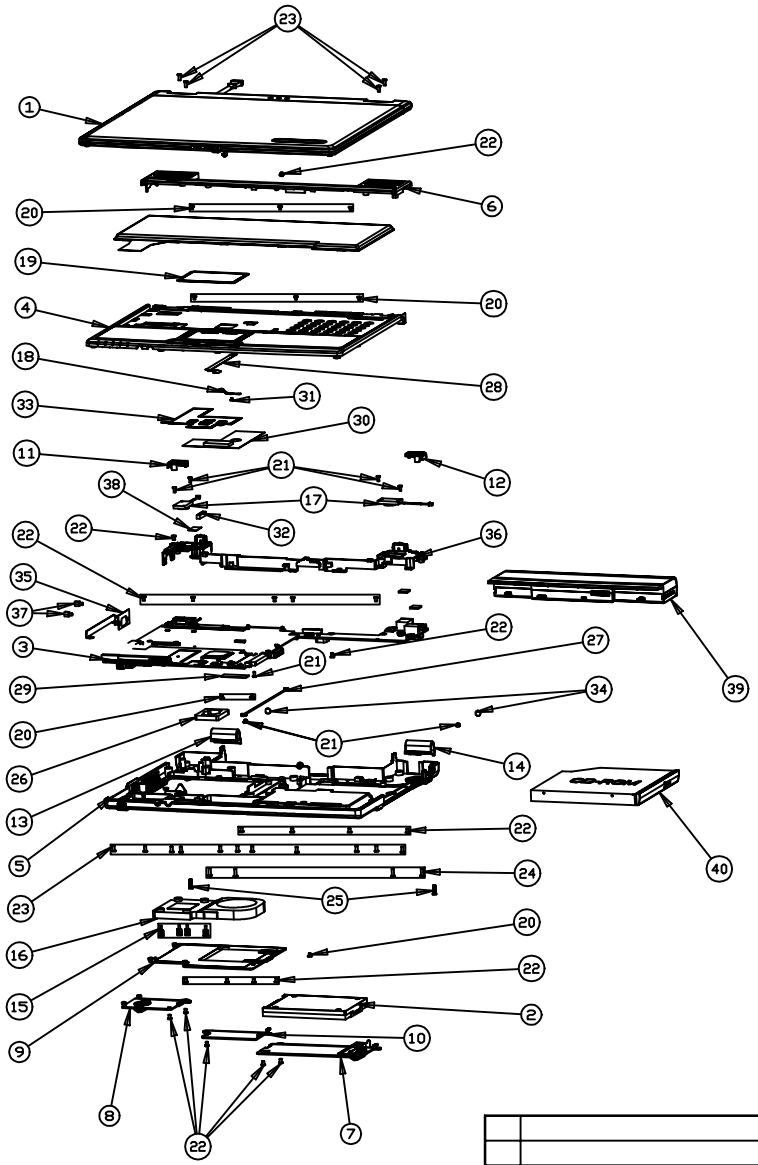
Part Number	Description	Location(S)
441677370002	RP;33*8 ,16P ,1/16W,5% ,1606,SM	
344678500021	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	
344678500022	RP;470*4,8P,1/16W,5%,1206,SMT	
361400003030	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	
441677370003	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	
225600000054	RP;820*4 ,8P,1/32W,5% ,1206,SMT	
225600000061	RP;820*8 ,10P,1/32W,5% ,1206,SMT	
242600000315	RUBBER;DOWN,LCD,8081	
242600000439	RUBBER;DOWN,LCD,8081	
242669600005	RUBBER;SILICONE RUBBER,24x17.5,T	
338536010008	RUBBER;SILICONE RUBBER,T=1.5mm,D	
342503200004	S/W;CD ROM SYSTEM DRIVER,8381	
345677300001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
346503100005	S/W;CD-ROM,B'S RECORDER GOLD2.0	
346503200202	SCREW;M2L3,K-HEAD(+),NIW/NLK	
346677300001	SHIELDING ASSY;HDD,8081	
346677300004	SHRINK TUBE;300V,125,I.D=2.5,T=0	
346677300006	SHRINK TUBE;UL,600V,105'C,ID2.5*	
361400003005	SOLDER CREAM;NOCLEAN,P4020870980	
411677370001	SOLDER CREAM;NOCLEAN,P4020870980	
310111103013	SOLDER CREAM;SH-6309,SHENMAO,63/	
331000007025	SOLDER PASTE;NO CLEAN,RMA,CK3000	CON1
333025000005	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
335152000085	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	F1
345677300002	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	

Part Number	Description	Location(S)
346677300005	SOLDER WIRE;63/37,1.2,NA,N/C,PRC	
361200005001	SPACER;SOCKET 462,TETRA	
365350000003	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
411677370002	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL	
271002101301	SPC-SCREW;M2.6L10,NIB,K-HD,NY	R5,R6
271002331301	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	FR1,FR2
271044100101	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	RM
271045507103	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	RS1,RS2,RS3
271071101301	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	R28,R29,R32,R33,R7,R8,R9
271071103302	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/	R20,R21,R3
271071104101	SPC-SCREW;M2L2,NIW/NLK,K-HD	R23,R24,R25,R26,R30,R34
271071105301	SPC-SCREW;M2L2,NIW/NLK,K-HD	R2,R4
271071224301	SPC-SCREW;M2L3,NIB,K-HD,t0.8,NLK	R1
271071499311	SPC-SCREW;M3L3,NIB,K-HD(+)	R22
272005104705	SPEAKER ASSY,APOLLON	C21,C6,C7
272075101404	SPONGE;320*290*10,CAIMAN,PWR	C13
272075103408	SPONGE;COVER-SWITCH,MB,APOLLON	C10,C12,C14,C20,C22,C23,C24,C2
272075223702	SPONGE;CPU-SOCKET,MB,APOLLON	C1,C2,C3
272075471409	SPONGE;D/D-B,APOLLON	C5
273000130006	SPONGE;RTC,APOLLON	L1
286002040001	SPRING SCREW;HEATSINK,APOLLON	IC4
286301414001	STAND OFF;AM20-30,GP3	IC1
286387506001	STAND OFF;AM20-45,APOLLON	IC3
288100056005	SW;PUSH BUTTON,STS-043-A,5P,12V/	ZD1,ZD2
288110355001	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	D2

9. 8381 Spare Part List-12

Part Number	Description	Location(S)
288111544001	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	D1
288200144008	TAPE;INSULATING,POLYESTER FILM,1	Q1
288200717001	THERMAL PAD;NORTH BRIDGE,APOLLON	SD1
316677300001	THERMISTOR;10K,1%,RA,DISK,103AT-	
288208107001	THERMOSETTING BOND;80837,LOCTITE	Q2,Q5
283467540001	TOUCHPAD MODULE;TM41PUC2311-2,DI	IC2
422677300002	TRANS;2N7002LT1,N-CHANNEL FET,ES	CN4
422677300004	TRANS;2N7002LT1,N-CHANNEL FET,ES	CN3
422677300005	TRANS;3LN01S,N-MOSFET,SMCP	CN1
422677300006	TRANS;AO4404,N-MOSFET,ID=8.5A,0.	CN2
441674800032	TRANS;AO4404,N-MOSFET,ID=8.5A,0.	
342502900001	TRANS;AO4406,N-MOS,.0165OHM,SO8	
333050000117	TRANS;AO4406,N-MOS,.0165OHM,SO8	
441677310031	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	
335152000026	TRANS;AO4410,N-MOSFET,ID=18A,0.0	
335152000097	TRANS;AO4807,DUAL PMOS,5A,SO8	
342502900001	TRANS;DTA144EKA,PNP,SMT	
600100010009	TRANS;DTA144WK,PNP,SMT	
624200010140	TRANS;DTC114TKA,10K,N-MOSFET,SOT	
541667880032	TRANS;DTC144TKA,N-MOSFET,SOT-23	
221675340001	TRANS;DTC144WK,NPN,SOT-23,SMT	
222600020049	TRANS;DTC144WK,NPN,SOT-23,SMT	
222600020310	TRANS;MMBT2222AL,NPN,TO236AB	
242662300009	TRANS;MMBT2222AL,NPN,TO236AB	
242669900009	TRANS;MMBT3904L,NPN,Tr35NS,TO236	

Part Number	Description	Location(S)
222671620001	TRANS;MMBT3906L,PNP,Tr35NS,TO236	
421015560001	TRANS;SI2301DS,P-MOSFET,SOT-23	
541667880031	TRANS;SI2302DS,N-MOSFET,SOT-23	
565167880001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	
222668820003	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	
222678500001	TRANS;SI4835DY,PMOS,6A/30V,.035,	
461678800002	TRANS;TPC8107,13A/30V,P-MOSFET,S	
222670820003	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
224670830002	VARISTOR;280V,5.6X3.8MM,TVB280-0	
227678500001	WIRE ;#20AWG,UL1007,L=140mm,RED;	
227678500002	WIRE ;#20AWG,UL1007,L=230mm,BLAC	
221675320002	WIRE ;#26AWG,UL1007,L=215mm,BLUE	
221675350003	WIRE ;#26AWG,UL1007,L=290mm,YELL	
221675350004	WIRE ASSY,MDC-MODEM,APOLLON	
221675350005	WIRE ASSY;BATT TO MB,FOR LYNX,MO	
242600000088	WIRE ASSY;LCD 14,AU,XN04-2,8081	
227678800003	XFMR;CI8.5,16T/2600T(.21ψ),220m	
451678800051	XSFORMER;10/100 BASE,LF-H41S,SMT	
242670800113	XTAL;10MHZ,50PPM,16PF,7*5,4P,SMT	
242678800001	XTAL;14.318MHZ,32PF,50PPM,8*4.5,	
242679900005	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	
442678800001	XTAL;25MHZ,20PF,30PPM,8.0*4.5,SM	
332810000033	XTAL;32.768KHZ,20PPM,12.5PF,CM20	
		P/N:526267881002



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
40			1	ASSY	
39	441677370001	BATTERY ASSY;8081(Panasonic)	1	ASSY	
38	346678500008	INSULATOR;SPK,8081	1	PART	
37	342665500010	CFM-SUYIN,S-STANDOFF,#4-40H4.8,NIW,NLK	2	PART	
36	342678500003	BRACKET;I/O,8081	1	PART	
35	342678500004	BRACKET;VGA,8081	1	PART	
34	345678500002	RUBBER;DOWN,LCD,8081	2	PART	
33	346678800002	AL-FOIL;T/P,8381	1	PART	
32	345678800009	GASKET;ID-BKT,20*4*4,8381	1	PART	
31	370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	1	PART	TP-GN*1
30	340676400025	CU FOIL ASSY;SOUTH BRIDGE,APOLLON	1	PART	
29	345676400032	THERMAL PAD;NORTH BRIDGE,APOLLON	1	PART	
28	422676400001	FFC;TOUCH PAD,APOLLON	1	ASSY	
27	421676400001	WIRE ASSY,MDC-MODEM,APOLLON	1	ASSY	
26	345676400016	SPONGE;RTC,APOLLON	1	PART	
25	370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	2	PART	HOUSING-REARCOVER*2
24	370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	4	PART	HOUSING-SPKCOVER*4
23	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	15	PART	HOUSING-COVER*11 HINGE-ID*4
22	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	21	PART	MB-HOUSING*6 SPKCOVER-HOUSING*1 ALL-COVER*9 CD-ROM*2 HOUSING-ID*2 ID-MB*1
21	370102010502	SPC-SCREW;M2L5,NIB,K-HD,t0.8,NLK	7	PART	SPEAKER*4 MB-DD*1 HINGE-COVER*2
20	370102010301	SPC-SCREW;M2L3,NIB,K-HD,t0.8,NLK	9	PART	TOP-HOUSING*3 KEYBOARD*3 MDC-MB*2
19	345678500001	PLATE;T/P,COVER,8081	1	PART	
18	341678500001	PLATE;T/P,GROUND,8081	1	PART	
17	340676400009	SPEAKER ASSY;APOLLON	2	ASSY	
16	340678800005	HEATSINK ASSY;MPT,8381	1	ASSY	
15	340676400019	SPRING SCREW;HEATSINK,APOLLON	4	PART	
14	344678500015	COVER;HINGE;R,8081	1	PART	
13	344678500014	COVER;HINGE;L,8081	1	PART	
12	344678500013	COVER;REAR,R,8081	1	PART	
11	344678500012	COVER;REAR,L,8081	1	PART	
10	344678500010	COVER;MDC,8081	1	PART	
9	340678800006	COVER ASSY;CPU,8381	1	ASSY	
8	340678500007	COVER ASSY;MINI-PCI,8081	1	ASSY	
7	340678500006	COVER ASSY;HDD,8081	1	ASSY	
6	340678500003	COVER ASSY;SPEAKER,8081	1	ASSY	
5	340678800001	HOUSING ASSY;CASE,8381	1	ASSY	
4	340678800002	COVER ASSY;TOP,8381	1	ASSY	
3	411678800001	PWA;PWA-8381,MOTHER BD	1	ASSY	
2	451678800001	HDD ME KIT;8381	1	ASSY	
1			1	ASSY	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± RANGE	Pla.	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	08-Jul-03	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.250	DRAWING NAME		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	R00A

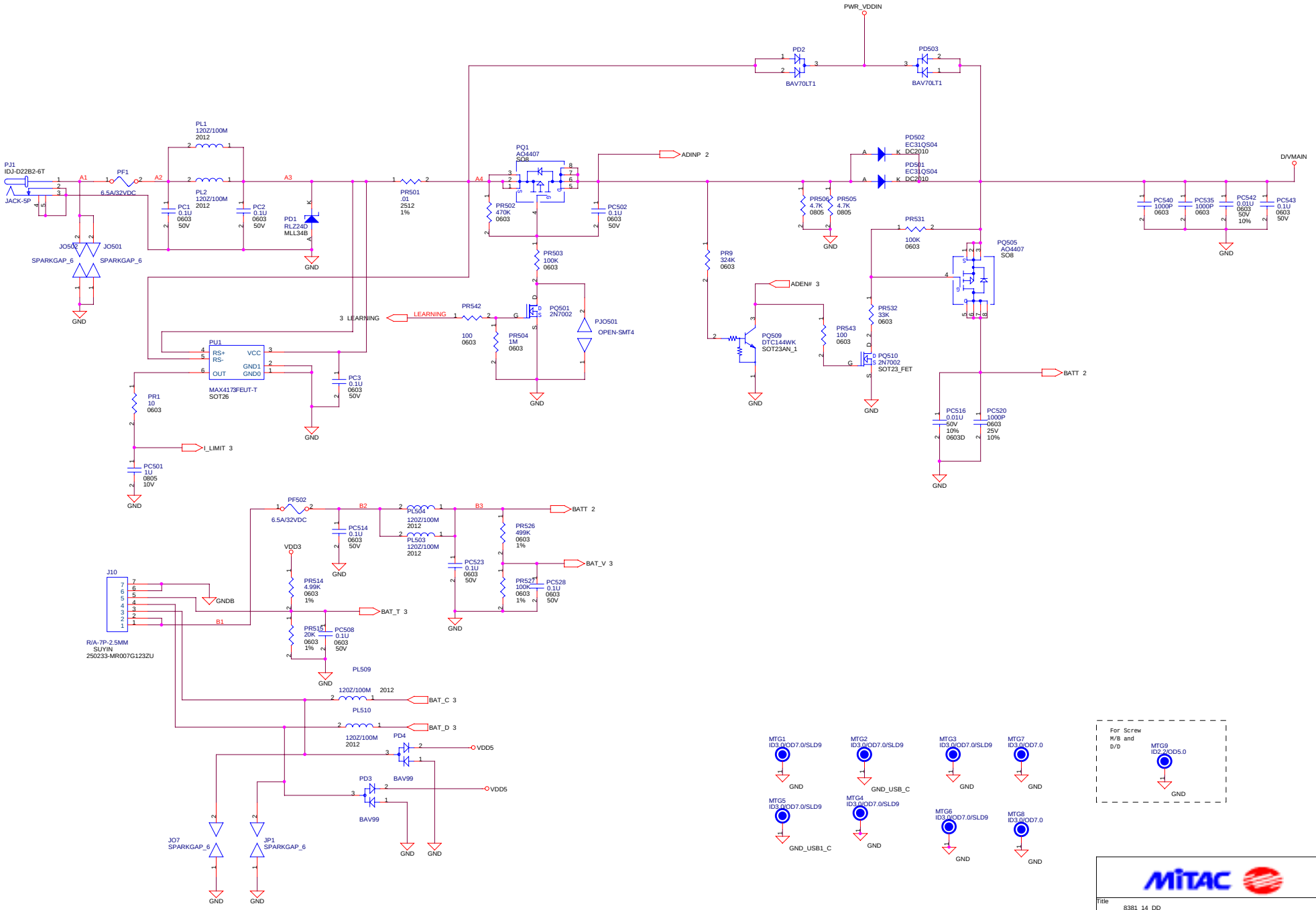
MiTAC Technology Corp.

model name8081-ASSY-MAIN-ROBERT

file nameMAIN_ASSY_8381

SHEET NO. 1 OF 1

8381 D/D R00



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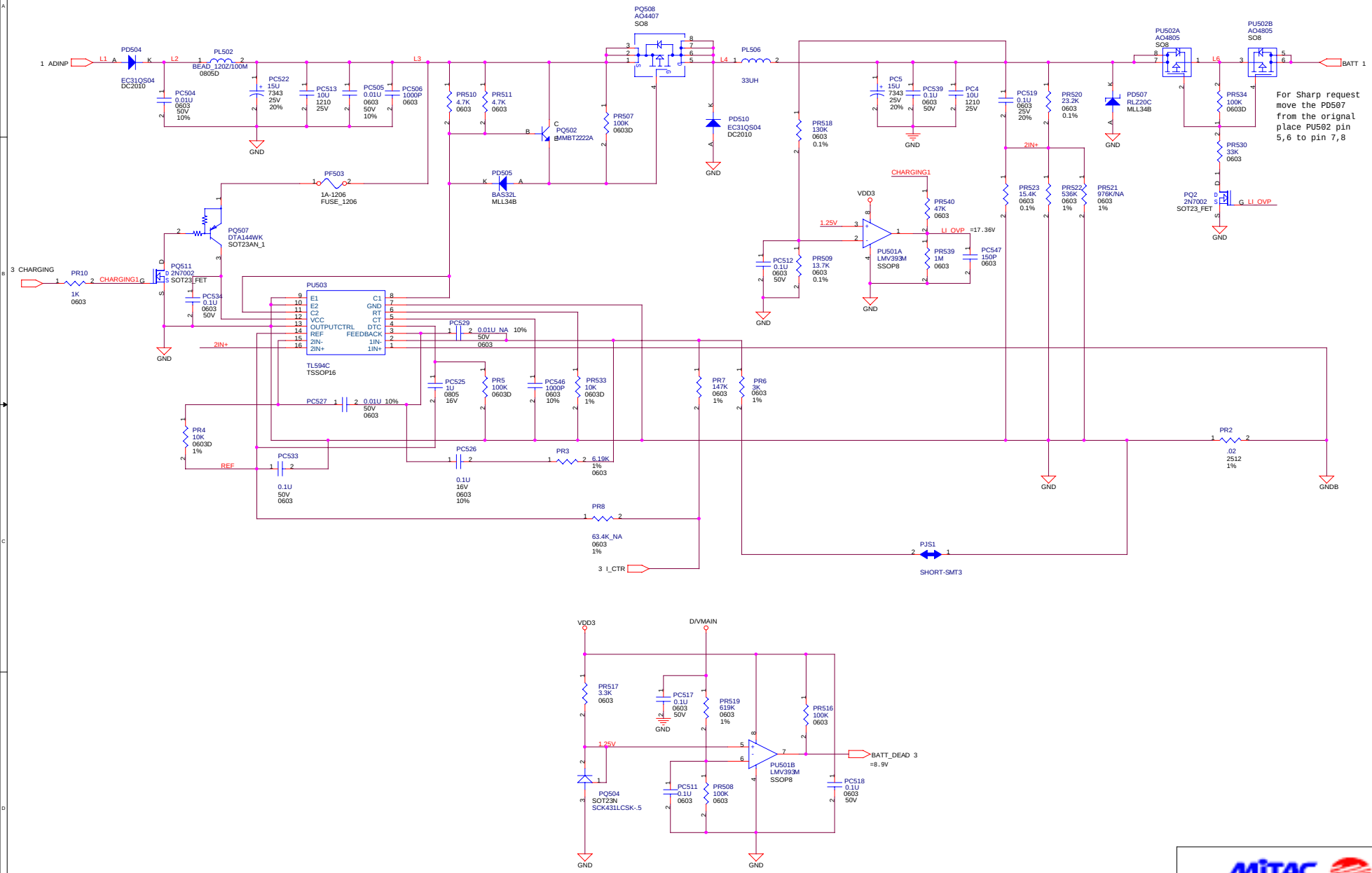
Size C	Document Number <Doc>	Rev R00
Date: 星期一, 四月 28, 2003	Sheet 1 of 4	

CHARGING



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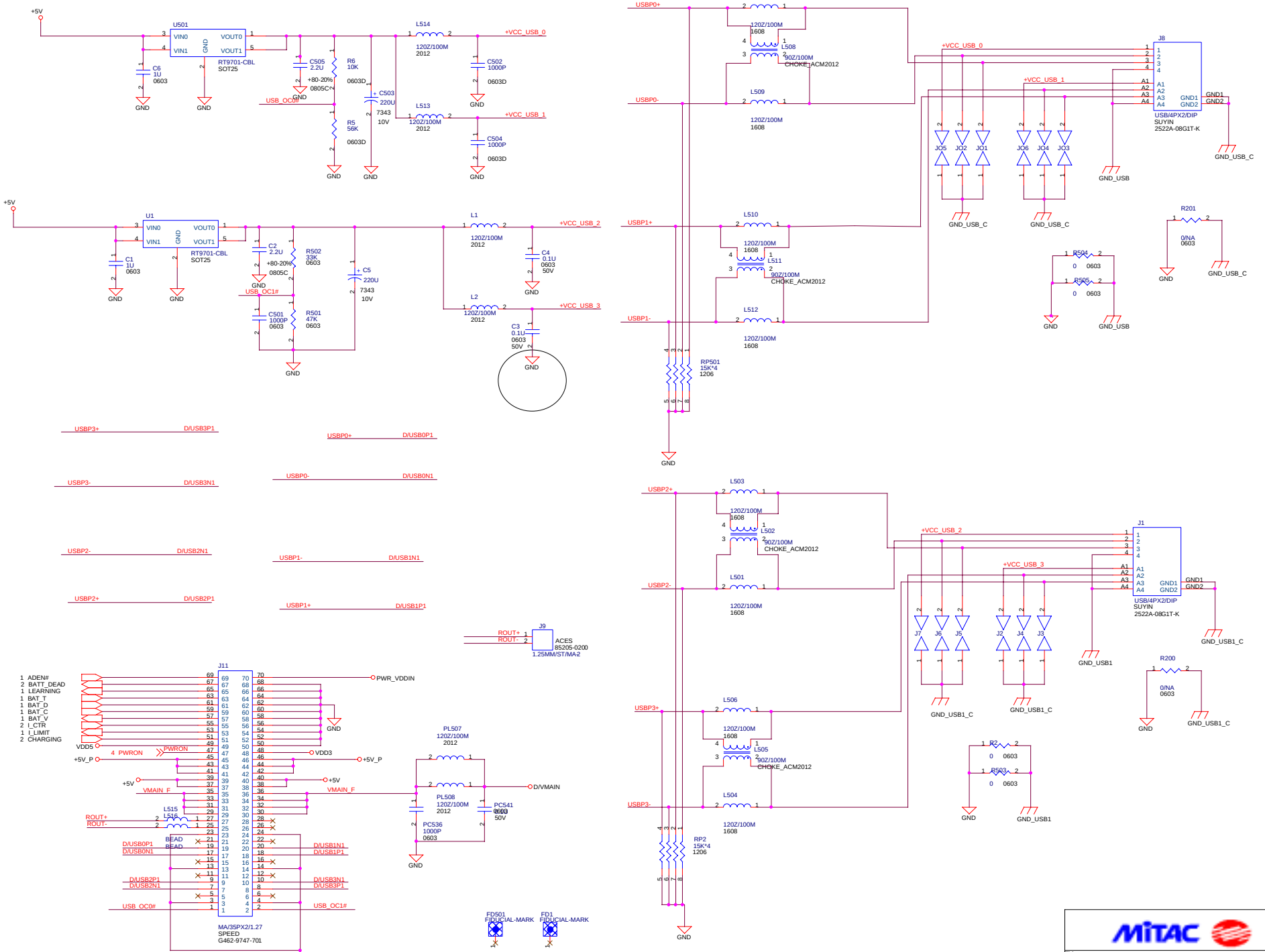
+5V
U501
VIN0
VIN1
VOUT0
VOUT1
GND
RT9701-CBL
SOT25
C6
1U
0603
C505
2.2U
+80-20%
0805C
R6
10K
0603D
R5
56K
0603D
C503
220U
7343
10V
L514
120Z/100M
2012
L513
120Z/100M
2012
C502
1000P
0603D
C504
1000P
0603D
+VCC_USB_0
+VCC_USB_1
USB_OC0#
GND
U1
C1
1U
0603
C2
2.2U
+80-20%
0805C
R502
33K
0603
R501
47K
0603
C501
1000P
0603
USB_OC1#
C5
220U
7343
10V
L1
120Z/100M
2012
L2
120Z/100M
2012
C4
0.1U
0603
50V
C3
0.1U
0603
50V
+VCC_USB_2
+VCC_USB_3
USBP3+
D/USB3P1
USBP3-
D/USB3N1
USBP2-
D/USB2N1
USBP2+
D/USB2P1
USBP0+
D/USB0P1
USBP0-
D/USB0N1
USBP1-
D/USB1N1
USBP1+
D/USB1P1
J9
ROUT+
ROUT-
ACES
85205-0200
1.25MM/ST/MA2
J11
1 ADEN#
2 BATT_DEAD
1 LEARNING
1 BAT_T
1 BAT_D
1 BAT_C
1 BAT_V
2 I_CTR
1 I_LIMIT
2 CHARGING
VDD5
4 PWRON
PWRON
PWR_VDDIN
VDD3
+5V_P
VMAIN_F
L515
L516
BEAD
BEAD
MA/35PX2/1.27
SPEED
G462-9747-701
PL507
120Z/100M
2012
PL508
120Z/100M
2012
PC536
1000P
0603
PC541
0603
50V
D/VMAIN
FD501
FIDUCIAL-MARK
FD1
FIDUCIAL-MARK
USBP0+
USBP0-
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L511
L512
120Z/100M
1608
90Z/100M
CHOKE_ACM2012
RP501
15K*4
1206
J8
USB/4PX2/DIP
SUYIN
2522A-08G1T-K
GND1
GND2
JO5
JO2
JO1
JO6
JO4
JO3
GND_USB
GND_USB_C
R504
R505
0
0603
R201
0/NA
0603
USBP2+
USBP2-
USBP3+
USBP3-
L503
L502
L501
L506
L505
L504
RP2
15K*4
1206
J1
J7
J6
J5
J2
J4
J3
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GND_USB1_C
R200
R2
R503
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Size
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Rev
R00
Date:
星期一, 四月 28, 2003
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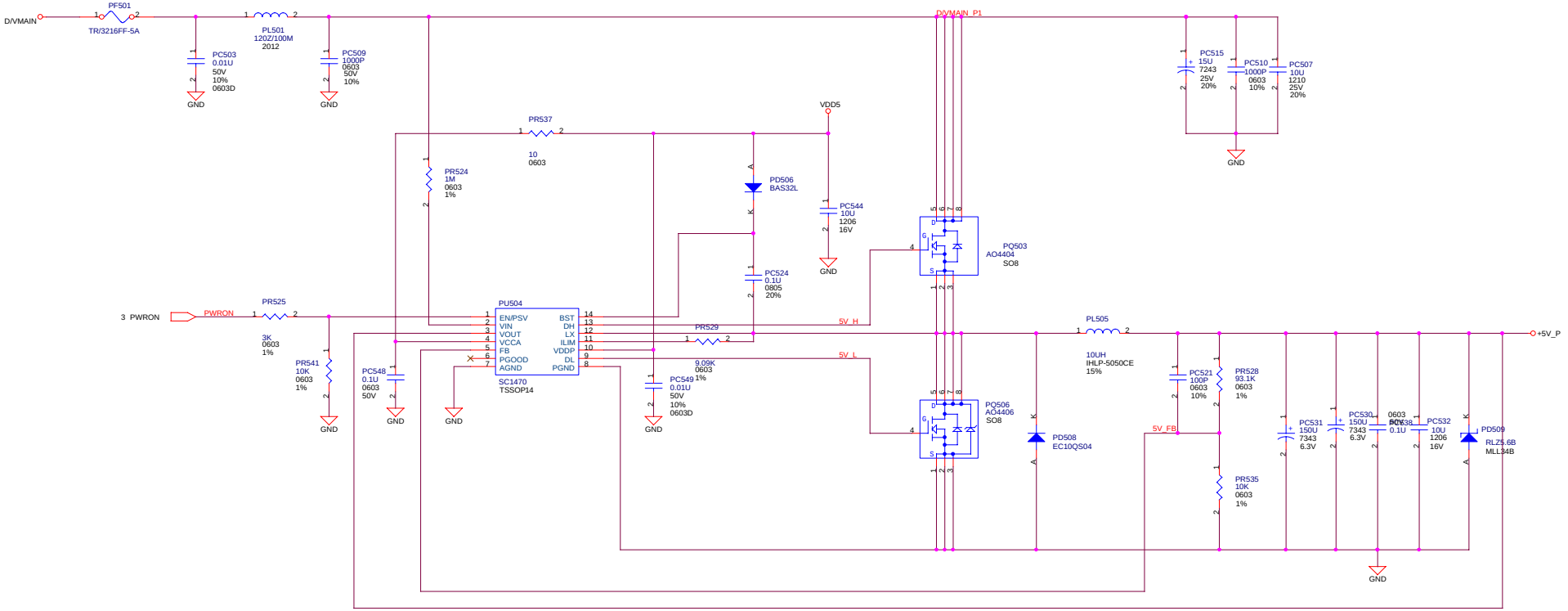
of
4

SYSTEM POWER +5V



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8381

Project Code :

IDSEL

IDSEL	Device
AD11	
AD18	
AD19	
AD21	CardBus
AD22	

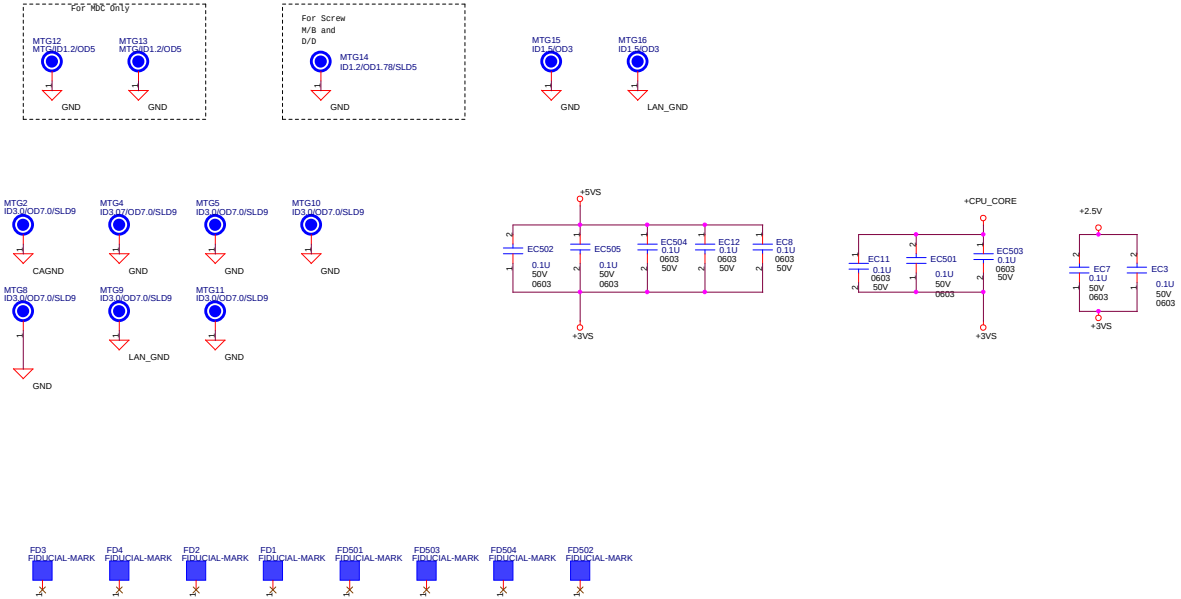
BUSMASTER

REQ	Device
REQ0	CardBus
REQ1	
REQ2	
REQ3	
REQ4	LAN

PCIINT

PCIINT	Device
INTA	NB
INTB	CardBus
INTC	
INTD	

REVISION	TAPEOUT DATE HISTORY
R0A	First Draft
R0B	Page 10 Enhance Lid Switch Function by KBC



DRAWN	DESIGN	CHECK	ISSUES

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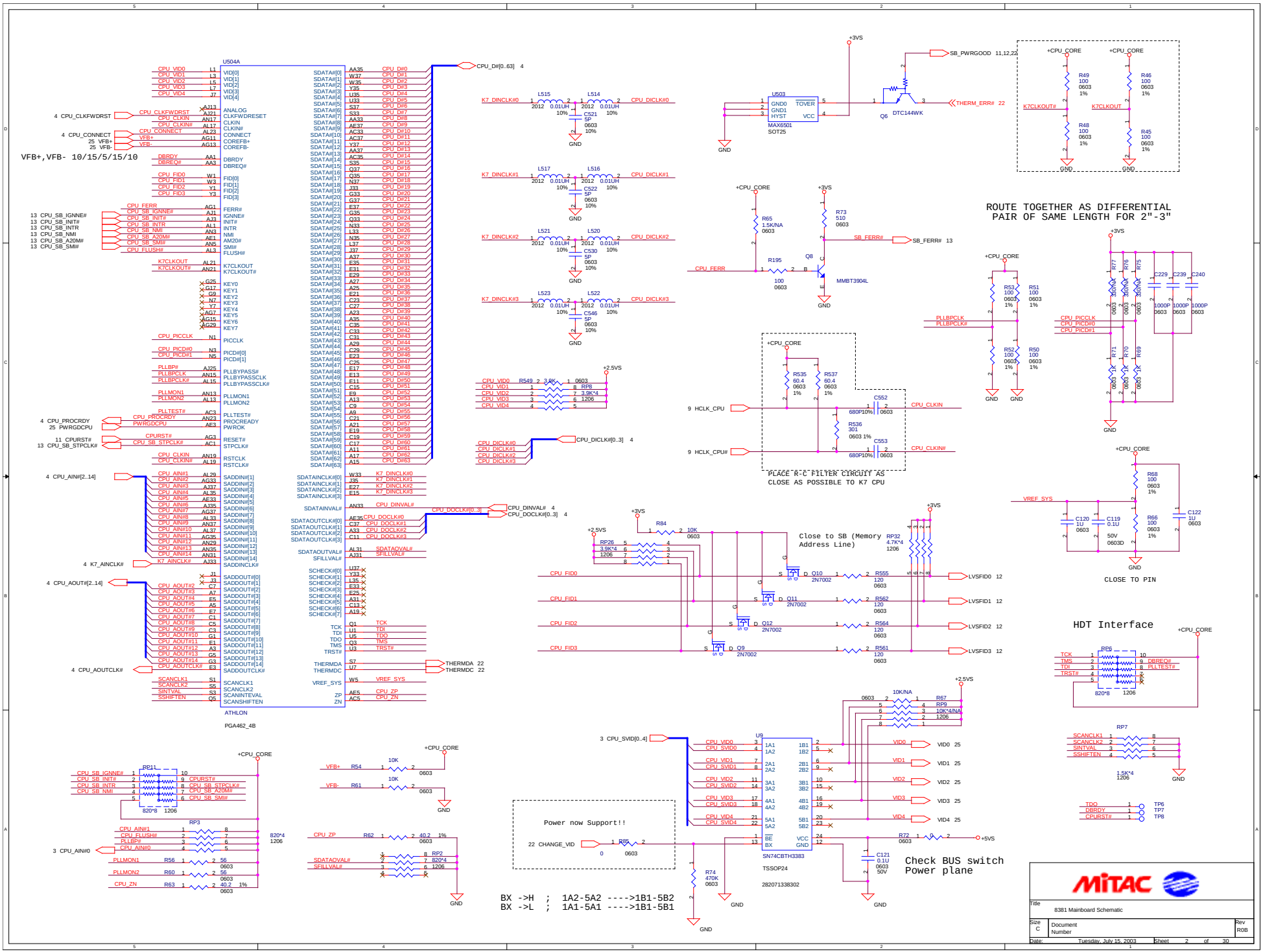
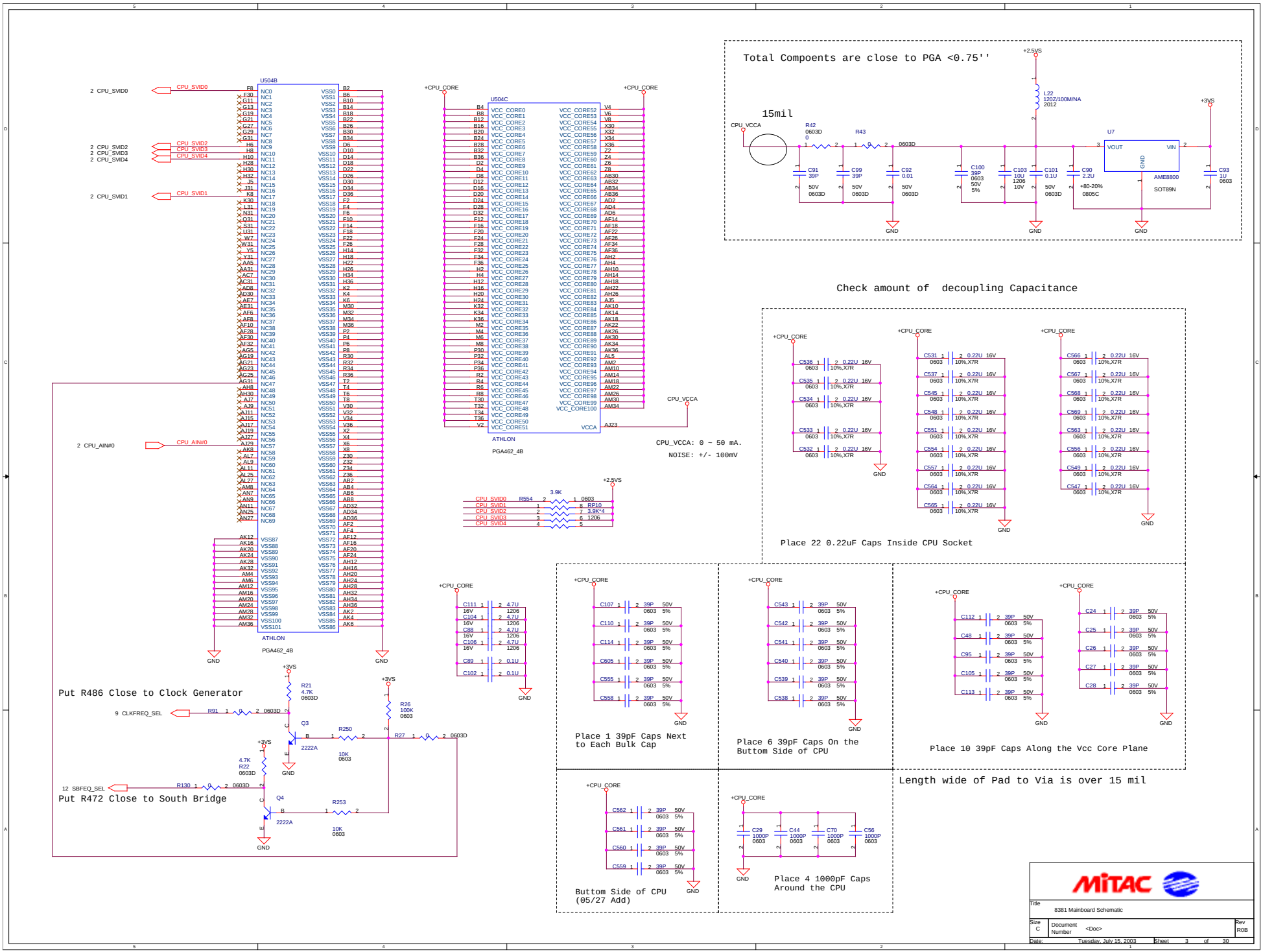
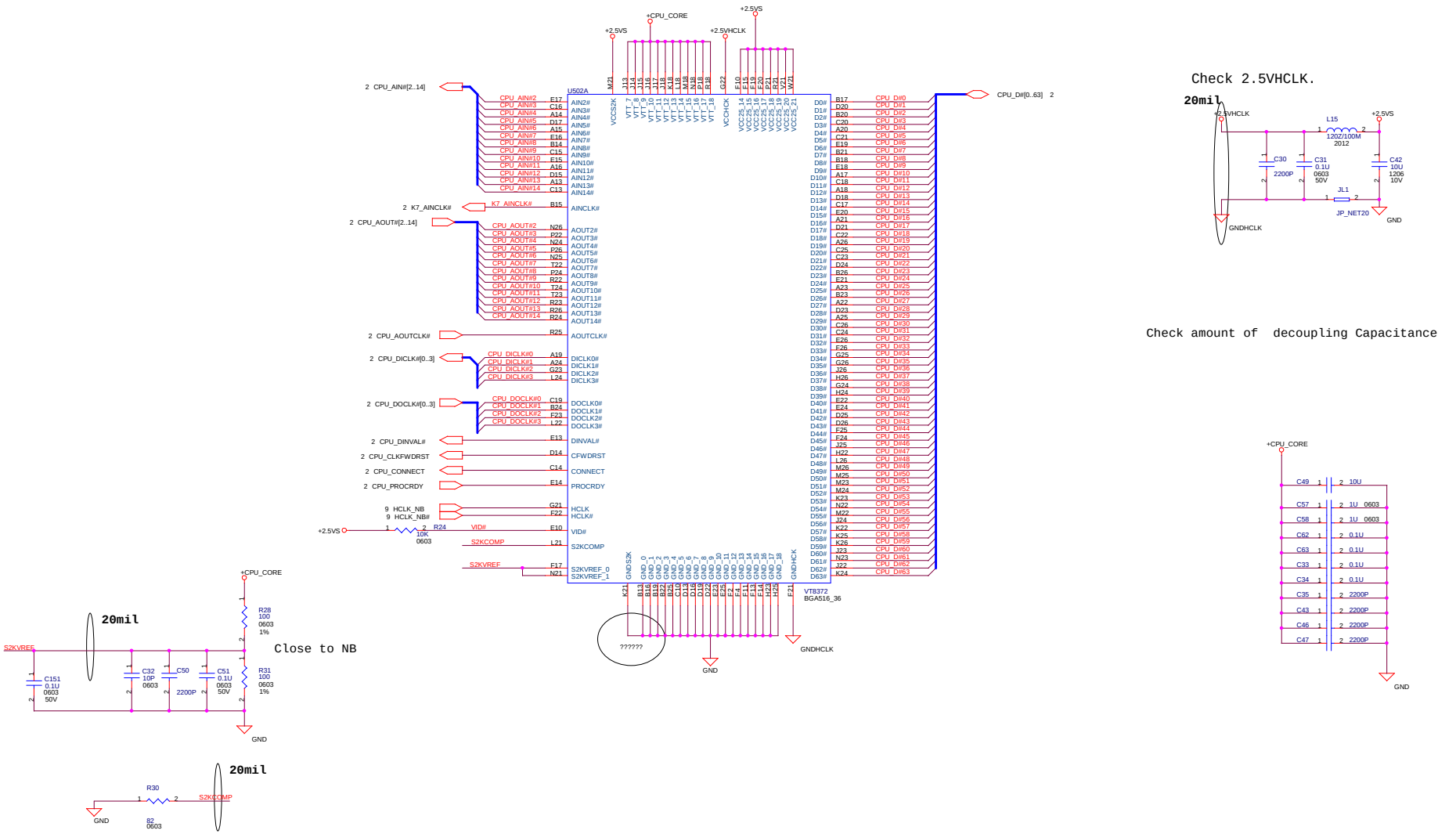
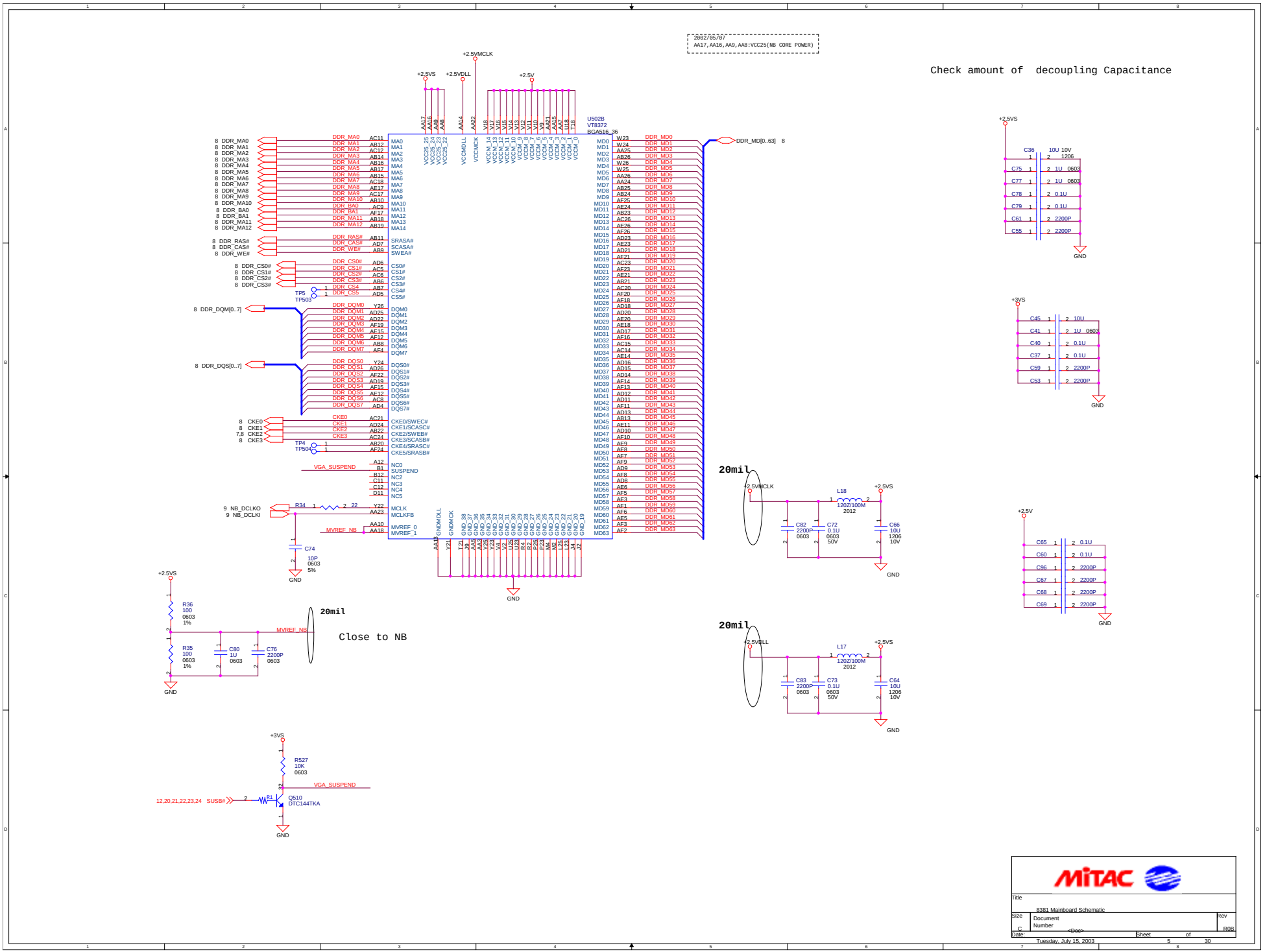
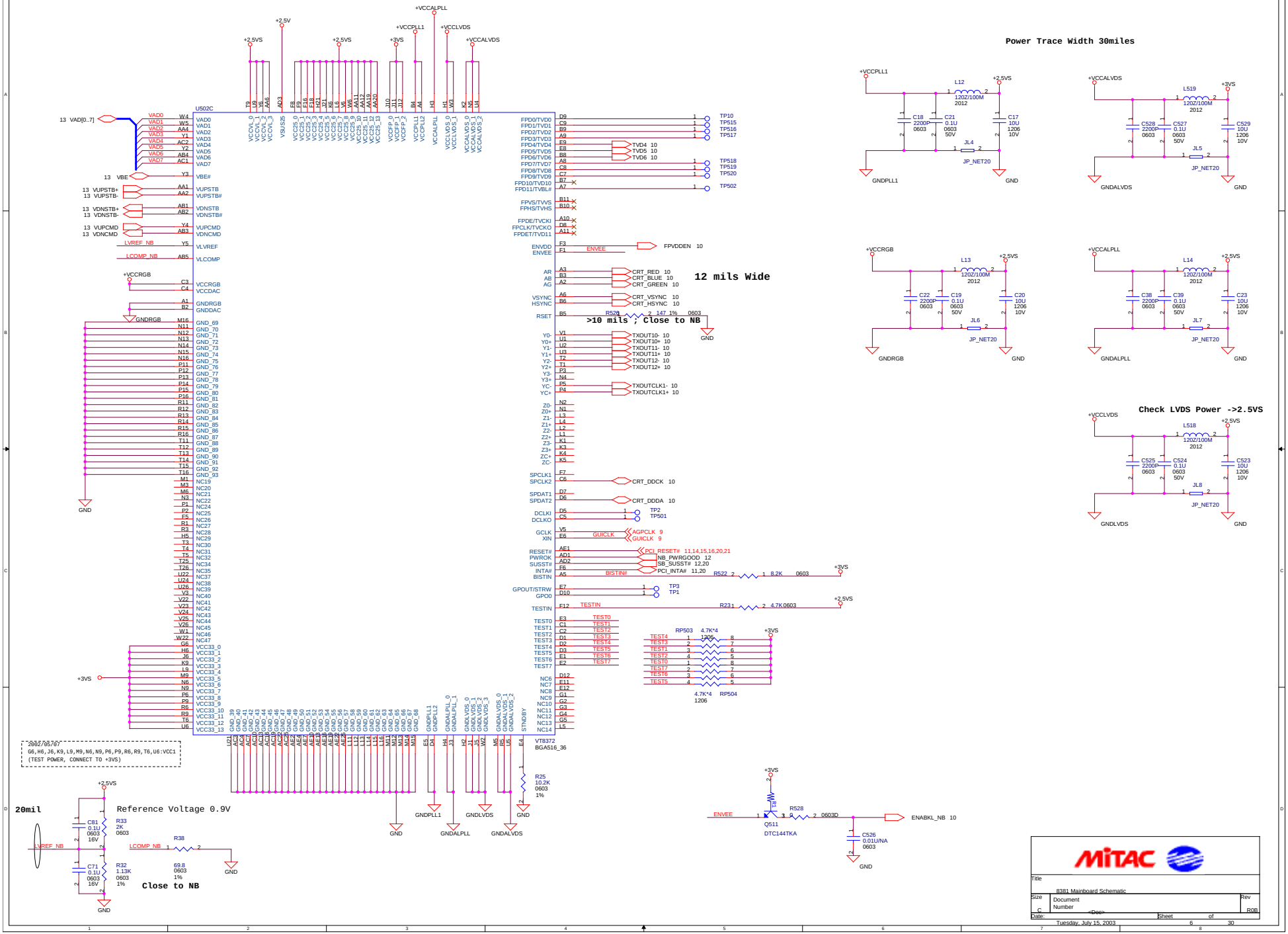


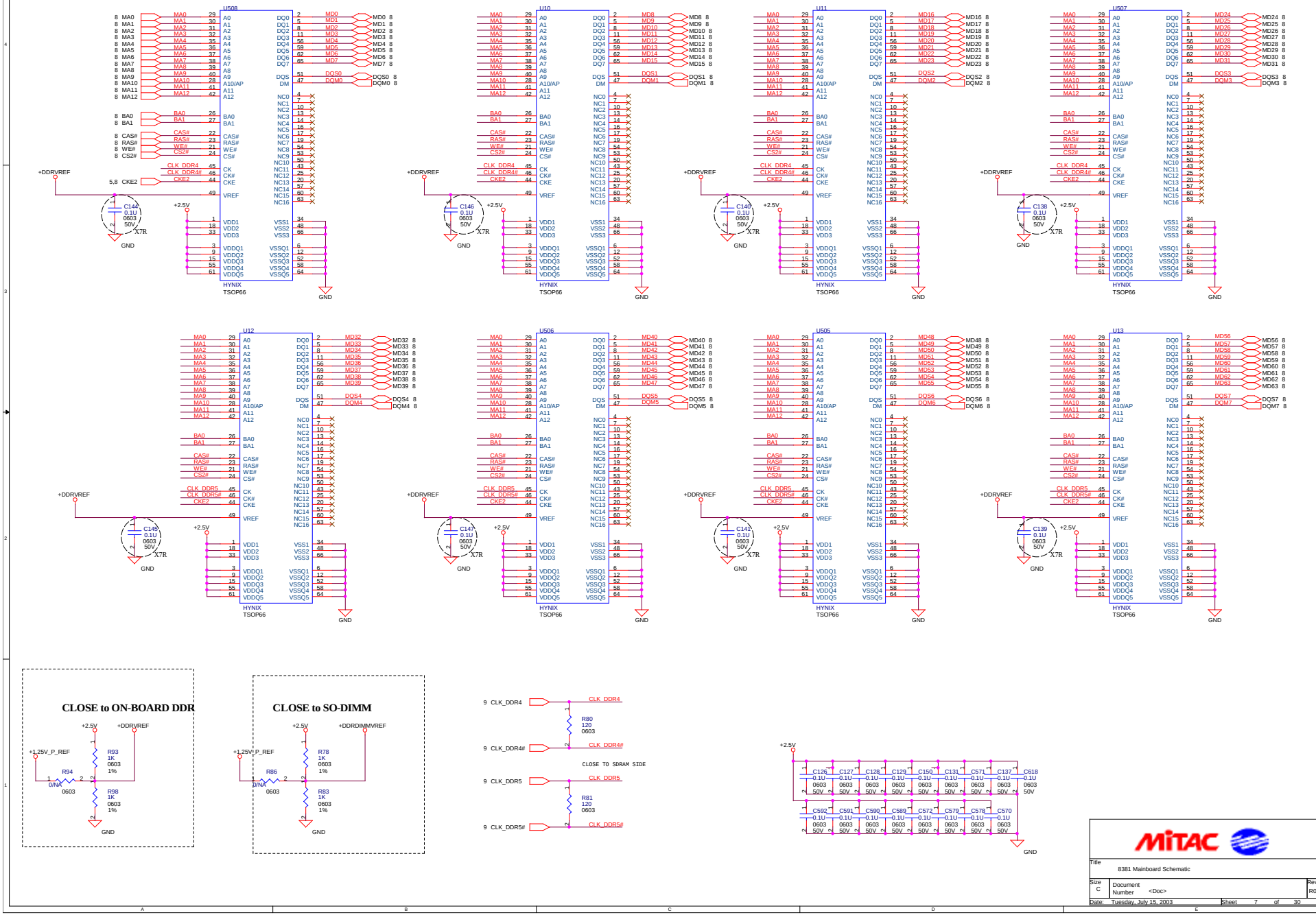


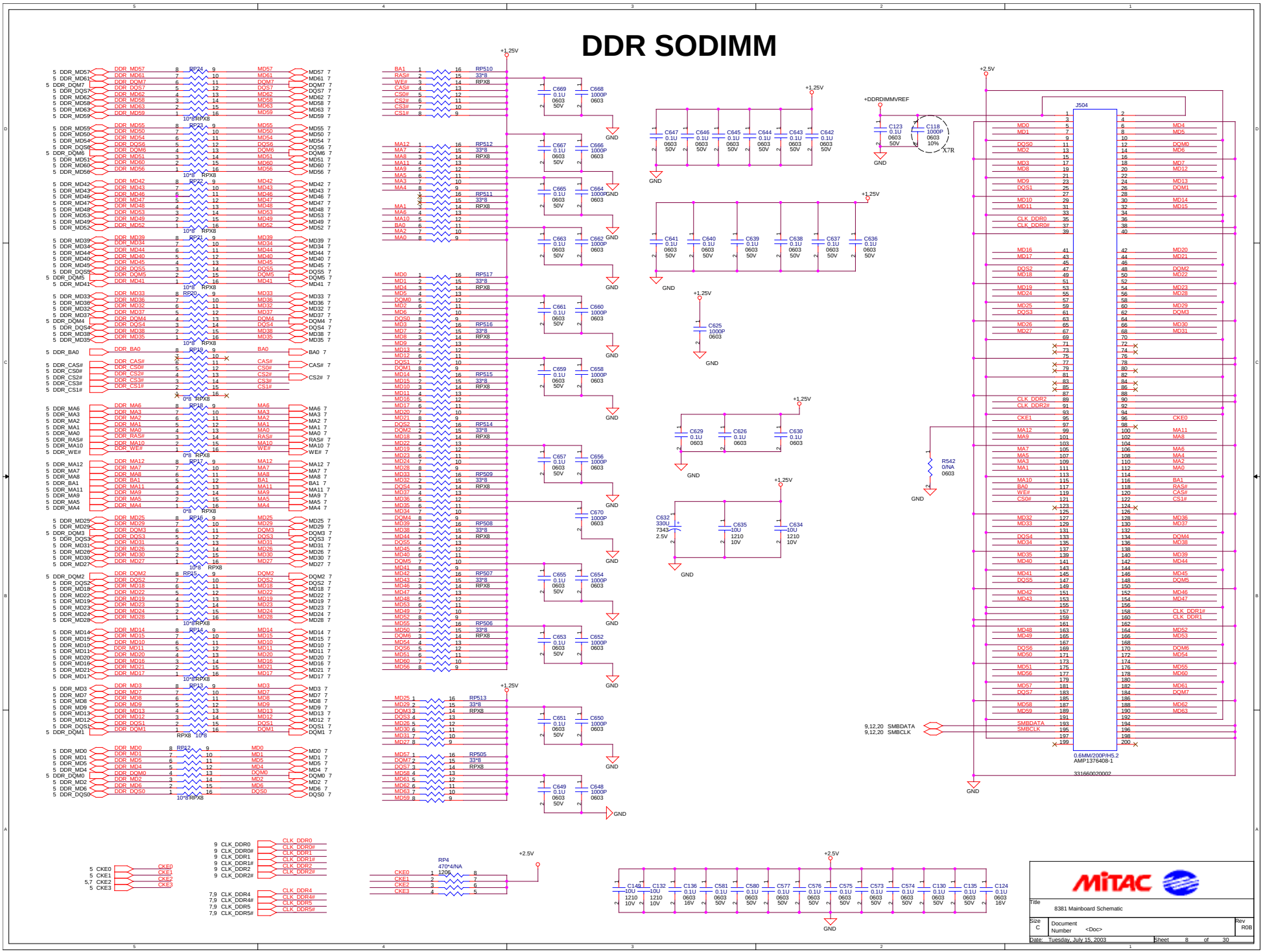


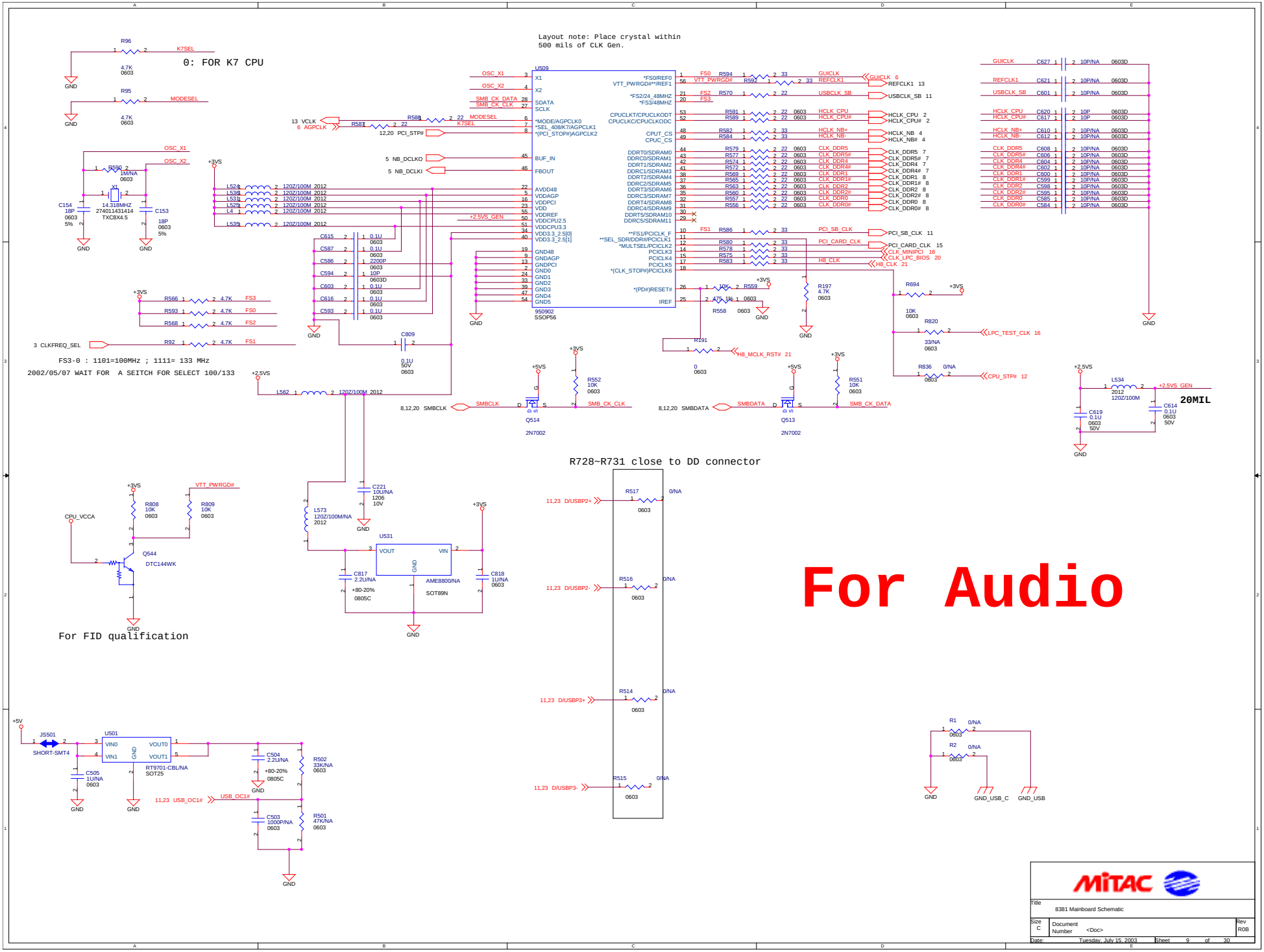




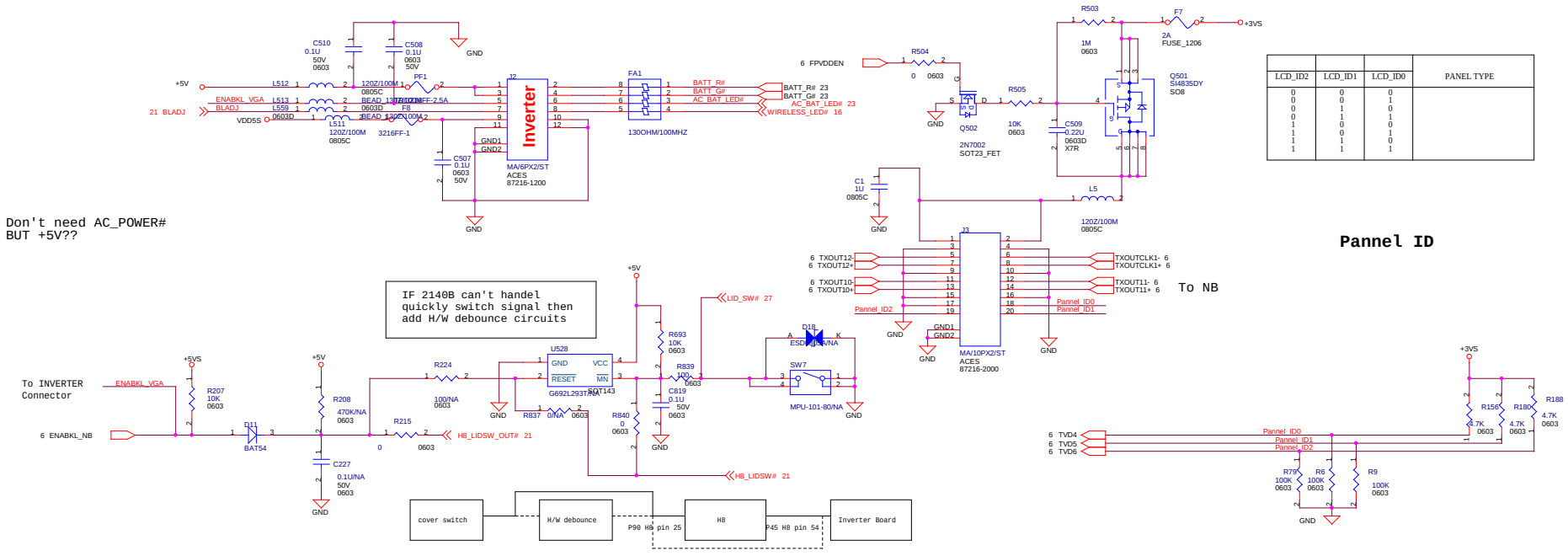
ON BOARD DDR





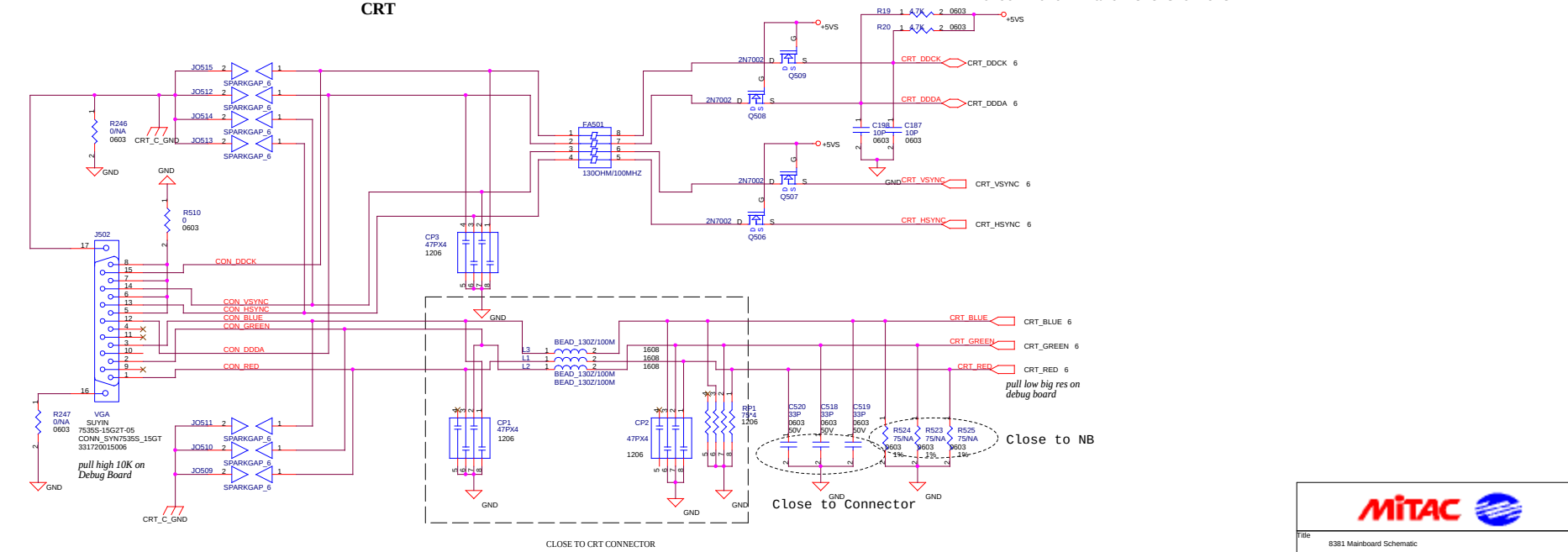


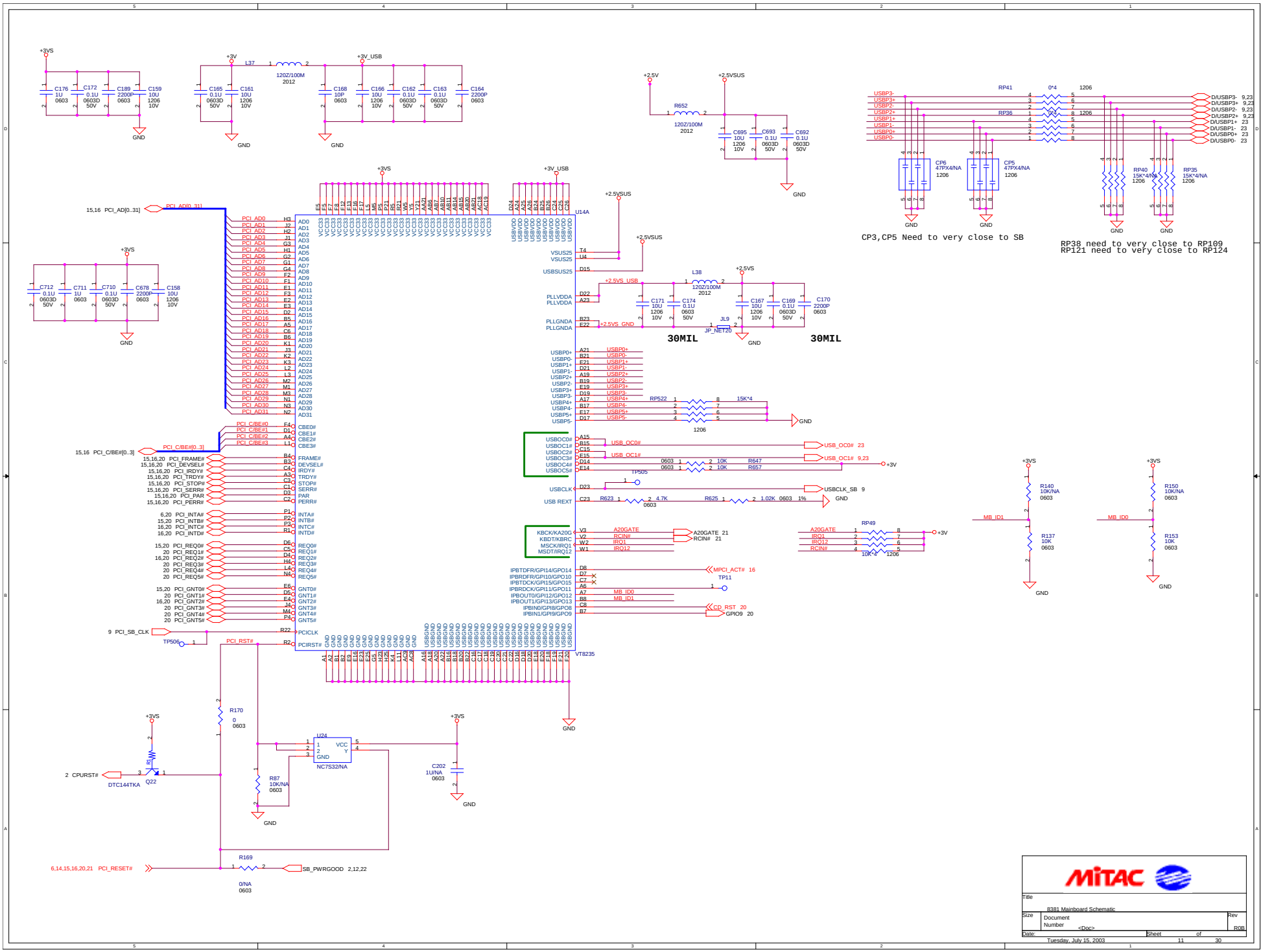
INVERTER

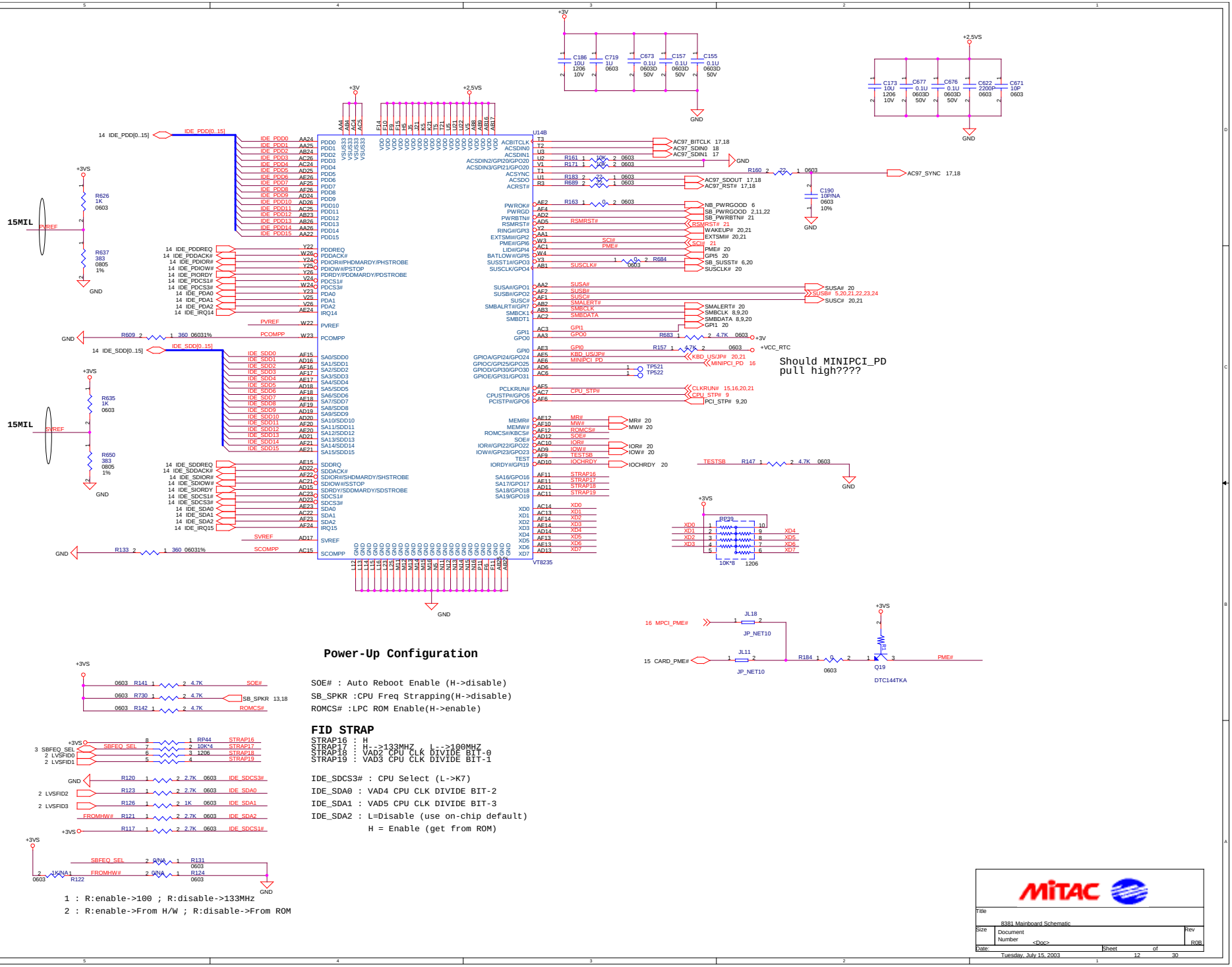


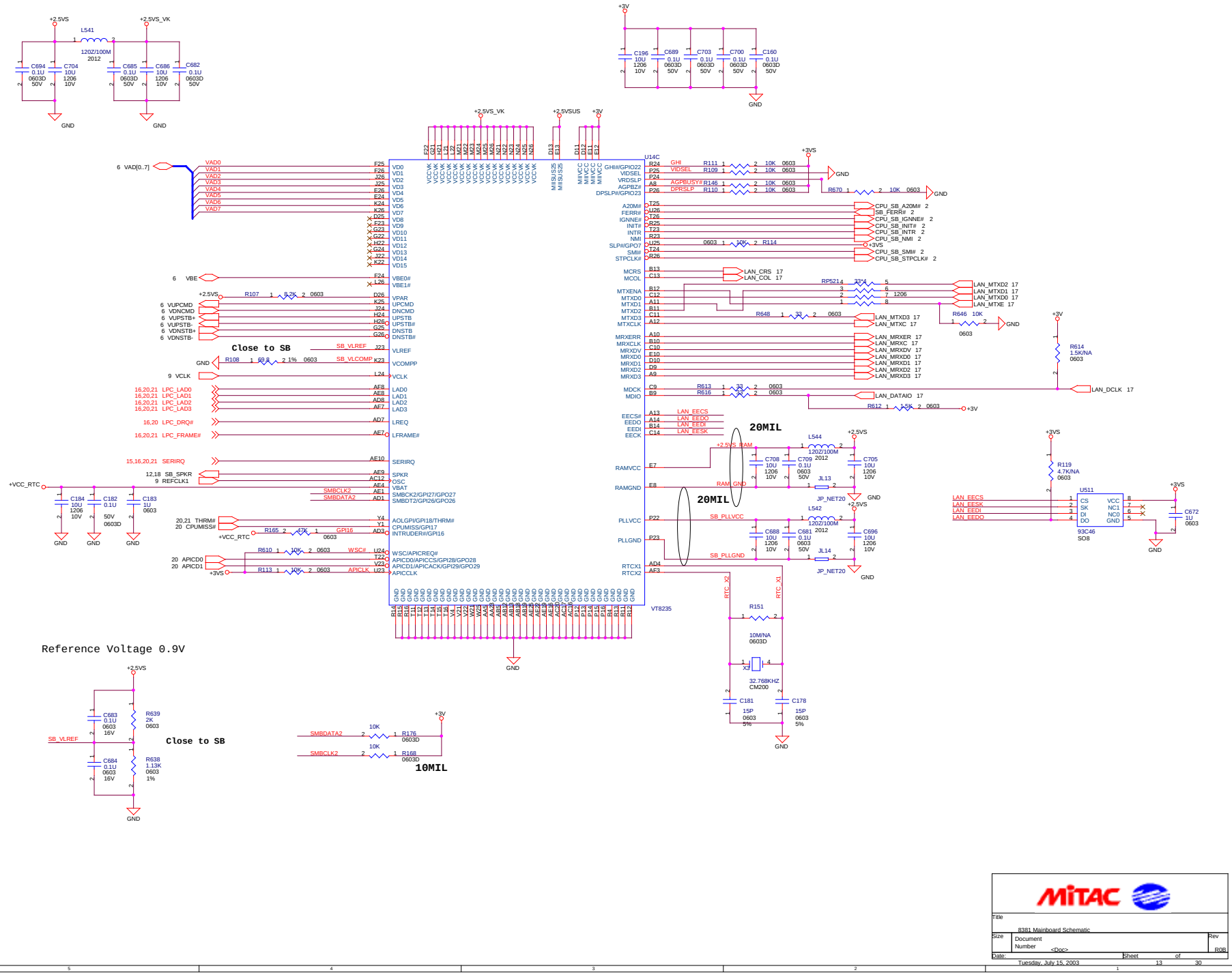
Check Power Plane is 3VS or 5VS

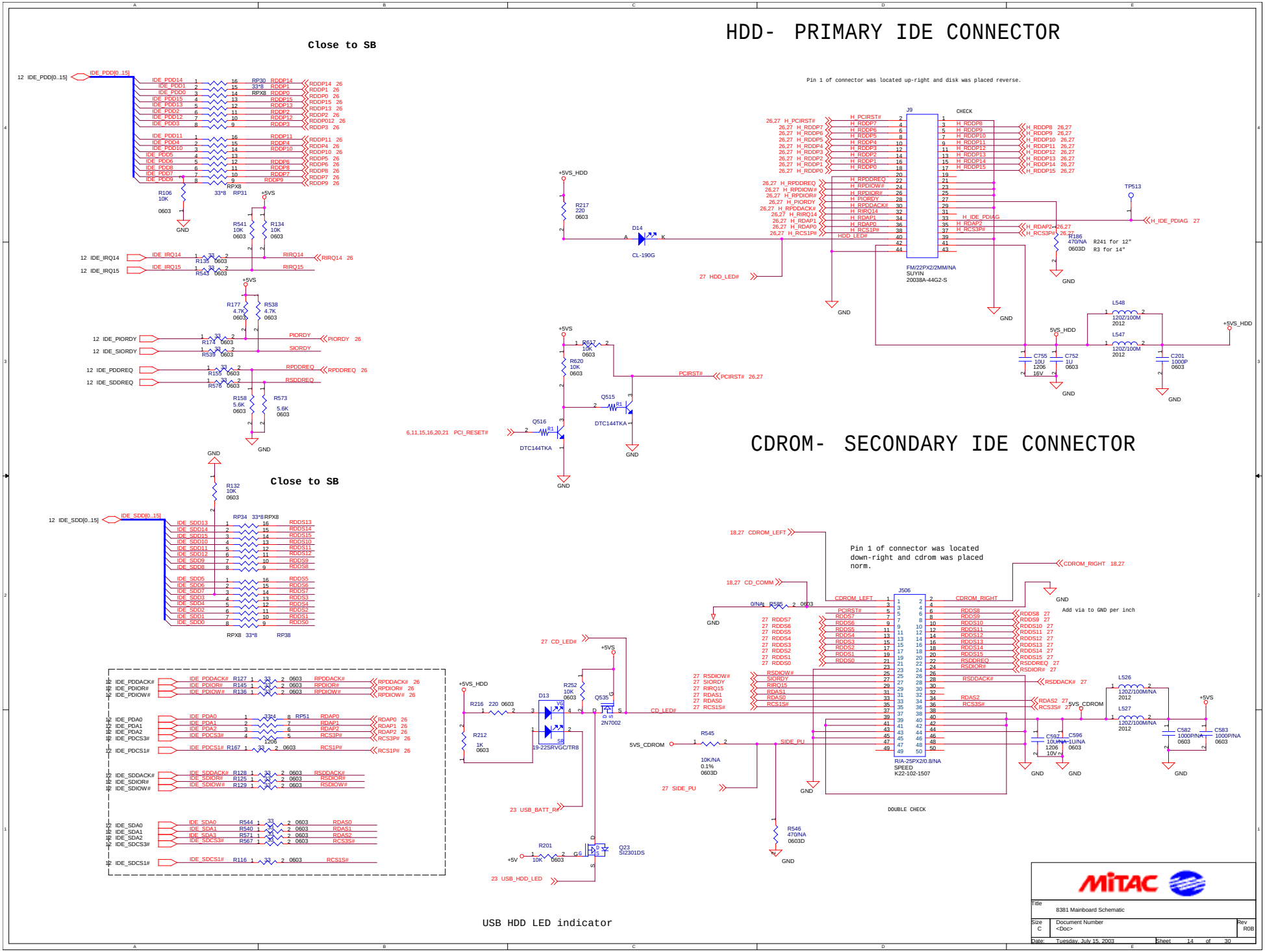
CRT



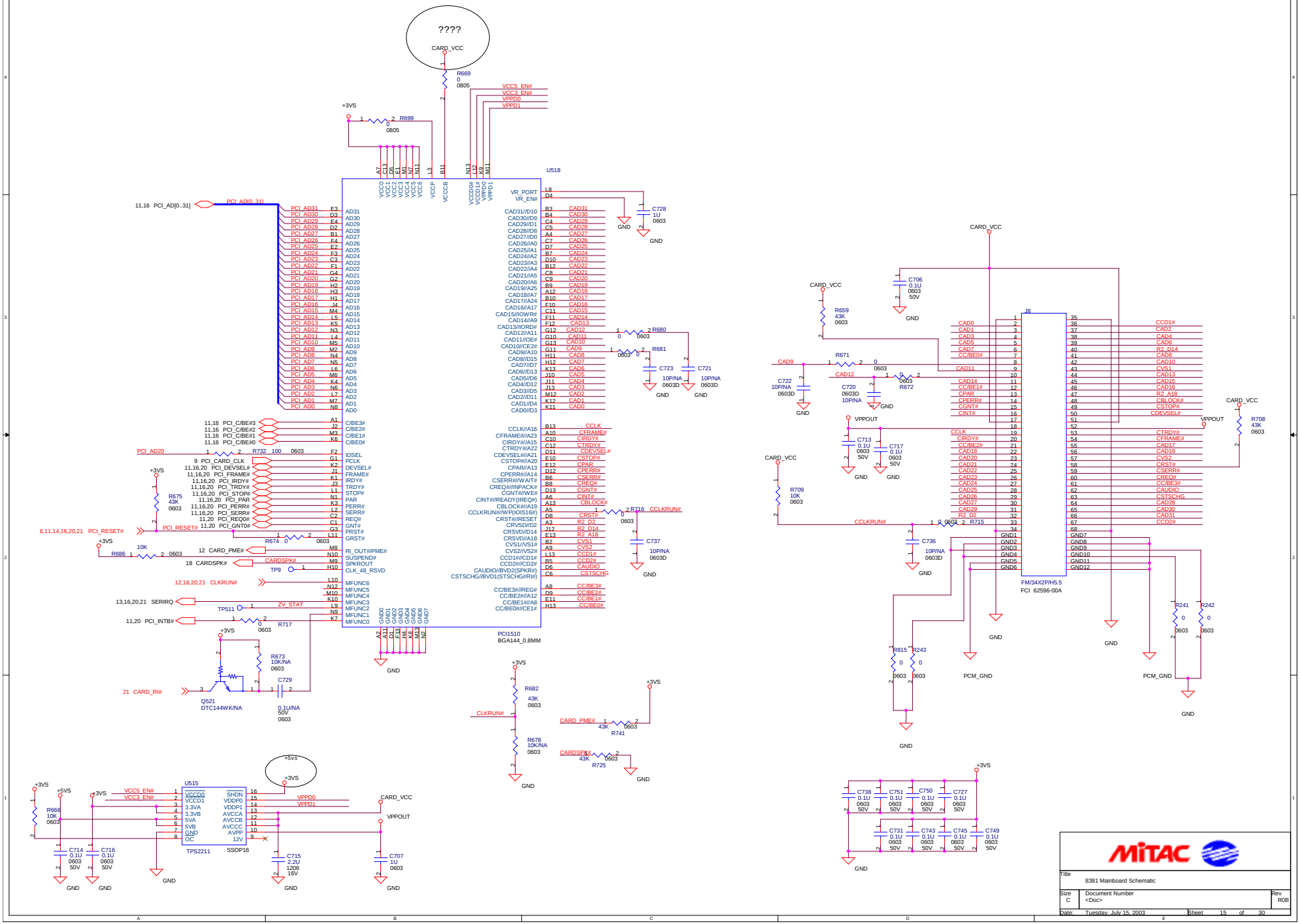


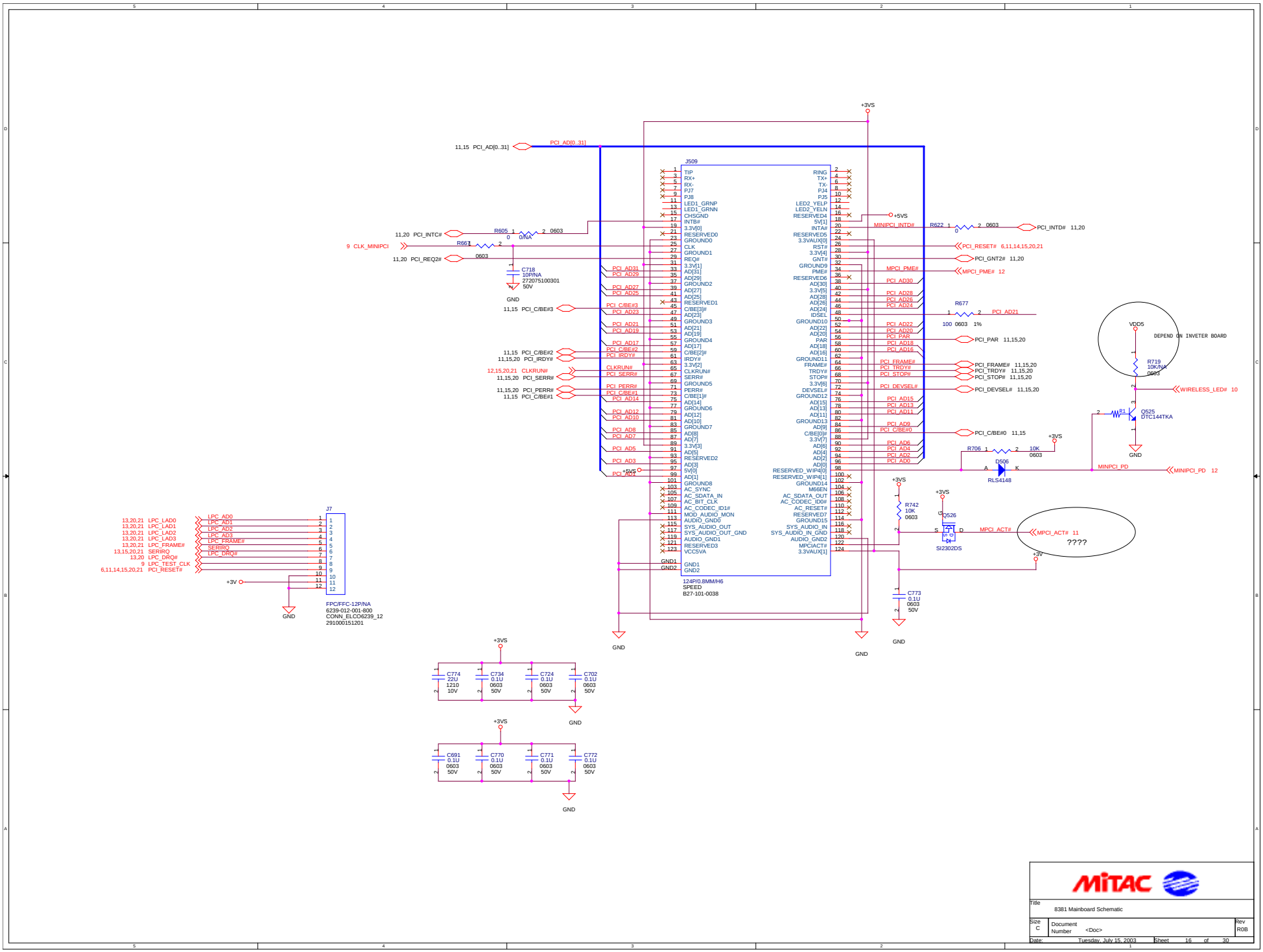






CARDBUS CONTROLLER





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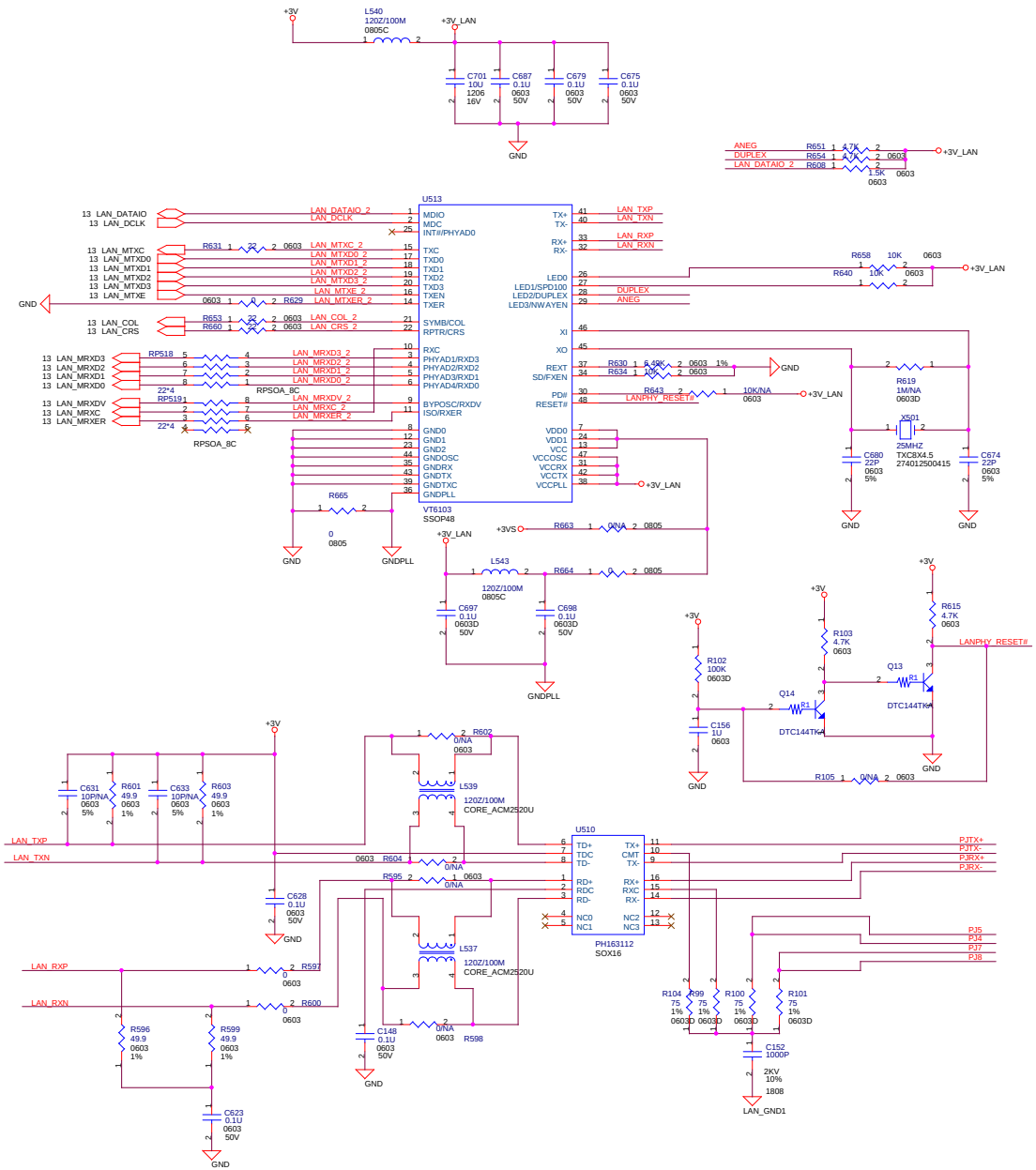
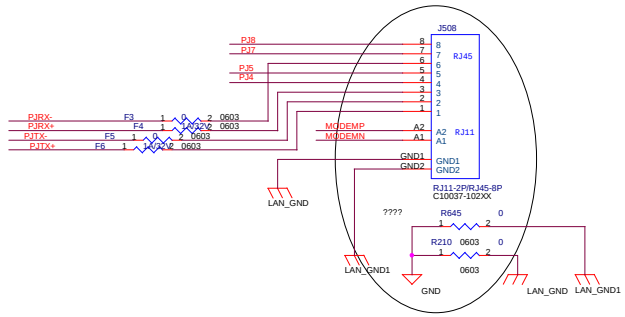


RJ45 & MDC CONNECTOR

RJ45



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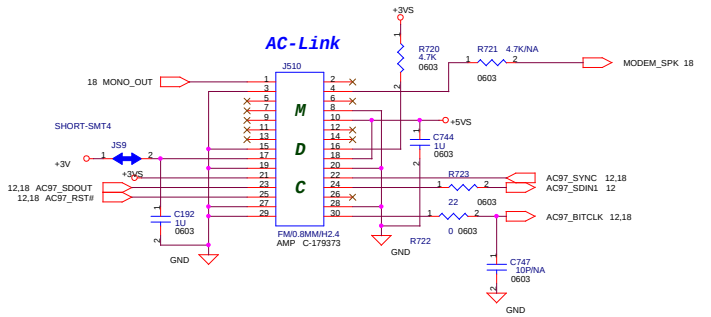
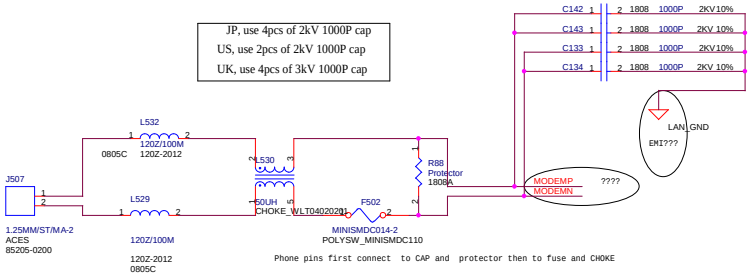


MDC JUMP WIRE CONNECTOR RJ-11



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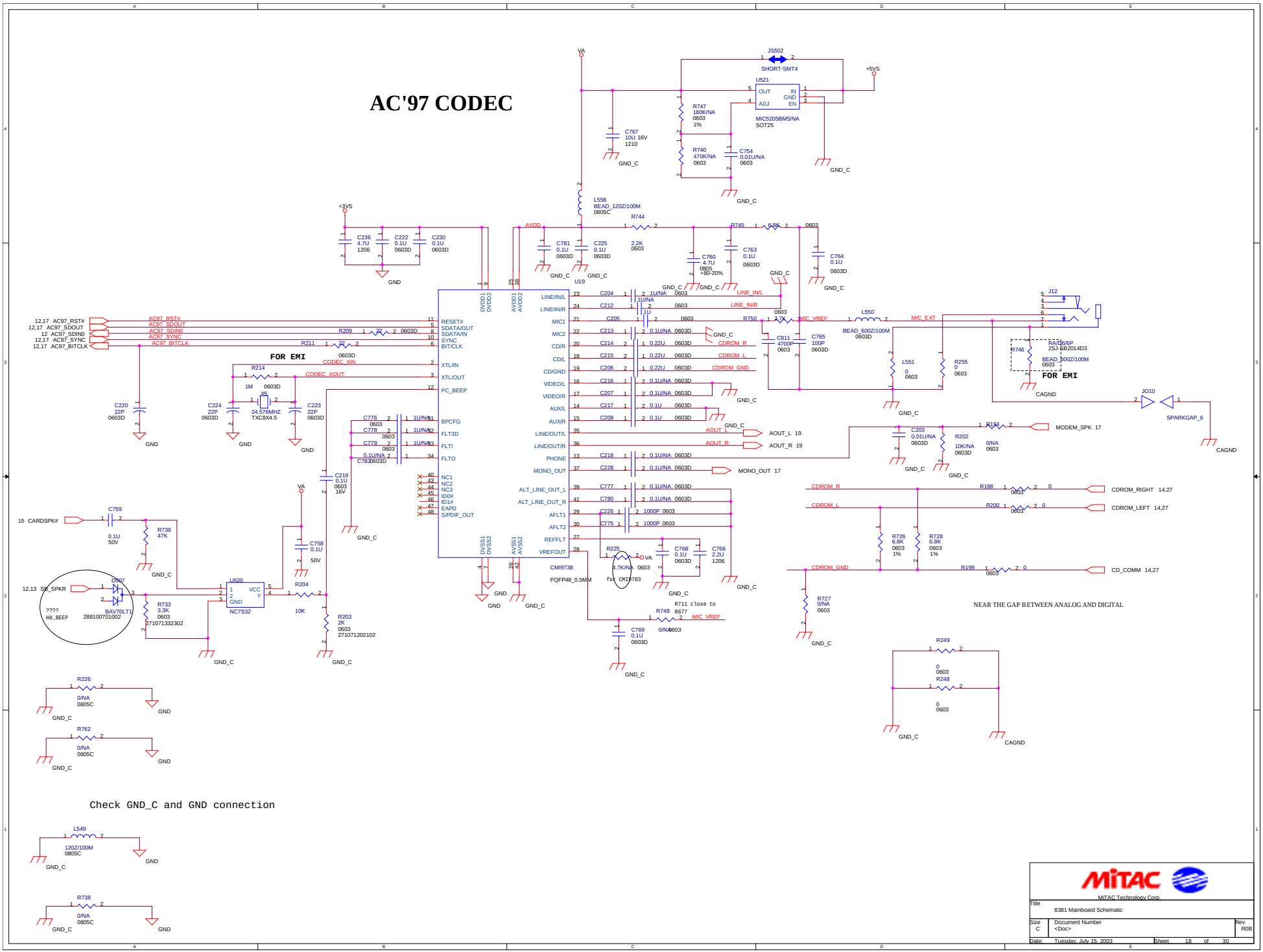
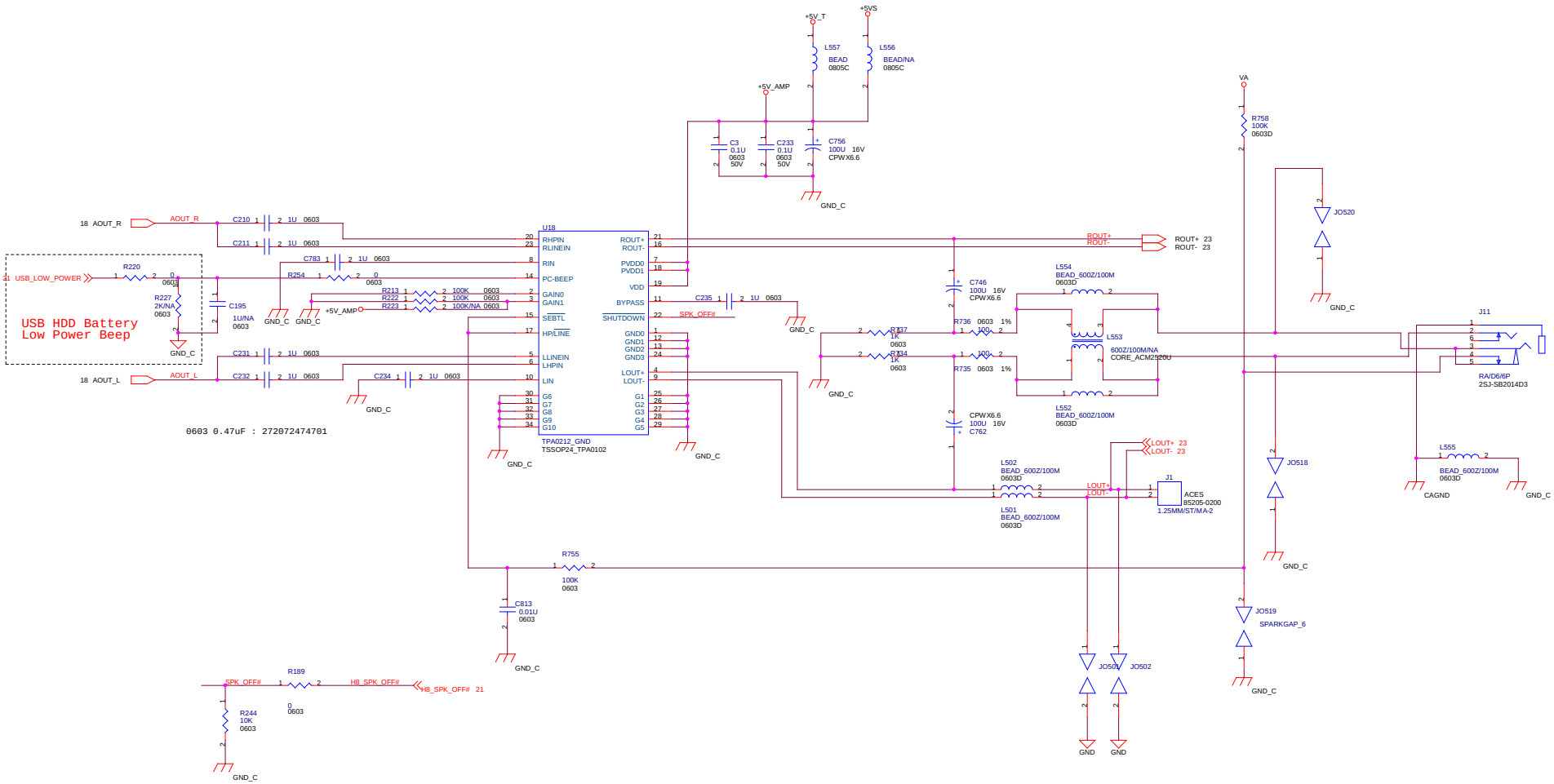


AUDIO AMPLIFIER - TPA0212



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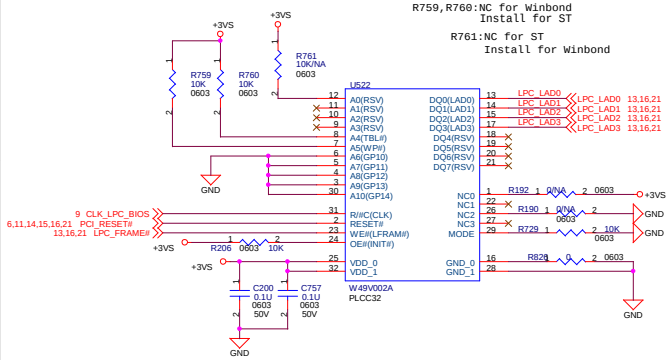
Sw12,sw13 for 14"

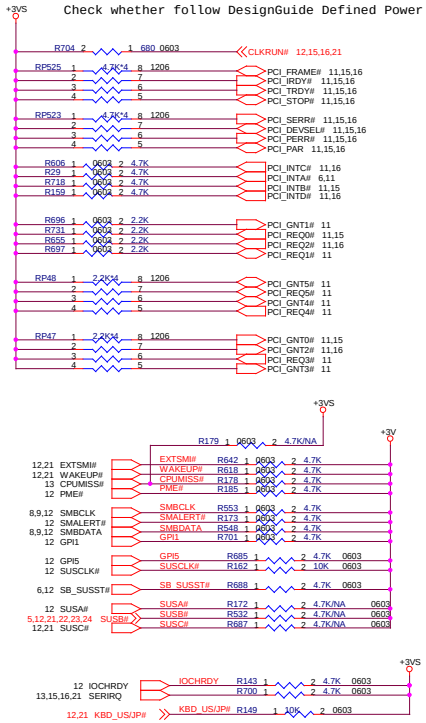
SYSTEM BIOS

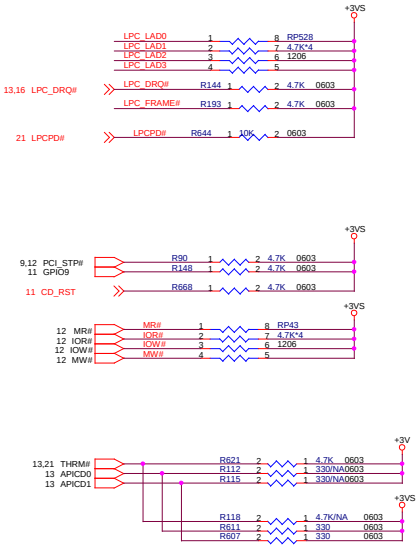
PIN2 :PCIRST# or PCIRST#B
???
R759,R760:NC for Winbond
Install for ST
R761:NC for ST
Install for Winbond



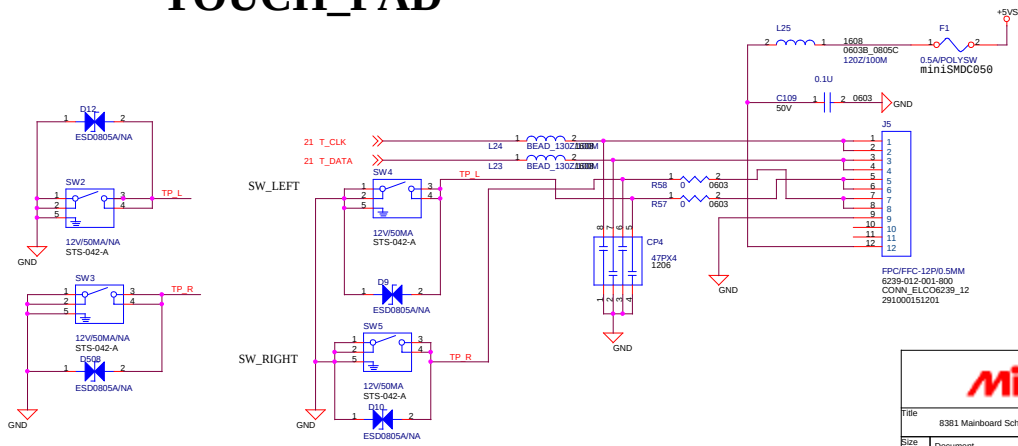
PCI PULL-HIGH

Check whether follow DesignGuide Defined Power Plane





TOUCH_PAD



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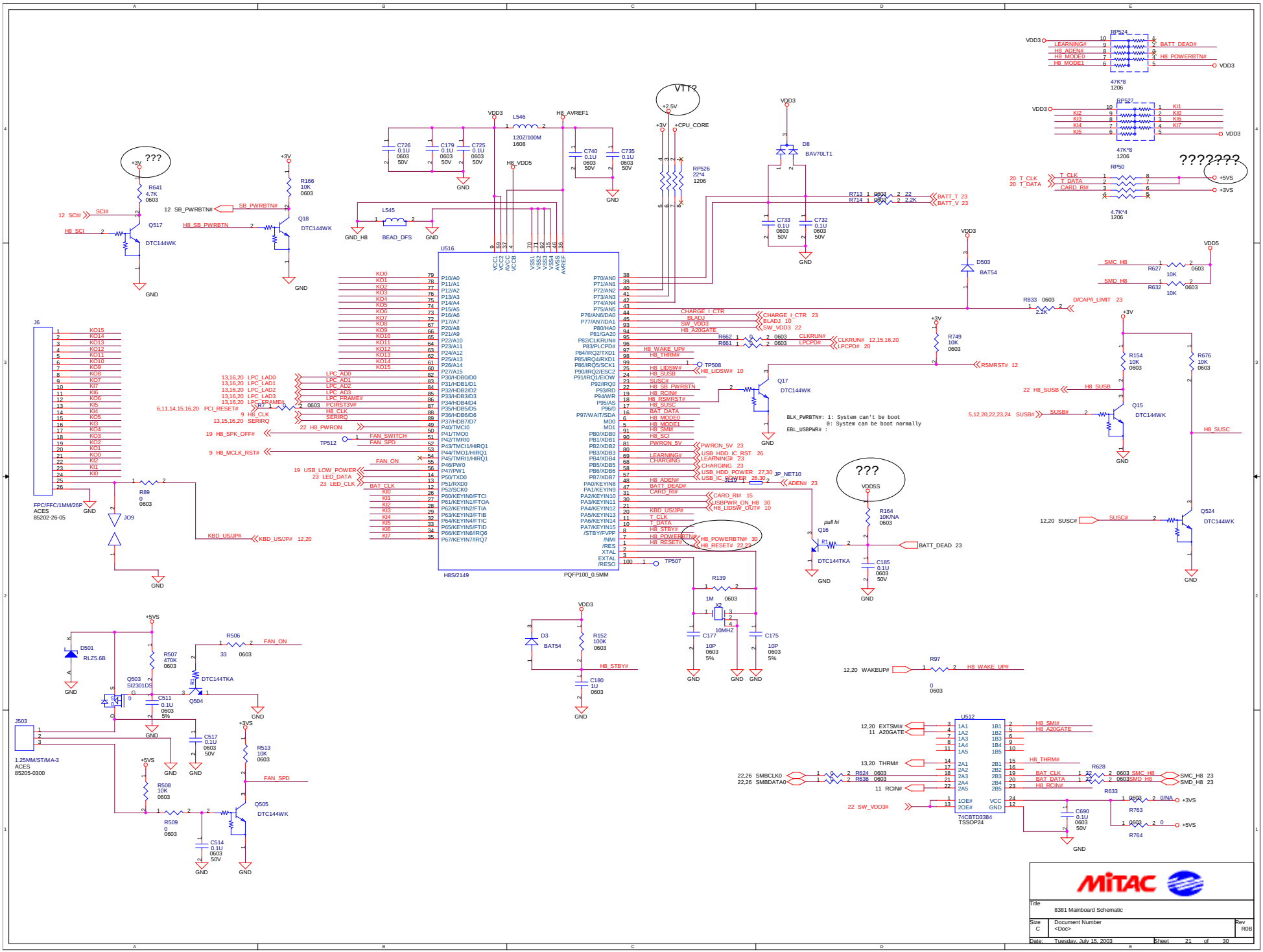
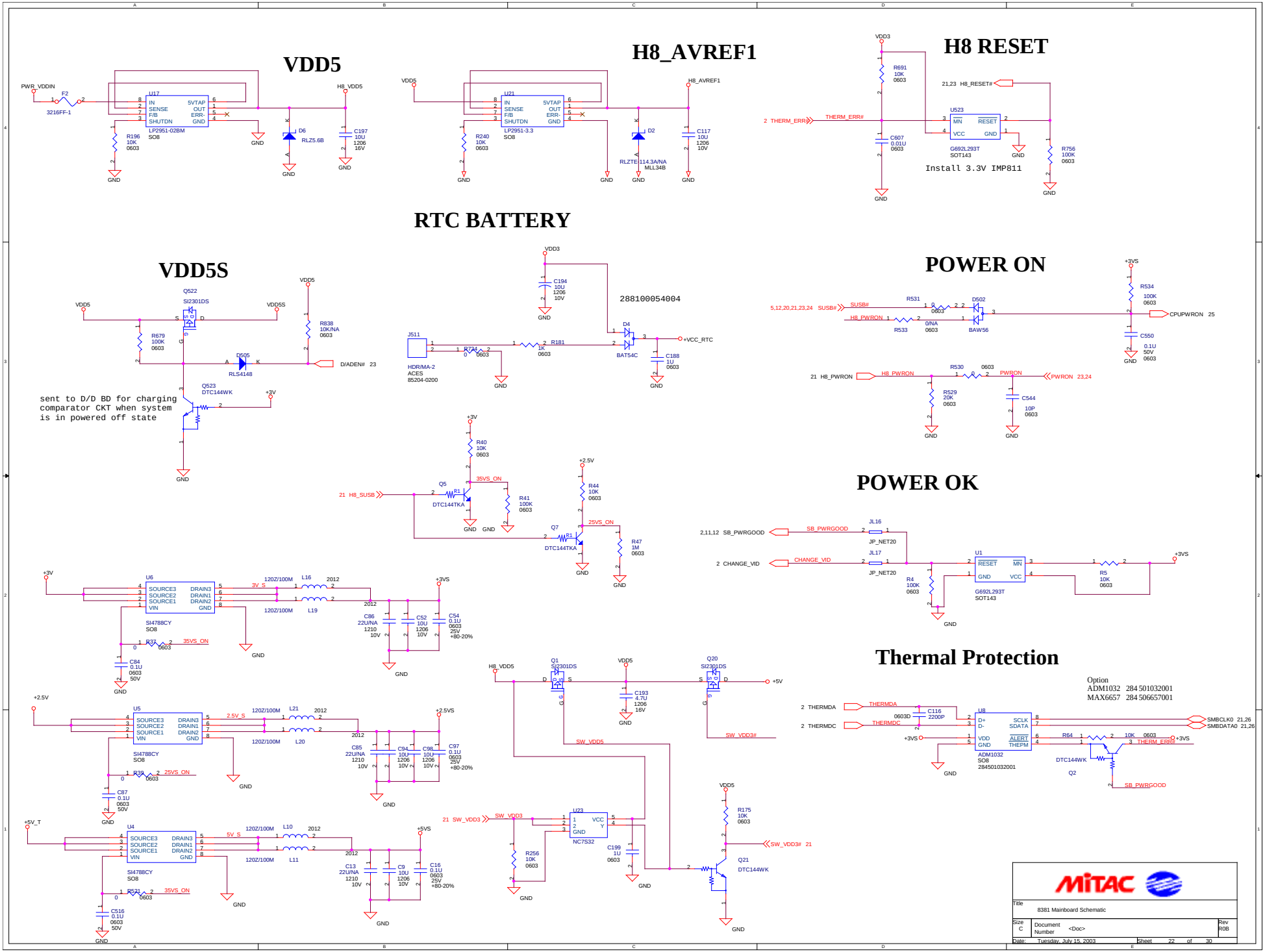
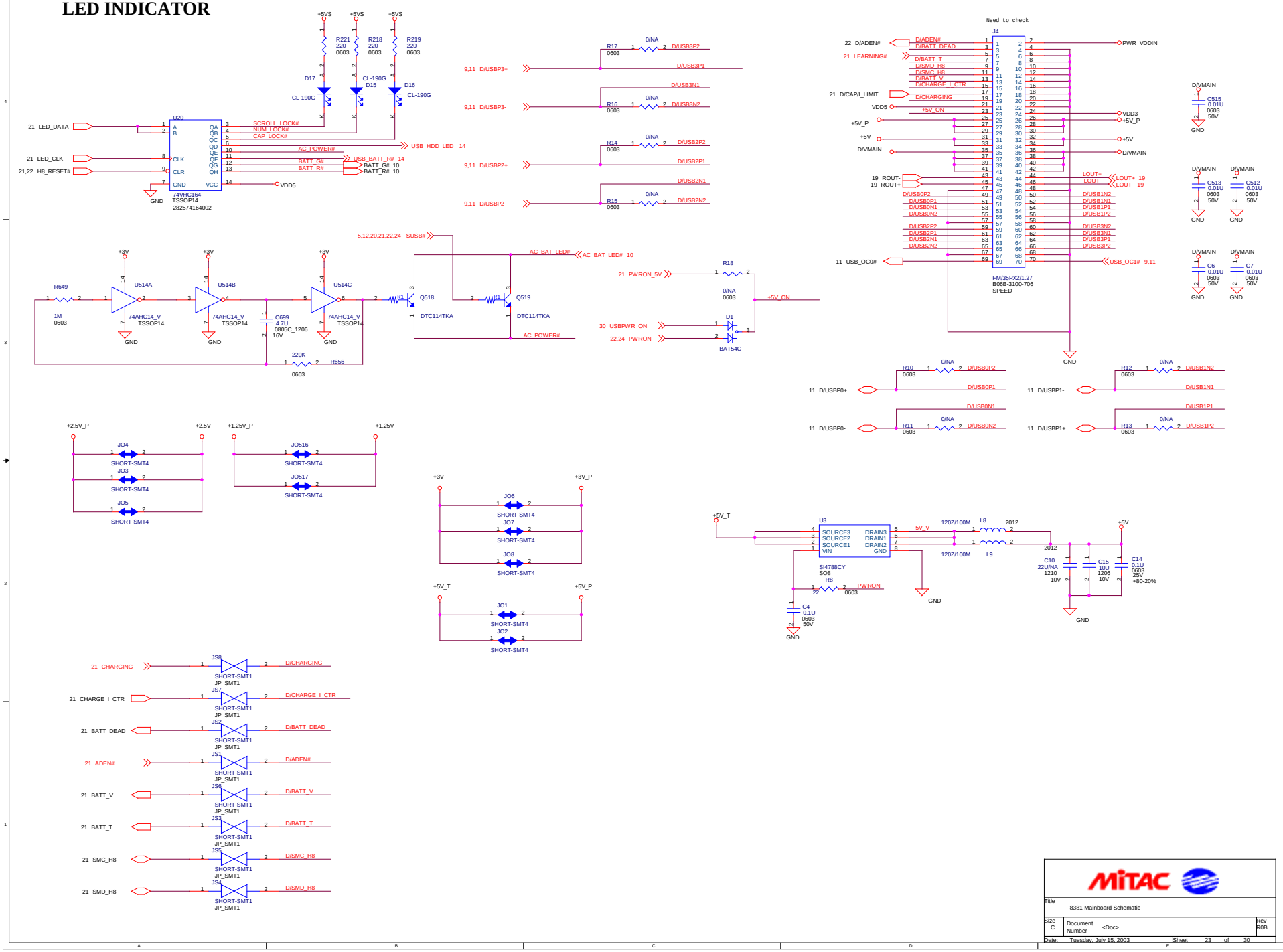
Date: Tuesday, July 15, 2003	Sheet 20 of 30	





LED INDICATOR



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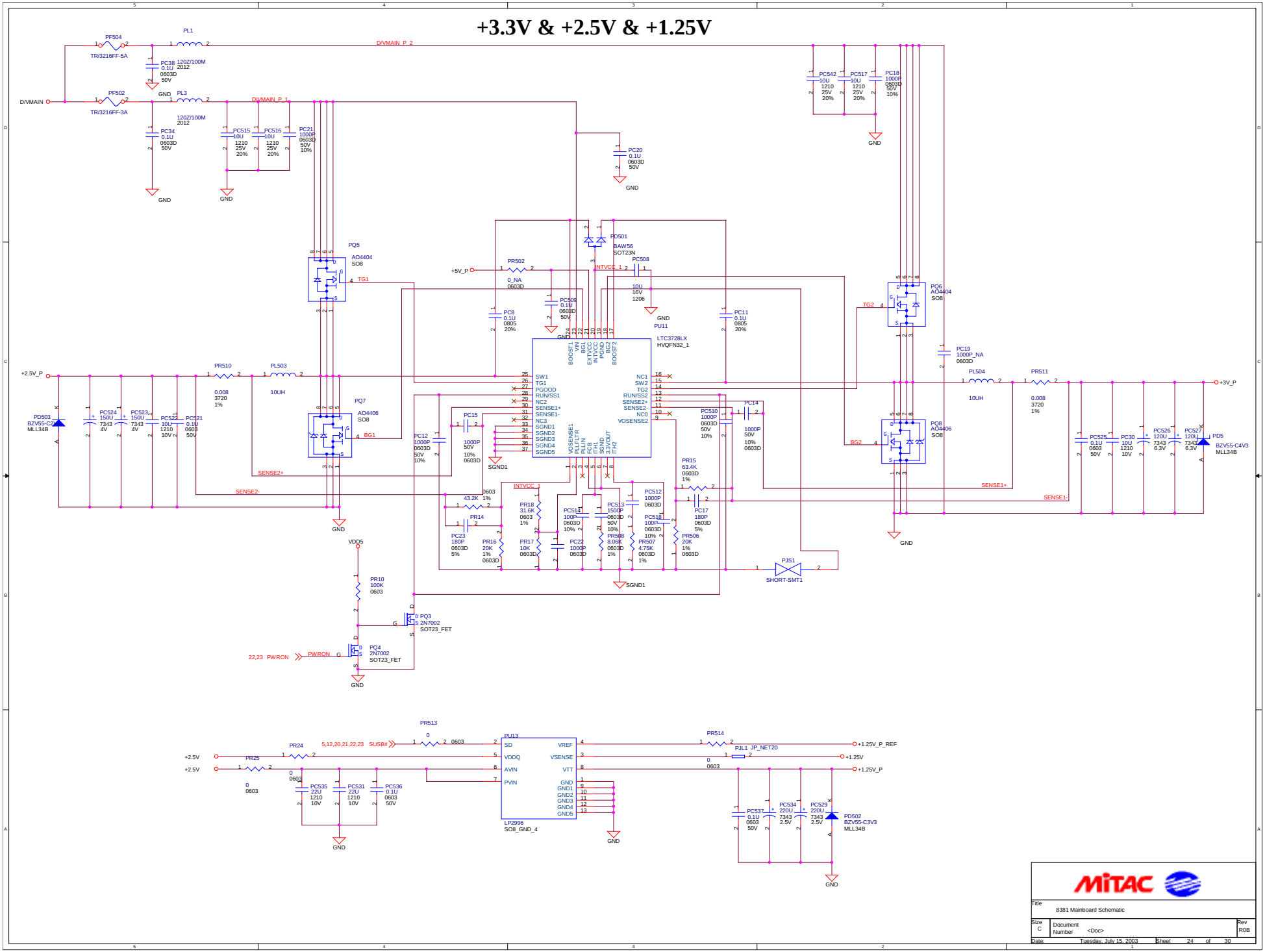
+3.3V & +2.5V & +1.25V



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Title: 8381 Mainboard Schematic

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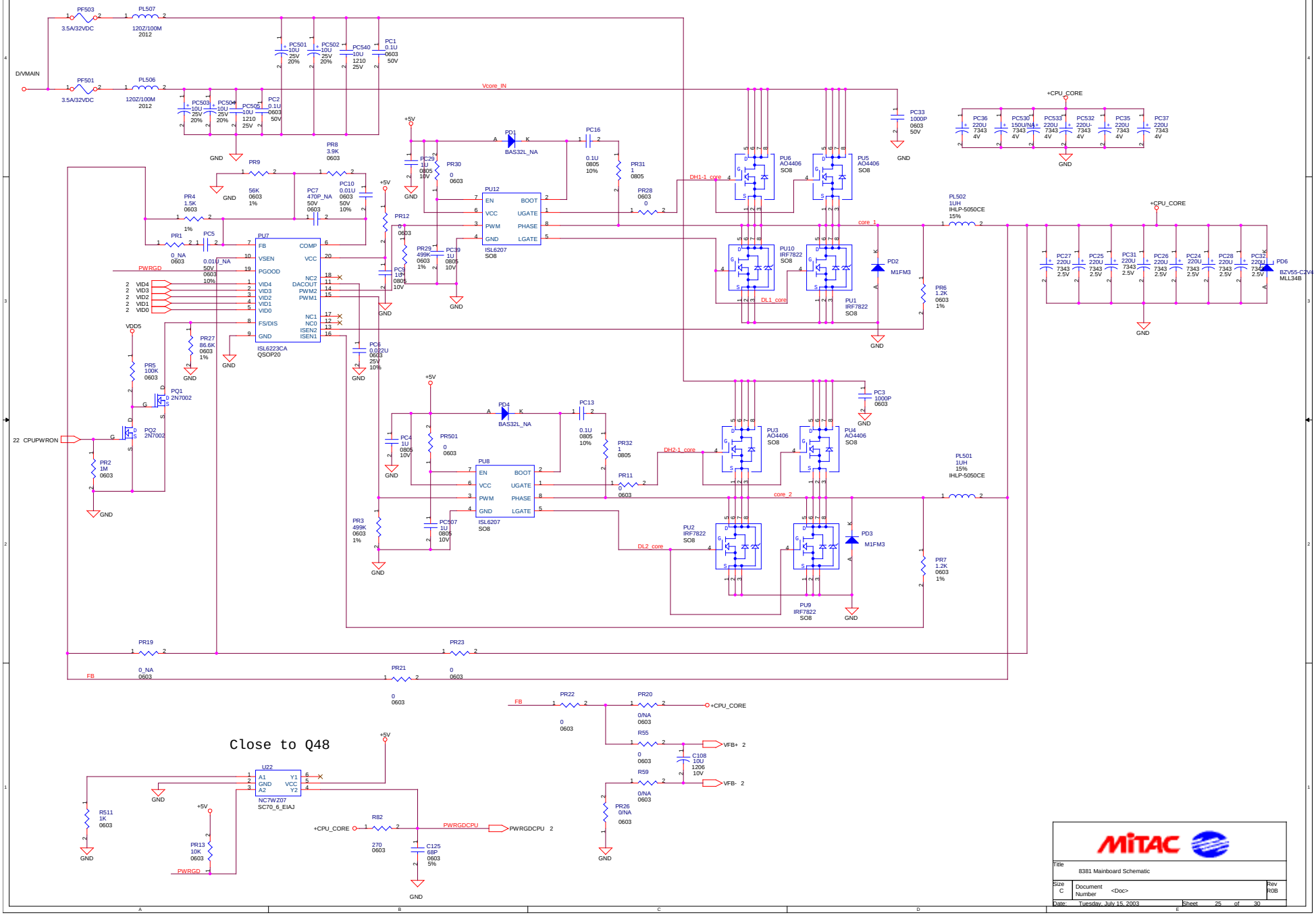
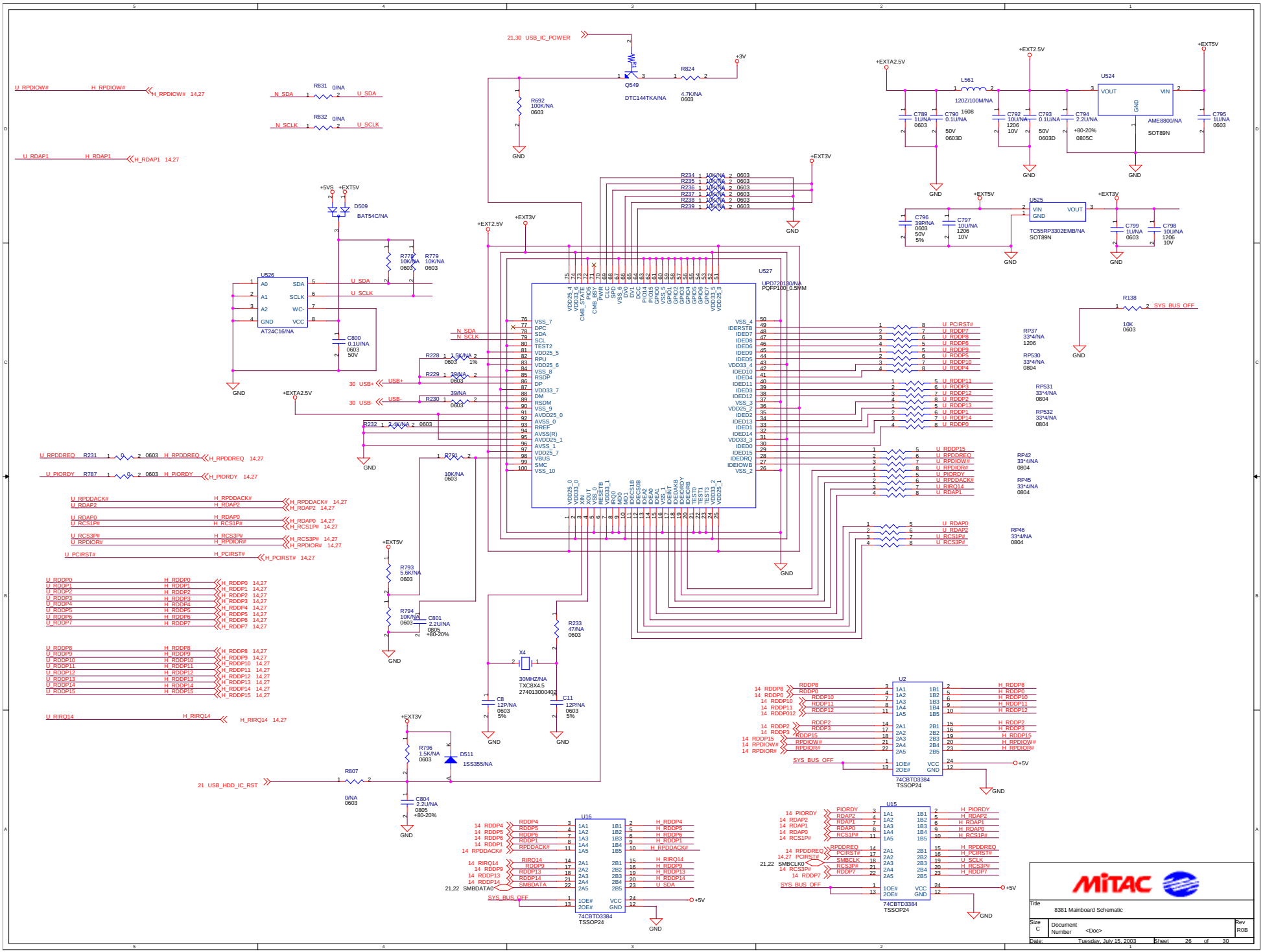
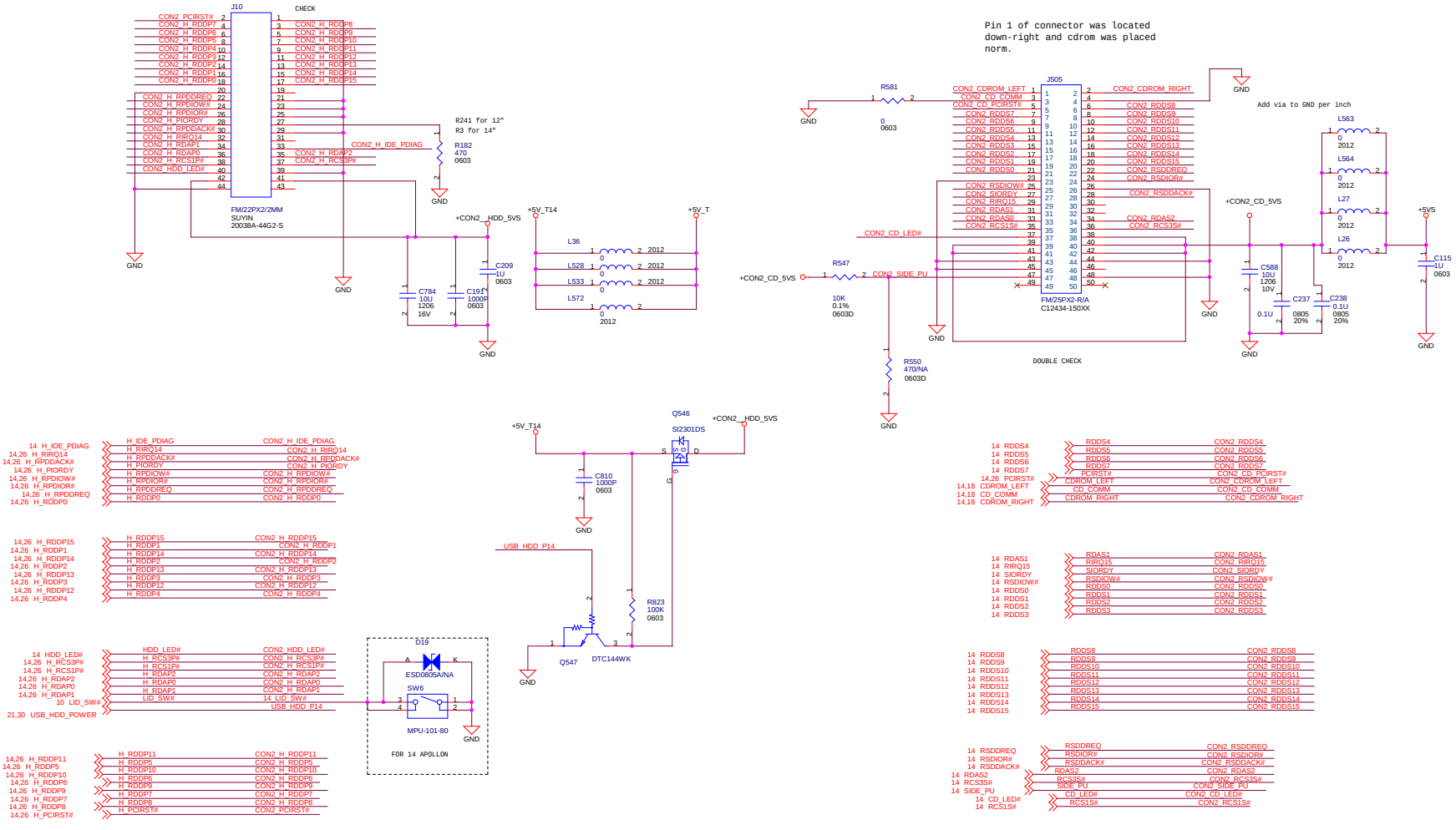
CPU_CORE





For APOLLON 14"



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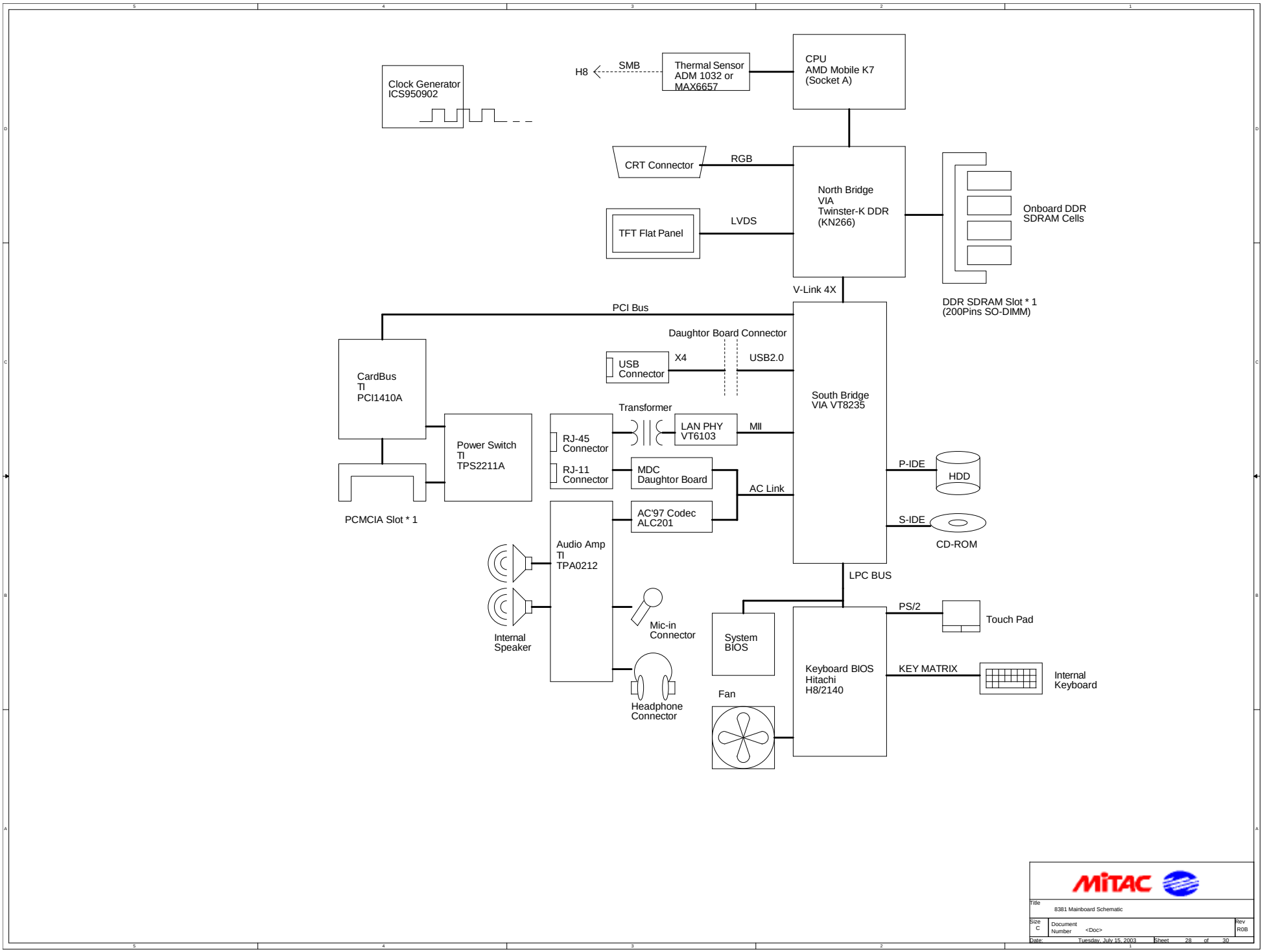
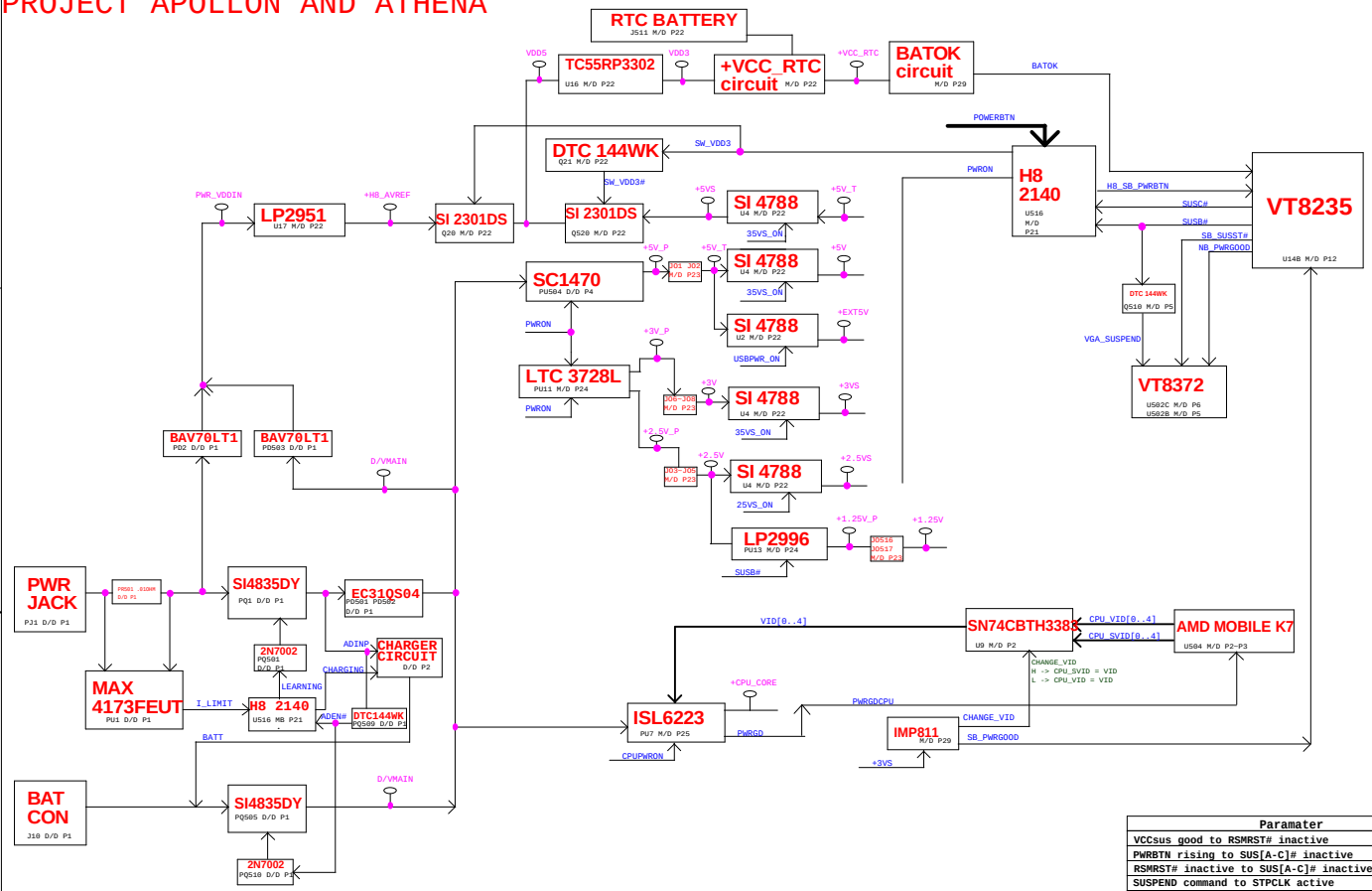


POWER SEQUENCE OF THE PROJECT APOLLON AND ATHENA



The power sequence of VT8235

Date : Jul 09,2002

Power On Sequence with default OFF

```
RTC power       lllrhhhhhhhhhhhhhhhhhhhhhh
Suspend power   lllllrhhhhhhhhhhhhhhhhhhh
RSMRST#         lllllllrhhhhhhhhhhhhhhhhh
Core power      lllllllllllllrhhhhhhhhhh
PWRGD           lllllllllllllllrhhhhhhhh
PWRBTN#         hhhhhhhhhhflrhhhhhhhhhhhh
SUS[A-C]        lllllllllllrhhhhhhhhhhhh
```

Power On Sequence with default ON

```
RTC power       lllrhhhhhhhhhhhhhhhhhhhhhh
Suspend power   lllllrhhhhhhhhhhhhhhhhhhh
RSMRST#         lllllllrhhhhhhhhhhhhhhhhh
Core power      lllllllllllllrhhhhhhhhhh
PWRGD           lllllllllllllllrhhhhhhhh
PWRBTN#         hhhhhhhhhhhhhhhhhhhhhhhh
SUS[A-C]        lllllllllllrhhhhhhhhhhhh
```

Power On Suspend sequence without RESET (S1)

```
Power           hhhhhhhhhhhhhhhhhhhhhhhhhhhhh
POS command     zznozzzzzzzzzzzzzzzzzzzzzzzz
Stop Grant      zzzznozzzzzzzzzzzzzzzzzzzzzz
Resume event    zzzzzzzzzzzzzzznozzzzzzzzzzz
STPCLK#         hhhflllllllllllllllllrhhhhhh
SLP#            hhhhhhflllllllllllllrhhhhhh
SUSTAT#         hhhhhhhflllllllllllrhhhhhhh
CPUSTP#         hhhhhhhflllllllllllrhhhhhhh
PCISTP#         hhhhhhhflllllllllrhhhhhhhhh
SUSA            hhhhhhhhflllllllllrhhhhhhhh
SUS[B-C]        hhhhhhhhhhhhhhhhhhhhhhhhhhh
```

Power On Suspend sequence with CPU/PCI RESET

```
Power           hhhhhhhhhhhhhhhhhhhhhhhhhh
POS command     zzznozzzzzzzzzzzzzzzzzzzzz
Resume event    zzzzzzzzzzzzzzznozzzzzzzzz
STPCLK#         hhhhhflllllllllrhhhhhhhhh
SLP#            hhhhhhflllllllllrhhhhhhhh
SUSTAT#         hhhhhhhhhhhhhhhhhhhhhhhhh
CPUSTP#         hhhhhhhflllllllllrhhhhhhh
PCISTP#         hhhhhhhflllllllllrhhhhhhh
SUSA            hhhhhhhhflllllllrhhhhhhhh
SUS[B-C]        hhhhhhhhhhhhhhhhhhhhhhhhh
PCIRST#         hhhhhhhhhhhhhhhflllllllrh
```

Suspend to RAM sequence

```
PWRGD           hhhhhhhhhflllllllllllrhhhh
Power           hhhhhhhhhhhhflllllllrhhhhh
POS command     zzznozzzzzzzzzzzzzzzzzzzzz
Resume event    zzzzzzzzzzzzzzzznozzzzzzzz
STPCLK#         hhhhhflllllrh"""""""""hhhhh
SLP#            hhhhhhflllllrh"""""""""hhhhh
SUSTAT#         hhhhhhhflllllllllllllllrhh
CPUSTP#         hhhhhhhhflll"""""""""llrhhh
PCISTP#         hhhhhhhhflll"""""""""llrhhh
SUS[A-B]        hhhhhhhhflllllllllrhhhhhhh
PWRGD           hhhhhhhhhflllllllllrhhhhhh
SUSC            hhhhhhhhhhhhhhhhhhhhhhhhhh
PCIRST#         hhhhhhhhhhfl"""""""""llllrh
```

Suspend to DISK sequence

```
PWRGD           hhhhhhhhhflllllllllllrhhhh
Power           hhhhhhhhhhhhflllllllrhhhhh
POS command     zzznozzzzzzzzzzzzzzzzzzzzz
Resume event    zzzzzzzzzzzzzzzznozzzzzzzz
STPCLK#         hhhhhflllllrh"""""""""hhhhh
SLP#            hhhhhhflllllrh"""""""""hhhhh
SUSTAT#         hhhhhhhflllllllllllllllrhh
CPUSTP#         hhhhhhhhflll"""""""""llrhhh
PCISTP#         hhhhhhhhflll"""""""""llrhhh
SUS[A-C]        hhhhhhhhflllllllllrhhhhhhh
PWRGD           hhhhhhhhhflllllllllrhhhhhh
PCIRST#         hhhhhhhhhhfl"""""""""llllrh
```

Paramater	Min	Max	Unit
VCCsus good to RSMRST# inactive	1		ms
PWRBTN rising to SUS[A-C]# inactive	4	5	RTCCLK
RSMRST# inactive to SUS[A-C]# inactive (default ON)	12	14	ms
SUSPEND command to STPCLK active	1	2	RTCCLK
STPCLK active to SLP# active (after stop grant cycle)		1	RTCCLK
SLP# active to SUSTAT# active		1	RTCCLK
SUSTAT# active to CPUSTP#/PCICTP# active		1	RTCCLK
CPUSTP#/PCISTP# active to SUS[A-C]# active		1	RTCCLK
Resume event to SUS[A-C] inactive		1	RTCCLK
SUSA# inactive to CPUSTP#/PCISTP# inactive	1		RTCCLK
PWRGD to CPUSTP#/PCISTP# inactive	1		RTCCLK
CPUSTP#/PCISTP# inactive to SUSTAT# inactive	1		ms
SUSTAT# inactive to PCIRST# inactive	250	375	us
	1		RTCCLK

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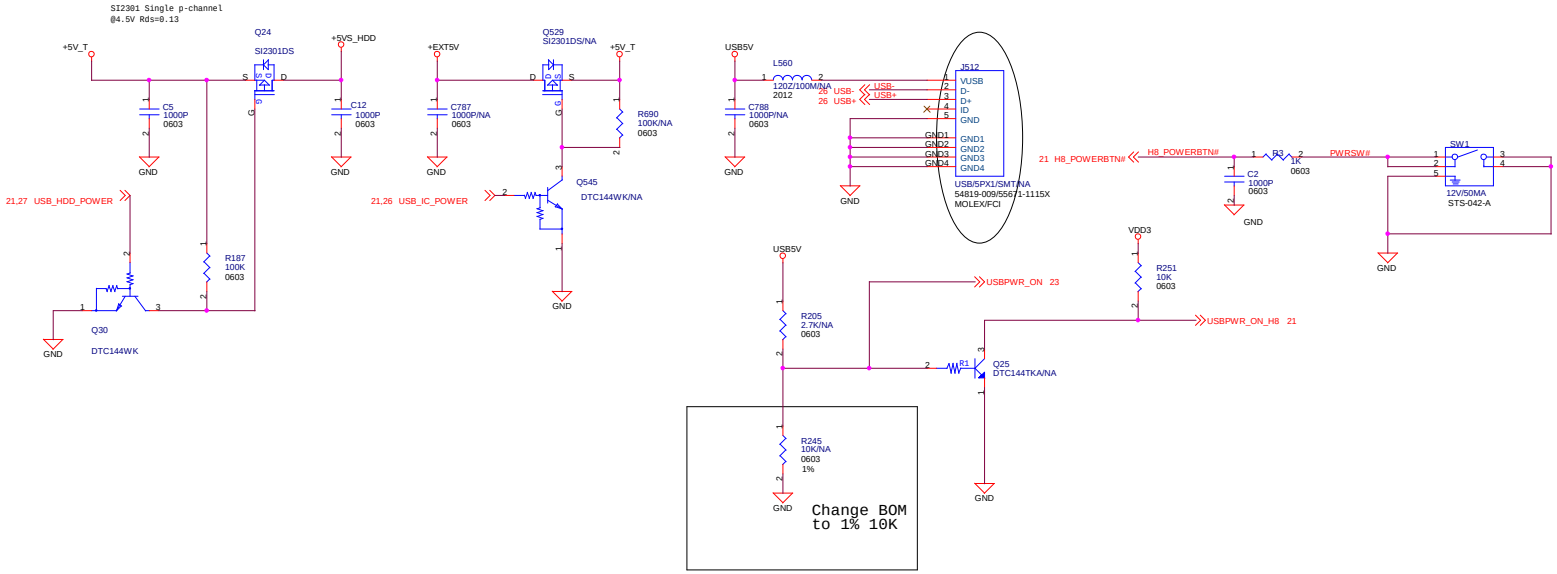
USB 2.0 HDD Power Control



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Reference Material

- **AMD Athlon XP Processor Model8 Data Sheet …….. … *AMD Corp***
- **VIA VT8372 North Bridge …… *VIA Technology INC***
- **VIA VT8235 South Bridge …… *VIA Technology INC***
- **HITACH H8S/2149 Hardare Specification……. *MITACH INC***
- **8381 Hardware Engineering Specification ……. *Technology Corp./MiTAC***

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