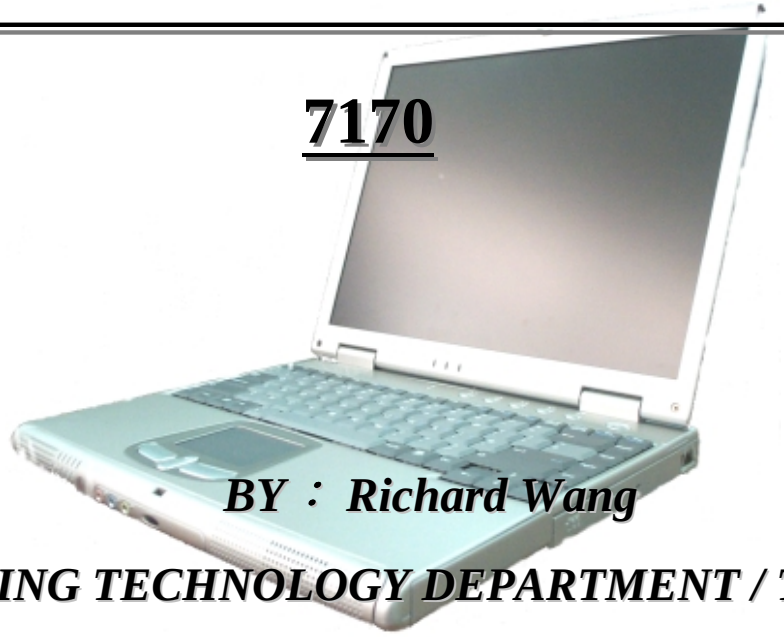
SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR

7170



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MiTAC

7170 N/B MAINTENANCE

CONTENTS

1. Hardware Engineering Specification ---------- **3**
- 1.1 Introduction ---------- 3
- 1.2 Hardware System ---------- 4
- 1.3 System Power Management ---------- 34
- 1.4 Firmware - System BIOS & Keyboard BIOS ---------- 37
- 1.5 Peripheral Component ---------- 39

2. System Assembly & Disassembly ---------- **43**
- 2.1 System View ---------- 43
- 2.2 System Disassembly ---------- 46

3. Definition & Location Connectors / Switches Setting ---------- **65**
- 3.1 7170 Main Board ---------- 65
- 3.2 7170 DC Power Board ---------- 68
- 3.3 7170 ESB Board ---------- 69
- 3.4 7170 Touch Pad Board ---------- 69

4. Definition & Location Of Major Components ---------- **70**
- 4.1 7170 Main Board ---------- 70

5. Pin Descriptions Of Major Components ---------- **72**
- 5.1 Pentium III/Celeron µPGA2 CPU ---------- 72
- 5.2 VIA VT8603 Twister North Bridge Controller ---------- 78
- 5.3 VIA VT8231 Sorth Bridge Controller ---------- 88

7170 N/B MAINTENANCE

CONTENTS

6. System Block Diagram ---------- 100

7. Maintenance Diagnostic ---------- 101
- **7.1 Introduction ---------- 101**
- **7.2 Error Codes ---------- 102**
- **7.3 Diagnostic Tools ---------- 108**
- **7.4 Circuit ---------- 108**

8. Trouble Shooting ---------- 109
- **8.1 No Power ---------- 110**
- **8.2 No Display ---------- 118**
- **8.3 VGA Controller Failure ---------- 121**
- **8.4 Memory Test Error ---------- 123**
- **8.5 Keyboard (K/B) , Touch-Pad (T/P) , ESB Test Error ---------- 125**
- **8.6 CD-ROM Drive Test Error ---------- 127**
- **8.7 Hard Drive Test Error ---------- 129**
- **8.8 USB Port Test Error ---------- 131**
- **8.9 PIO Port Test Error ---------- 133**
- **8.10 Audio Failure ---------- 135**

9. Spare Parts List ---------- 137

10. System Explode View ---------- 146

11. Circuit Diagram ---------- 147

12. Reference ---------- 175

7170 N/B MAINTENANCE

1. Hardware Engineering Specification

1.1. Introduction

1.1.1. General Description

This document describes the system hardware engineering specification for 7170 portable notebook computer system. The 7170NB is a excellently high performance and highly portable platform.

1.1.2. System Overview

The Architecture of 7170NB is based on PCI - ISA structure. It provides a high performance platform on PCI bus up to 33MHz and is fully compatible with IBM PC/AT specification which have standard hardware peripheral interface and supports AGP 4X(133MHz). 7170NB adopts Intel Celeron 128K integrated level 2 cache in a FC-PGA package which have an excellent ability of code execution for multimedia applications operating at 700/733/766 and 800MHz & Intel Pentium Ⅲ CPU , 256K integrated level 2 cache in a FC-PGA package which have an excellent ability of code execution for multimedia applications operating at 800/866/933/1G and 1.33GHz

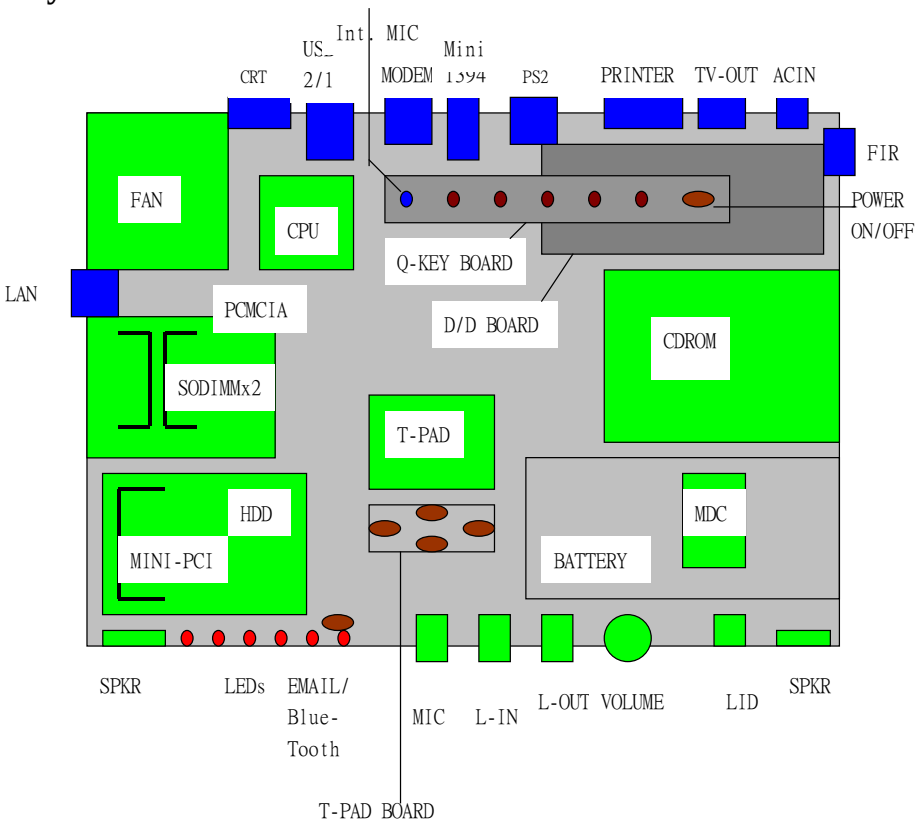
The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS ROM setup which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides LEDs to display system status, such as HDD, FDD, CD-ROM, NUM LOCK, CAP LOCK, SCROLL LOCK, AC Power indicator and battery present, capacity & charging, email/Blue-tooth status 7170NB system is equipped with one 2.5”, hard disk drive(supports Ultra DMA33/66), one 5 1/4" 24x CD-ROM drive(DVD optional), one USB floppy, one 56kbps Fax/Modem, one 10/100 Mb LAN, one PCMCIA sockets, internal keyboard, Touch pad with scroll-up/down buttons, two stereo speakers, TFT LCD panel, one FIR, PIO/TV-OUT, one VGA connector for CRT and one PS/2 port for external keyboard or mouse. System also provides in-system flash ROM programming for easy future upgrade.

A full set of software drivers and utilities are available to allow advanced operating system such as Windows 98 , Windows 98SE ,Window NT ,Window2000, Windows ME and Windows XP to take full advantages of the hardware capabilities. Features such as bus mastering IDE, Windows 98-ready Plug & Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will describe more detail for each individual sub-systems and functions.

1.2. Hardware System

1.2.1 System block



1.2.2 System parts

- CPU : Intel Celeron (700/733/766/800MHz) with FC-PGA package OR
  Intel Pentium Ⅲ (800EB/866/933/1000/1133MHz) with FC-PGA package
  Space reserve for VIA CyrixIII
- CORE LOGIC :
  VIA VT8603 (North Bridge : 66/100/133 SOCKET 370 CPU
  Integrated S3 Savage4 AGP4X Graphics Core with LVDS Interface
  Memory Controller Supporting PC100/PC133 SDRAM
  VIA VT8231(South Bridge) : PC99 Compliant PCI to ISA Bridge
  Integrated Super-IO (LPT, COM)
  Integrate Fast Ethernet
  AC97 Audio, USB, RTC
  UltraDMA-33/66 Master Mode PCI-EIDE Controller for HDD, DROM/DVD
  ACPI, EPM, SMBus, Temperature Monitor
- PCMCIA Controller : TI PC4410(PCMCIA) + TPS2211(Power Switch)
- 1394 Controller : TI PC4410(MAC) + TSB41AB1(PHY)
- FIR Controller : NS 97338VJG
- Embedded Controller : Hitachi H8/3437S
- Audio System : Codec RealTek ALC200 (or Crystal CS4299) PQFP + Amp. TI TPA0202
- FIR Module : HP HSDL-3600#007 IR module

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- Thermal Sensor : AD1021 (or Genesys Logic GL528SM)
- Memory System : Two 144 pin SO-DIMM (PC100/PC133 64/128/256MB)
- Flash Memory (BIOS) : 28F020(2M bit)
- 56.6K FAX/MODEM RJ11 : 30 pin MDC board
- LAN RJ45 : VT8231(MAC) + LSI80227(PHY)
- Mini PCI : Wireless LAN/ Modem
- Other Function : Reserve Blue Tooth function

1.2.3 CPU

Intel Celeron Processor for the FC-PGA370 socket

- Available at 800/ 766/ 733/ 700/ 733/ 700/ 667/ 633/ 600/ 566 /533 /533/ 500/ 466/ 433/ 400/ 366/ 333 / 300 MHz core frequencies with 128KB level-two cache (on die). (300/ 266 MHz core frequencies without level-two cache).
- Intel's latest Celeron processors in the FC_PGA package are manufactured using the advanced 0.18 micron technology.
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Dynamic execution microarchitecture.
- Operates on a 66MHz, transaction-oriented system bus.
- Specifically designed for uni-processor based Value PC systems, with the capabilities of MMX technology.
- Power Management capabilities.
- Optimized for 32-bit applications running on advanced 32-bit operating systems.
- Integrated high performance 32KB instruction and data, nonblocking, level-one cache : separate 16KB instruction and 16KB data caches.
- Integrated thermal diode.

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Pentium Ⅲ Processor for the FC-PGA370 socket

- Available in 1.133G/ 1.0G/ 933/ 866/ 800EB/ 733/ 667,600EB/ 533EB MHz for 133 MHz system bus.
- Available in 850/ 800/ 750/ 700/ 650/ 600E/ 550E and 550E MHz for 100 MHz system bus.
- System bus frequency at 100 MHz and 133 MHz(“E” denotes support for Advanced Transfer Cache and Advanced system buffering ;”B” denotes support for a 133MHz System bus where both bus frequencies are available for order per each given core
- Available in versions that incorporate 256KB Advanced Transfer Cache(on-die, full speed Level 2(L2) cache with Error Correcting Code(ECC))
- Dual Independent Bus (DIB) architecture:
  Separate dedicated external System Bus and dedicated internal high-speed Cache bus.
- Internet Streaming SIMD Extensions for enhanced video ,sound and 3D performance
- Binary compatible with applications running on previous members of the Intel microprocessor line.
- Dynamic execution micro architecture.
- Intel Processor Serial Number.
- Power Management capabilities
- System Management mode
- Multiple low-power states.
- Optimized for 32-bit applications running on advanced 32-bit operating system.

7170 N/B MAINTENANCE

- Flip Chip pin Grid Array (FC-PGA) packaging technology ;FC-PGA processors deliver high performance with improved handling protection and socketability.
- Integrated high performance 16KB instruction and 16KB data, nonblocking, level one cache.
- 256 KB Integrated Full Speed level two cache allows for low latency on read/store operations.
- Double Quad Word Wide (256bit) cache data bus provides extremely high throughput on read/store operations.
- 8-way cache associativity provides improved cache hit rate on reads/store operations.
- Error-correcting code for Systen Bus data.
- Enables systems which are scaleable for up to two processor.

1.2.4 Core Logic Controller :

1.2.4.1 VIA Twister VT8603 (with Mobile VGA Savage4)

CPU Interface

- Socket 370 support for Intel Pentium III, Pentium II, and Celeron processors
- 66/100/133 MHz CPU FrontSide Bus (FSB)
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
- Dynamic deferred transaction support

Advanced High-Performance DRAM Controller

- DRAM interface runs synchronous (66/66, 100/100, 133/133) mode or pseudo-synchronous (66/100, 100/66, 100/133,133/100) mode with FSB
- Concurrent CPU, AGP, and PCI access
- Supports SDRAM and VCM SDRAM memory types
- Support 3 DIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
- 64-bit data width
- Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
- SDRAM X-1-1-1-1-1-1-1 back-to-back accesses

7170 N/B MAINTENANCE

🗁 **Integrated Savage4 2D/3D/Video Accelerator**

– Optimized Shared Memory Architecture (SMA)

– 8 to 32 MB frame buffer using system memory

– Floating point triangle setup engine

– Single cycle 128-bit 3D architecture

– 8M triangles/second setup engine

– 140M pixels/second trilinear fill rate

– Full internal AGP 4x performance

– S3 DX7 texture compression (S3TCÔ)

– Next generation, 128-bit 2D graphics engine

– High quality DVD video playback

– Flat panel monitor support

– 2D/3D resolutions up to 1920x1440

🗁 **3D Rendering Features**

– Single-pass multiple textures

– Anisotropic filtering

– 8-bit stencil buffer

– 32-bit true color rendering

– Specular lighting and diffuse shading

– Alpha blending modes

– Massive 2K x 2K textures

– MPEG-2 video textures

– Vertex and table fog

– 16 or 24-bit Z-buffering

– Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects

🗁 **2D Hardware Acceleration Features**

– ROP3 Ternary Raster Operation BitBLTs

– 8, 16, and 32 bpp mode acceleration

🗁 **Motion Video Architecture**

– High quality up/down scaler

– Planar to packed format conversion

– Motion compensation for full speed DVD playback

– Hardware subpicture blending and highlights

– Multiple video windows for video conferencing

– Contrast, hue, saturation, brightness and gamma controls

– Digital port for NTSC/PAL TV encoders

7170 N/B MAINTENANCE

🗁 **Extensive LCD Support**

– 36-bit DSTN/TFT flat panel interface with 256 gray shade support

– Integrated 2-channel 110 MHz LVDS interface

– Support for all resolutions up to 1280x1024

– ZV-Port Interface

– Panel power sequencing

– Hardware Suspend/Standby control

🗁 **Flat Panel Monitor Support**

– 12-bit TFT flat panel interface to TMDS encoders

– Digital Visual Interface (DVI) 1.0 compliant

🗁 **Concurrent PCI Bus Controller**

– PCI 2.2 compliant, 32-bit 3.3V PCI interface with 5V tolerant inputs

– Supports up to 5 PCI masters

– PCI to system memory data streaming support

– Delay transaction from PCI master accessing DRAM

– Symmetric arbitration between Host/PCI bus for optimized system performance

7170 N/B MAINTENANCE

- **Advanced System Power Management Support**
  - – Dynamic power down of SDRAM (CKE)
  - – Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - – PCI and AGP bus clock run and clock generator control
  - – VTT suspend power plane preserves memory data
  - – Suspend-to-DRAM and self-refresh power down
  - – Low-leakage I/O pads
  - – ACPI 1.0 and PCI Bus Power Management 1.1 compliant
- **Full Software Support**
  - – Drivers for major operating systems and APIs: [Windows 9x, Windows NT 4.0, Windows 2000, Direct3D, DirectDraw and DirectShow, OpenGL ICD for Windows 9x, NT, and 2000]
  - – North Bridge/Chipset and Video BIOS support
- **Additional Features**
  - – 250 MHz RAMDAC with Gamma Correction
  - – 12-bit interface to external TV encoder
  - – I 2 C Serial Bus and DDC Monitor Communications
  - – 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O
- **35 x 35mm PBGA package with 552 balls**

1.2.4.2 South Bridge VIA VT8231

- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - – Combine with VT82C694X for a complete 66 / 100 / 133 MHz Socket370 AGP 4x system (Apollo Pro133A)
  - – Combine with VT8601 for a complete 66 / 100 / 133 MHz Socket370 system with integrated 2D/3D graphics (Apollo ProMedia)
  - – Inter-operable with Intel or other Host-to-PCI bridges for a complete PC99 compliant PCI/AGP system
- **Integrated Peripheral Controllers**
  - – Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
  - – Integrated USB Controller with two root hub and four function ports
  - – Dual channel UltraDMA-33 / 66 master mode EIDE controller
  - – AC-link interface for AC-97 audio codec and modem codec
  - – HSP modem support
  - – Integrated SoundBlasterPro / DirectSound compatible digital audio controller
- **Integrated Legacy Functions**
  - – Integrated Keyboard Controller with PS2 mouse support
  - – Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - – Integrated Bus Controller including DMA, timer, and interrupt controller
  - – Serial IRQ for docking and non-docking applications

– Flash EPROM, 32Mbit (4Mbyte) EPROM and combined BIOS support

– Fast reset and Gate A20 operation

🗁 **Fast Ethernet Controller**

– High performance PCI master interface with scatter / gather and bursting capability

– Standard MII interface to Ethernet or HomePNA PHYceiver

– 1 / 10 / 100 MHz full and half duplex operation

– Transmit data buffer byte alignment for low CPU utilization

– Separate 2K byte FIFOs for receive and transmit of full Ethernet packets

– Flexible dynamically loadable EEPROM algorithm

– Physical, Broadcast, and Multicast address filtering using hashing function

– Flexible wakeup events: link status change, magic packet, unicast physical address match, predefined pattern match

– Software controllable power down

🗁 **UltraDMA-33 / 66 / 100 Master Mode PCI EIDE Controller**

– Dual channel master mode PCI supporting four Enhanced IDE devices

– Transfer rate up to 100MB/sec to cover up to PIO mode 4, multi-word DMA mode 2, and UltraDMA mode 5

– Thirty-two levels (doublewords) of prefetch and write buffers per channel

– Dual DMA engine for concurrent dual channel operation

– Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 / 98 / 2000 compliant

– Full scatter gather capability

– Support ATAPI compliant devices including DVD devices

– Support PCI native and ATA compatibility modes

– Complete software driver support

🗁 **Integrated Super IO Controller**

– Supports IR port, parallel port, and floppy disk controller functions

– Serial Port Programmable character lengths (5,6,7,8)
Even, odd, stick or no parity bit generation and detection
Programmable baud rate generator
Independent transmit/receiver FIFOs Modem Control
Plug and play with 96 base IO address and 12 IRQ options

– Fast IR (FIR) port
IrDA 1.0 SIR and IrDA 1.1 FIR compliant
IR function through the second serial port
Infrared-IrDA (HPSIR) and ASK (Amplitude Shift Keyed) IR

– Multi-mode parallel port
Standard mode, ECP and EPP support
Dynamic and static switch between parallel port pinout and FDC pinout
Plug and play with 192 base IO address, 12 IRQ and 4 DMA options

– Floppy Disk Controller
16 bytes of FIFO
Data rates up to 1Mbps
Perpendicular recording driver support
Two FDDs with drive swap support
Plug and play with 48 base IO address, 12 IRQ and 4 DMA options

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🗁 **SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller**

– Dual full-duplex Direct Sound channels between system memory and AC97 link

– PCI master interface with scatter / gather and bursting capability

– 32 byte FIFO of each direct sound channel

– Host based sample rate converter and mixer

– Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors

– Loopback capability for re-directing mixed audio streams into USB and 1394 speakers

– Hardware SoundBlaster Pro for Windows DOS box and real-mode DOS legacy compatibility

– Plug and play with 4 IRQ, 4 DMA, and 4 I/O space options for SoundBlaster Pro and MIDI hardware

– Hardware assisted FM synthesis for legacy compatibility

– Direct two game ports and one MIDI port interface

– Complete software driver support for Windows-95/98/2000 and Windows-NT

🗁 **MC97 HSP Modem Controller**

– PCI bus master interface with scatter / gather and burst capability

– Standard AC97 codec interface for MC or AMC codec

– Wake on ring in APM or ACPI mode through AC97 link

– Supported by most HSP modem vendors

7170 N/B MAINTENANCE

🗁 **Universal Serial Bus Controller**

– USB v.1.1 and Intel Universal HCI v.1.1 compatible

– Eighteen level (doublewords) data FIFO with full scatter and gather capability

– Root hub and four function ports

– Integrated physical layer transceivers with optional over-current detection status on USB inputs

– Legacy keyboard and PS/2 mouse support

🗁 **System Management Bus Interface**

– One master / slave SMBus and one slave-only SMBus

– Host interface for processor communications

– Slave interface for external SMBus masters

🗁 **Voltage, Temperature, Fan Speed Monitor and Controller**

– Five universal input channels for voltage or temperature sensing

– Two fan-speed monitoring channels

– Input channel for thermal diode in Intel™ high speed Pentium II™ / Pentium III™ CPUs

– Programmable control, status, monitor and alarm for flexible desktop management

– External thermister or internal bandgap temperature sensing

– Automatic clock throttling with integrated temperature sensing

– Internal core VCC voltage sensing

– Flexible external voltage sensing arrangement (any positive supply and battery)

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Sophisticated PC99-Compatible Mobile Power Management

– Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management

– ACPI v1.0 Compliant

– APM v1.2 Compliant

– CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support

– PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control

– Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up

– Multiple suspend power plane controls and suspend status indicators

– One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer

– Normal, doze, sleep, suspend and conserve modes

– Global and local device power control

– System event monitoring with two event classes

– Primary and secondary interrupt differentiation for individual channels

– Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up

– Multiple internal and external SMI sources for flexible power management models

– One programmable chip select and one microcontroller chip select

– Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field

– Thermal alarm on either external or any combination of three internal temperature sensing circuits

7170 N/B MAINTENANCE

– Hot docking support

– I/O pad leakage control

🗁 **Plug and Play Controller**

– PCI interrupts steerable to any interrupt channel

– Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, audio, soundblaster, MIDI

– Steerable DMA channels for integrated parallel, and soundblaster pro controllers

– One additional steerable interrupt channel for on-board plug and play devices

– Microsoft Windows 2000 TM , Windows ME TM ,Windows 98SE TM , Windows 98 TM , Windows NT TM , Windows 95 TM and plug and play
BIOS compliant

🗁 **Built-in NAND-tree pin scan test capability**

🗁 **0.30um, 3.3V, low power CMOS process**

🗁 **Single chip 27x27 mm, 376 pin BGA**

1.2.5 PCMCIA/1394 Link Controller: PCI4410

The PCI4410 supports the following features:

- A 209-ball MicroStar Ball Grid Array (GHK) package
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards
- Single PC Card or CardBus slot with hot insertion and removal
- Burst transfers to maximize data throughput on the PCI bus and the CardBus bus
- Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture allows greater than 130M bps sustained throughput from CardBus-to-PCI and fromPCI-to-CardBus
- Interface to parallel single-slot PC Card power interface switches like the TI TPS2211
- Up to five general-purpose I/Os
- Five PCI memory windows and two I/O windows available to the 16-bit PC Card socket
- Two I/O windows and two memory windows available to the CardBus socket
- Exchangeable Card Architecture (ExCA) compatible registers are mapped in memory and I/O space
- Intel 82365SL-DF and 82365SL register compatible
- Distributed DMA (DDMA) and PC/PCI DMA
- 6-Bit DMA on the PC Card socket

- PCI Bus Lock (LOCK)
- Advanced Submicron, Low-Power CMOS Technology
- Internal Ring Oscillator

1.2.6 LAN PHY: LSI80227

🗁**features:**

- Single Chip 100Base-TX / FX/10Base-T Physical Layer Solution
- 3.3V Version of SEEQ 80221
- Dual Speed - 10/100 Mbps
- Half And Full Duplex
- MII Interface To Ethernet Controller
- MI Interface For Configuration & Status
- Optional Repeater Interface
- AutoNegotiation: 10/100, Full/Half Duplex
- Meets All Applicable IEEE 802.3 Standards
- On Chip Wave Shaping - No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- Interface to External 100Base-T4 PHY
- LED Outputs: Link/Activity/ Collision/ Full Duplex/ 10/100/ User Programmable

- Many User Features And Options
- Few External Components
- 3.3V Supply with 5V Tolerant I/O
- 64L TQFP

1.2.7 Embedded Controller : Hitachi H8/3437S

CPU

- Two-way general register configuration
  Eight 16-bit registers or Sixteen 8-bit registers
- High-speed operation
  Maximum clock rate : 16Mhz at 5V

Memory

- Include 32KB ROM and 1KB RAM

16-bit free-running timer

- One 16-bit free-running counter
- Two output-compare lines
- Four input capture lines

8-bit timer (2 channels)

- Each channel has one 8-bit up-counter , two time constant registers

PWM timer (2 channels)

- Resolution :1/250
- Duty cycle can be set from 0 to 100%

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- **I^2C bus interface (one channel)**
  - Include single master mode and slave mode
- **Host interface (HIF)**
  - 8-bit host interface port
  - Three host interrupt requests (HIRQ1,11,12)
  - Regular and fast A20 gate output
- **Keyboard controller**
  - Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up interrupts
  - And sense ports
- **A/D converter**
  - 10-bit resolution
  - 8 channels : single or scan mode (selectable)
- **D/A converter**
  - 8-bit resolution
  - 2 channels
- **Interrupts**
  - Nine external interrupt lines : NMI# , IRQ0 to 7#
  - 26 on-chip interrupt sources
- **Power-down modes**
  - Sleep mode
  - Software standby mode
  - Hardware standby mode

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- **A single chip microcomputer**
- **On-chip flash memory**
- **Maximum 64-kbyte address space**
- **Support three PS/2 port for external keyboard ,mouse and internal track pad.**
- **Support SMI,SCI trigger input:**
- **Cover switch**
- **Battery charging control**
- **Smart Battery monitoring**
- **Control D/D system on/off**
- **Fan control and LED indicator serial interface**
- **100pin TQFP**

1.2.8 Audio System

1.2.8.1 AC97 CODEC : ALC200 (or CS4299) -PQFP

- **AC '97 2.1 Compatible**
- **Industry Leading Mixed Signal Technology**
- **20-bit Stereo Digital-to-Analog Converter and 18-bit Ste-reo Analog to Digital Converter with Sample Rate Conversion**
- **Four Analog Line-level Stereo Inputs for Connection from LINE IN, CD, VIDEO, and AUX**
- **Two Analog Line-level Mono Inputs for Modem Sub-system and Internal PC Beeper**
- **Mono Microphone Input Switchable from Two External Sources**
- **High Quality Differential CD Input**
- **Dual Stereo Line-level Outputs**
- **Extensive Power Management Support**
- **Meets or Exceeds Microsoft's ® PC 98 and PC 99 Audio Performance Requirements**
- **3D Stereo Enhancement**
- **Sample Rate Converters**

7170 N/B MAINTENANCE

🗁 **combined with driver software and an AC'97 CODEC provides a complete high quality audio solution,**

Feature Include:

- MPU-401 interface
- FM synthesizer
- Game Port (disable in 7170 NB system)
- MIDI port. (disable in 7170 NB system)
- MODEM
- CD-ROM
- User-Defined GPIO
- Volume Control: Rotary VR
- Stereo BTL 2x1 W Amplifiers(TPA0202) With 8 Ohm Load.
- 16 Bit Stereo ADC & DAC For Record And Play Back
- Programmable Sample Rates From 4kHz To 44.1kHz For Record And Playback
- Microphone in * 1 (3.5 mm phone-jack)
- Headphone out * 1: stereo (3.5mm phone-jack) (disable in 7170 NB system)
- Built-in Speaker * 2 (1w, 8 ohm)
- Built-in Microphone * 1

1.2.9 IR Module : HSDL-3600#007

- **Fully Compliant to IrDA 1.1 Specifications**
  - 115.2 kb/s to 4 Mb/s operation
  - excellent nose-to-nose operation
- **Compatible with ASK, HP-SIR**
- **IEC825-Class 1 Eye Safe**
- **Wide Operating Voltage Range**
  - 2.7 V to 5.25 V
- **Small Module Size**
  - 4.0 x 12.2 x 5.1 mm (HxWxD)
- **Complete Shutdown**
  - TXD, RXD, PIN diode
- **Low Shutdown Current**
  - 10 nA typical
- **Adjustable Optical Power Management**
  - Adjustable LED drive-current to maintain link integrity
- **Single Rx Data Output**
  - FIR Select pin switch to FIR
- **Integrated EMI Shield**
  - Excellent noise immunity
- **Edge Detection Input**
  - Prevents the LED from long turn-on time
- **Interface to various Super I/O and Controller Devices**
- **Designed to Accommodate Light Loss with Cosmetic Window**

1.2.10 Memory System

1.2.12.2 Main memory

SO-DIMM

- Two SO-DIMM sockets on Mother Board for expansion
- Supports JEDEC specification : 144 SO-DIMM socket
- Supports 3.3V PC100/PC133 SDRAM DIMM
- 2 banks on each socket

The memory subsystem supports two 3.3V 144-pin SO-DIMM sockets for totally up to 512MB of Main memory. Here are some main memory system essential characteristics:

144-pin SO DIMM socket	2
Memory Voltage	3.3V ± 10%
Memory Module Type	64MB/128MB/256MB
Banks on DIMM	4
Bank Ordering	Auto ordering by BIOS
Memory type selection	Auto-detect by BIOS
Mixed type DRAM support	Yes

1.2.11 Mass Storage Sub-system

7170NB system is an two spindles NB. There are one removable 2.5" hard disk drive and 24X CD-ROM or DVD or CDRW installed in it. This IDE interface is compliant with ATA specification and UltraDMA 33/66MB.

1.2.12 I/O Interface

- One standard parallel port with Output only/Bi-direction/ECP/EPP functions
- One serial ports, for FIR/MIR/SIR/SHARP ASK
  COM port assignment COM2: IR / RS-232 / Disable
- One external CRT connector for CRT display
- One PS/2 interface for external KB, mouse or other PS2 devices
- One CARDBUS sockets support type II.
- Two USB V1.1 connector
- One DC Jack for Adapt in
- One MODEM RJ-11 phone jack for PSTN line and one RJ-45 for 10/100 base LAN.
- Dual stereo line level speaker outputs
- Microphone input and one internal microphone.
- Tunable volume by variable resistor
- One Mini-PCI socket support Type IIIA.

1.2.13 Special Feature Function2

1.2.13.1. Hot Key Function

Keys Combination	Feature	Meaning
Fn + F5	Display switch	Rotate display mode in LCD only, CRT only and simultaneously display and TV output.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increase the LCD brightness
Fn + F8	Contrast down	Decrease the LCD contrast
Fn + F9	Contrast up	Increase the LCD contrast
Fn + F10	Enable/Disable battery warming beep	Toggle battery low beep warming on/off
Fn + F11	Panel on/off	Toggle Display (panel , CRT,TV) On/Off
Fn + F12	Suspend to Dram/HDD	Force the computer into either suspend to HDD or suspend to DRAM mode depending on BIOS setup

1.2.13.2. Flash ROM (BIOS)

7170 NB system utilizes the state-of-the-art Flash EEPROM technology. User can upgrade the system BIOS in the future just running the program from MiTAC.

1.2.13.3. LED Indicators

System has nine status LED indicators to display system activity which include below LCD panel unit and above keyboard:

1. Three LED indicators below LCD panel unit:
   From left to right that indicate AC POWER, BATTERY POWER and BATTERY STATUS

- **AC POWER**: This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.
- **BATTERY POWER**: This LED lights green when the notebook is being powered by batteries, and flashes (on 1 second, off 1 second) when Suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.
- **BATTERY STATUS** : During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.
- **Five LED indicators in front of palm rest:**
  From left to right that indicates **CD-ROM/MO, HARD DISK DRIVE, , NUM LOCK, CAPS LOCK and SCROLL LOCK.**
- **Email/ Blue-Tooth LED indicators in front of palm rest:**
  The left side green LED flashing means new mail coming. Otherwise the LED is always OFF. The right side red LED ON means Blue-Tooth module turn ON.

1.3 System Power Management

1.3.1 System Management Mode

7170NB system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the SMM and power management modes supported.

1.3.1.1. Full-On Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

1.3.1.2. Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology will be clock throttling. This can save battery power without loosing much computing capability.
The CPU power consumption and temperature is lowered in this mode.

1.3.1.3. Standby Mode

For more power saving, it turns of f the peripheral component. In this mode, the following is the status of each device.

- CPU : stop grant
- VGA: software suspend
- LCD : backlight off
- HDD: spin down
- FDD : standby
- FDD : standby

1.3.1.4. Suspend Mode

The most chipsets of the system is entering power down mode for more power saving.

Suspend to RAM :

CPU: off

N.B: off

S.B: partial off

VGA: Suspend

PCMCIA: Standby

Audio: off

Suspend to HDD :

All devices are stopped clock and power-off, only EC is lived if battery or ac still plug in .At this time , system status is saved in HDD. All system status will be restored when toggle power button system powered on again.

1.3.1.5. Other Power Management Functions

1.3.1.5.1. HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. **When the VGA activity monitoring is enabled, the performance of the system will have some impact.**

1.3.1.5.2. Cover Switch

System automatically provides power saving on monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover . There are three functions to be chosen.

1.3.2 Other Power Management Functions

1.3.2.1. HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. **When the VGA activity monitoring is enabled, the performance of the system will have some impact.**

1.3.2.2. Cover Switch

System automatically provides power saving on monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover . There are three functions to be chosen.

1. Switch to CRT
2. Panel Off
3. Suspend --- Depend on BIOS setting (STR or STD)

1.3.2.3. Battery Warning

System also provides battery capacity monitoring and gives user a warning so that users have chance to save their data before battery dead. Also , this function protects system from mal-function while battery capacity is low.

1.3.2.4. Battery Warning State

7170 NB system provides battery management function and gives warning while battery is in It's low power state. When the battery capacity is below 9% (Battery Warning State), system will generate beep for every 4 seconds (System beeps only if BIOS setup enable Battery Warning Beeping). When hearing the beeping, it is recommended that user should plug in AC adapter to get power from external source, or stop working and save his data file to prevent disastrous results.

1.3.2.5. Battery Dead State

When the battery voltage level reach 11 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.3. Fan Power on/off Management

The fan is always on except suspend power off to cool the CPU temperature down.

1.4 Firmware - System BIOS & Keyboard BIOS

7170NB use Phoenix BIOS as the system firmware and keyboard firmware .For further detail information regarding the firmware , please refer to 7170NB software document.
(refer software engineer spec)

1.4.1 SYSTEM RESOURCE

1.4.1.1 PCI INT MAP

INT	DEVICE
INTA	CARDBUS
INTB	(VGA in North Bridge)
INTC	MINI PCI
INTD	USB/ MINI PCI(REV) 1394/ LAN

1.4.1.2 PCI BUS MASTER REQUEST

REQ	DEVICE
REQ0	CARDBUS
REQ1	No Used
REQ2	VGA (in North Bridge)
REQ3	MINI PCI
REQ4	LAN

1.4.1.3 IDSEL

AD BUS	DEVICE
AD11	VGA (in North Bridge)
AD17	MINI PCI
AD21	CARDBUS
AD28	South Bridge
AD29	LAN

1.5 Peripheral Component

1.5.1 LCD

UNIPAC UB133X01-2 TFT XGA

- pixels : 1024(H) By 768(V)
- screen size : 13.3inch
- colors : 262k(3x6 bit)
- interface : LVDS single cannel
- lump : CCFL
- D/C for panel : 3.3V
- Power Consumption : 3.66W(typ)
- Weight : 500g (typ)
- Lamp starting voltage : 925 Vrms (typ)

1.5.2 Internal Keyboard

IBM 106 key compatible keyboard layout

Key pitch : 19mm

Length : 300mm

Thickness : 5.3mm

Keycap pull off force : >= 800g

MAX. keytop depressing force :

~To withstand 5 Kgf at the center of keytop for 1 minute.

Keytop Strength :

~To withstand 1Kgf at X and Y directions for 5 sec.

Power Requirement :

~The keyswitch shall require DC 6V at 0.3 mA maximum.

Contact Resistance :

~ The contact resistance is 500 ohm maximum at 200g force.

Operating Temperature : -10 to 60 degree C

High Temperature Storage : 65 degree C.

Window95 applied

1.5.3 Floppy Disk Drive

- Please use external USB Floppy Disk Device.

1.5.4 Touch Pad

Synaptics (4 buttons):

- Model TM41P-350
- Vcc : 5V +- 0.5
- Icc(max) : 4 mA
- Interface : PS/2
- X/Y position resolution : 1000 points/inch
- Dimension : 65mm x 49mm x 4.6mm

- Effective area : 60mm x 44 mm
- Operating Temp. : 0 - 60 degree C
- Storage Humidity : 5 - 95 %,
- Storage Temp. : -40 - + 65 degree C
- ESD : 15KV applied to front surface

1.5.5 CD-ROM or DVD-ROM or CD-RW Drive

- Disk speed: X24/higher speed CD-ROM or X8 speed DVD-ROM or CD-RW.
- Host interface: IDE/ATAPI
- Ejection: Manual eject using the eject button/Automatically eject using the tray

1.5.6 HDD

- Support Ultra DMA
- 2.5” , 8.45/9.5 mm height
- Formatted Storage Capacity 10/20 GB

1.5.7 LED Indicators

Upper LEDs on D/D board

- AC. POWER, BATTERY POWER, CHARGER STATUS,

Lower LEDs on M/B board

- HARD DISK DRIVE, CD-ROM, NUM LOCK, CAPS LOCK, SCROLL LOCK and Emial/Blue-tooth status..

1.5.8 IR port

- HSDL-3600#007 IR Module
- Meet IrDA Physical Layer Specification
- 1 cm to 1 Meter Operating Distance
- 30 degree Viewing Angle (± 15 degree)
- Support Two Channels - 2.4 Kb/s to 115.2Kb/s and 1.15Mb/s to 4.0 Mb/s

1.5.9 CMOS Battery

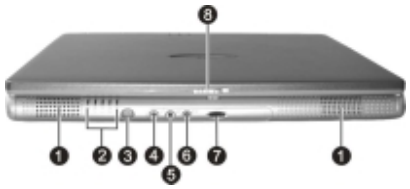
- VARTA CR2032 non-chargeable lithium battery
- Put in battery holder, can be replaced
- Nominal voltage : 3V
- Nominal capacity : 65mAh
- Recommended continuous Drain : 0.2 mA
- Recommended Pulse Drain : 12 mA
- Weight : 3.2 g

2. System Assembly & Disassembly

2.1 System View

2.1.1 Front View

❶ Stereo Speaker Set
❷ Device Indicators
❸ Mail-Received Button/Indicator
❹ Microphone Connector
❺ Audio Input Connector
❻ Audio Output Connector
❼ Volume Control
❽ Top Cover Latch



2.1.2 Left-Side View

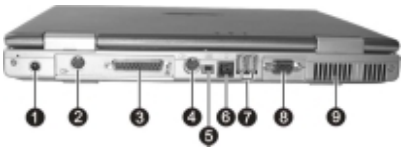
❶ Kensington Lock
❷ Ventilation Openings
❸ RJ-45 Connector
❹ PC Card Slot
❺ Hard Disk Drive

2. System Assembly & Disassembly

2.1.3 Right-Side View

❶ Battery Pack
❷ CD-ROM/DVD-ROM Drive
❸ IR Port

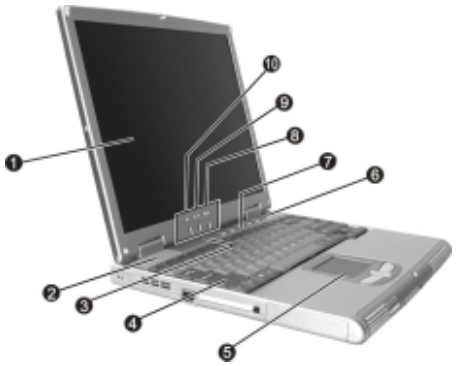
2.1.4 Rear View



❶ Power Connector
❷ S-Video Output Connector
❸ Parallel Port
❹ PS/2 Port
❺ IEEE 1394 Port
❻ RJ-11 Connector
❼ USB Ports
❽ VGA Port
❾ Ventilation Openings

2. System Assembly & Disassembly

2.1.5 Top-Open View



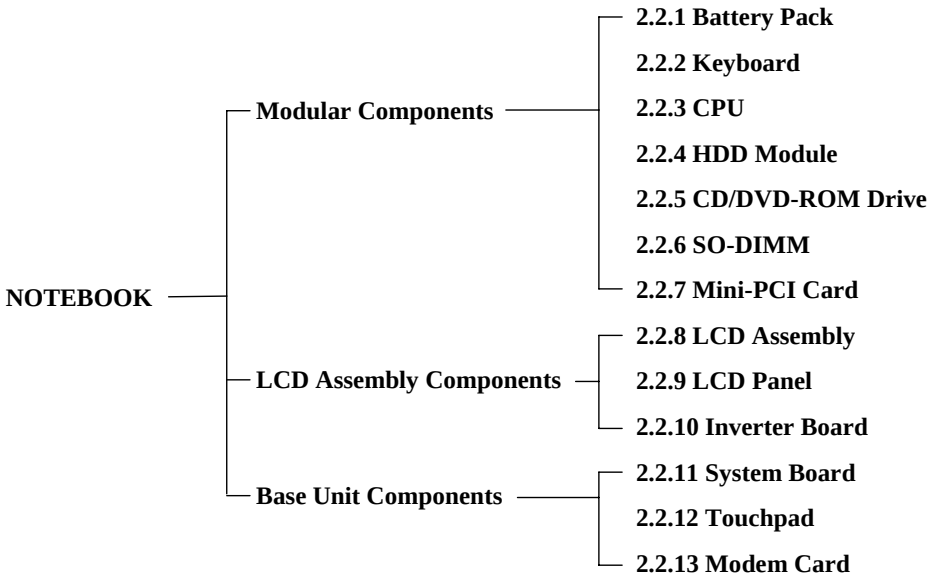
❶ LCD Screen
❷ Ventilation Openings
❸ Microphone
❹ Keyboard
❺ Touchpad
❻ Power Button
❼ Easy Start Buttons
❽ Battery Charge Indicator
❾ Battery Power Indicator
❿ AC Power Indicator

2. System Assembly & Disassembly

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



7170 N/B MAINTENANCE

2. System Assembly & Disassembly

2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the release lever to the “unlock” (🔓) position (❶), then slide and hold the release lever outwards and pull the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” (🔒) position.

2. System Assembly & Disassembly

2.2.2 Keyboard

Disassembly

1. Open the top cover. Install a small rod, such as a straightened paper clip, into the eject hole near the power connector of the notebook. (Figure 2-2)

Figure 2-2

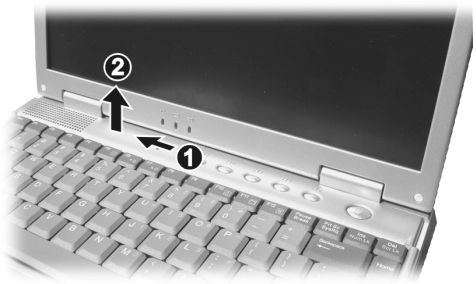


Figure 2-3

2. Push the rod firmly and slide the LED panel to the left (❶). Then lift the LED panel up from the left side (❷). (Figure 2-3)

2. System Assembly & Disassembly

3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-4)

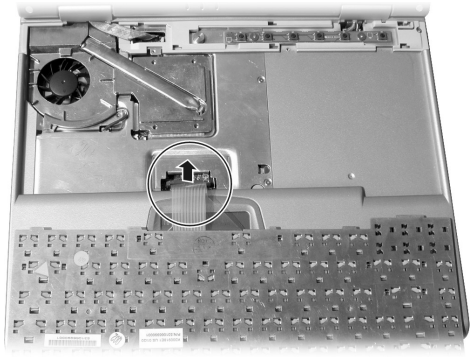


Figure 2-4

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the LED panel.

2. System Assembly & Disassembly

2.2.3 CPU

Disassembly

1. Remove the LED panel and keyboard to access the CPU compartment. (See section 2.2.2 Disassembly.)
2. Remove four screws fastening the heatsink and disconnect the fan's power cord to free the heatsink from the CPU module. (Figure 2-5)

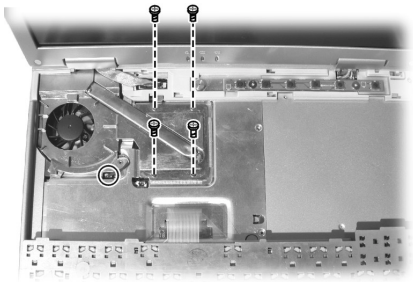


Figure 2-5

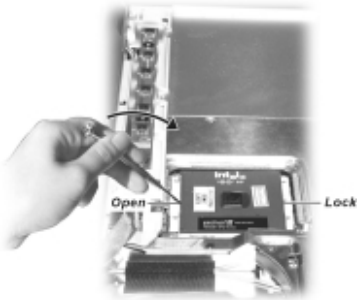


Figure 2-6

3. Insert a minus screwdriver 101 (JIS standard) into the "OPEN" hole of the socket, and push the screwdriver toward the CPU to free the CPU. Now you can take out the CPU from the socket. (Figure 2-6)

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket, and insert the CPU pins into the holes. Insert the flat screwdriver into the "CLOSE" hole of the socket, and push the screwdriver toward the CPU to secure the CPU in place.
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the keyboard and LED panel.

2. System Assembly & Disassembly

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the HDD module out of the compartment. (Figure 2-7)

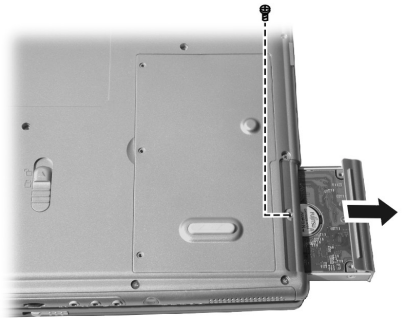


Figure 2-7

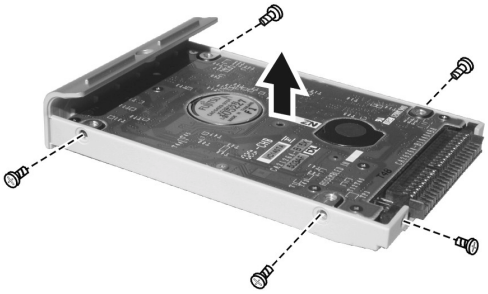


Figure 2-8

3. Remove five screws to separate the hard disk drive from the metal shield. (Figure 2-8)

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with five screws.
2. Slide the HDD module into the compartment and secure with one screw.

2. System Assembly & Disassembly

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Remove the LED panel and keyboard. (See section 2.2.2 Disassembly.)
2. Remove two screws locking the CD/DVD-ROM drive. (Figure 2-9)

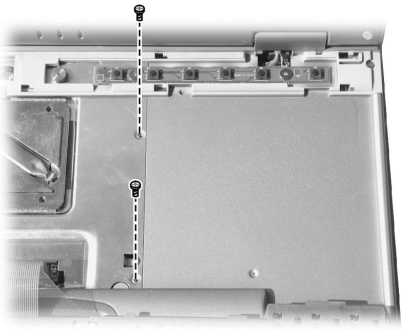


Figure 2-9

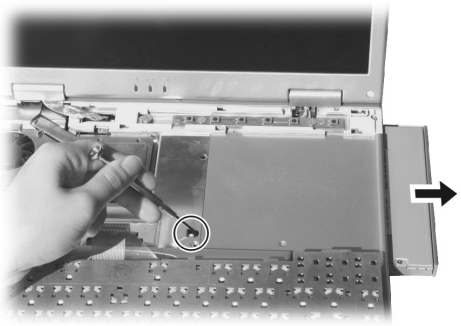


Figure 2-10

3. Use the screwdriver to push the metal pad to the right and the CD/DVD-ROM drive will pop out. Hold the CD/DVD-ROM drive and slide it outwards carefully. (Figure 2-10)

Reassembly

1. Push the CD/DVD-ROM drive into the compartment.
2. Secure the CD/DVD-ROM drive with two screws.
3. Replace the keyboard and LED panel.

2. System Assembly & Disassembly

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down.
2. Remove three screws to access the SO-DIMM socket.
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-11)

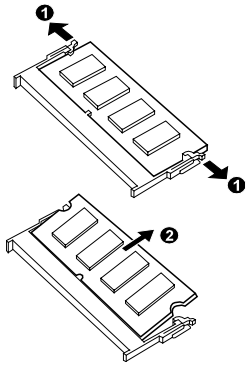


Figure 2-11

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace three screws to lock the SO-DIMM socket cover.

2. System Assembly & Disassembly

2.2.7 Mini PCI Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove three screws to access the Mini PCI socket.
3. Pull the retaining clips outwards and remove the Mini PCI card. (Figure 2-12)

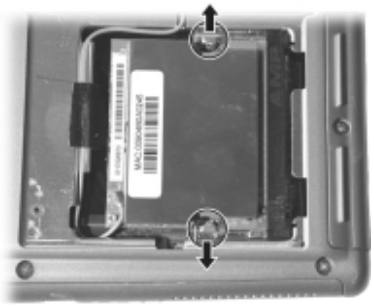


Figure 2-12

Reassembly

1. To install the Mini PCI card, match the notched part of the Mini PCI card with the socket's projected part and firmly insert the Mini PCI card into the socket at 20-degree angle. Then push down until the retaining clips lock the Mini PCI card into position.
2. Replace three screws to lock the SO-DIMM socket cover.

2. System Assembly & Disassembly

2.2.8 LCD Assembly

Disassembly

1. Carefully put the notebook upside down and remove three screws to access the Mini PCI socket.
2. Disconnect the antenna from the connector on the Mini PCI socket. (Figure 2-13)

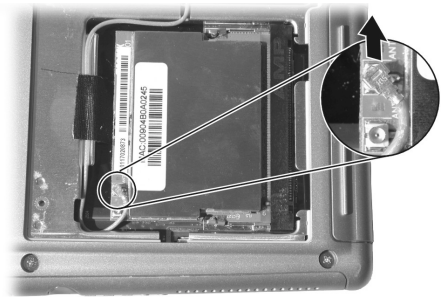


Figure 2-13

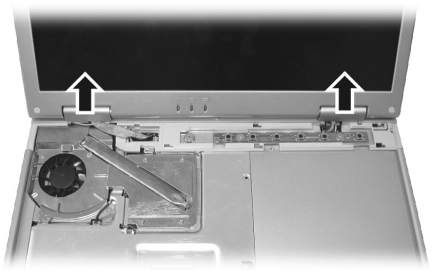


Figure 2-14

3. Open the top cover. Remove the LED panel, keyboard, and heatsink . (See section 2.2.2 and 2.2.3 Disassembly.)
4. Pull out the antenna from the CPU compartment.
5. Remove the two hinge covers. (Figure 2-14)

2. System Assembly & Disassembly

6. Disconnect the LCD cable from the system board, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (Figure 2-15)

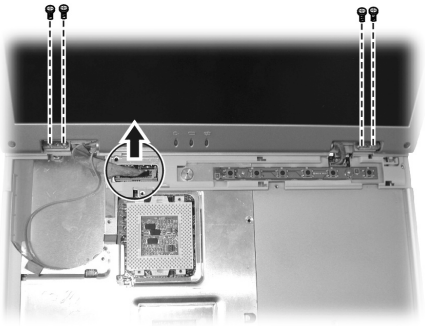


Figure 2-15

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the antenna to the connector on the Mini PCI socket.
3. Reconnect the LCD cable to the system board.
4. Replace the heatsink, keyboard and LED panel.two hinge covers.
5. Replace two hinge covers.

2. System Assembly & Disassembly

2.2.9 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
2. Remove the four rubber pads and four screws on the corners of the panel. (Figure 2-16)

Figure 2-16

Figure 2-17

3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.
4. Remove the two screws on two sides and two screws on the lower part of of the LCD panel, and disconnect the cable from the inverter board. (Figure 2-17)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the four screws and four rubber pads.
3. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2. System Assembly & Disassembly

2.2.10 Inverter Board

Disassembly

1. Remove the LCD assembly and detach the LCD frame (see instructions in previous two sections).
2. To remove the inverter board on the bottom of the LCD assembly, disconnect the cable and remove one screw. (Figure 2-18)

Figure 2-18

Reassembly

1. Fit the inverter board back into place and secure with one screw.
2. Reconnect the cable.
3. Replace the LCD frame. (See section 2.2.9 Reassembly.)
4. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2. System Assembly & Disassembly

2.2.11 System Board

Disassembly

1. Remove the battery pack, LED panel, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See the Disassembly parts in previous sections.)
2. Remove thirteen screws on the bottom of the notebook. (Figure 2-19)

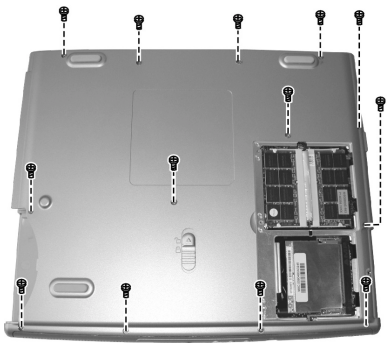


Figure 2-19

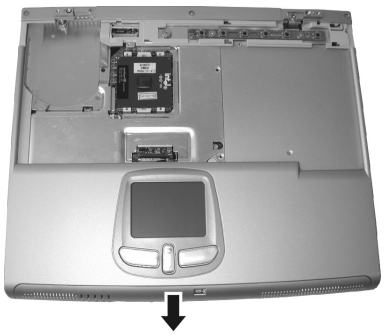


Figure 2-20

3. Remove the speaker assembly from the notebook. (Figure 2-20)

2. System Assembly & Disassembly

4. Remove two screws on the rear side of the notebook. Then remove three screws fastening the base unit cover and one screw in the CPU compartment. (Figure 2-21)

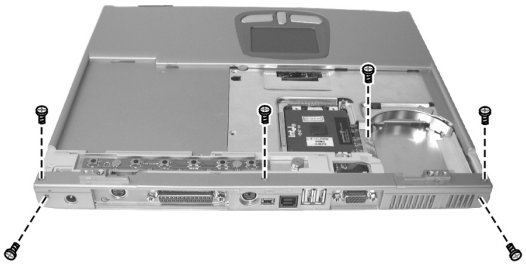


Figure 2-21

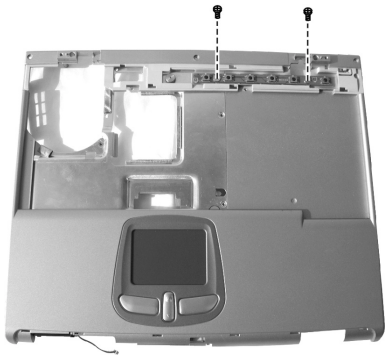


Figure 2-22

5. Remove two screws fastening the LED board. (Figure 2-22)

2. System Assembly & Disassembly

6. Lift up the base unit cover and disconnect the touchpad cable. (Figure 2-23)

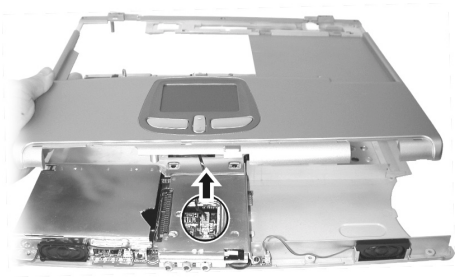


Figure 2-23

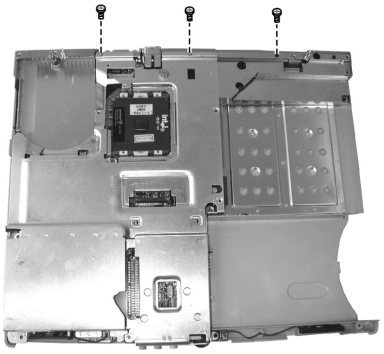


Figure 2-24

7. Remove three screws from the base. (Figure 2-24)

2. System Assembly & Disassembly

8. Disconnect two cables from the system board and lift up the base unit to access the system board. (Figure 2-25)

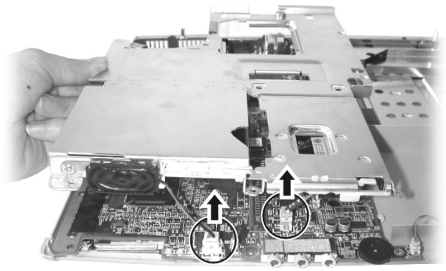


Figure 2-25

Reassembly

1. Reconnect two cables to the system board.
2. Replace three screws fastening the base unit.
3. Reconnect the touchpad cable and replace the base unit cover.
4. Replace two screws fastening the LED board.
5. Replace one screw in the CPU compartment and three screws fastening the base unit cover.
5. Replace two screws on the rear side of the notebook.
6. Replace the speaker assembly.
7. Replace thirteen screws on the bottom of the notebook.
8. Replace the battery pack, LED panel, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly.

2. System Assembly & Disassembly

2.2.12 Touchpad

Disassembly

1. Remove the base unit cover. (See steps 1-6 in section 2.2.11 Disassembly.)
2. Remove the six screws to lift up the touchpad holder and touchpad panel. (Figure 2-26)

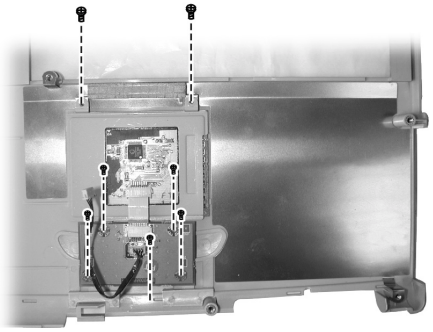


Figure 2-26

Reassembly

1. Replace the touchpad holder and touchpad panel, and secure with six screws.
2. Assemble the notebook. (See section 2.2.11 Reassembly.)

2. System Assembly & Disassembly

2.2.13 Modem Card

Disassembly

1. Disassemble the notebook to access the system board. (See section 2.2.11 Disassembly.)
2. Remove the two screws fastening the modem card. (Figure 2-27)

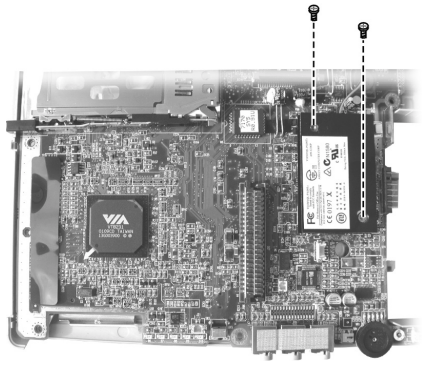


Figure 2-27

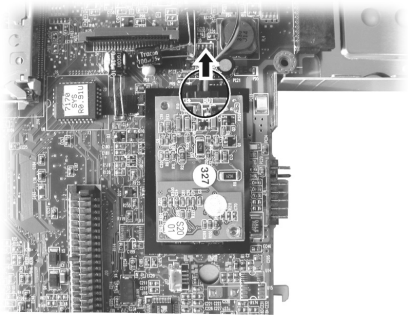


Figure 2-28

3. Disconnect the cable from the modem card. (Figure 2-28)

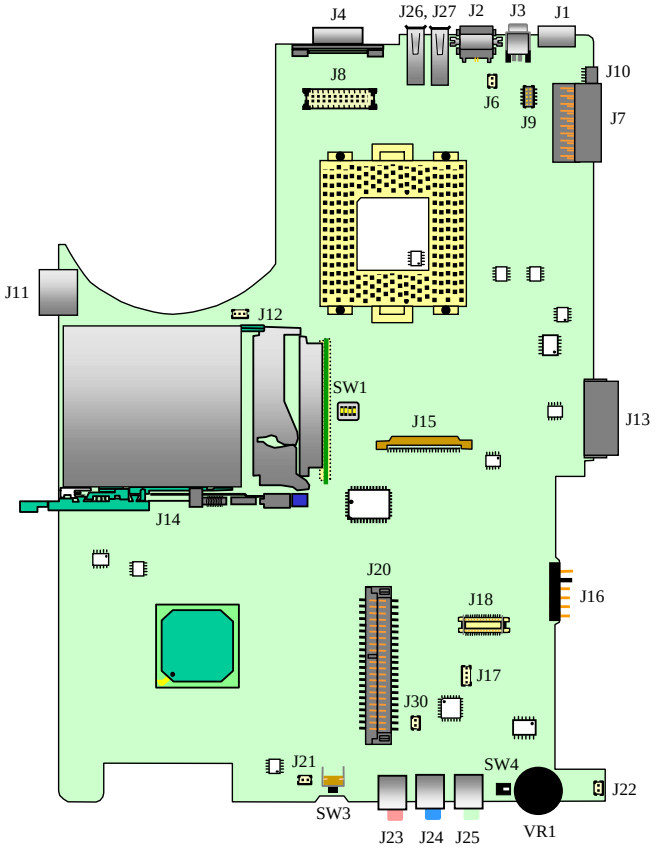
Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See section 2.2.11 Reassembly.)

7170 N/B MAINTENANCE

3. Definition & Location Connectors / Switches Setting

3.1 7170 Main Board (Side A-1)

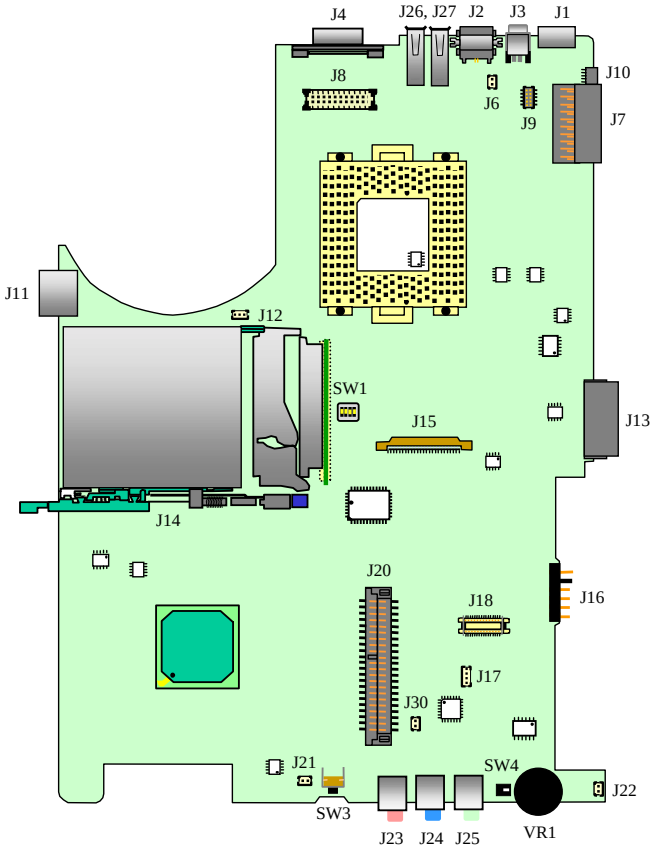


- **J1 : PS2 Connector. (SH17)**
- **J2 : RJ11 Phone Jack. (SH18)**
- **J3 : IEEE 1394 Connector. (SH14)**
- **J4 : External VGA Connector. (SH9)**
- **J6 : Modem Daughter Board To RJ11 Connector. (SH18)**
- **J7 : Main Board To DC Power Board Connector. (SH22)**
- **J8 : LCD Panel Module Connector. (SH9)**
- **J9 : Easy Start Button Connector. (SH17)**
- **J10 : Main Board To DC Power Board Connector. (SH22)**
- **J11 : RJ45 LAN Connector. (SH18)**
- **J12 : CPU FAN Connector. (SH17)**
- **J13 : CD-ROM Device Connector. (SH12)**
- **J14 : PCMCIA Card Bus Connector. (SH14)**
- **J15 : Internal Keyboard Connector. (SH17)**

7170 N/B MAINTENANCE

3. Definition & Location Connectors / Switches Setting

3.1 7170 Main Board (Side A-2)

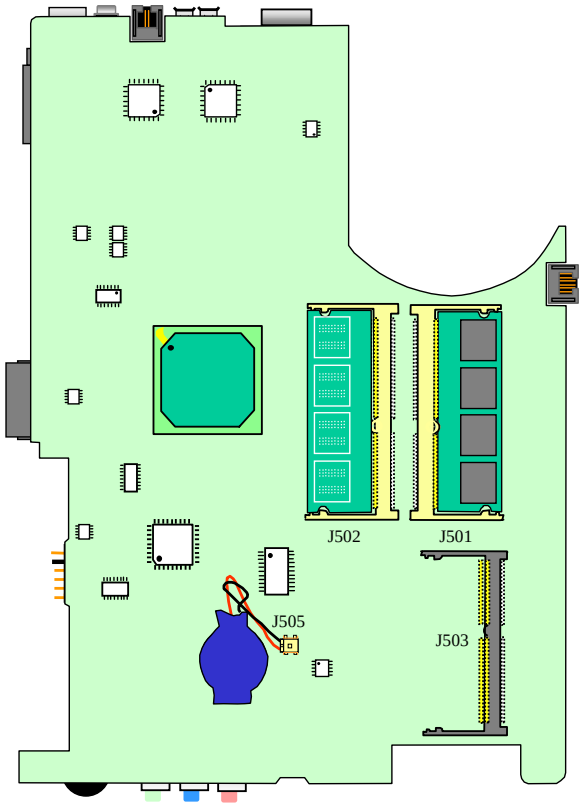


- **J16 : Battery Connector. (SH21)**
- **J17 : Touch Pad Connector. (SH15)**
- **J18 : Modem Daughter Board AC-Link Connector. (SH18)**
- **J20 : Hard Disk Connector. (SH12)**
- **J21,J22 : L,R Internal Speaker Connector. (SH13)**
- **J23 : External Micro Phone Jack. (SH13)**
- **J24 : Line In. (SH13)**
- **J25 : Line Out Phone Jack. (SH13)**
- **J26,J27 : USB Port Connector. (SH15)**
- **J30 : Internal Micro Phone Jack. (SH13)**
- **VR1 : Volume Control. (SH13)**
- **SW1 : Panel Type Select. (SH6)**
- **SW3 : E-Mail Button. (SH17)**
- **SW4 : Cover Switch. (SH17)**

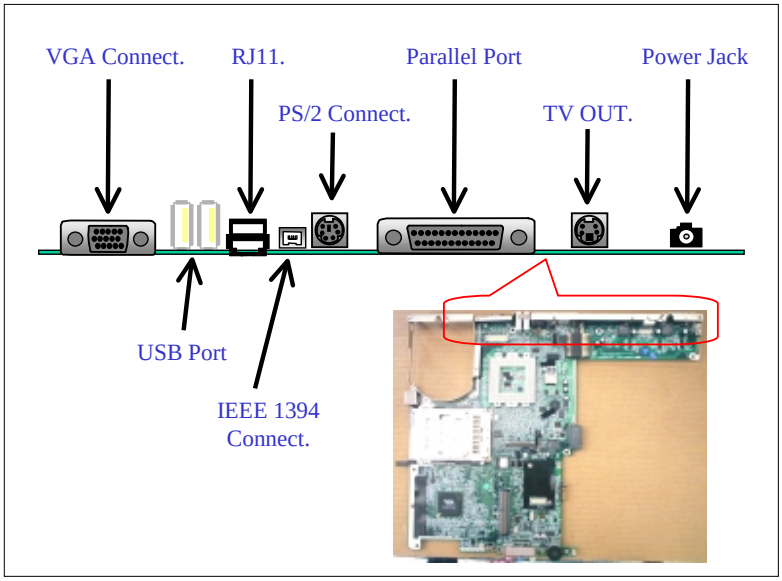
7170 N/B MAINTENANCE

3. Definition & Location Connectors / Switches Setting

3.1 7170 Main Board (Side B)



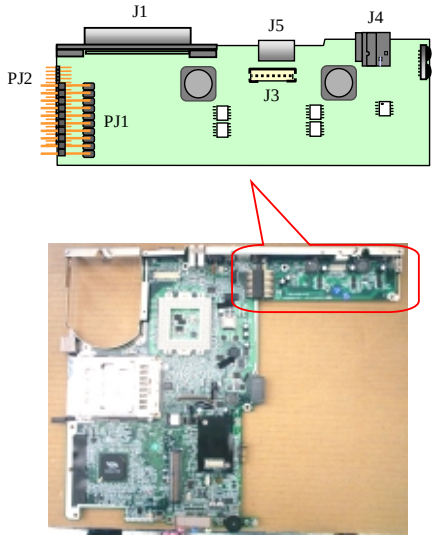
- **J501 : 144 Pin SO-DIMM Extension Memory Socket. (SH8)**
- **J502 : 144 Pin SO-DIMM Extension Memory Socket. (SH8)**
- **J503 : QTC Connector. (SH19)**
- **J505 : RTC Battery Connector. (SH12)**



7170 N/B MAINTENANCE

3. Definition & Location Connectors / Switches Setting

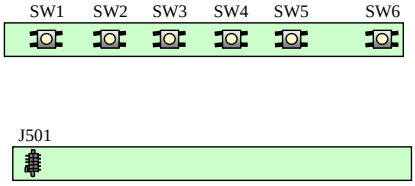
3.2 7170 DC Power Board (Side A)



- **J1 : Parallel Port Connector. (SH3)**
- **J3 : Inverter Board Connector. (SH2)**
- **J4 : Power Jack Board Connector. (SH2)**
- **J5 : TV Out Connector. (SH3)**
- **PJ1 : DC Power Board To Main Board Connector. (SH2)**
- **PJ2 : DC Power Board To Main Board Connector. (SH2)**

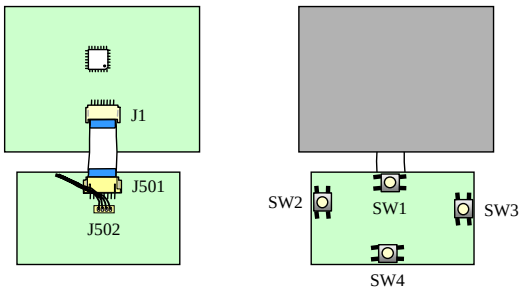
3. Definition & Location Connectors / Switches Setting

3.3 7170 ESB Board (Side A,B)



- J501 : Easy Start Button Connector.
- SW1 : Programmable Easy Start Button Switch.
- SW2 : Programmable Easy Start Button Switch.
- SW3 : Programmable Easy Start Button Switch.
- SW4 : Programmable Easy Start Button Switch.
- SW5 : Programmable Easy Start Button Switch.
- SW6 : Programmable Easy Start Button Power Switch.

3.4 7170 Touch Pad Board (Side A,B)

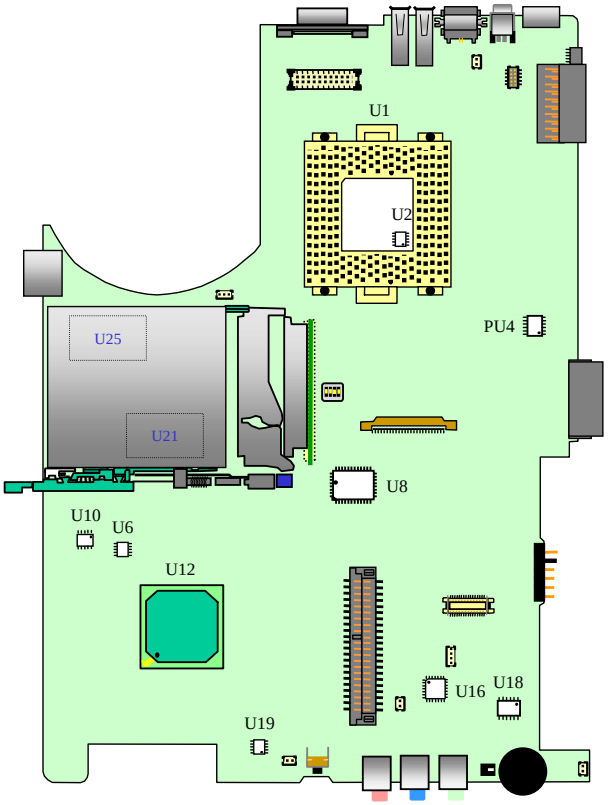


- J501 : Touch Pad Board To Touch Pad Connector.
- J502 : Touch Pad Board To Main Board Connector.
- SW1 : Scroll Up Button Switch.
- SW2 : Left Button Switch.
- SW3 : Right Button Switch.
- SW4 : Scroll Down Button Switch.

7170 N/B MAINTENANCE

4. Definition & Location Major Components

4.1 7170 Main Board (Side A)

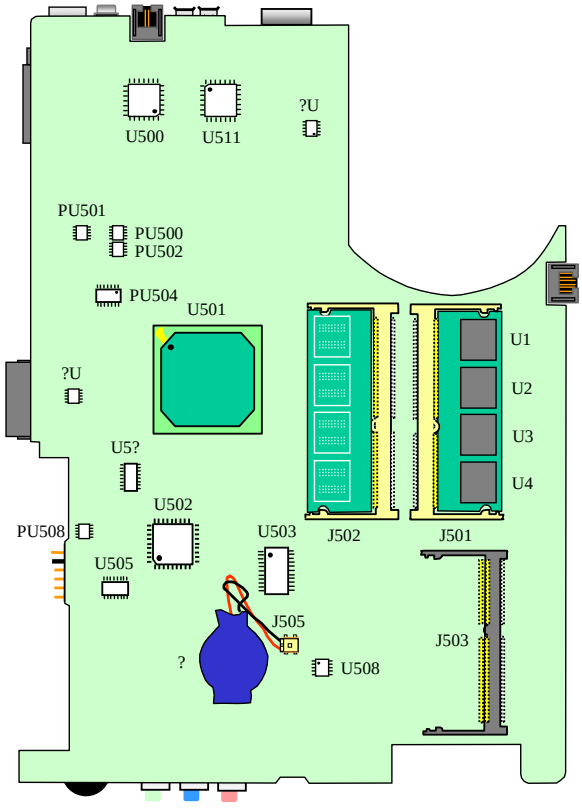


- U1 : PIII/Celeron FC-PGA 370-Pin Socket. (SH4)
- U2 : GL528SM Thermal Recorder. (SH4)
- U6 : 93C468 Serial EEPROM. (SH11)
- U8 : 28F020-PLCC Flash ROM BIOS. (SH15)
- U10 : NM24C02N. (SH14)
- U12 : VT8231 South Bridge. (SH10)
- U16 : ALC200 Audio Codec. (SH13)
- U18 : TPA0202 Audio Amplifier. (SH13)
- U19 : 74VHV164. (SH9)
- U21 : PCI 4410GHK PCMCIA Card Bus Controller. (SH14)
- U25 : LSI 80227. (SH18)
- PU4 : SC 1401CSS. (SH20)

7170 N/B MAINTENANCE

4. Definition & Location Major Components

4.1 7170 Main Board (Side B)



- **U500 : TSB 41AB1 1394 PHY. (SH14)**
- **U501 : TWINSTER North Bridge. (SH6)**
- **U502 : H8/34347 Micro Controller. (SH17)**
- **U503 : ICS9248-195 Clock Generator. (SH16)**
- **U505 : SN74CBTD3384 Level Shift. (SH17)**
- **U511 : CH7005C TV Encoder. (SH9)**
- **PU504 : MAX1717. (SH20)**
- **PU6 : TL594C PWM. (SH22)**

5. Pin Descriptions Of Major Components

5.1 Pentium III/Celeron µPGA2 CPU-1

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O-GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O-GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

7170 N/B MAINTENANCE

5.1 Pentium III/Celeron µPGA2 CPU-2

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 38 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III processor is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0] — System Bus Frequency** 00 — 66 MHz 01 — 100 MHz 10 — Reserved 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

Signal Name	I/O	Signal Description
DBSY#	I/O-GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-Ω, 1% resistor.
FERR#	O 1.5V Tolerant Open-drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

7170 N/B MAINTENANCE

5.1 Pentium III/Celeron µPGA2 CPU-3

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

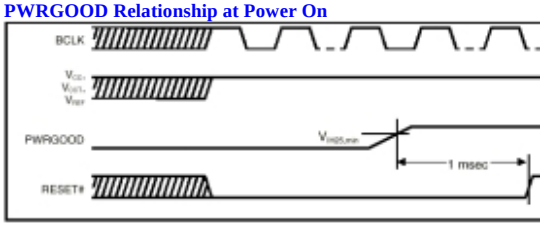
7170 N/B MAINTENANCE

5.1 Pentium III/Celeron µPGA2 CPU-4

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 17 (Section 3.7) and be followed by a 1 ms RESET# pulse.

PWRGOOD Relationship at Power On



PWRGOOD Relationship at Power On

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω1% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *Pentium II Processor Developer's Manual*. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are high. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

5.1 Pentium III/Celeron µPGA2 CPU-5

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-Ω, 1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

7170 N/B MAINTENANCE

5.1 Pentium III/Celeron µPGA2 CPU-6

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

7170 N/B MAINTENANCE

5.2 VIA VT8603 Twister North Bridge Controller-1

VT8603 / Twister OVERVIEW

Twister (VT8603) is a high performance, cost-effective and energy efficient SMA chip set for the implementation of mobile personal computer systems with 66 MHz, 100 MHz and 133 MHz CPU host bus (“Front Side Bus”) frequencies and based on 64-bit Socket-370 and Slot-1 (Intel Pentium III, Pentium-II and Celeron) super-scalar processors.

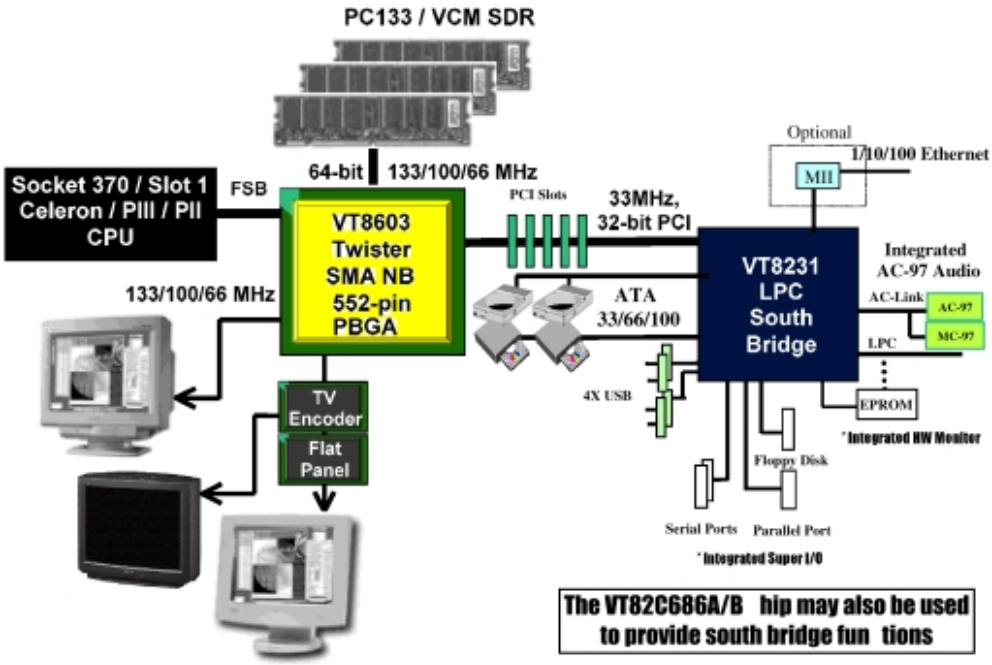


Figure 1. Twister System Block Diagram with VT8231 PCI-LPC South Bridge

7170 N/B MAINTENANCE

5.2 VIA VT8603 Twister North Bridge Controller-2

Twister integrates VIA's VT82C694X system controller, S3's Savage4 2D/3D graphics accelerator and S3's flat panel interfaces into a single 552 BGA package. The Twister SMA system controller provides superior performance between the CPU, DRAM and PCI bus with pipelined, burst, and concurrent operation.
Twister supports six banks of DRAMs up to 1.5Gbyte of system memory with 256Mbit DRAM technology. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix /match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 100/133 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M /32MxN DRAMs. The DRAM controller can run at either the host CPU Front Side Bus frequency (100 / 133 MHz) or pseudo-synchronous to the CPU FSB frequency (PC100 with the FSB at 133 MHz or PC133 with the FSB at 100 MHz) with built-in PLL timing control.

Twister supports a 32-bit 3.3 / 5V system bus (PCI) that is synchronous / pseudo-synchronous to the CPU bus. The chip Also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels(doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

Twister also integrates S3®'s Savage™ graphics accelerator into a single chip. Twister brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, Twister is an ideal solution for the consumer, corporate mobile users and entry level professionals.

The industry's first integrated AGP 4X solution, Twister combines AGP 4X performance with S3's DX6 texture Compression (S3TC) and massive 2Kx2K textures to deliver unprecedented 3D performance and image quality for the Value PC mobile market.

5.2 VIA VT8603 Twister North Bridge Controller-3

The 352-pin VT8231 BGA PCI-LPC bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.2 compliant). The VT8231 also includes an integrated Super I/O, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33 / 66 / 100 for 33 / 66 / 100 MB/sec transfer rate, integrated four USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, integrated AC-97 link for basic audio and HSP based modem functions, integrated hardware monitoring and OnNow / ACPI compliant advanced configuration and power management interface. The VT8231 also has an integrated MAC and 10Mbit PHY for LAN connection. It can bypass the internal PHY with external home PNA with a 1Mbit PHY or a 10/100Mbit PHY through the MII interface.

For sophisticated power management, Twister provides independent clock stop control for the CPU / SDRAM and PCI and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8231 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

High-Performance 3D Accelerator

Featuring a new super-pipelined 128-bit engine, Twister utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. Twister also offers the industry’s only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering ?enabling stunning image quality without performance loss. Twister further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. Twister’s advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

Twister’s advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

5.2 VIA VT8603 Twister North Bridge Controller-4

DVD Playback and Video Conferencing

Twister provides the ideal architecture for high quality MPEG-2 based DVD applications and video conferencing. For DVD playback, Twister's video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. For video conferencing, Twister's multiple video windows enable a cost effective solution.

LCD and Flat Panel Monitor Support

Twister supports a wide variety of DSTN or TFT panels through a 36-bit interface. This includes support for VGA, SVGA, XGA, SXGA+, UXGA, and UXGA+ TFT color panels with 9-bit, 12-bit, 18-bit (both 1 pixel/clock and 2 pixels/clock), and 24-bit interfaces. Enhanced STN hardware with 256 gray scale support and advanced frame rate control to provide up to 16.7 million colors. In addition, the integrated 2-channel LVDS interface can support another panel. All resolutions are supported up to 1280x1024. The integrated ZV-Port allows display of video from an external source.

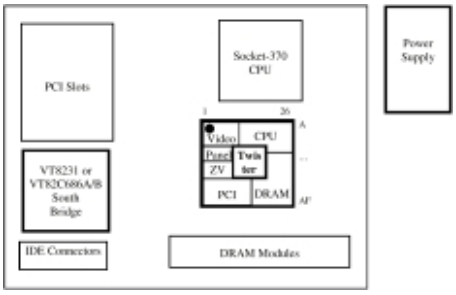
An alternative to the 36-bit panel interface is a 12-bit interface to a TMDS encoder. This interface is Digital Visual Interface (DVI) 1.0 compliant.

5.2 VIA VT8603 Twister North Bridge Controller-5

VT8603 / Twister Pin Descriptions

CPU Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
HA[31:3]#	(see pinout tables)	IO	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the Twister during cache snooping operations.
HD[63:0]#	(see pinout tables)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
ADS#	J24	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
BNR#	D26	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	E26	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The Twister drives this signal to gain control of the processor bus.
DBSY#	H26	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	F26	IO	**Defer**. The Twister uses a dynamic deferring policy to optimize system performance. The Twister also uses the DEFER# signal to indicate a processor retry response.
DRDY#	J23	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	G24	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	G26	I	**Hit Modified**. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	G23	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	E25, F25, F24, F23 E24	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G25	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	H25, K23 H23	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]# — Response type** 000 — Idle State 001 — Retry Response 010 — Defer Response 011 — Reserved 100 — Hard Failure 101 — Normal Without Data 110 — Implicit Writeback 111 — Normal With Data
CPURST#	A19	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.
CPURSTD#	E22	O	**CPU Reset Delayed.** CPU reset output delayed by 2T.
BREQ0#	J25	O	**Bus Request 0.** Bus request output to CPU.

Note: Clocking of the CPU interface is performed with HCLK.
Note: Internal pullup resistors are provided on all GTL interface pins. If the CPU does not have internal pullups, these north bridge internal pullups may be enabled to allow the interface to meet GTL bus interface specifications (see MA6 strap description).
The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



5.2 VIA VT8603 Twister North Bridge Controller-6

DRAM Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MA14 /graphics strap **MA13** /graphics strap **MA12 / BA1** /strap, **MA11 / BA0** /strap, **MA10** **MA9** /strap, **MA8** /strap, **MA7** /strap, **MA6** /strap, **MA5** /strap, **MA4** / graphics strap, **MA3** / graphics strap, **MA2** / graphics strap, **MA1** / graphics strap, **MA0**/ graphics strap	AF25 AE25 AE24 AD24 AE26 AD25 AD26 AC24 AC25 AC26 AB24 AB25 AB26 AB23 AA23	O/I	**Memory Address.** DRAM address lines / strap options MA12 strap – Host Freq Select lsb (see MA8 below for msb) MA11 strap – IOQ Level (0=4-level, 1=1-level) MA9 strap – Clock select (0=Use PLLs, 1=Clocks on XIN/PD10 pins) MA8 strap – Host Freq Select msb (00=66, 01=100, 10=auto, 11=133) MA7 strap – Graphics Test Mode (0=Normal, 1=Test) MA6 strap – GTL Internal Pullups (0=Enable, 1=Disable) MA5 strap – PCI Frequency (0=33 MHz, 1=66 MHz) MA4 strap – Graphics PCI Interrupt (0=Enable, 1=Disable) MA3 strap – Graphics I/O (0=Enable, 1=Disable) MA2 strap – Graphics PCI Base Address (0=Map0, 1=Map1) MA14,13,1,0 – Graphics OEM-Defined Panel Type (Note: all non-graphics straps default to 0 if not connected to a strap resistor. See Table 9 for graphics strap definitions and defaults.)
CS[5:0]# **RAS[5:0]#**	W21, Y22 Y23, Y24 Y25, Y26	O	**Chip Select.** (Synchronous DRAM) Chip select of each bank. **RAS.** (FPG/EDO DRAM)
DQM[7:0] **CAS[7:0]#**	AF23, AD23, W25, W26, AE23, AF24, W23, V23	O	**Data Mask.** (Synchronous DRAM) Data mask of each byte lane **CAS.** (FPG/EDO DRAM)
SRASA# **SRASB# / CKE5** **SRASC# / CKE4**	AA24 AA25 AA26	O	**Row Address Command Indicator.** For support of up to three synchronous DRAM DIMM slots. “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1) and “C” controls banks 4-5 (module 2).

Signal Name	PIN #	I/O	Signal Description
SCASA# **SCASB# / CKE3** **SCASC# / CKE1**	U22 V25 V24	O	**Column Address Command Indicator.** For support of up to three synchronous DRAM DIMM slots. “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1) and “C” controls banks 4-5 (module 2).
SWEA# / MWEA **SWEB#/MWEB#/CKE2** **SWEC#/ MWEC#/CKE0**	U24 U25 U26	O	**Write Enable Command Indicator.** For support of up to three synchronous DRAM DIMM slots. Used as MWE# for FPG/EDO memory. “A” controls banks 0-1 (module 0), “B” controls banks 2-3 (module 1) and “C” controls banks 4-5 (module 2).
CKE0 / SWEC# **CKE1 / SCASC#** **CKE2 / SWEB#** **CKE3 / SCASB#** **CKE4 / SRASC#** **CKE5 / SRASB#**	U26 V24 U25 V25 AA26 AA25	O	**SDRAM Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

5.2 VIA VT8603 Twister North Bridge Controller-7

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
AD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	AD7, AD9, AB11, AF12	IO	**Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	AE9	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	AC10	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	AD10	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	AE10	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	AB9	IO	**Device Select.** This signal is driven by the Twister when a PCI initiator is attempting to access main memory. It is an input when the Twister is acting as a PCI initiator.
PAR	AB10	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	AF10	IO	**System Error.** The Twister will pulse this signal when it detects a system error condition.
LOCK#	AE5	IO	**Lock.** Used to establish, maintain, and release resource lock.
PREQ#	AC15	I	**South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	AD15	O	**South Bridge Grant.** This signal driven by the Twister to grant PCI access to the South Bridge.
REQ[3:0]#	AD4, AE4, AD5, AC5	I	**PCI Master Request.** PCI master requests for PCI.
GNT[3:0]#	AE3, AF3, AF4, AB5	O	**PCI Master Grant.** Permission is given to the master to use PCI.
REQX#	AF2	I	**PCI Master Request.** PCI master request for PCI.
GNTX#	AE2	O	**PCI Master Grant.** Permission is given to the master to use PCI.
PCLK	AB15	I	**PCI Clock.** From external clock generator.
PCKRUN#	AF15	IO	**PCI Clock Run.** May be used to stop PCI clock.

Signal Name	PIN #	I/O	Signal Description
INTA#	W5	O	**PCI Interrupt Out.** An asynchronous active low output used to signal an event that requires handling on behalf of the internal integrated graphics controller. If MA2 is strapped high at reset (clearing CR36[0]) no interrupt will be requested during PCI configuration. The default drive strength is 24 Ma (other drive strengths may be selected via CR80[1-0]).
WSC#	AA11	O	**Write Snoop Complete.** Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed.

5.2 VIA VT8603 Twister North Bridge Controller-8

LCD Panel Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
FPD[35:0]	(see pin table)	O	**Panel Data.** Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1.
FPDET	AA16	I	**Panel Detect.** If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
FPVS	G3	O	**Panel VSYNC.** Internally pulled down.
FPHS	G5	O	**Panel HSYNC.** Internally pulled down.
FPDE	H3	O	**Panel Data Enable.** Internally pulled down.
FPCLK	G4	O	**Panel Clock.** Internally pulled down during reset. 8mA is the default. 16mA may also be selected.
ENVDD	F1	O	**Enable VDD.** This signal is driven high to external logic to initiate a flat panel power up sequence.
ENVEE	H5	O	**Enable VEE.** This signal is driven high to a programmable time after ENVDD is driven high during a flat panel power up sequence.
FPGPIO	G1	I/O	**General Purpose Input / Output.**

Flat Panel Monitor (DVI) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
FPD[11:0]	(see pin table)	O	**Panel Data.** Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1. This function is selected on these pins when SR31[4] = 1.
FPDET	AA16	I	**Panel Detect.** If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
FPVS	G3	O	**Panel VSYNC.** Internally pulled down.
FPHS	G5	O	**Panel HSYNC.** Internally pulled down.
FPDE	H3	O	**Panel Data Enable.** Internally pulled down.
FPCLK	G4	O	**Panel Clock.** Internally pulled down during reset. 8mA is the default. 16 mA may also be selected.

ZV-Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ZVD[15:0]	(see pin table)	I	**ZV-Port Data Bus.** Video Input
ZVCLK	U3	I	**ZV-Port Clock.**
ZVHS	T3	I	**ZV-Port Horizontal Sync.**

TV Encoder Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
TVD[11:0]	(see pin table)	O	**TV Data.** Internally pulled down during reset
TVCLK	V4	I	**TV Clock.** Input clock from encoder. Internally pulled down.
TVCLKR	K5	O	**TV Return Clock.** Output clock to TV encoder. Internally pulled down.
TVVS	W3	O	**TV VSYNC.** Internally pulled down during reset
TVHS	V5	O	**TV HSYNC.** Internally pulled down during reset
TVBLK#	L1	O	**TV Blanking.** Internally pulled down during reset

CRT Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
RSET	E3	A	**Reference Resistor.** Tie to GNDRGB through an external 140_ resistor to control the RAMDAC full-scale current value.
COMP	E4	A	**Compensation.** Tie to VCC25 through a 0.1 µF capacitor**.**
RED	C2	A	**Analog Red.** Analog red output to the CRT monitor.
BLUE	D2	A	**Analog Blue.** Analog blue output to the CRT monitor.
GREEN	D3	A	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	E2	O	**Horizontal Sync.** Output to CRT.
VSYNC	E1	O	**Vertical Sync.** Output to CRT.

LVDS Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
Y[2:0]P	Y5, W4, AA3	A	**LVDS Data Positive Output.**
Y[2:0]M	AA5, Y4, AB3	A	**LVDS Data Negative Output.**
YCP	AB1	A	**LVDS Clock Positive Output.**
YCM	AC1	A	**LVDS Clock Negative Output.**
Z[2:0]P	AA4, AC3, AC2	A	**2 nd LVDS Data Positive Output.**
Z[2:0]M	AB4, AD3, AD2	A	**2 nd LVDS Data Negative Output.**
ZCP	AD1	A	**2 nd LVDS Clock Positive Output.**
ZCM	AE1	A	**2 nd LVDS Clock Negative Output.**

5.2 VIA VT8603 Twister North Bridge Controller-9

Miscellaneous Functions			
Signal Name	**PIN #**	**I/O**	**Signal Description**
XIN	A2	I	**Reference Frequency Input.** An external 14.318 MHz crystal is connected between XOUT and this pin. Alternatively, an external oscillator can be connected.
XOUT	A3	O	**Crystal Output.** This pin drives the crystal via an internal oscillator. If an external oscillator is connected to XIN, this pin can be left unconnected.
SPCLK[2:1]	M2, F3	IO	**Serial Port Clocks.** These are the clocks for serial data transfer. SPCLK1 is typically used for I^2C communications. As an output, it is programmed via CRA0[0]. As an input, its status is read via CRA0[2]. In either case the serial port must be enabled by CRA0[4] = 1. SPCLK2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[0]. As an input, its status is read via CRB1[2]. The port is enabled via CRB1[4] = 1.
SPDAT[2:1]	M3, F2	IO	**Serial Port Data.** These are the data signals used for serial data transfer. SPDAT1 is typically used for I^2C communications. As an output, it is programmed via CRA0[1]. As an input, its status is read via CRA0[3]. In either case the serial port must be enabled by CRA0[4] = 1. SPDAT2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[1]. As an input, its status is read via CRB1[3]. The port is enabled via CRB1[4] = 1.
GPOUT	AA12	O	**General Purpose Output.** This pin reflects the state of SRD[0].
GOP0	C3	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].
STPAGP#	C4	I	**Stop AGP.** Power management for internal AGP.
AGPBUSY#	B4	I/O	**AGP Busy.** Power management for internal AGP.
STANDBY	F4	I	**Standby.** Used to put the integrated graphics controller in the standby state.
SUSPEND	F5	I	**Suspend.** Used to put the integrated graphics controller in the suspend state.
SUSST#	AC22	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

Clock / Reset Control			
Signal Name	**PIN #**	**I/O**	**Signal Description**
HCLK	G22	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all Twister logic that is in the host CPU domain.
PCLK	AB15	I	**PCI Clock.** This pin receives a buffered host clock divided-by-2, 3, or 4 to create 33 MHz. This clock is used by all of the Twister logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1, 3:1, or 4:1 as shown in the table below. The host CPU clock must lead the PCI clock by 2.0 ± 1.0 nsec. Typical Clock Frequency Combinations Rx68[1:0] / Mode / Host Clock / AGP Clock / PCI Clock 00 / 2x / 66 MHz / 66 MHz / 33 MHz 01 / 3x / 100 MHz / 66 MHz / 33 MHz 10 / 4x / 133 MHz / 66 MHz / 33 MHz 11 / Reserved
MCLK	J22	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	K22	I	**DRAM Clock Feedback.** Input from the external clock buffer.
RESET#	AE15	I	**Reset.** Input from South Bridge chip. When asserted, this signal resets the Twister and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.
CPURST#	A19	O	**CPU Reset.** GTL output level.
CPURSTD#	E22	O	**CPU Reset Delayed.** Reset output delayed by 2T.

5.2 VIA VT8603 Twister North Bridge Controller-10

Power, Ground, and Test			
Signal Name	**PIN #**	**I/O**	**Signal Description**
VCC3	(see pin list)	P	**Power** for **I/O Interface Logic** (3.3V ±5%).
VCC25	(see pin list)	P	**Power** for **Internal Logic** (2.5V ±5%).
VCC5	U6	P	**Power** for **5V Input Tolerance** (5V ±5%).
VSUS25	AA22	P	**Suspend Power** (2.5V ±5%).
VCCRGB	D1	P	**Power for CRT** (2.5V ±5%).
VCCA	H21, H22	P	**Power for Analog** (2.5V ±5%)
VCCDAC	C1	P	**Power for DAC Digital Logic** (2.5V ±5%)
VCCPLL1	B3	P	**Power for PLL1** (2.5V ±5%).
VCCPLL2	A5	P	**Power for PLL2** (2.5V ±5%).
VCCLPLL	AB2	P	**Analog Power for LVDS PLL** (2.5V ±5%).
VCCLVDS	W1, W2	P	**Analog Power for LVDS** (3.3V ±5%).
VDDD	Y2	P	**Digital Power for LVDS** (2.5V ±5%).
GND	(see pin table)	P	**Ground**
GNDA	L21, L22	P	**Ground for North Bridge Host CPU Clock Circuitry.** Connect to main ground plain through a ferrite bead.
GNDRGB	A1	P	**Connection point for RGB load resistors**
GNDDAC	B1	P	**Ground for DAC Analog Circuitry**
GNDPLL1	A4	P	**Ground for PLL1**
GNDPLL2	B5	P	**Ground for PLL2**
GNDLPLL	Y3	P	**Ground for LVDS PLL**
GNDLVDS	Y1, AA1	P	**Ground for LVDS Analog Circuitry**
GNDD	AA2	P	**Ground for LVDS Digital Circuitry**
GTLREF	E12, E21	P	**CPU Interface GTL+ Voltage Reference.** 2/3 VTT ±2%
PLLTST	K24	I	**PLL Test Input.** Pull down with 4.7K resistor for normal operation.
BISTIN	F15	I	**BIST In.** This pin is used for testing and must be left unconnected or tied high on all board designs.
DFTIN	F11	I	**DFT In.** This pin is used for testing and must be left unconnected or tied high on all board designs.
NC	R21, V22, W22, AB22	-	**No Connect.** Reserved for future use. Do not connect.

5.3 VIA VT8231 South Bridge Controller-1

VT8231 OVERVIEW

The VT8231 South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel, AMD, and VIA / Cyrix based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI /LPC system. The VT8231 includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8231 also supports the UltraDMA-33, 66, and 100 standards to allow reliable data transfer rates up to 100 MB/sec throughput. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

b) Integrated LAN Fast Ethernet controller (MAC) with Media Independent Interface (MII) to external Ethernet PHY or HomePNA PHY. The LAN controller operates at 1 / 10 / 100 Mbit/sec transfer rates using either full and half duplex operation and has separate 2Kbyte FIFOs for receive and transmit of full ethernet packets. The internal high-performance PCI interface has scatter / gather and bursting capability and can align bytes in the transmit data buffer to reduce CPU utilization. The LAN interface can perform address filtering on physical, broadcast, and multicast packets. The interface can also be configured for system wake up on link status change, receipt of magic packet, unicast physical address match on incoming packets, and predefined pattern match in the incoming data.

c) LPC (Low Pin Count) interface for BIOS ROM plus optional conventional BIOS ROM support

d) Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT8231 includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

e) Keyboard controller with PS2 mouse support

f) Real Time Clock with 256 byte extended CMOS. In addition to standard RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

5.3 VIA VT8231 South Bridge Controller-2

g) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

h) Hardware monitoring subsystem for managing system / motherboard voltage levels, temperatures, and fan speeds

i) Full System Management Bus (SMBus) interface with one master / slave port and one slave-only port

j) 16550-compatible serial I/O port with “Fast-IR”infrared communications port option.

k) Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.

l) Game port and MIDI port

m) Standard floppy disk drive interface

n) ECP/EPP-capable parallel port with floppy disk controller pinout option

o) Serial IRQ for docking and non-docking applications

p) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.

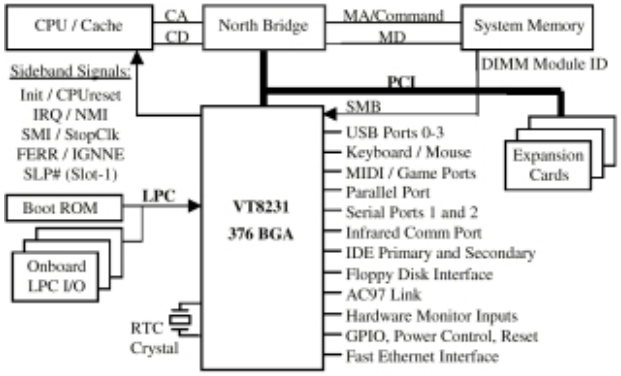


Figure 1. PC System Configuration Using the VT8231

5.3 VIA VT8231 South Bridge Controller-3

Pin Descriptions

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles. IDSEL is internally connected to AD28.
C/BE[3:0]#	C5, D6, A8, F10	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	F6	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C7	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
STOP#	D7	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	A7	IO	**Device Select.** The VT8231 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8231-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
PAR	C8	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	E7	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8231 can be programmed to generate an NMI to the CPU.
PINTA-D#	B2, B1, C3, C2	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PINTA# PINTB# PINTC# PINTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTA# PCI Slot 3 INTC# INTD# INTA# INTB# PCI Slot 4 INTD# INTA# INTB# INTC# PCI Slot 5 INTA# INTB# INTC# INTD#
PCICLK	M17	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.

Signal Name	PIN #	I/O	Signal Description
PCKRUN#	R5	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8231 drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100Ω resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "Apollo MVP4 Design Guide" for more details.
PCIRST#	E4	O	**PCI Reset.**
PCISTP#/ GPO6	T4	O	**PCI Stop.**
CPUSTP#/ GPO5	P4	O	**CPU Stop.**
PREQH#	C1	O	**PCI Request.** This signal goes to the North Bridge REQ4# input to request the PCI bus for high priority access. The internal LAN requests the PCI bus using this signal, so if the LAN subsystem is used, this signal must be connected (one of the H/LREQ/GNT 1 and 2 pairs provided by the VT8231 may be used to implement the fifth PCI slot if desired). If the LAN subsystem is not used, PREQH# / PGNTH# may optionally remain unconnected.
PGNTH#	D3	I	**PCI Grant.** This signal is driven by the North Bridge GNT4# signal to grant high priority PCI access to the VT8231.
PREQL#	D2	O	**PCI Request.** This signal goes to the North Bridge PREQ# input to request the PCI bus for normal priority access.
PGNTL#	D1	I	**PCI Grant.** This signal is driven by the North Bridge PGNT# output to grant normal priority PCI access to the VT8231.
HREQ1#/ GPI10	Y11	I / IO	**High Priority Request 1.** Device 0 Function 4 RxE5[3] = 1.
HGNT1#/ GPO8	W11	O / IO	**High Priority Grant 1.** Device 0 Function 4 RxE5[3] = 1.
HREQ2#/ GPI11	V11	I / IO	**High Priority Request 2.** Device 0 Function 4 RxE5[3] = 1.

5.3 VIA VT8231 South Bridge Controller-4

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
HGNT2#/ GPO9	T10	O / IO	**High Priority Grant 2.** Device 0 Function 4 RxE5[3] = 1.
LREQ1#/ GPI12	U10	I / IO	**Low Priority Request 1.** Device 0 Function 4 RxE5[2] = 1.
LGNT1#/ GPO10	Y10	O / IO	**Low Priority Grant 1.** Device 0 Function 4 RxE5[2] = 1.
LREQ2#/ GPI13	W10	I / IO	**Low Priority Request 2.** Device 0 Function 4 RxE5[2] = 1.
LGNT2#/ GPO11	V10	O / IO	**Low Priority Grant 2.** Device 0 Function 4 RxE5[2] = 1.

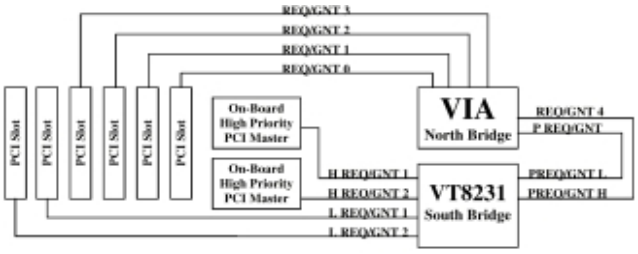


Figure 5. PCI Request / Grant Connections Using the VT8231

CPU Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
CPURST	U4	OD	**CPU Reset.** The VT8231 asserts CPURST to reset the CPU during power-up.
INTR	R6	OD	**CPU Interrupt.** INTR is driven by the VT8231 to signal the CPU that an interrupt request is pending and needs service.
NMI	T5	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8231 generates an NMI when either SERR# or IOCHK# is asserted.
INIT	V5	OD	**Initialization.** The VT8231 asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
STPCLK#	V6	OD	**Stop Clock.** STPCLK# is asserted by the VT8231 to the CPU to throttle the processor clock.
SMI#	Y5	OD	**System Management Interrupt.** SMI# is asserted by the VT8231 to the CPU in response to different Power-Management events.
FERR#	U5	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.
IGNNE#	T6	OD	**Ignore Numeric Error.** This pin is connected to the "ignore error" pin on the CPU.
SLP#/ GPO7	U6	OD	**Sleep** (F4 RxE4[4] = 1). Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.
A20M#	W5	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20). See Device 0 Function 0 Rx59[1].
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.** Connect to cathode of first external temperature sensing diode.
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.** Connect to anode of first external temperature sensing diode.

Note: Connect each of the above signals to 4.7KΩ pullup resistors to VCC3.

5.3 VIA VT8231 South Bridge Controller-5

Strap Options			
Signal Name	**PIN #**	**I/O**	**Signal Description**
Strap/SUSA#/ GPO1	P1	I / O	**CPURST / INIT Polarity** H: Slot-1 / Socket-370 / Slot-A / Socket-A L: Socket-7
Strap/MCCS#/ GPO17	W6	I / O	**CPU Frequency Strapping** H: Disable L: Enable
Strap/ SA16	Y14	I / IO	**BIOS ROM Interface** H: LPC L: Conventional
Strap/ SA17	T13	I / IO	**Auto Reboot** H: Disable (recommended) L: Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1 or H) or driving it low during reset with a 7407 TTL open collector buffer (for 0 or L) as shown in the suggested circuit below:

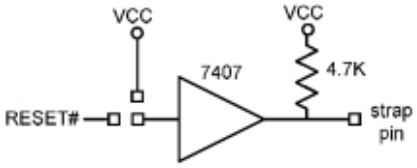


Figure 6. Strap Option Circuit

Advanced Programmable Interrupt Controller (APIC) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
WSC#/ GPI14	V4	I / I	**Internal APIC Write Snoop Complete.** F0 Rx58[6] = 1. Asserted by the north bridge to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to perform an APIC interrupt.
APICD0/ GPO28	W4	O / O	**Internal APIC Data 0.** F0 Rx58[6] = 1.
APICD1/ GPO29	Y4	O / O	**Internal APIC Data 1.** F0 Rx58[6] = 1.
APICCLK/ GPI9	Y3	I / I	**APIC Clock.** F0 Rx58[6] = 1.

Low Pin Count (LPC) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
LFRAME#	W8	O	**LPC Frame.**
LDRQ#/ GPI15	Y8	I / I	**LPC Data Request.** F0 Rx58[5] = 1 and F4 RxE5[7] = 0.
LAD[3-0]	V7,W7,Y7,V8	IO	**LPC Address / Data.**

Note: For LPC control, see Device 0 Function 0 Rx58[5] and Rx59[4-3]
Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

Serial EEPROM Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
EECS#	C18	O	**Serial EEPROM Chip Select.**
EECK	E16	O	**Serial EEPROM Clock.**
EEDO	D17	O	**Serial EEPROM Data Output.**
EEDI	E17	I	**Serial EEPROM Data Input.**

5.3 VIA VT8231 South Bridge Controller-6

LAN Controller - Media Independent Interface (MII)			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MCOL	G17	I	**MII Collision Detect.** From the external PHY.
MCRS	G16	I	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	C20	O	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	D18	IO	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C19	I	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3], **MRXD[2]**, **MRXD[1]**, **MRXD[0]**	D19 D20 E18 E19	I I I I	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	E20	I	**MII Receive Data Valid.**
MRXERR	F18	I	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	F17	I	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3], **MTXD[2]**, **MTXD[1]**, **MTXD[0]**	G20 G19 G18 F20	O O O	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	F19	O	**MII Transmit Enable.** Indicates transmit active from the MII port to the PHY.

The internal LAN controller uses the high priority PCI bus request / grant pair (PREQH# / PGNTH#) to request PCI bus access from the chipset north bridge.

Universal Serial Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
USBP0+	B18	IO	**USB Port 0 Data +**
USBP0-	A18	IO	**USB Port 0 Data -**
USBP1+	B19	IO	**USB Port 1 Data +**
USBP2+	B20	IO	**USB Port 2 Data +**
USBP2-	A20	IO	**USB Port 2 Data -**
USBP3+	C17	IO	**USB Port 3 Data +**
USBP3-	B17	IO	**USB Port 3 Data -**
USBCLK	C15	I	**USB Clock.** 48MHz clock input for the USB interface
USBOC0#	A17	I	**USB Port 0 Over Current Detect.** Port 0 is disabled if this input is low.
USBOC1#	D16	I	**USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low
USBOC2#/ LA20/ GPI20 / GPO20	W13	I / IO/ I / O	**USB Port 2 Over Current Detect.** Port 2 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[4] = 1
USBOC3#/ LA21/ GPI21 / GPO21	Y13	I / IO/ I / O	**USB Port 3 Over Current Detect.** Port 3 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[5] = 1

5.3 VIA VT8231 South Bridge Controller-7

System Management Bus (SMB) Interface (I^2C Bus)			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SMBCK1	R3	IO	**SMB / I^2C Channel 1 Clock.**
SMBCK2/ GPIO27	R1	IO / IO	**SMB / I^2C Channel 2 Clock†.** F4 Rx55[3] = 0.
SMBDT1	T1	IO	**SMB / I^2C Channel 1 Data.**
SMBDT2/ GPIO26	R2	IO / IO	**SMB / I^2C Channel 2 Data†.** F4 Rx55[3] = 0.
SMBALRT#/ GPI7	T2	I / I	**SMB Alert.** (System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. The same pin is used as General Purpose Input 6 whose value is reflected in Rx48[6] of function 4 I/O space

Note: SMBus #2 is a slave-only device used to supply status for external Alert-On-LAN (AOL)

UltraDMA-33 / 66 Enhanced IDE Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PDRDY/ PDDMARDY/ PDSTROBE	N19	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY/ SDDMARDY/ SDSTROBE	Y20	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR#/ PHDMARDY/ PHSTROBE	N18	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR#/ SHDMARDY/ SHSTROBE	W19	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers

Signal Name	**PIN #**	**I/O**	**Signal Description**
PDIOW#/ PSTOP	P20	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW#/ SSTOP	Y19	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	P19	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	U17	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	N20	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	W20	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	T14	I	**Primary Channel Interrupt Request.**
IRQ15	U14	I	**Secondary Channel Interrupt Request.**

MIDI Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MSI	G4	I	**MIDI Serial In**
MSO	J4	O	**MIDI Serial Out**

AC97 Audio / Modem Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ACRST#	G2	O	**AC97 Reset**
ACSYNC	G1	O	**AC97 Sync**
ACSDOUT	H3	O	**AC97 Serial Data Out**
ACSDIN0	H1	I	**AC97 Serial Data In 0**
ACSDIN1	H2	I	**AC97 Serial Data In 1**
ACBITCLK	J3	I	**AC97 Bit Clock**

5.3 VIA VT8231 South Bridge Controller-8

UltraDMA-33 / 66 Enhanced IDE Interface (continued)			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PDCS1#	L18	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	L19	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	U18	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	U19	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	M20, M18, M19	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	V20, V18, V19	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	T17, R17, T18, T20, P17, N16, R19, P18, R18, R20, N17, P16, T19, U20, R16, T16	IO	**Primary Disk Data**
SDD[15-0]/ SA[15-0]	W18, V17, Y17, W16, V15, Y15, W14, T15, U15, U16, V14, W15, Y16, V16, W17, Y18	IO	**Secondary Disk Data / ISA Address**

Game Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
JAX	J1	I	**Joystick A X-axis**
JAY	K4	I	**Joystick A Y-axis**
JBX	K5	I	**Joystick B X-axis**
JBY	J2	I	**Joystick B Y-axis**
JAB1 / GPI28	G3	I	**Joystick A Button 1.** Device 0 Function 0 Rx53[7] = 0.
JAB2 / GPO12	H5	I	**Joystick A Button 2.** Device 0 Function 4 RxE5[4] = 1.
JBB1 / GPI29	F1	I	**Joystick B Button 1.** Device 0 Function 0 Rx53[7] = 0.
JBB2 / GPO13	H4	I	**Joystick B Button 2.** Device 0 Function 4 RxE5[4] = 1.

See Function 0 Rx77[6]

Floppy Disk Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
DRVDEN0	L17	O	**Drive Density Select 0.**
DRVDEN1	K17	O	**Drive Density Select 1.**
MTR0#	K18	O	**Motor Control 0.** Select motor on drive 0.
MTR1#	J16	O	**Motor Control 1.** Select motor on drive 1
DS0#	J17	O	**Drive Select 0.** Select drive 0.
DS1#	K19	O	**Drive Select 1.** Select drive 1
DIR#	K20	O	**Direction.** Direction of head movement (0 = inward motion, 1 = outward motion)
STEP#	J18	O	**Step.** Low pulse for each track-to-track movement of the head.
INDEX#	L20	I	**Index.** Sense to detect that the head is positioned over the beginning of a track
HDSEL#	H19	O	**Head Select.** Selects the side for R/W operations (0 = side 1, 1 = side 0)
TRK00#	H16	I	**Track 0.** Sense to detect that the head is positioned over track 0.
RDATA#	H20	I	**Read Data.** Raw serial bit stream from the drive for read operatrions.
WDATA#	J19	O	**Write Data.** Encoded data to the drive for write operations.
WGATE#	J20	O	**Write Gate.** Signal to the drive to enable current flow in the write head.
DSKCHG#	H18	I	**Disk Change.** Sense that the drive door is open or the diskette has been changed since the last drive selection.
WRTPRT#	H17	I	**Write Protect.** Sense for detection that the diskette is write protected (causes write commands to be ignored)

See also Parallel Port pin descriptions for optional Floppy Disk interface functionality

5.3 VIA VT8231 South Bridge Controller-9

Serial Port and Infrared Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
TXD	B15	O	**Transmit Data.** Serial port transmit data out.
RXD	E14	I	**Receive Data.** Serial port receive data in.
IRTX/ GPO14	R8	O / O	**Infrared Transmit.** IR transmit data out (Function 4 RxE5[5] = 1) selectable from serial port 1, 2, or 3.
IRRX/ GPO15	U8	I / O	**Infrared Receive.** IR receive data in (Function 4 RxE5[5] = 1) selectable to serial port 1, 2, or 3.
IRRX2/ GPIOB	T8	I	**Infrared Receive.** IR receive data in (see FIR I/O Rx33 and 34)
RTS#	A15	O	**Request To Send.** Indicator that the serial output port is ready to transmit data. Typically used as hardware handshake with CTS# for low level flow control. Designed for direct input to external RS-232C driver.
CTS#	B16	I	**Clear To Send.** Indicator to the serial port that an external communications device is ready to receive data. Typically used as hardware handshake with RTS# for low level flow control. Designed for input from external RS-232C receiver.
DTR#	A16	O	**Data Terminal Ready.** Indicator that serial port is powered, initialized, and ready. Typically used as hardware handshake with DSR# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DSR#	D14	I	**Data Set Ready.** Indicator to serial port that an external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DCD#	D15	I	**Data Carrier Detect.** Indicator to serial port that an external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
RI#	C16	I	**Ring Indicator.** Indicator to serial port that an external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).

Parallel Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PINIT#/ DIR#	B12	IO / O	**Initialize.** Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
STROBE#/ nc	A11	IO / -	**Strobe.** Output used to strobe data into the printer. I/O in ECP/EPP mode.
AUTOFD#/ DRVEN0	E11	IO / O	**Auto Feed.** Output used to cause the printer to automatically feed one line after each line is printed. I/O pin in ECP/EPP mode.
SLCTIN#/ STEP#	D12	IO / O	**Select In.** Output used to select the printer. I/O pin in ECP/EPP mode.
SLCT/ WGATE#	E13	I / O	**Select.** Status output from the printer. High indicates that it is powered on.
ACK# / DS1#	B14	I / O	**Acknowledge.** Status output from the printer. Low indicates that it has received the data and is ready to accept new data
ERROR#/ HDSEL#	F11	I / O	**Error.** Status output from the printer. Low indicates an error condition in the printer.
BUSY/ MTR1#	A14	I / O	**Busy.** Status output from the printer. High indicates not ready to accept data.
PE/ WDATA#	D13	I / O	**Paper End.** Status output from the printer. High indicates that it is out of paper.
PD7/ nc, **PD6**/ nc, **PD5**/ nc, **PD4**/ DSKCHG#, **PD3**/ RDATA#, **PD2**/ WRTPRT#, **PD1**/ TRK00#, **PD0**/ INDEX#	C14 A13 B13 C13 E12 A12 C12 D11	IO / - IO / - IO / - IO / I IO / I IO / I IO / I IO / I	**Parallel Port Data.**

As shown by the alternate functions above, in mobile applications the parallel port pins can optionally be selected to function as a floppy disk interface for attachment of an external floppy drive using the parallel port connector (see Super I/O Configuration Index F6[5]).

Serial IRQ			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SERIRQ	V9	I	**Serial IRQ.**

5.3 VIA VT8231 South Bridge Controller-10

Conventional BIOS ROM / ISA Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
LA21/ USBOC3# / GPI21 / GPO21 **LA20**/ USBOC2# / GPI20 / GPO20	Y13 W13	O O	**System Address Bus**. Allows access to physical memory devices (e.g., BIOS ROMs) up to 4 Mbytes. F4 RxE4[6] = 1.
SA[19:18], **SA17**/ strap, **SA16**/ strap, **SA[15:0]**/ SDD[15:0]	V13, U13, T13, Y14, W18, V17, Y17, W16, V15, Y15, W14, T15, U15, U16, V14, W15, Y16, V16, W17, Y18	IO	**System Address Bus**. These address lines are used to interface to BIOS ROMs but may also be used to implement a subset of the ISA bus if required. SA[19-16] are connected to ISA bus SA[19-16] directly. SA[19-17] are also connected to LA[19-17] of the ISA bus. SA17 strap – 0/1 = Enable / Disable Auto Reboot SA16 strap – 0/1 = Disable / Enable LPC ROM
SD[7-0]	T11, R11, U11, U12, Y12, W12, V12, R12	IO	**System Data.** SD[7:0] provide the data path for BIOS ROMs and other 8-bit devices residing on the ISA bus.
IOR#/ GPI22/ GPO22	U7	IO	**I/O Read.** Command to ISA I/O slave devices to indicate that the slave may drive data on to the ISA data bus. F4 RxE4[7] = 1.
IOW#/ GPI23 / GPO23	T7	IO	**I/O Write.** Command to ISA I/O slave devices to indicate that the slave may latch data from the ISA data bus. F4 RxE4[7] = 1.
MEMR#	W9	IO	**Memory Read.** Command to memory slave to indicate that it may drive data onto the ISA data bus.
MEMW#	Y9	IO	**Memory Write.** Command to memory slave to indicate that it may latch data from the ISA data bus.
IRQ1/ MSCK	N2	I	**Interrupt 1 (optional external Keyboard Controller).**
IRQ12/ MSDT	N4	I	**Interrupt 12 (optional external PS2 Mouse Controller).**
IRQ14	T14	I	**Interrupt 14 (IDE Primary Channel).**
IRQ15	U14	I	**Interrupt 15 (IDE Secondary Channel).**
SPKR	U9	O	**Speaker Drive.** Output of internal timer/counter 2.

Internal Keyboard Controller			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MSCK/ IRQ1	N2	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by F0 Rx51[2]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**. Interrupt 1 (external KBC).
MSDT/ IRQ12	N4	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by F0 Rx51[2]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 12**. Interrupt 12 (ext PS2 mouse ctlr).
KBCK/ A20GATE	M4	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by F0 Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT/ KBRC	N1	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by F0 Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS#/ ROMCS#	T9	O / O	**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip.

Chip Selects			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ROMCS#/ KBCS#	T9	O / O	**ROM Chip Select** (Rx51[0]=1). Chip Select to the BIOS ROM. See also Device 0 Rx40[5-4] and Rx41.
MCCS#/ GPO17/ strap	W6	O / IO	**Microcontroller Chip Select** (Device 0 Function 4 RxE4[3] = 0). Asserted during read or write accesses to I/O ports 62h or 66h. Strap: 0/1 = Enable / Disable CPU Frequency Strapping
PCS0#/ GPO16	Y6	O / IO / IO	**Programmable Chip Select 0.** (Device 0 Function 4 RxE4[2] = 0). Asserted during I/O cycles to programmable read or write ISA I/O port ranges.
PCS1#/ GPI19/ GPO19	G5	O / I / O	**Programmable Chip Select 1.** (Device 0 Function 4 RxE4[5] = 1)

5.3 VIA VT8231 South Bridge Controller-11

Hardware Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
UIC1	M1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC2	M3	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC3	M2	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC4	L4	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC5	L1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.**
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.**
VREF	K1	O	**Voltage Reference for Thermal Sensing** (2.2V ±5%)
FAN1	K2	I	**Fan Speed Monitor 1.** (3.3V only)
FAN2/ SLPBTN#/ GPI18/ GPO18	K3	I / I / I / O	**Fan Speed Monitor 2.** (3.3V only) (F4 RxE5[0] = 0)
DTEST/ GPIOD (30)	Y1	O	**Hardware Monitor Digital Test Out**
ATEST/ GPIOC (25) / CHSINOUT	J2	O	**Hardware Monitor Analog Test Out**

Power Management and External State Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PME#/ GPI6	U1	I / I	**Power Management Event.** (Rx74[1]=0) (1K PU to VCCS if not used)
EXTSMI#/ GPI2	W1	IOD / I	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VCCS if not used) (3.3V only)
SMBALRT#/ GPI7	T2	I / I	**SMB Alert** (System Management Bus I/O space Rx08[3] = 1). When the chip is enabled to allow it, assertion generates an IRQ or SMI or power management event. (10K PU to VCCS if not used)
THRM/ AOLGP / GPI17	P3	I / I / I	**Monitor Input - Thermal Alarm.** (F4 Rx40[7]=0) (1K PU to VCCS if not used)

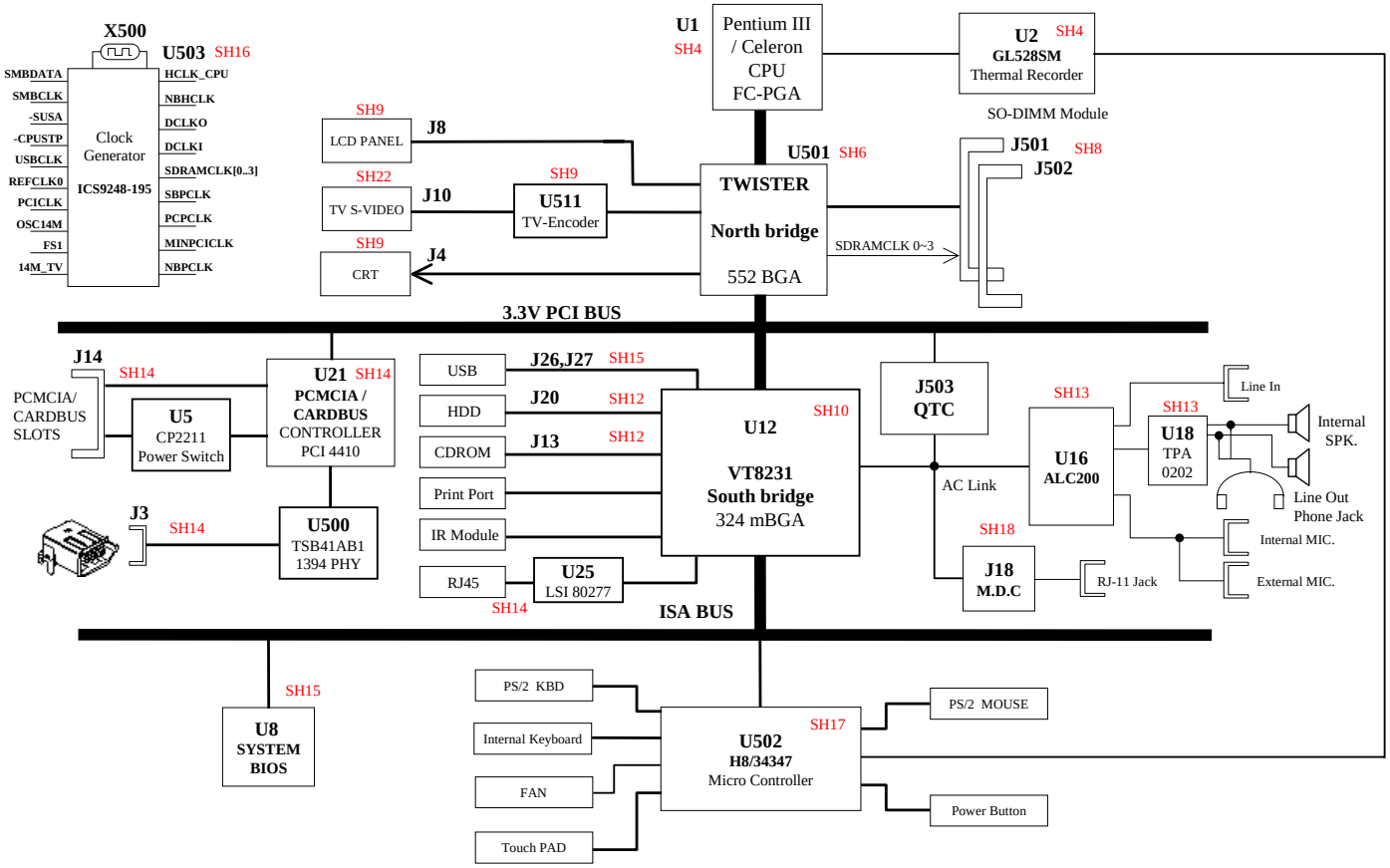
Signal Name	PIN #	I/O	Signal Description
LID/ GPI4	V2	I / I	**Monitor Input - Notebook Computer Display Lid Open / Closed.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT8231 performs a 200 usec debounce of this input if Function 4 Rx40[5] is set to 1. (10K PU to VCCS if not used)
RING#/ GPI3	U3	I / I	**Monitor Input – Modem Ring.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VCCS if not used)
BATLOW#/ GPI5	T3	I / I	**Monitor Input - Battery Low.** (10K PU to VCCS if not used)
CPUMISS/ GPI16	V1	I / I	**Monitor Input - CPU Missing.** Indicates whether the CPU is plugged in correctly.
AOLGPI/ GPI17/ THRM	P3	I / I / I	**Monitor Input - Awake On LAN External Event.** F4 Rx40[7]=1
INTRUDER#/ GPI8	F3	I / I	**Monitor Input – Chassis Intrusion.**
RSMRST#	F2	I	**Resume Reset.** Resets the internal logic connected to the VCCS power plane and also resets portions of the internal RTC logic.
SUSA#/ GPO1/ strap	P1	O / O / I	**Suspend Plane A Control** (Function 4 Rx54[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VCCS if not used)
SUSB#/ GPO2	P2	O / O	**Suspend Plane B Control** (Function 4 Rx54[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VCCS if not used)
SUSC#/ GPO	N3	O / O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.

5.3 VIA VT8231 South Bridge Controller-12

Power Management and External State Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SUSST1#/ GPO3	N5	O / O	**Suspend Status 1** (Function 4 Rx54[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VCCS.
SUSCLK/ GPO4	W2	O / O	**Suspend Clock** (Function 4 Rx55[1]=0). 32.768 KHz output clock for use by the North Bridge (e.g., Apollo MVP3 or MVP4) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VCCS.

Resets, Clocks, and Clock Control			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PWRGD	E2	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PWRBTN#	U2	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT8231 performs a 200us debounce of this input if Function 4 Rx40[5] is set to 1. (3.3V only)
SLPBTN#/ FAN2/ GPIO18	K3	I/ I/ IO	**Sleep Button** (Function 4 Rx40[6] = 0). Used by the power management subsystem to monitor an external system sleep button or switch. Connect to VCC if not used.
PCIRST#	E4	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT8231 will assert this pin during power-up or from the control register.
RTCX1	E3	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and for power-well power management logic.
RTCX2	F5	O	**RTC Crystal Output**: 32.768 KHz crystal output
OSC	T12	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
SLOWCLK / GPO0	R4	O	**Slow Clock.** Frequency selectable if PMU function 4 Rx54[1-0] is nonzero (set to 01, 10, or 11).
CPUSTP#/ GPO5	P4	O /O	**CPU Clock Stop** (Function 4 RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used. See also PMU I/O Rx2C[3].
PCISTP#/ GPO6	T4	O /O	**PCI Clock Stop** (Function 4 RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.

6. System Block Diagram



7170 N/B MAINTENANCE

7. Maintenance Diagnostic

7.1 Introduction

Every time the computer is turned on ,the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic post(378H) is written at the beginning of the test. Therefore , if the test fail, the user can determine where the problem occurs by reading the last value written to post 378H by the PIO debug board plug at PIO port.

7170 N/B MAINTENANCE

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

Phoenix BIOS Function Keys

The following are the special PhoenixBIOS function keys :

F2 Enter SETUP program during POST

Ctrl - Alt <- > Switch to slow CPU speed

Ctrl - Alt <+> Switch to fast CPU speed

The speed switching keys are only operational when speed switching is available.

POST Errors and Beep Codes

Recoverable POST Errors

Whenever a recoverable error occurs during POST, Phoenix BIOS displays an error message describing the problem.Phoenix BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero. An external ROM module (e.g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

Terminal POST Errors

There are several POST routines that issue a POST Terminal Error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters.)

7170 N/B MAINTENANCE

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

The routine derives the beep code from the test point error as follows :

1. The 8-bit error code is broken down to four 2-bit groups (Discard the most significant group if it is 00)
2. Each group is made one-based (1 through 4)by adding 1.
3. Short beeps are generated for the number in each group example :

Testpoint 01Ah = 00 01 10 10 = 1-2-3-3 beeps

Test Points and Beep Codes

At the beginning of each POST routine, the BIOS outputs the test point error code to I/O address 80h.Use this code during trouble shooting to establish at what point the system failed and what routine was being performed. Some motherboards are equipped with a seven-segment LED display that displays the current value of port 80h. For production boards which do not contain the LED display, you can purchase a card that performs the same function. If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempting to display the error code on upper left corner of the screen and on the port 80h LED display. It attempts repeatedly to write the error to the screen. This may cause "hash" on some CGA displays. If the system hangs before the BIOS can process the error, the value displayed at the last test performed. In this case, the screen does not display the error code. The following is a list of the checkpoint codes written at the start of each test and the beep codes issued for terminal errors. Unless otherwise noted, these codes are valid for PhoenixBIOS 4.0 Release 6.0.

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

CODE	Beeps	POST Routine Description
02h		Verify Real Mode
03h		Disable Non-Maskable Interrupt (NMI)
04h		Get CPU type
06h		Initialize system hardware
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Initialize CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize the local bus IDE
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard controller
24h		Set ES segment register to 4 GB
26h		Enable A20 line
28h		Auto size DRAM

CODE	Beeps	POST Routine Description
29h		Initialize POST Memory Manager
2Ah		Clear 512 KB base RAM
2Ch	1-3-4-1	RAM failure on address line xxxx*
2Eh	1-3-4-3	RAM failure on data bits xxxx* of low byte of memory bus.
2Fh		Enable cache before system BIOS shadow
30h	1-4-1-1	RAM failure on data bits xxxx* of high byte of memory bus.
32h		Test CPU bus-clock frequency
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate **Register with CMOS Values**
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
48h		Check video configuration against CMOS
49h		Initialize PCI bus and device
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
50h		Display CPU type and speed
51h		Initialize EISA board

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

CODE	Beeps	POST Routine Description
52h		Test keyboard
54h		Set key click if enabled
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Display CPU cache
5Ch		Test RAM between 512 and 640 KB
60h		Test extended memory
62h		Test extended memory address lines
64h		Jump to User Patch1
66h		Configure advanced cache registers
67h		Initialize Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display shadow-area message
6Eh		Display possible high address for NMB recovery
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialization
82h		Detect and install external RS232 posts

CODE	Beeps	POST Routine Description
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports
87h		Configure Motherboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Initialize local-bus hard-disk controllers
92h		Jump to User Patch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Search for option ROMs. One long, two short beeps on checksum failure
99h		Check for SMART Drive (optional)
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

CODE	Beeps	POST Routine Description
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Sean for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B2h		POST done-prepare to boot operating system
B4h	1	One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B9h		Prepare Boot
BAh		Initialize DMI parameters
BBh		Initialize PnP Option ROMs
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and back up reminders
C0h		Try to boot with INT 19
C1h		Initialize POST Error Manager (PEM)
C2h		Initialize error logging
C3h		Initialize error display function
C4h		Initialize system error handler
C5h		PnPnd dual CMOS (optional)

CODE	Beeps	POST Routine Description
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
D2h		Unknown interrupt
		The following are for boot block in Flash
E0h		Initialize the chipset
E1h		Initialize the bridge
E2h		Initialize the CPU
E3h		Initialize system timer
E4h		Initialize system I/O
E5h		Check force recovery boot
E6h		Checksum BIOS ROM
E7h		Go to BIOS
E8h		Set Huge Segment
E9h		Initialize Multi Processor
EAh		Initialize OEM special code
EBh		Initialize PCI and DMA
ECh		Initialize Memory type
EDh		Initialize Memory size
EEh		Shadow Boot Block
EFh		System memory test
F0h		Initialize interrupt vectors
F1h		Initialize Run Time Clock
F2h		Initialize video
F3h		Initialize System Management Manager

7. Maintenance Diagnostic

7.2 Error codes : Following is a list of error codes in sequent display on the PIO debug board.

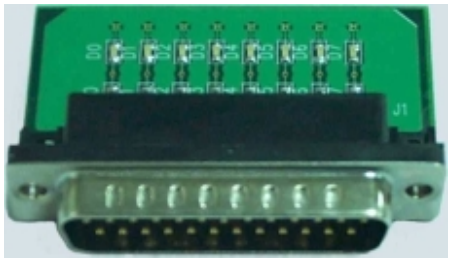
CODE	Beeps	POST Routine Description
F4h		Output one beep
F5h		Boot to Mini DOS
F6h		Clear Huge Segment
F7h		Boot to Full Dos

* If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays and additional word-bitmap (xxxx) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E1020" mean data bits12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32-bit bus. The BIOS also sends the bitmap to the port-80 LED display. It fist displays the check point code, followed by a delay, the high-order byte, anther delay, and then the low-order byte of the error. It repeats this sequence continuously.

7. Maintenance Diagnostic

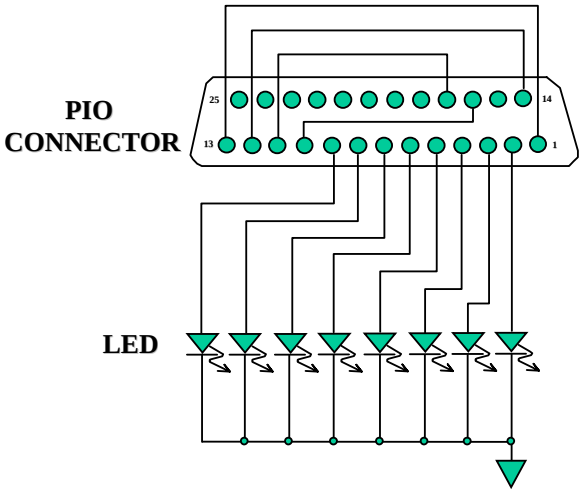
7.3 Diagnostic Tools :

- **LED * 8** OR
- **PIO CONNECTOR * 1**



P/N:411904800001
DESCRIPTION :PWA;PWA-378PORT DEBUG BD
Note:Order it from MIC/TSSC

7.4 CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

7170 N/B MAINTENANCE

8. Trouble Shooting

8.1 No Power

8.2 No Display

8.3 VGA Controller Failure

8.4 Memory Test Error

8.5 Keyboard(K/B) , Touch-pad(T/P) , ESB Test Error

8.6 CD-ROM Drive Test Error

8.7 Hard Drive Test Error

8.8 USB Port Test Error

8.9 PIO Port Test Error

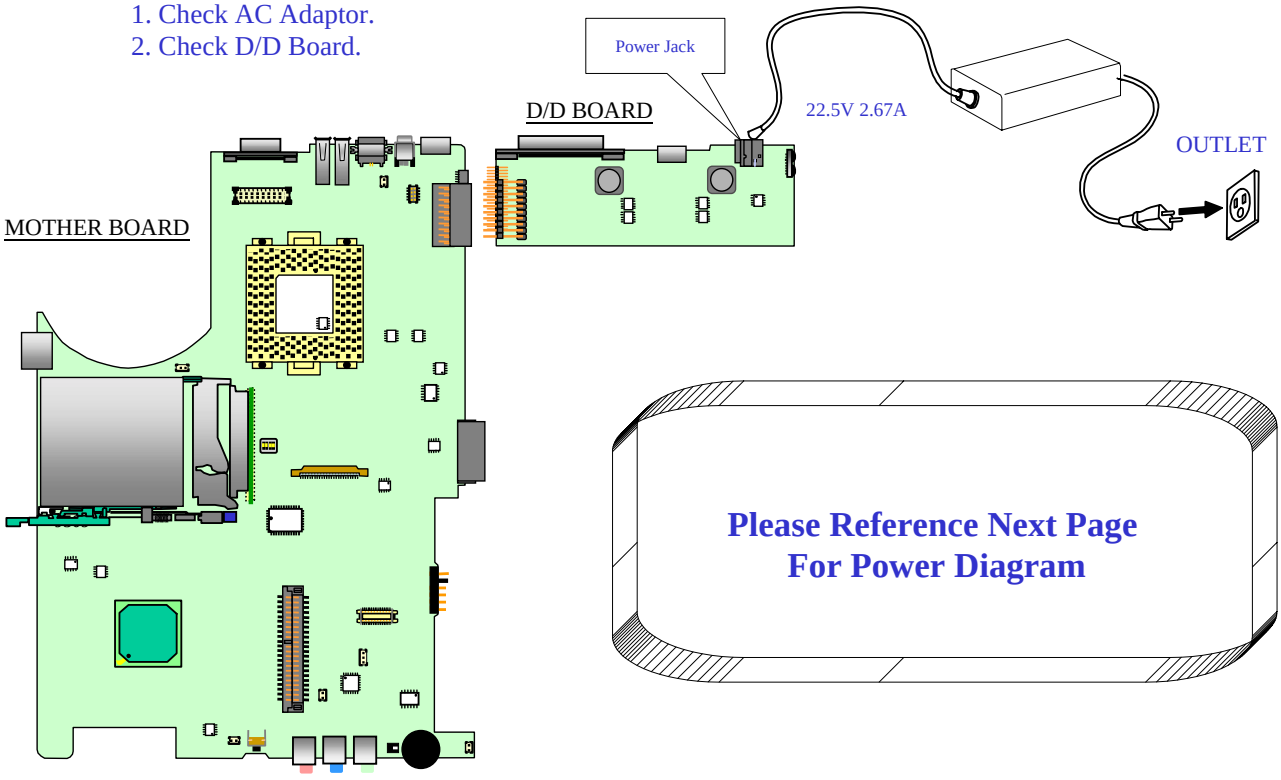
8.10 Audio Failure

7170 N/B MAINTENANCE

8.1 No Power:

When the power button is pressed, nothing happens ,power indicator does not light up.

1. Check AC Adaptor.
2. Check D/D Board.



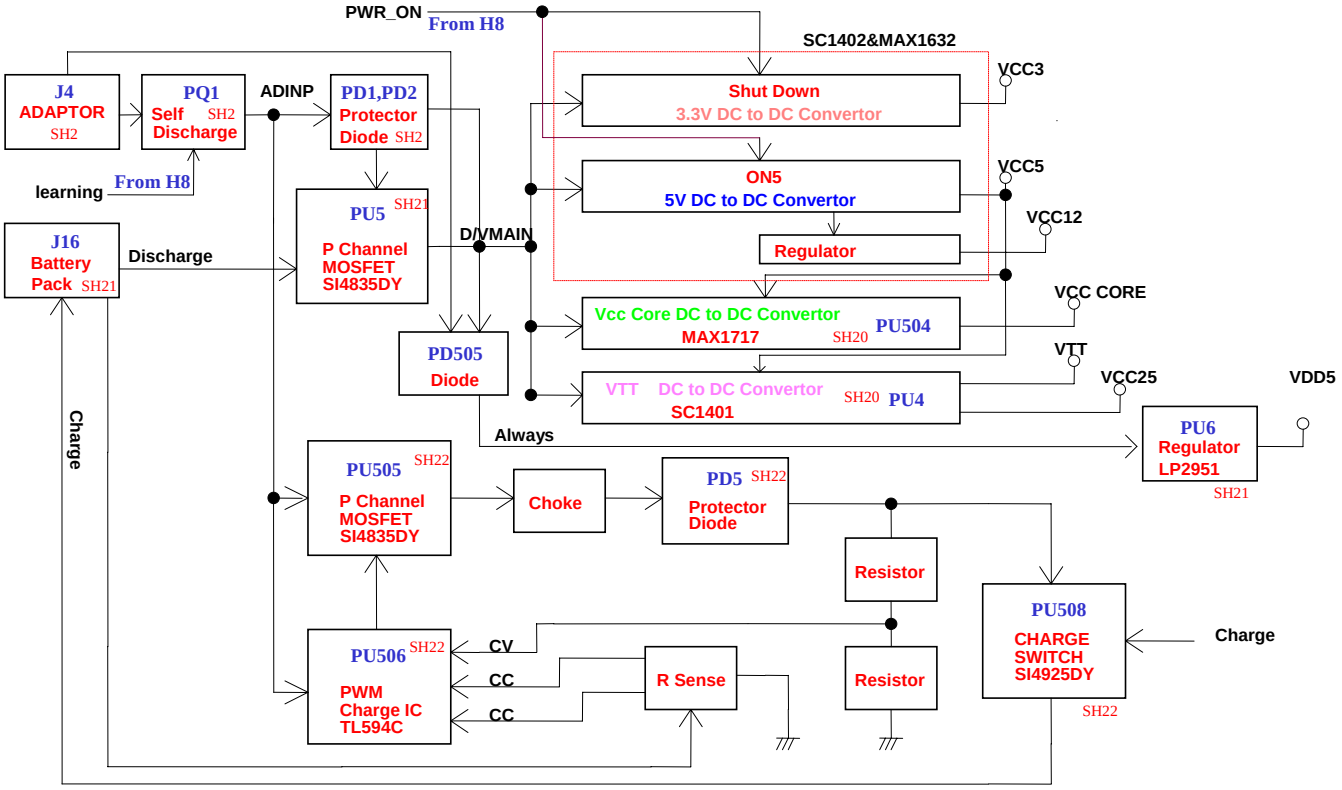
Please Reference Next Page For Power Diagram

7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

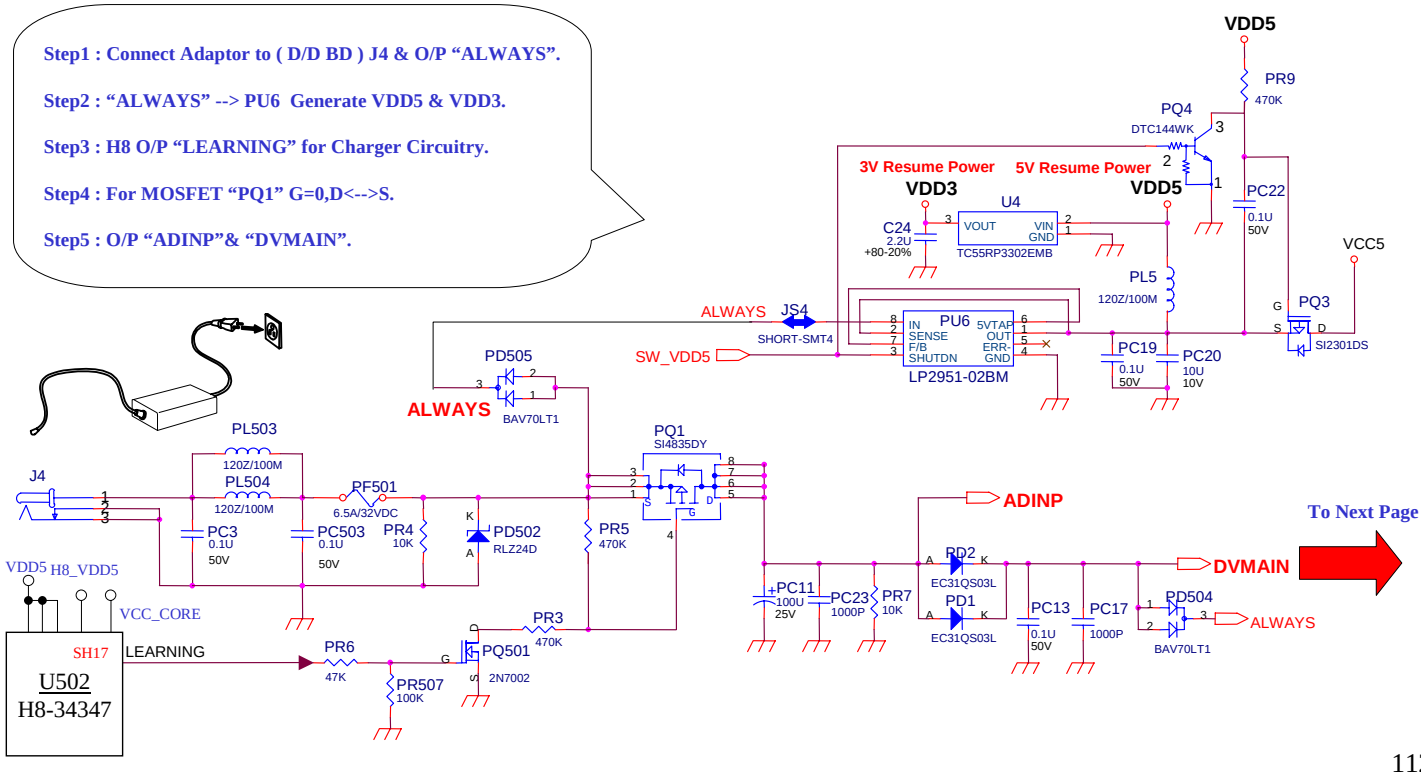
Step1 : Connect Adaptor to (D/D BD) J4 & O/P "ALWAYS".

Step2 : "ALWAYS" --> PU6 Generate VDD5 & VDD3.

Step3 : H8 O/P "LEARNING" for Charger Circuitry.

Step4 : For MOSFET "PQ1" G=0,D<-->S.

Step5 : O/P "ADINP"& "DVMAIN".

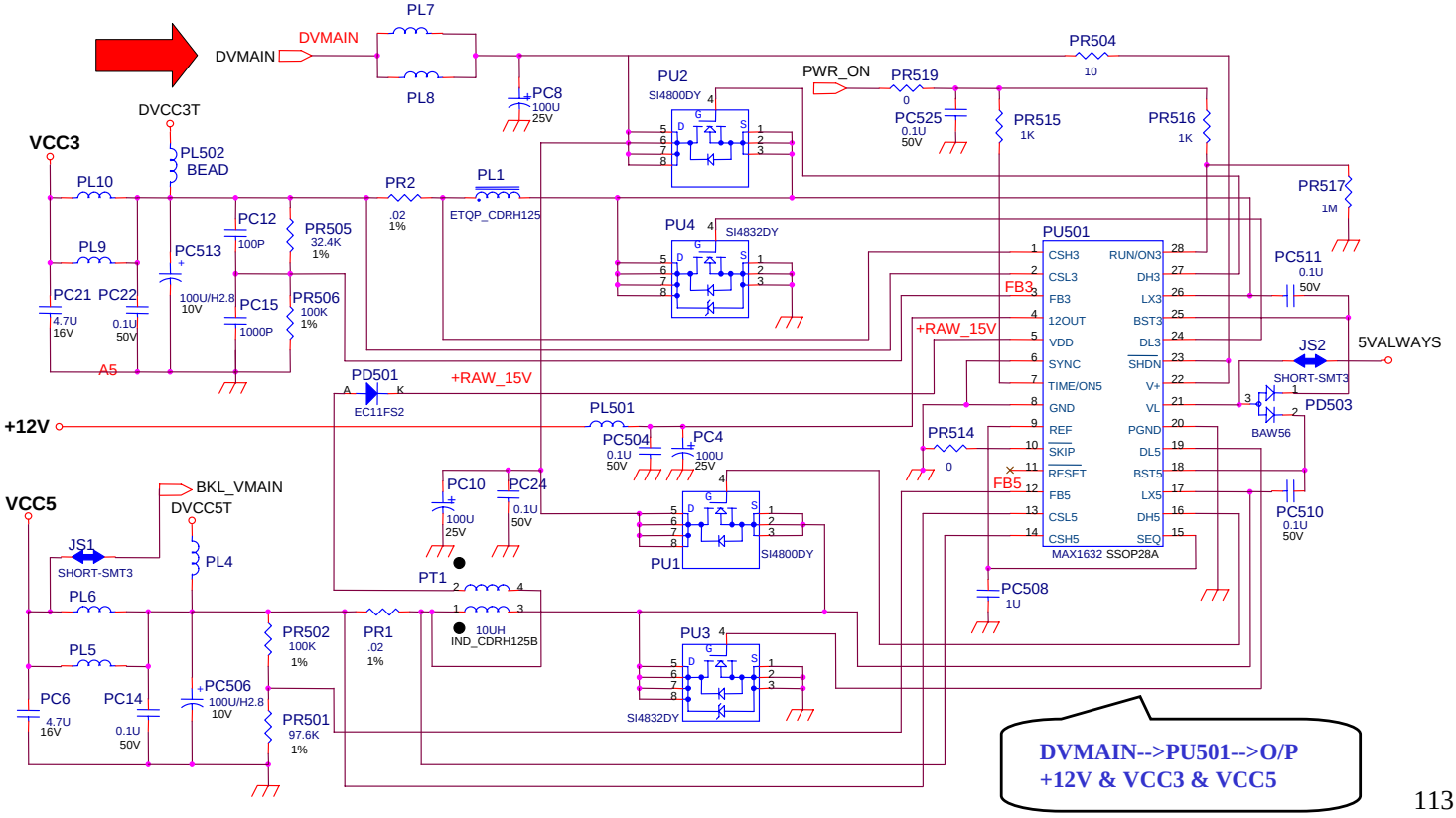


7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



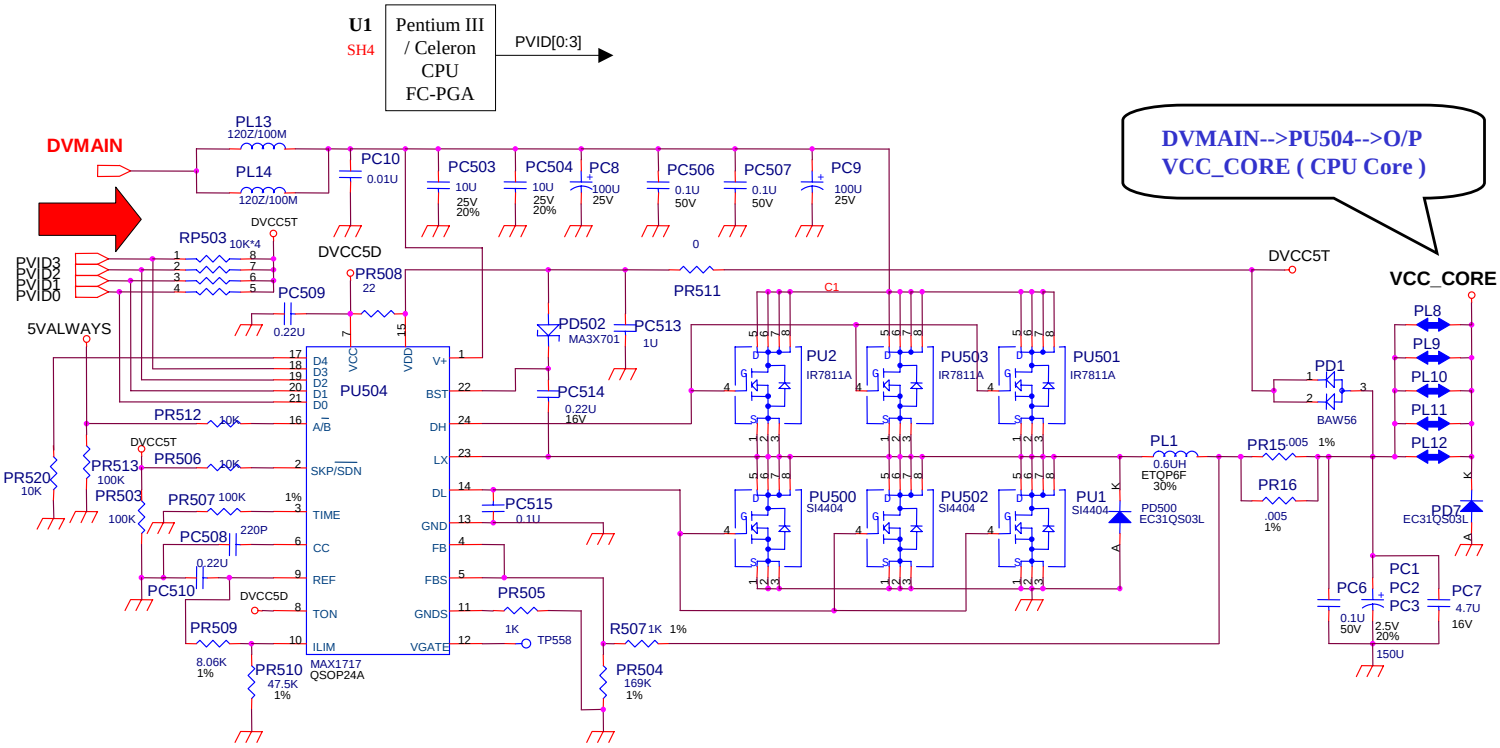
DVMAIN-->PU501-->O/P
+12V & VCC3 & VCC5

7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

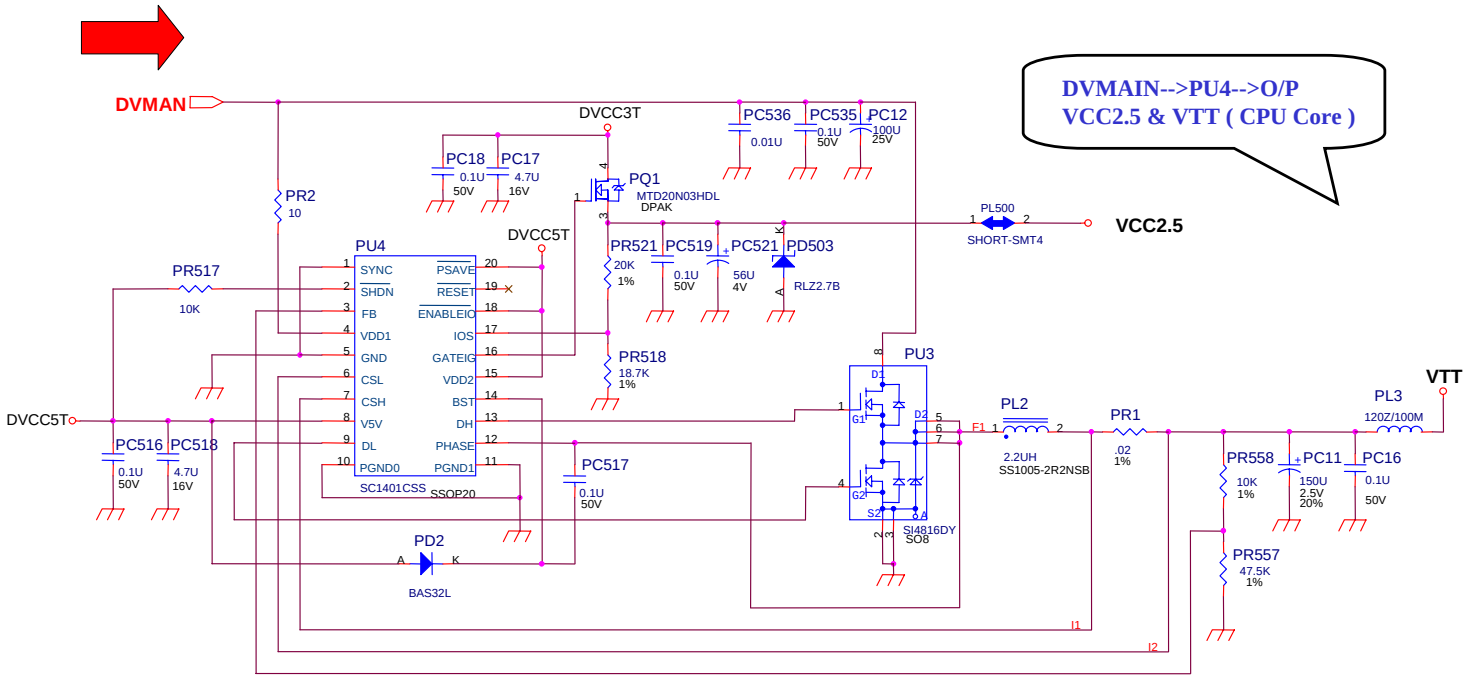


7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

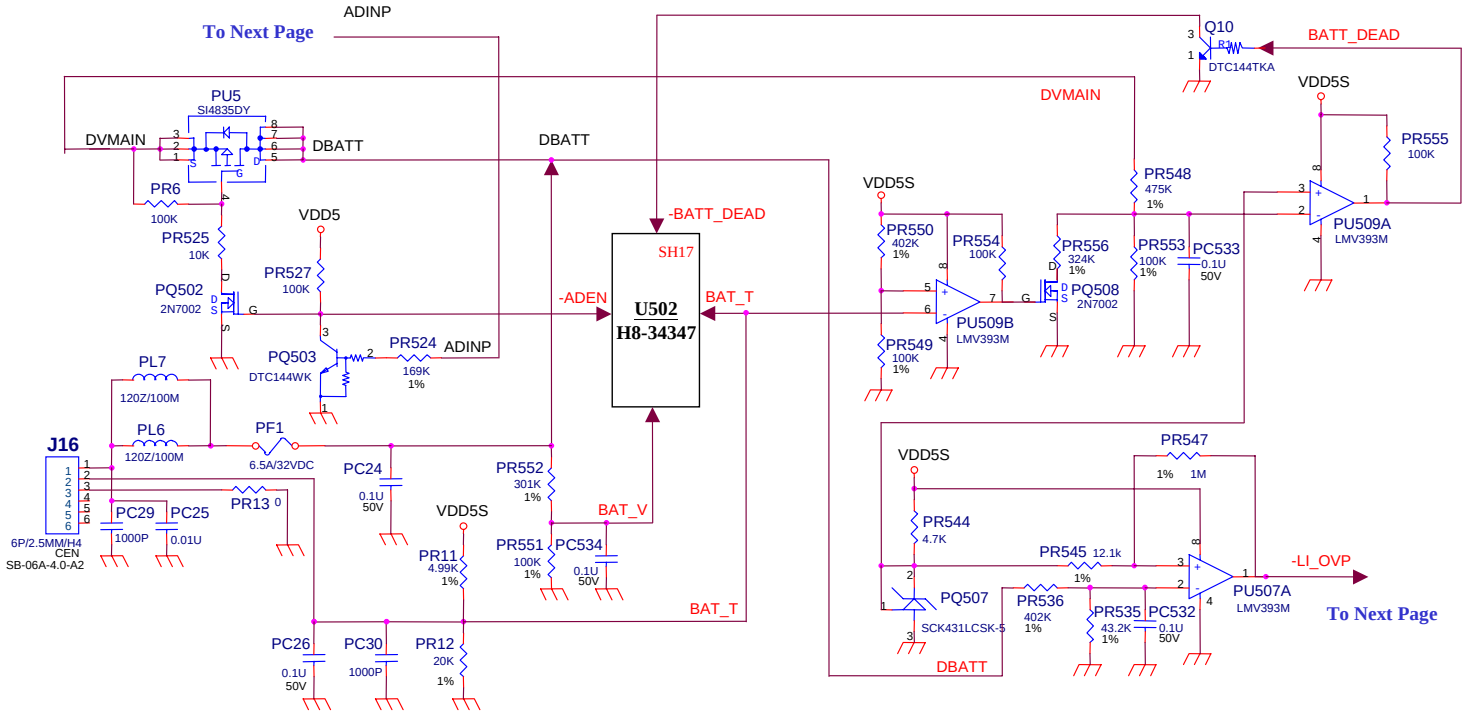


7170 N/B MAINTENANCE

8.1 No Power:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

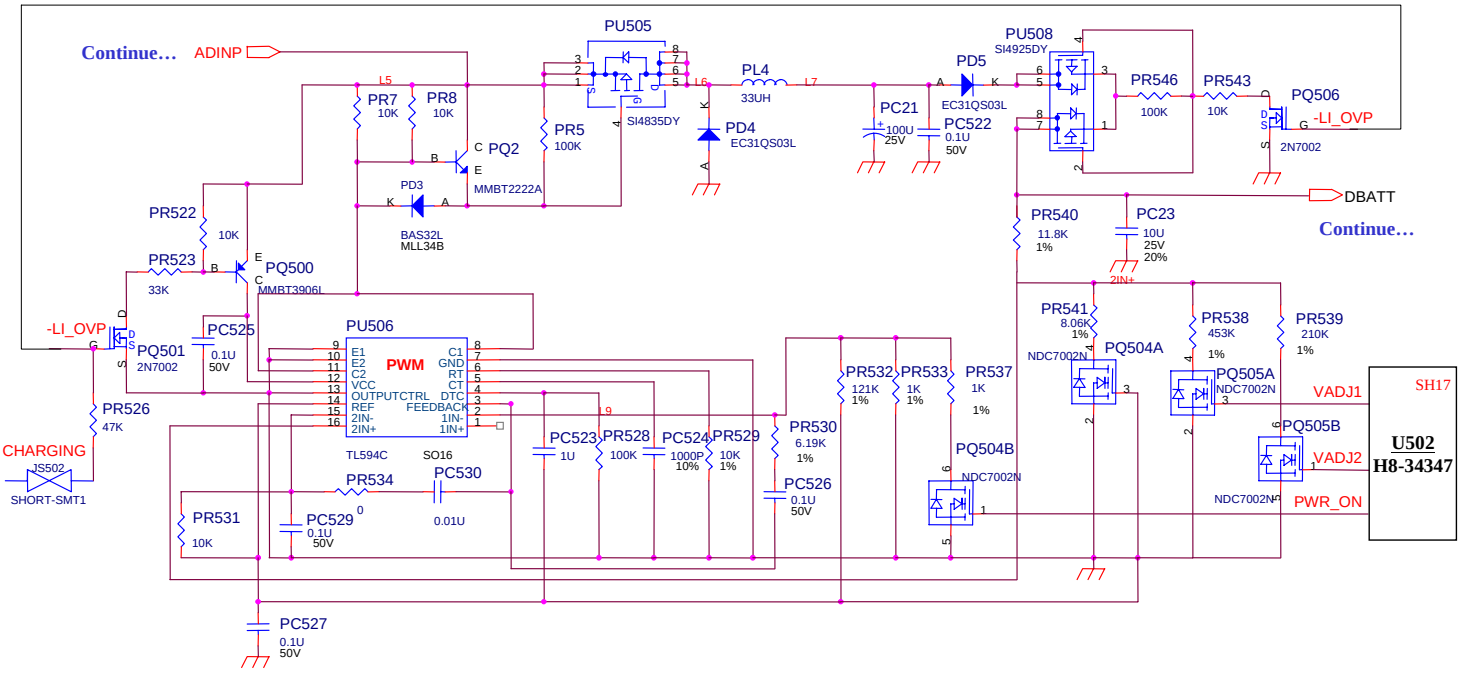


7170 N/B MAINTENANCE

8.1 No Power:

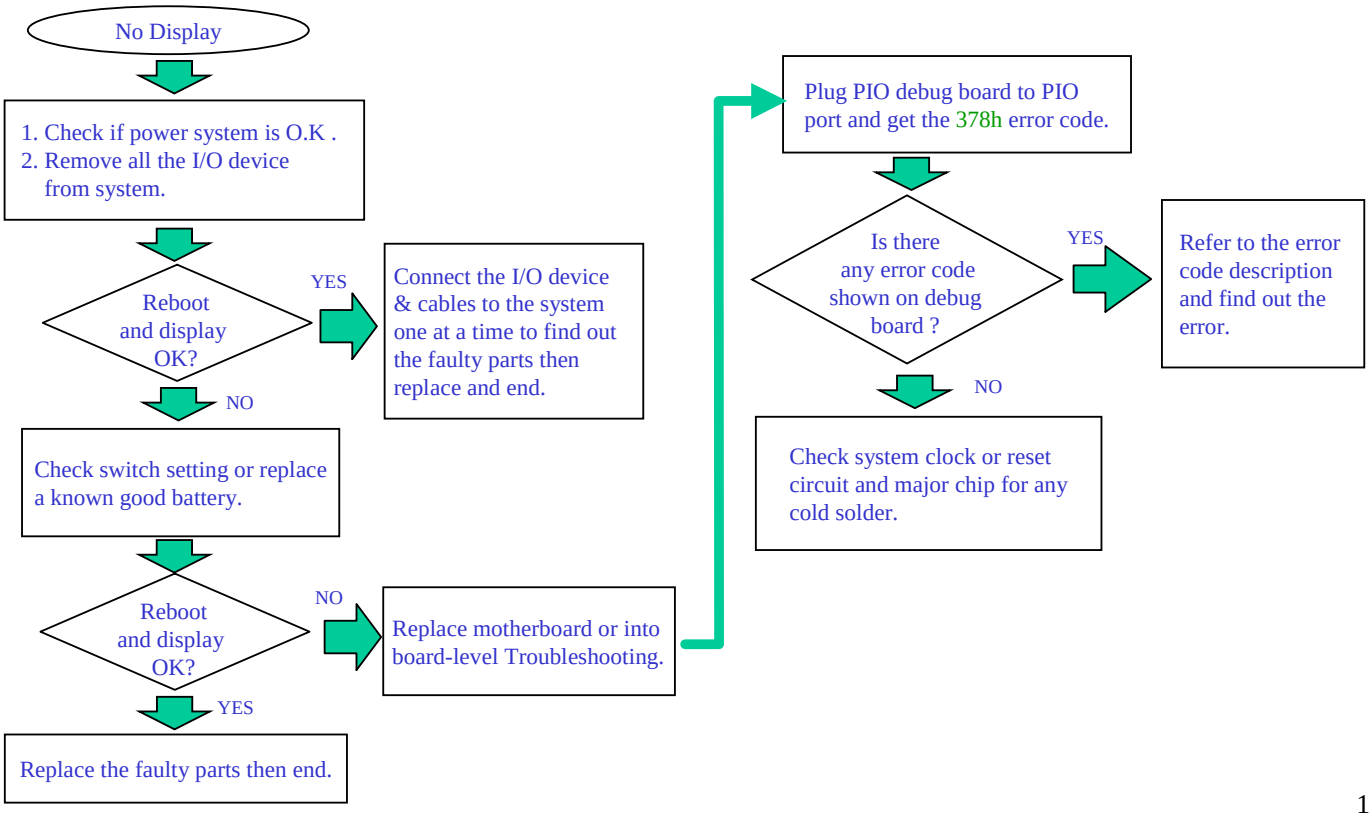
Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



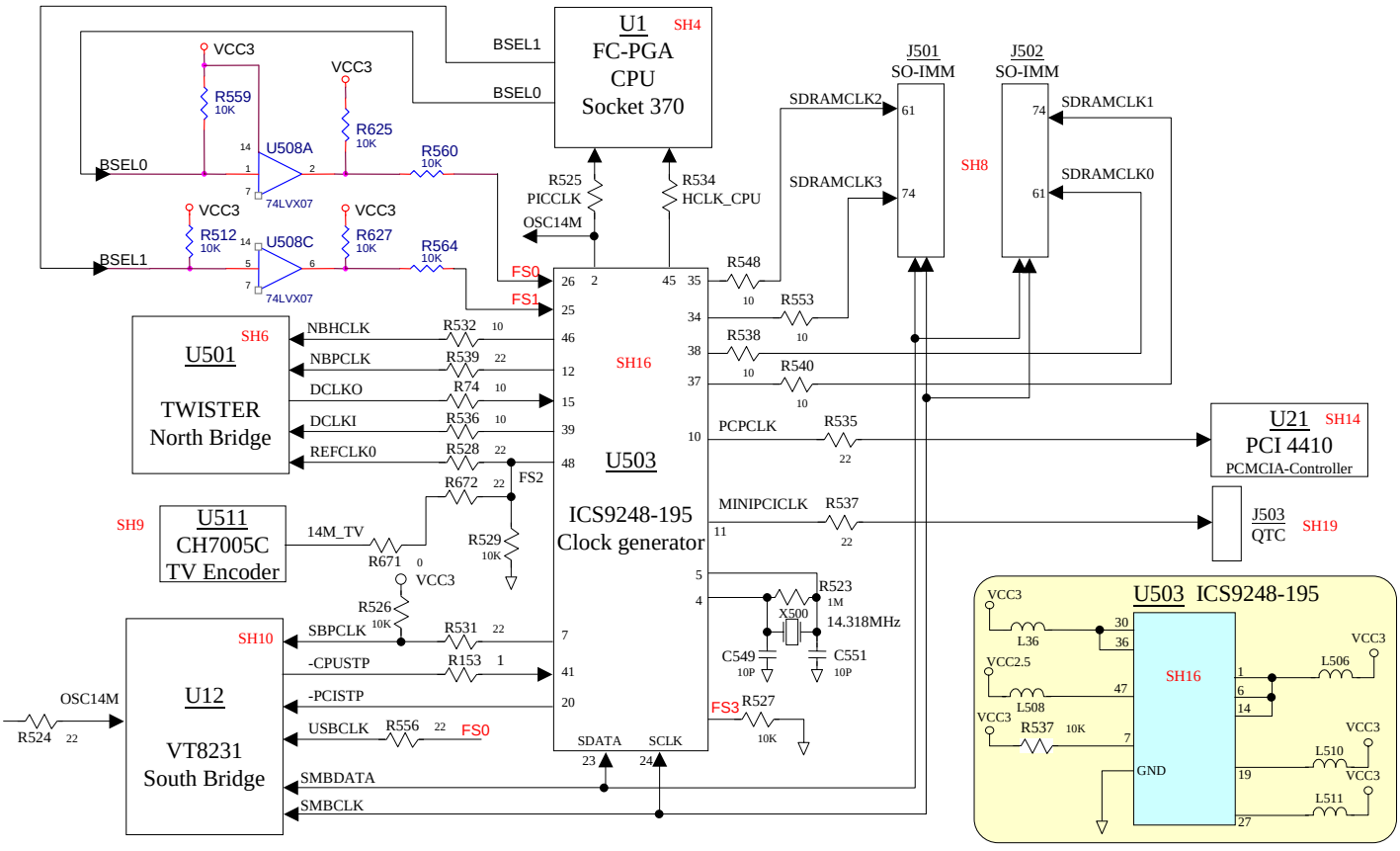
8.2 No Display

There is no display on both LCD and monitor

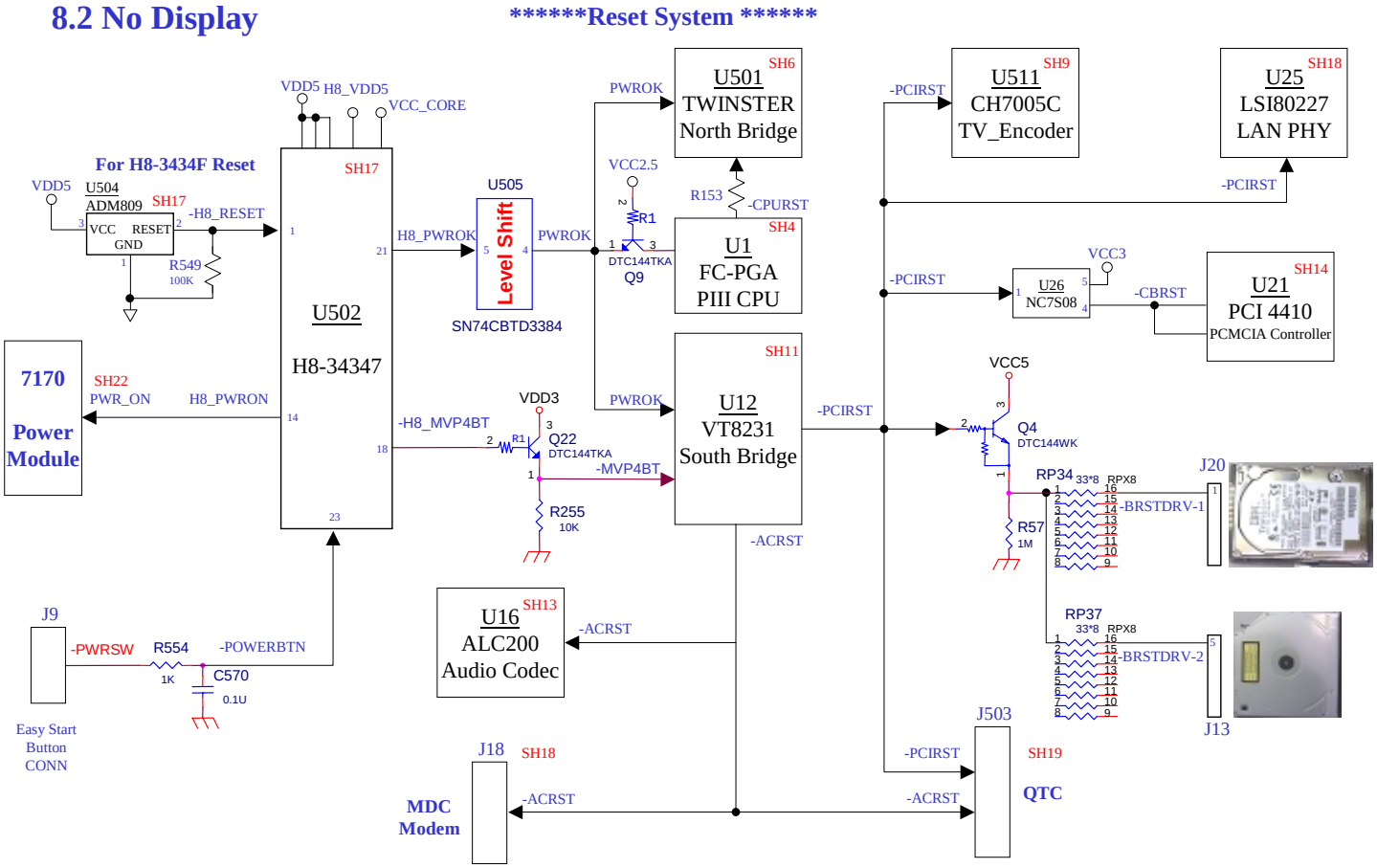


8.2 No Display

********System Clock Check ********

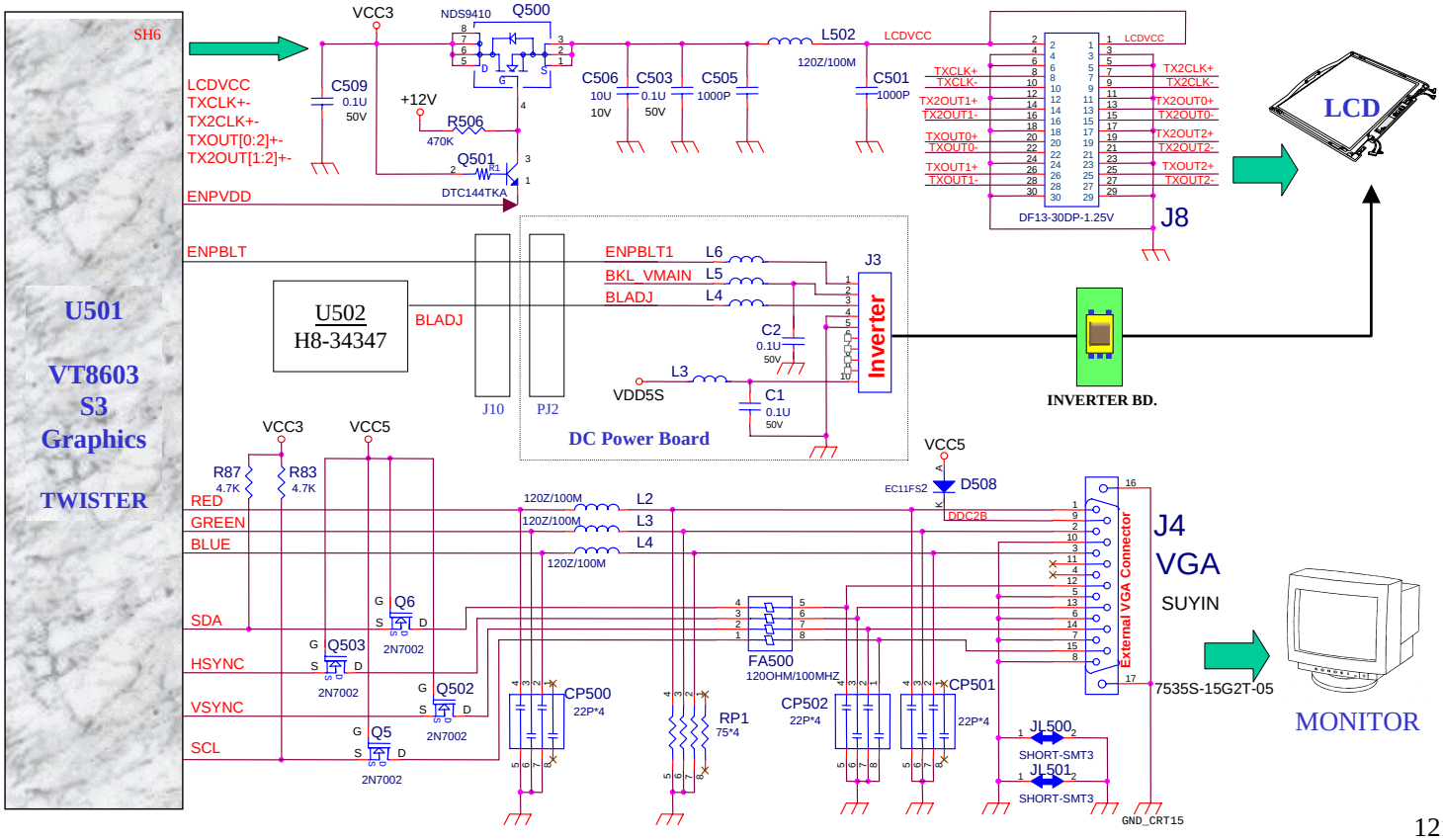


8.2 No Display



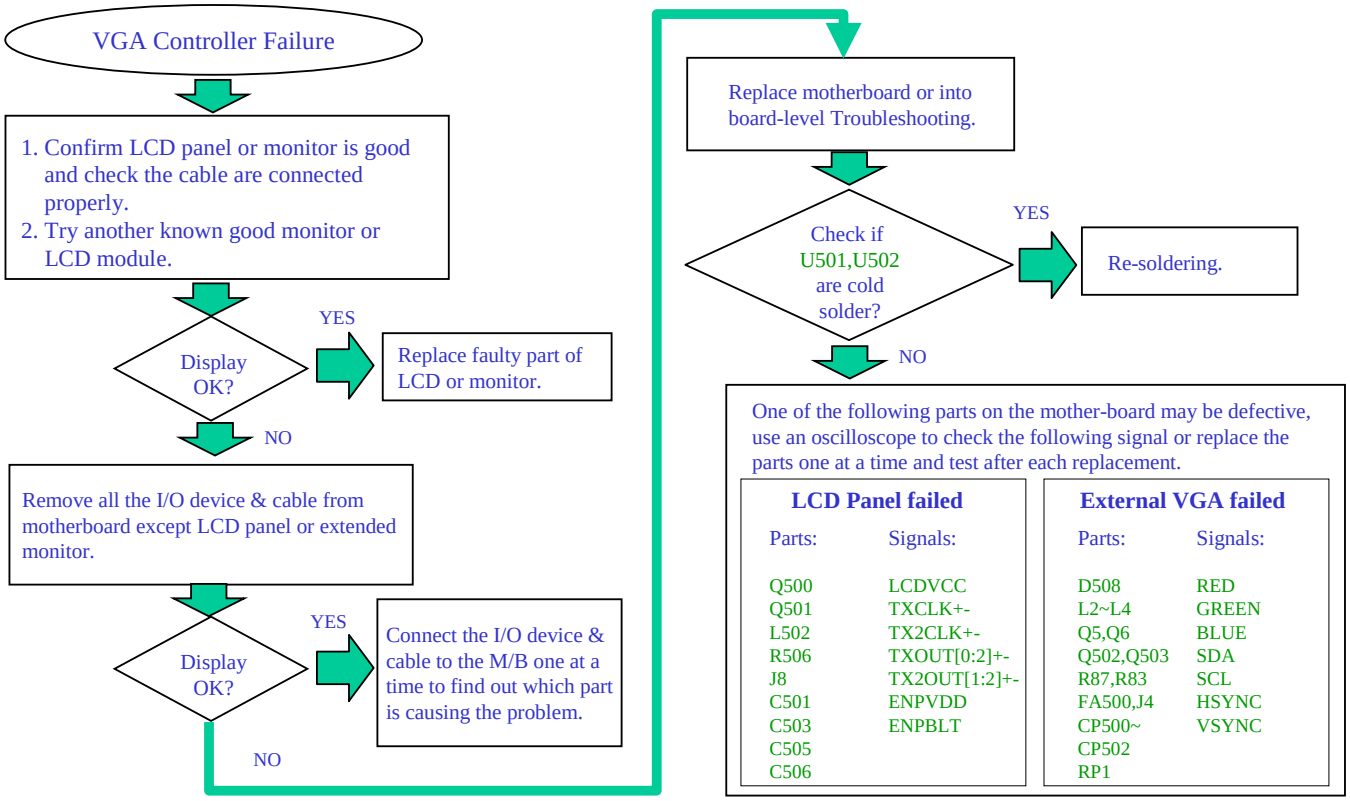
8.3 VGA Controller Failure

There is no display or picture abnormal on LCD or monitor.



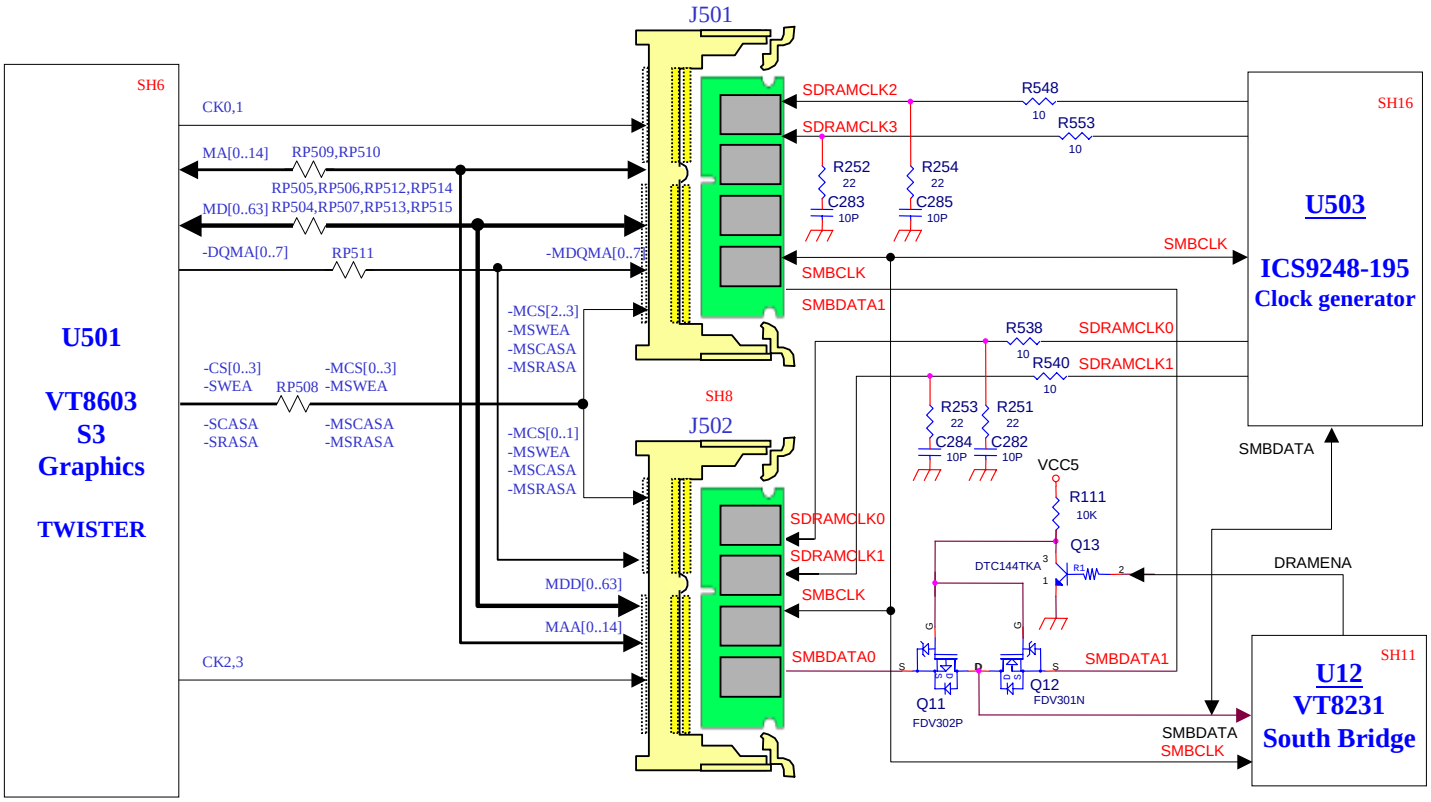
8.3 VGA Controller Failure

There is no display or picture abnormal on LCD or monitor.



8.4 Memory Test Error

Either one or two extend SO-DIMM RAM Module is failure or system hangs up.



8.4 Memory Test Error

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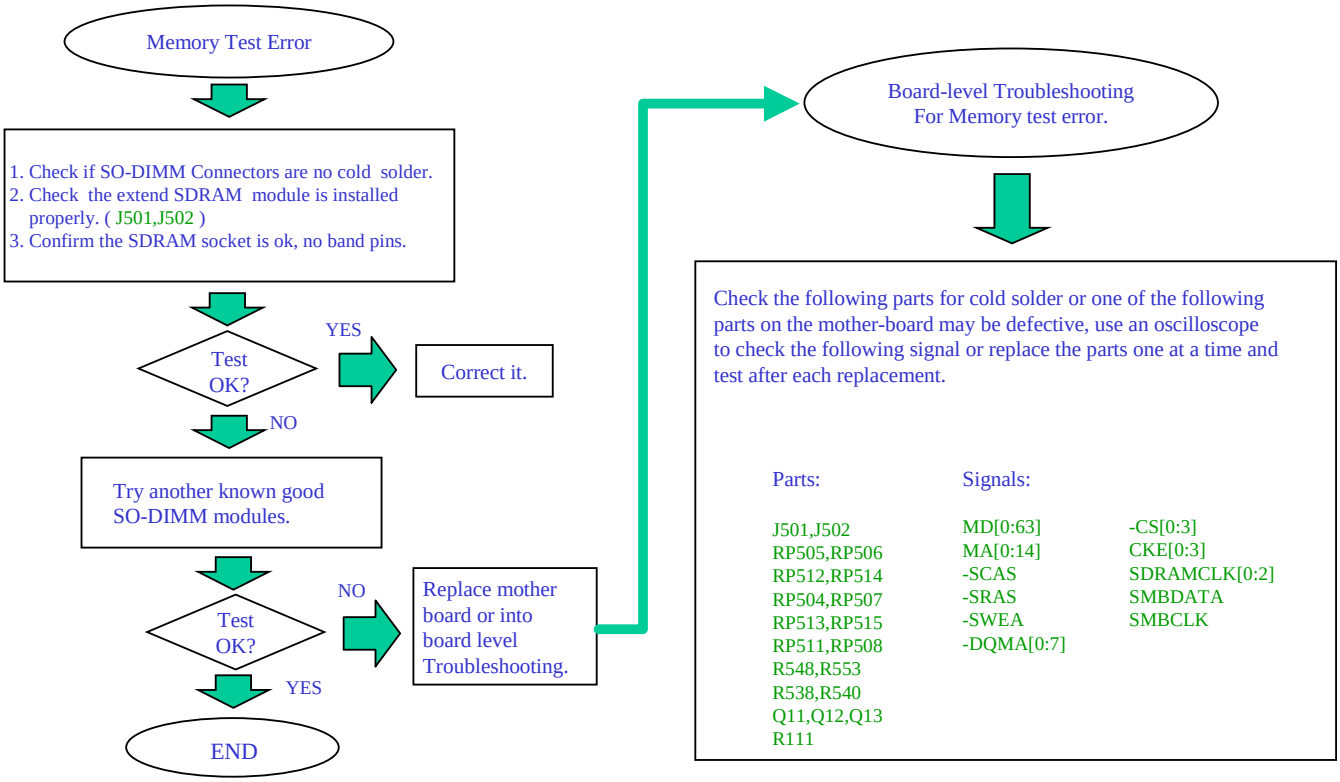
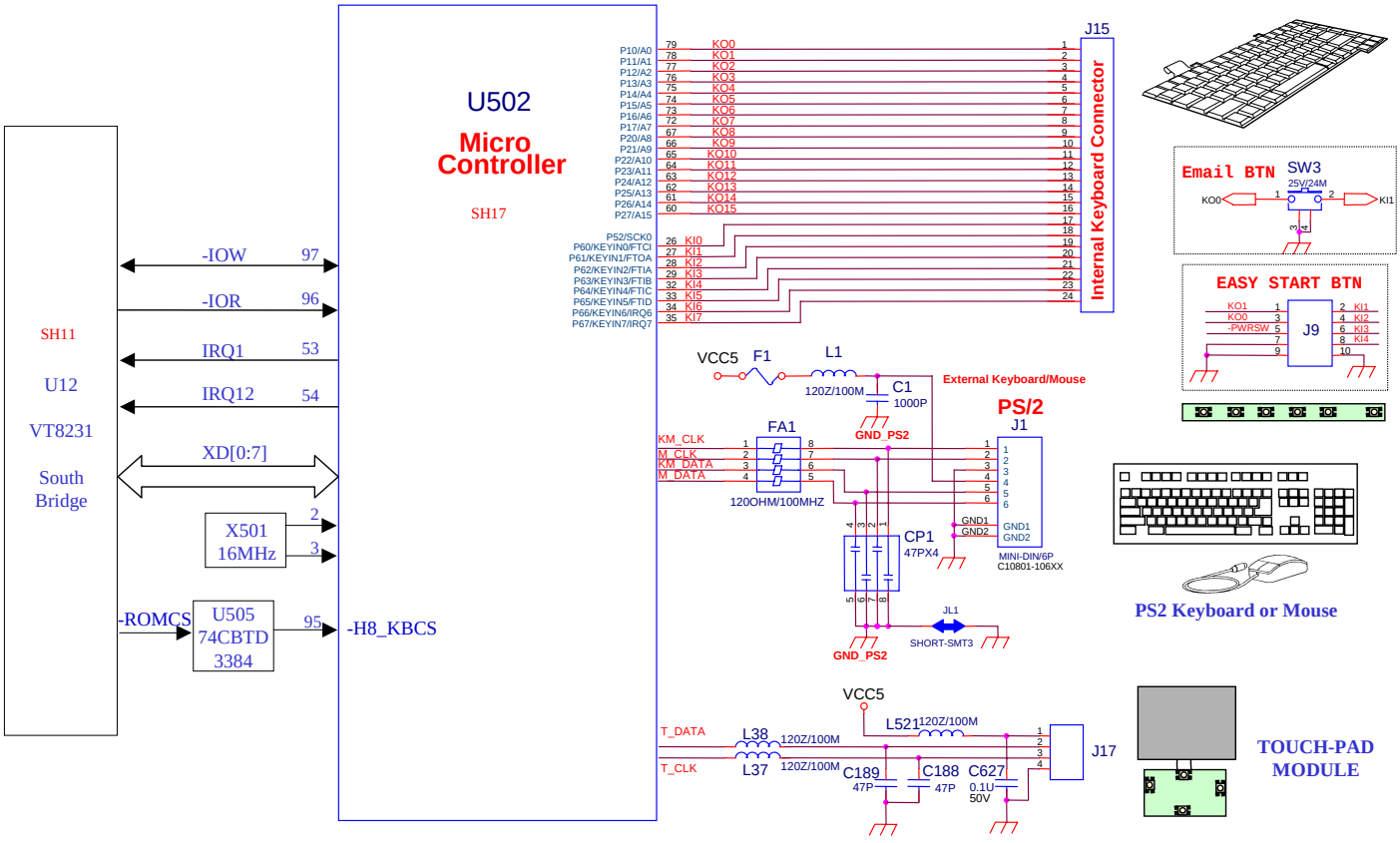


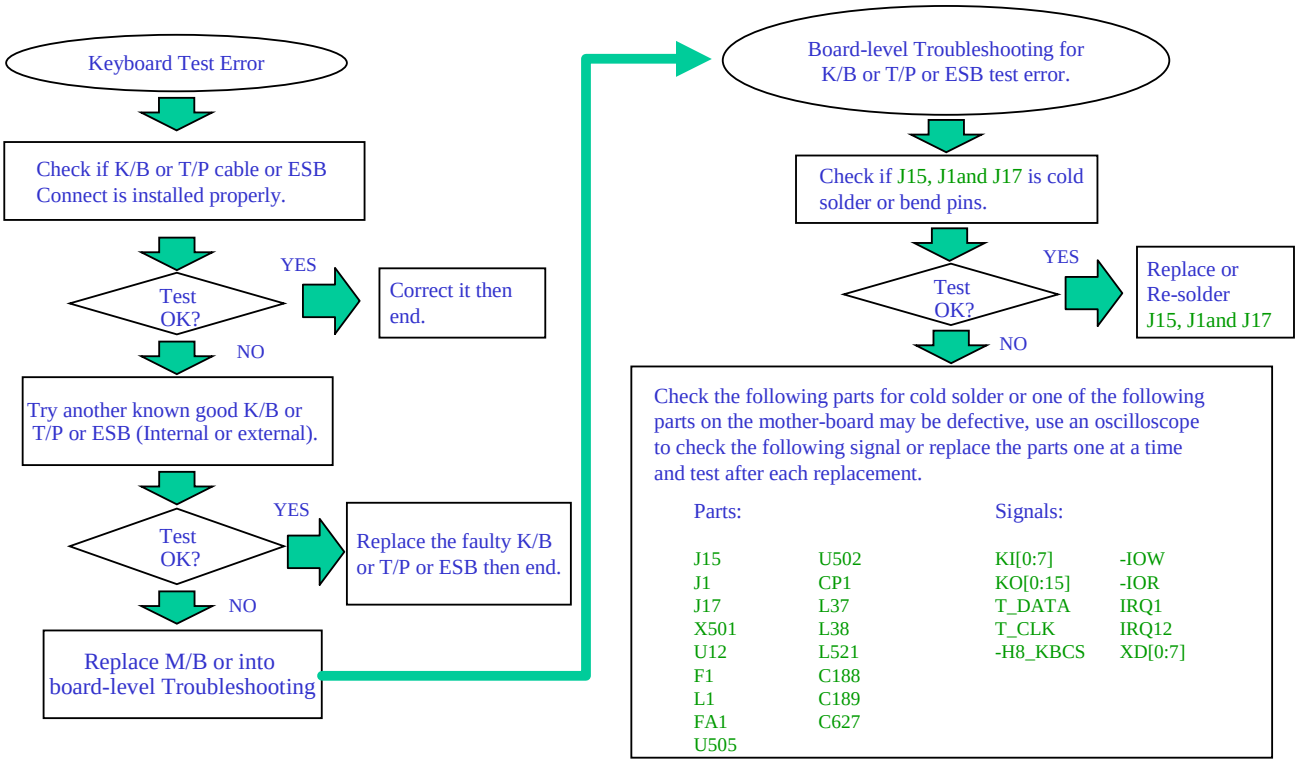
8.5 Keyboard(K/B) , Touch-pad(T/P) , ESB Test Error

Error message of keyboard failure is shown or any key doesn't work.



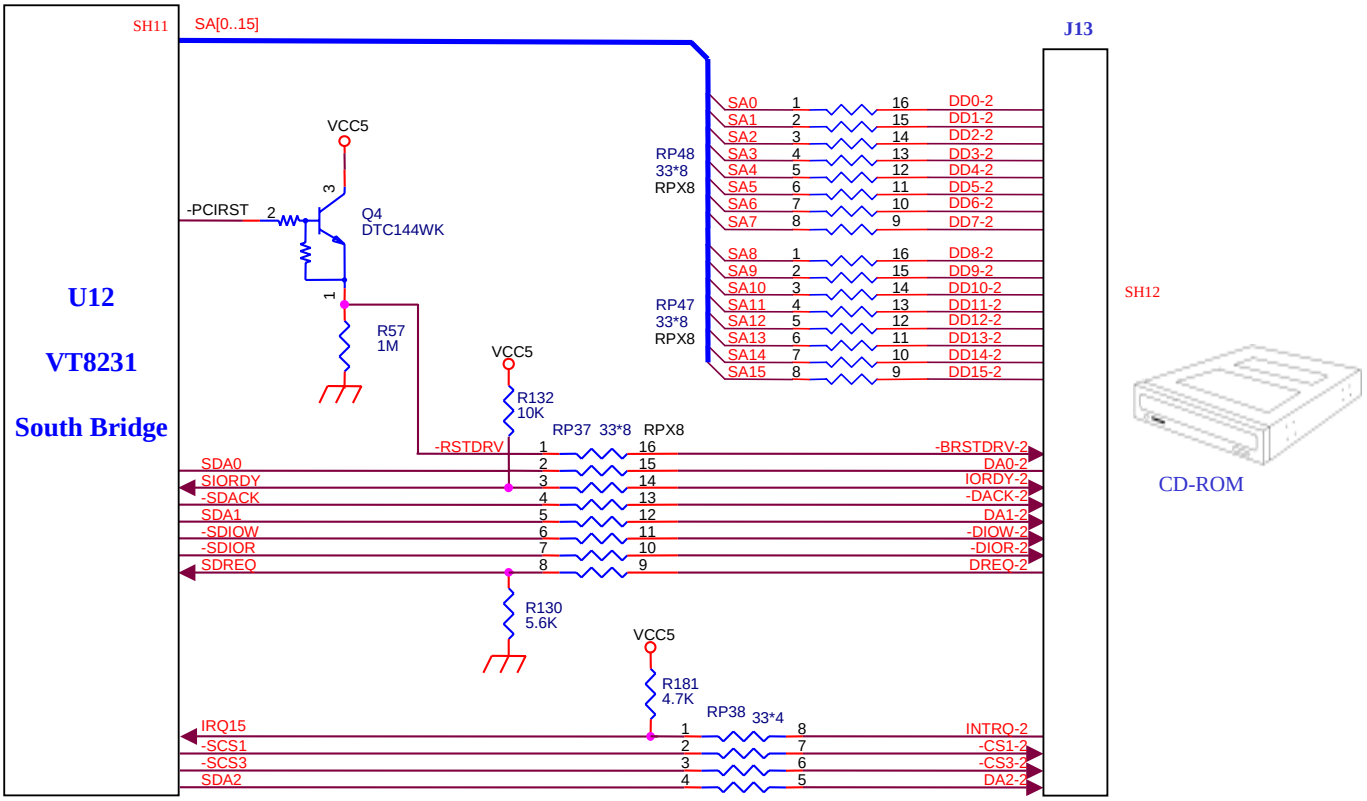
8.5 Keyboard(K/B) , Touch-pad(T/P) , ESB Test Error

Error message of keyboard or touch pad failure is shown or any key doesn't work.



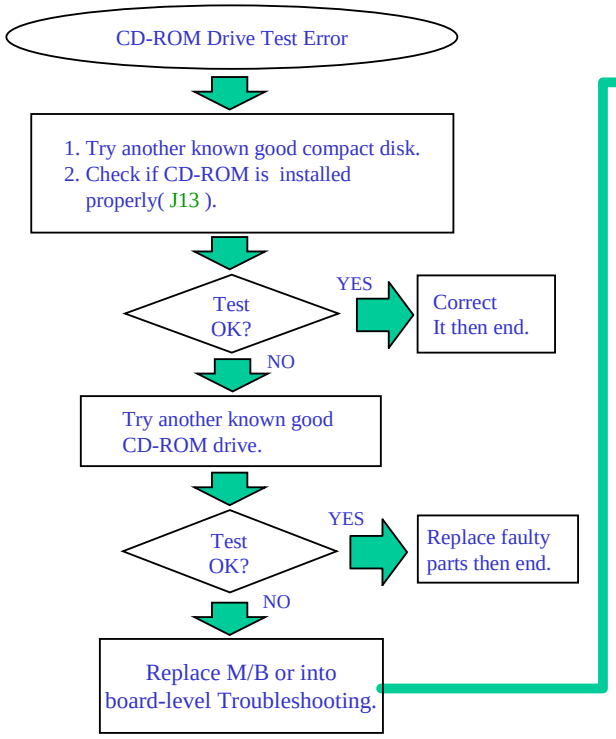
8.6 CD-ROM Drive Test Error

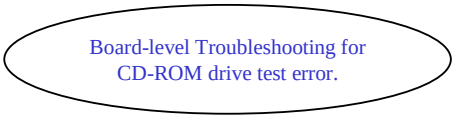
An error message is shown when reading data from CD-ROM drive.



8.6 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



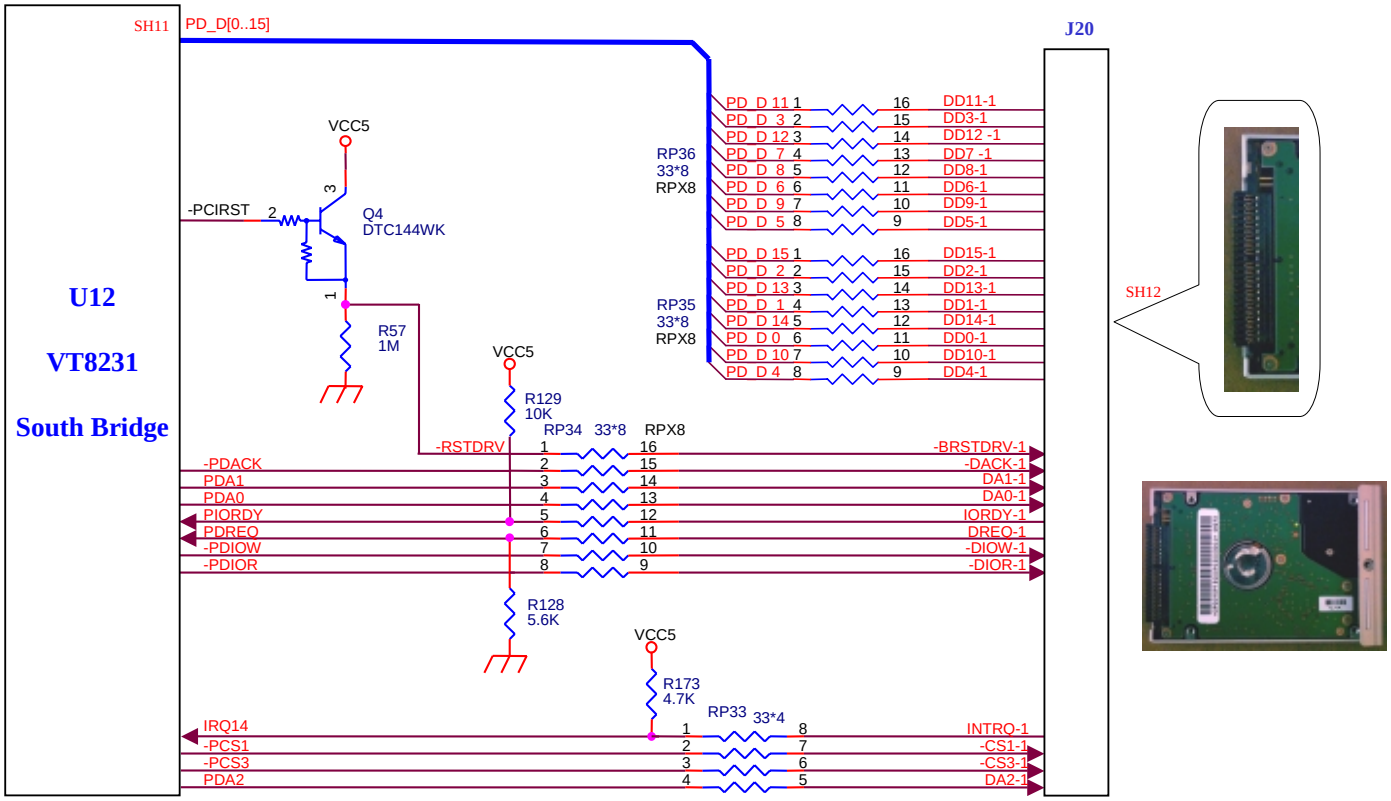


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U12, J13	SA[0~15]	-BRSTDRV-2
Q4, R57	-PCIRST	DA[0:2]-2
R132 ,R181	SDA[0:2]	IORDY-2
RP47, RP48	SIORDY	-DACK-2
RP37, RP38	-SDACK	-DIOW-2
R130	-SDIOW	-DIOR-2
	-SDIOR	DREQ-2
	SDREQ	INTRQ-2
	IRQ15	-CS1-2
	-SCS1	-CS3-2
	-SCS3	DA2-2

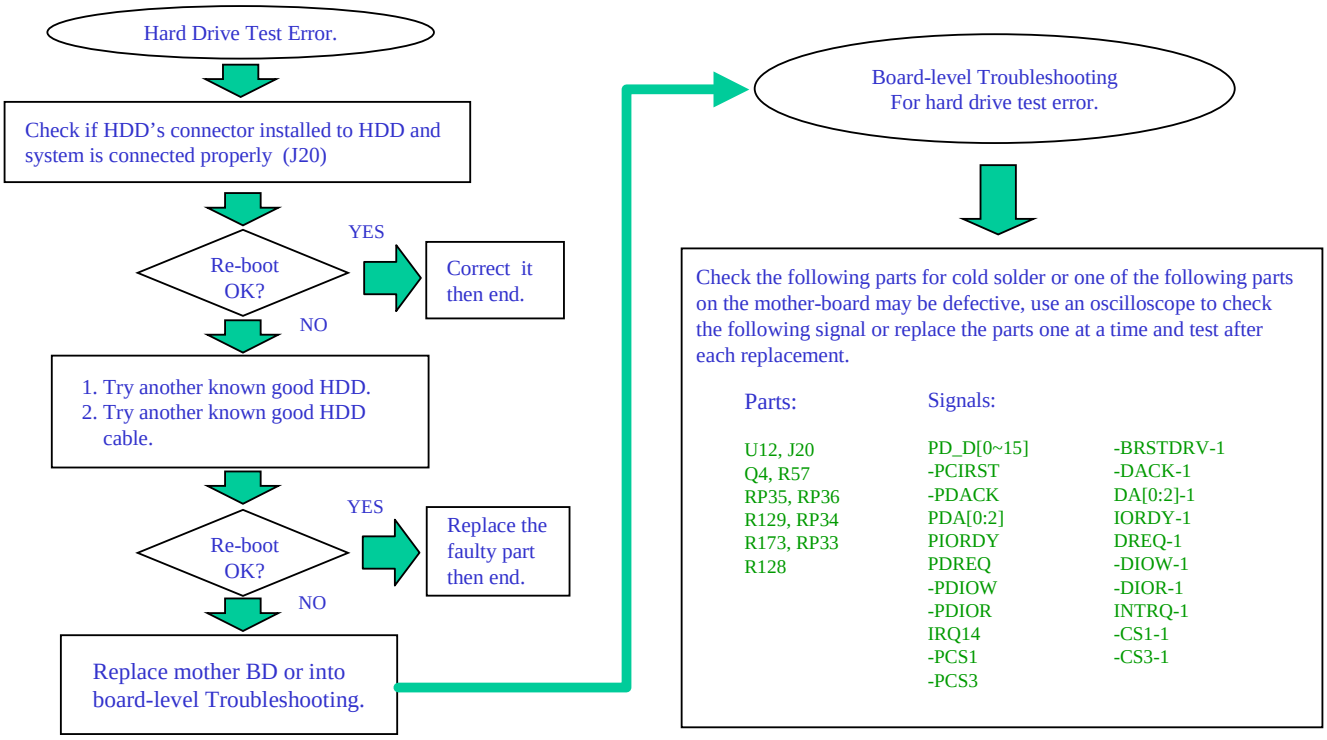
8.7 Hard Drive Test Error

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



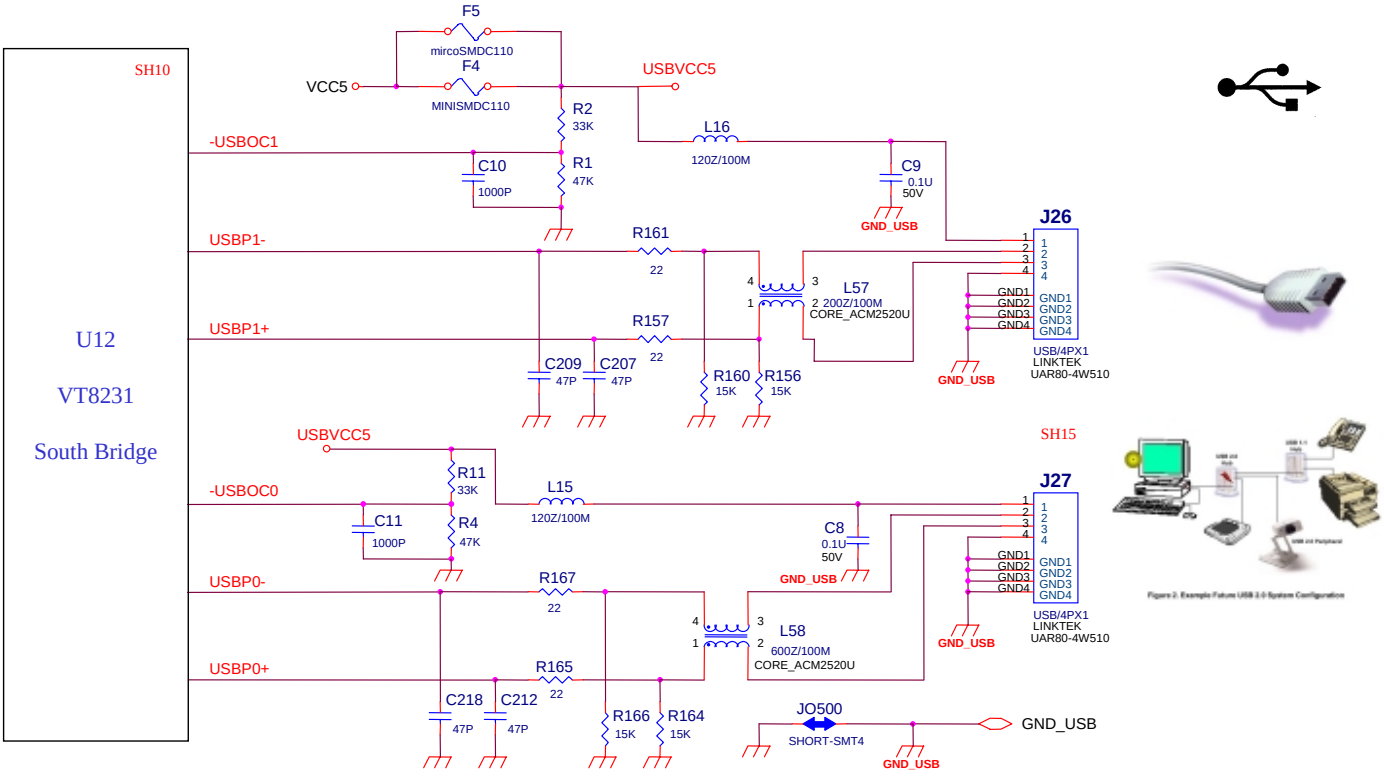
8.7 Hard Drive Test Error

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



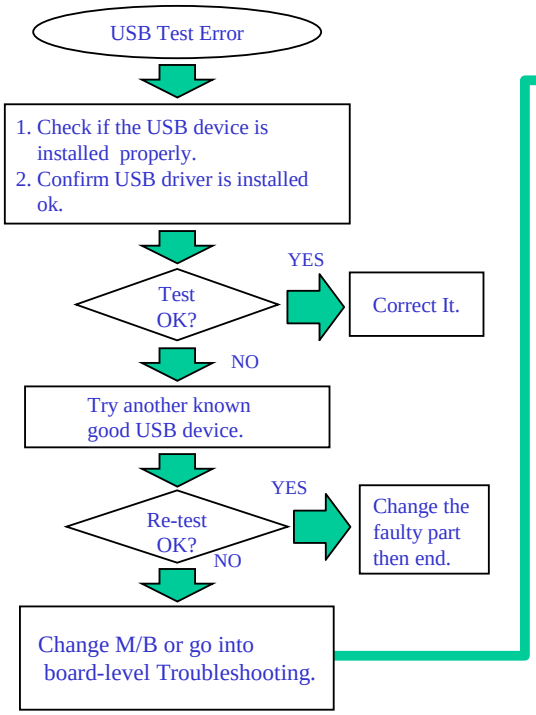
8.8 USB Port Test Error

An error occurs when a USB I/O device is installed.



8.8 USB Port Test Error

An error occurs when a USB I/O device is installed.



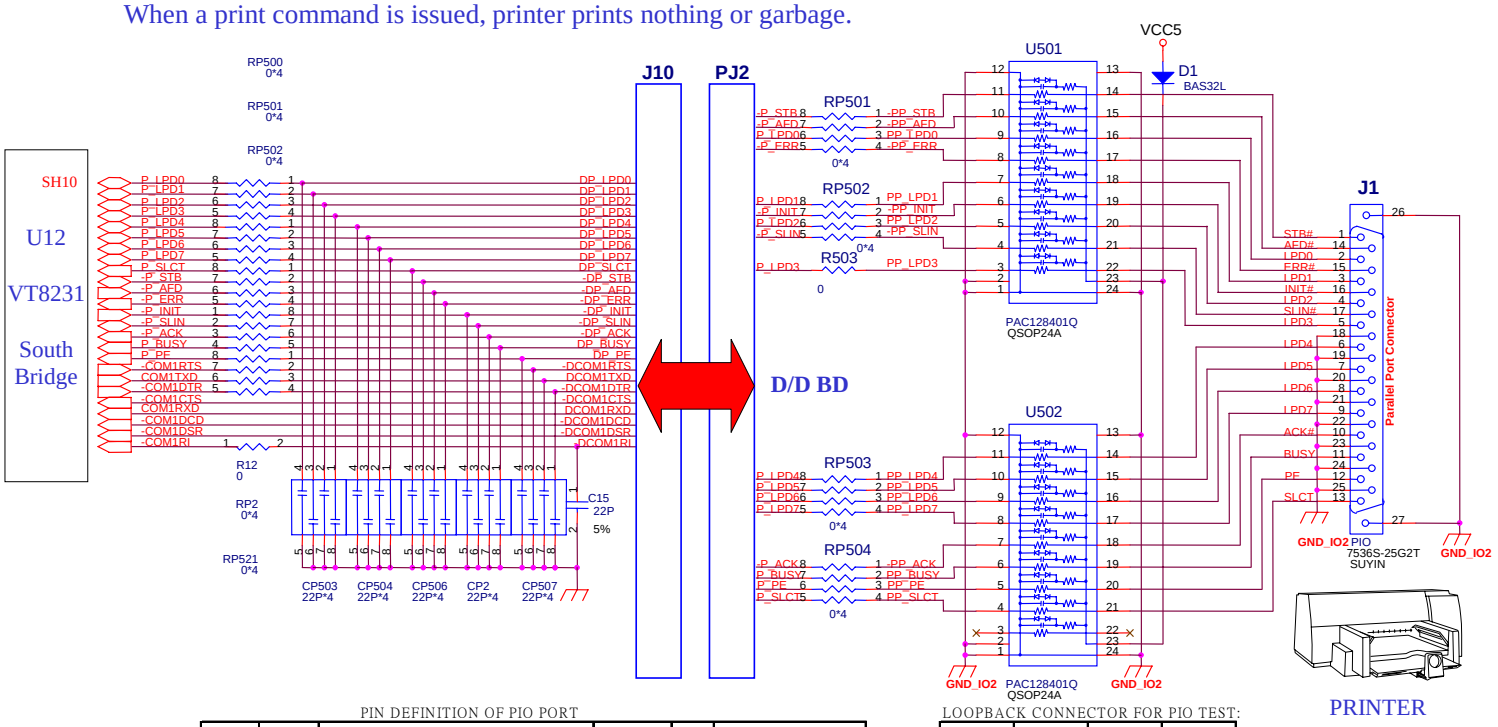
Board-level Troubleshooting
For USB test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Parts:	Signals:
J26	J27	VCC5
U12	U12	USBVCC5
F4, F5	F4, F5	
L16,R1, R2	L15	USBP1-
C9, C10	R1, R2	USBP1+
R157, R161	R11, R4	-USBOC1
L57, C209	C11, C8	
C207, R156	R167, R165	USBP0-
R160	L58, C218	USBP0+
	C212, R164	-USBOC0
	R166	

8.9 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

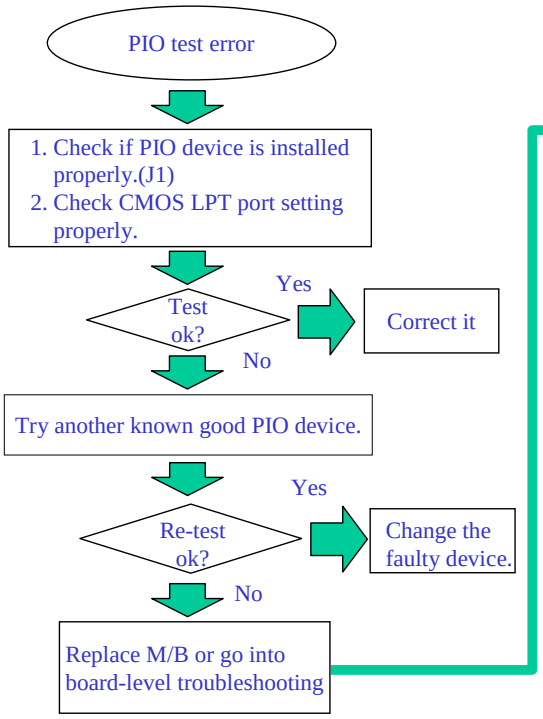
PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

8. 9 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



Board-level troubleshooting for PIO test error

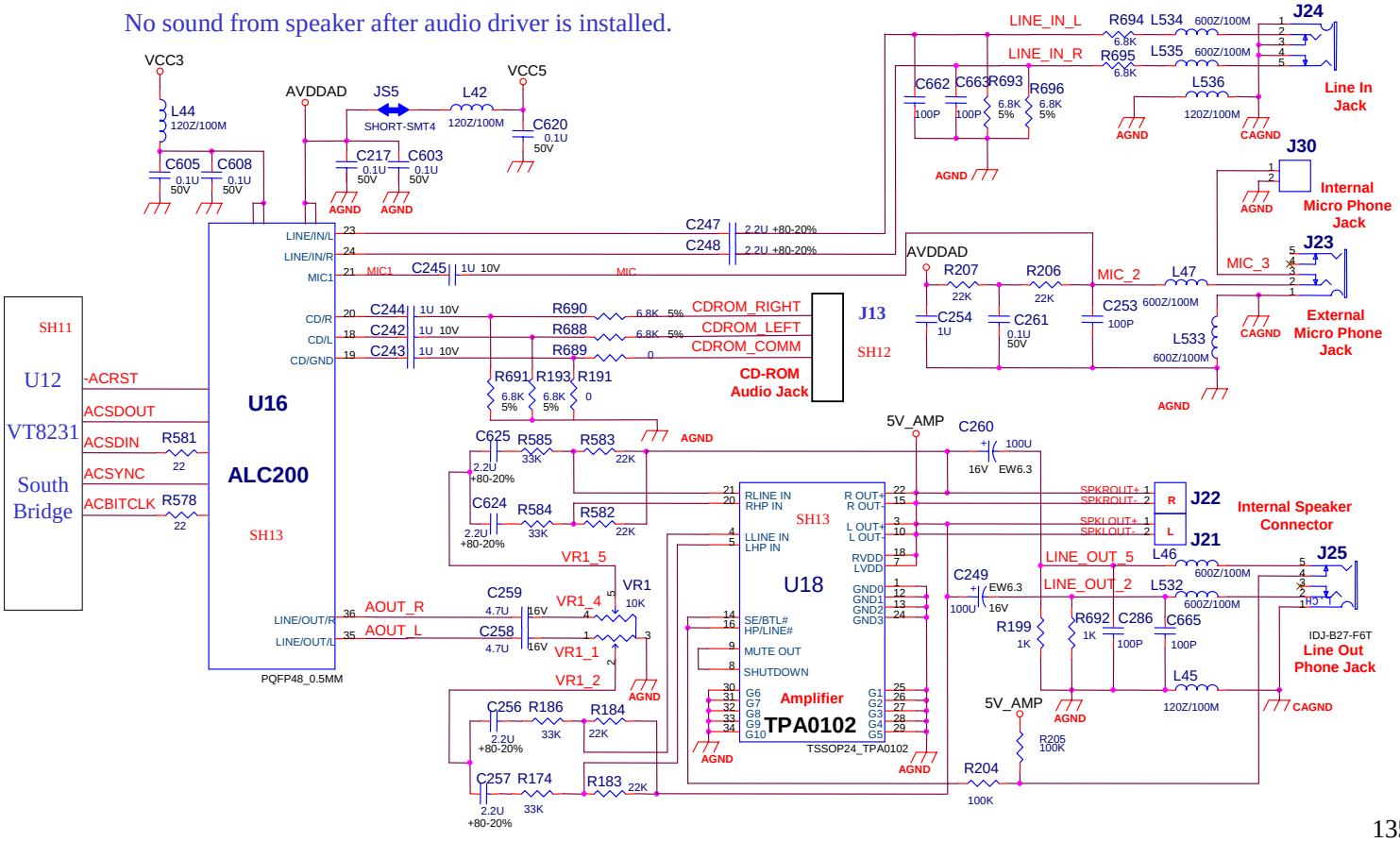
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

On D/D BD

PARTS:	PARTS:	SIGNALS:	SIGNALS:
U12, J10	RP501	P_LPD[0:7]	P_PF
JP2, J1	RP502	P_SLCT	-COM1RTS
RP500, RP501	R503	-P_STB	-COM1TXD
RP502, RP521	RP503	-P_AFD	-COM1DTR
RP2, R12	RP504	-P_ERR	-COM1CTS
CP503, CP504	U501	-P_INIT	-COM1RXD
CP506, CP507	U502	-P_SLIN	-COM1DCD
CP2, C15	D1	-P_ACK	-COM1DSR
		P_BUSY	-COM1RI

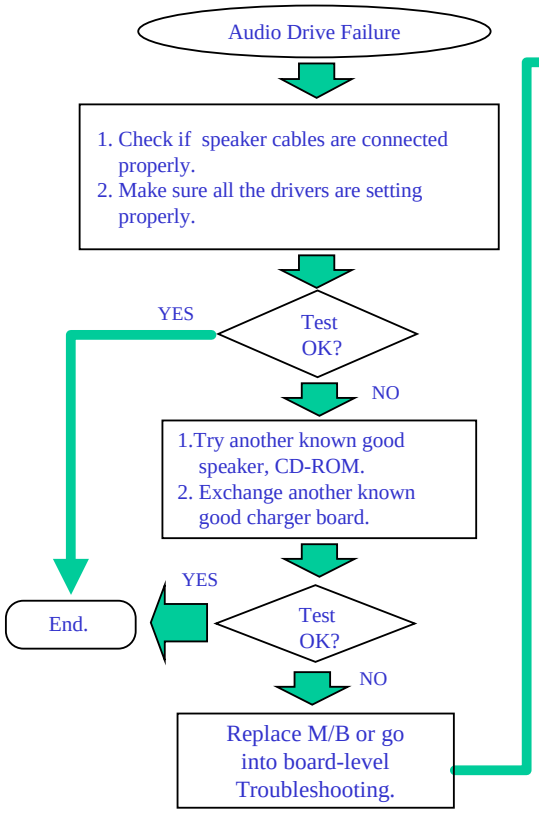
8.10 Audio Failure

No sound from speaker after audio driver is installed.



8.10 Audio Failure

No sound from speaker after audio driver is installed.



Board-level Troubleshooting for audio test error.

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1. If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
J25, J21, J22	AOUT_R
U12, U16	AOUT_L
C258,C259	SPKROUT+
U18,VR1	SPKROUT-
C624, C625	SPKLOUT+
R582~R585	SPKLOUT-
C260, L46	LINE_OUT_5
C256, C257	LINE_OUT_2
R174, R183	
R184, R186	
R204, R205	
C249, L532	
R199, L45	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U12, U16	MIC
J23, J30	MIC_2
R207, R206	MIC_3
L47, L533	
C254, C261	
C253	

3. If no sound cause of CD-ROM,or Line In check the following parts & signals:

Parts:	Signals:
U12, U16	CDROM_LEFT
C242~C244	CDROM_RIGHT
R688~R693	CDROM_COMM
J13	LINE_IN_L
C247, C248	LINE_IN_R
R694, R695	
L534, L535	
C662, C663	
R693, R696	
L536	

9. Spare Parts List-1

Part Number	Description	Location(s)
441999900201	AC ADPT ASSY OPTION;M722	
442051200001	AC ADPT ASSY;19V/3.16A,DELTA	
541666990001	AK;01-EN,BOX,7170	
541666990032	AK;EN,7170,UTILITY ONLY	
441999900051	BATT ASSY OPTION;LI,9-CELL,7170	
442669900003	BATT ASSY;11.1V/5.4AH,LI,E-ONE,7170	
340669900022	BEZELASSY;DVD ROM,PIONEER,7170	
221669940001	BOX;AK,7170	
340669900020	BRACKET ASSY;I/O,TV-OUT,7170	
340669900021	BRACKET ASSY;TOUCHPAD,7170	
343669900006	BRACKET;CD-ROM,7170	
341669900004	BRACKET;LCD,14.1",HYUNDAI,L,7170	
341669900003	BRACKET;LCD,14.1",HYUNDAI,R,7170	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z CORE	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C111,EC1,EC10,EC11,EC
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C1,C2,C509,PC13,PC14,P
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C100,C104,C118,C119,C
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,SMT	PC509,PC510,PC514
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C2
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,SMT	PC17,PC23
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,SMT	C1,C10,C107,C109,C11,C
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC524
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,SMT	C510,C511,C512,C513
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,SMT	C253,C286,C662,C663,C

Part Number	Description	Location(s)
272431105901	CAP;100U ,10V ,20%,7343,SMT	PC505,PC506,PC513,PC5
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SMT	C208,C21,C214,C219,C2
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,SMT	C133,C150,C20,C506,C5
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,SMT	PC23,PC503,PC504
272431157506	CAP;150U ,UD,2.5V ,20%,7343,SP-CON	PC1,PC11,PC2,PC3
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	PC508
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	C103,C115,C116,C126,C
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	PC507
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C247,C248,C256,C257,C
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y5V	C167,C168,C586,C591,C
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,SMT	PC508
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C15,C207,C209,C212,C2
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,SMT	C57
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C18
272431337506	CAP;330U,4V,20%,7343,SMT	PC31
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y5V	PC19,PC21,PC6
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y5V	C258,C259,C610,C611,C
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,SMT	C188,C189
272431566501	CAP;56U ,TT,4V,20%,SP-CON,7343,SMT	PC521
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C575,C576
272431826501	CAP;82U ,2.5V,20%,SP-CON,7343,SMT	C51,C60,C68,PC500,PC5
221669950007	CARD BOARD;BTM,PALLET,7170	
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	

9. Spare Parts List-2

Part Number	Description	Location(s)
221670020009	CARTON;NON-BRAND,TW,7521	
431669900002	CASE KIT;TV-OUT,7170	
344669900010	CASE;HDD,7170	
451669900051	CD ROM ME KIT;24X,7170	
273000500035	CHOKE COIL;0.6UH,1.44mOHM,20%,27A	PL1
273000111002	CHOKE COIL;120OHM/100MHZ,20%,3216	L57,L58
273000500044	CHOKE COIL;2.2UH,2.7mOHM,20%,3.10A	PL2
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,SMT	L8
331000006011	CON;BATT,6P,2.5MM,R/A,CEN LINK	J16
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J4
331720025005	CON;D,FM,25P,2.775,R/A	J1
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,SMT	J18
291000142402	CON;FPC/FFC,24P,1MM,H5.5,ST,ACES	J15
291000150812	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,W/GND,AC	J501
331040020004	CON;HDR,FM,10P*2,2.54MM,R/A,H8,49	J7
331030044013	CON;HDR,FM,22*2,2MM,ST,C16805	
331040044011	CON;HDR,FM,22P*2,1.27MM,R/A,H3MM	J10
291000011024	CON;HDR,FM,5P*2,1.27MM,ST,H4.5,SPEED	J501
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J3
331040020005	CON;HDR,MA,10P*2,2.54MM,R/A,H8.49	PJ1
291000013012	CON;HDR,MA,15P*2,1.25MM,ST,H4.8,ACES	J8
331040020006	CON;HDR,MA,22P*2,1.27MM,R/A,H3MM	PJ2
291000024409	CON;HDR,MA,22P*2,2MM,R/A,SMT,ALLTOP	J20
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIROSE	J505

Part Number	Description	Location(s)
331040050006	CON;HDR,MA,50P,0.8MM,R/A,ALLTOP	J13
291000011023	CON;HDR,MA,5P*2,1.27MM,ST,H10.4,SPEED	J9
291000256821	CON;IC CARD,68P,.635MM,62598-22A,FCI	J14
331000004018	CON;IEEE1394,MA,4P,.8MM,R/A,LINKTEK	J3
331870004010	CON;MINI DIN,4P,R/A,W/GROUND,C10801	J5
331870006013	CON;MINI DIN,6P,R/A,W/GROUND,73156	J1
291000251241	CON;PCI CARD,124P,FM,.8MM,SMT	J503
291000810203	CON;PHONE JACK,2P,H=8.5,R/A,SMT	J2
291000810802	CON;PHONE JACK,8P,H=12.59,R/A,RJ45	J11
331910003034	CON;POWER JACK,3P,D=2.5,SINGATRON	J4
331840005028	CON;STEREO JACK,5P,R/A,W10.4,BLUE	J24
331840005029	CON;STEREO JACK,5P,R/A,W10.4,GREEN	J25
331840005027	CON;STEREO JACK,5P,R/A,W10.4,PINK	J23
331000004025	CON;USB,MA,R/A,4P*1,2MM,85116-4011,ACES	J26,J27
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J21,J22,J30,J6
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J12
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J502
291000410404	CON;WFR,MA,4P,1.25MM,ST,SMT,HIROSE	J17
345669600065	CONDUCTIVE TAPE;MB,SDRAM,RACE	
345669600053	CONDUCTIVE TAPE;PCMCIA,RACE	
313000150093	CORE;LAN CORE,230OHM/100MHZ,LF-100	
340669900010	COVER ASSY;14.1"LCD COVER,7170	
340669900006	COVER ASSY;7170	
340669900018	COVER ASSY;ID1,7170	

9. Spare Parts List-3

Part Number	Description	Location(s)
340669900009	COVER ASSY;KEYBOARD COVER,7170	
340669900015	COVER ASSY;RAM-MINIPCI COVER,7170	
340669900008	COVER ASSY;SPEAKER COVER,7170	
344669900003	COVER;HINGE,7170	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,SMT	CP1,CP2,CP500,CP501,C
291006214426	DIMM SOCKET;144P,.8MM,AMP353870,RAC	J501
291006214427	DIMM SOCKET;144P,.8MM,H4,AMP1318144	J502
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D1
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D1,D19,D2,D507,PD2,PD
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	PD504,PD505
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D3
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D30,D31,D32,D33
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D500,D501
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D500,D501,D502,D503,D
288100056003	DIODE;BAW56,70V,215MA,SOT-23	PD503
288100056003	DIODE;BAW56,70V,215MA,SOT-23	PD1
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200V	PD501
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200V	D508
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD1,PD2
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD4,PD5,PD500,PD7
288137010001	DIODE;MA3X70100L,30V,700MA,SOT-23	PD502
288100027001	DIODE;RLZ2.7B,ZENER,2.6-2.91,5%,SMT	PD503
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD502
288100012002	DIODE;SK12,VRRM20V,SMT	D4,D5

Part Number	Description	Location(s)
344668900053	DUMMY-CARD;PCMCIA,M722	
523499999028	DVD ASSY OPTION;8X,7170	
523424379020	DVD DRIVE;8X,DVD-K11TA,PIONEER	
523466990004	DVD ROM ASSY;8X,K11,PIONEER,7170	
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~105'C	PC10,PC11,PC4,PC5,PC8
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~105'C	PC12,PC21,PC8,PC9
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,SMT	C249,C260
227669900005	END CAP; HEATSINK, AK BOX,7170	
227669900001	END CAP;7170	
227669900004	END CAP;BATTERY,7170	
227669900002	END CAP;FDD,FRAME,7170	
227669900003	END CAP;FDD,T/B,7170	
481669900002	F/W ASSY;KBD CTRL,7170	U502
481669900003	F/W ASSY;SYS/VGA BIOS,REV8231,7170	U8
523499993004	FDD DRIVER OPTION;EXT. FDD,7170	
523411442043	FDD KIT;MITSUMI,D353FU,USB,7170	
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN,NZ	FA1
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN,NZ	FA1,FA500
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,MLB	L4,L6,L501,L502,L503,L5
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,MLB	L17,L2,L22,L24,L26,L29,
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	L1,L3,L5,PL10,PL4,PL5,P
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	L1,L15,L16,L20,L36,L43,
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1608	L46,L47,L532,L533,L534
422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	

7170 N/B MAINTENANCE

9. Spare Parts List-4

Part Number	Description	Location(s)
346664900010	FILM;LCD PROTEC,.14.2",235*300,5027	
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,SMT	U1
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SMT	F1,F2,F5,F500
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1
345669600048	GASKET;FDD,SHORT,RACE	
345669600033	GASKET;SUPPORT,EXT RAM,L,RACE	
345669600042	GASKET;USB,10X15X0.3,RACE	
523416340057	HD DRIVE;20GB,2.5",DJSA-220,H=9.5MM	
451669900071	HDD ME KIT;7170	
340669900003	HEATSINK ASSY;CPU,7170	
340669900007	HOUSING ASSY;7170	
340669900011	HOUSING ASSY;LCD 14.1",HYUNDAI,7170	
441669900031	HOUSING ASSY;M/B,TV-OUT,7170	
451669900001	HOUSING KIT;7170	
344600030002	IC CARD CON PART;68P,62601-22ROC,FCI	
331650037014	IC SOCKET;370P,ZIF,SOCKET370,CENLIN	U1
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP-24	U505
282007407001	IC;74LVC07,HEX-BUFFER, TSSOP14,14P	U508
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,14P	U19
284580227001	IC;80227,LAN-PHY,TQFP,64P,SMT	U25
284501021002	IC;ADM1021,TEMPERATURE MTR,SSOP16	U2
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,SOT2	U504
284500200005	IC;ALC200,AC97 CODEC,TQFP,48P	U16

Part Number	Description	Location(s)
284507005001	IC;CH7005C,TV ENCODER,3/5V,PQFP,44P	U511
286302211002	IC;CP2211,POWER DISTRI SW,SSOP16	U5
324180786021	IC;CPU,P-III,866MHZ,FCPGA,370P	
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SMT	U6
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U10
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF020	
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
284509248019	IC;ICS9248-195,CLOCK GEN,SSOP,48P	U503
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU507,PU509
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,SO	PU6
286329510001	IC;LP2951CM-3.3,VOLTAGE REGULATOR	PU7
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU501
286301717001	IC;MAX1717,PWM,QSOP,24P	PU504
281300732001	IC;NC7S32,SINGLE OR GATE,SC70-5	U507
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70-5P	U26,U514
286307805010	IC;NJM78L05UA,VOL REGULATOR,SOT,89P	U513
284501284001	IC;PAC1284-01Q,TERMIN. NETWK,QSOP24	U501,U502
284504410005	IC;PCI4410A,CARDBUS/OHCI,uBGA,209P	U21
286301401001	IC;SC1401,PWN CTRL,SSOP,20P	PU4
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ507
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU506
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24P	U18
284500411001	IC;TSB41AB1,1394 PHY,PQFP,64P	U500
284508231002	IC;VT8231,PCI/ISA,BGA,376P,SMT	U12

9. Spare Parts List-5

Part Number	Description	Location(s)
284508603002	IC;VT8603,PCI/AGP/VGA,BGA,552P,SMT	U501
273000990018	INDUCTOR;10uH,CDRH125,SMT	PL1
273000990023	INDUCTOR;10UH,CDRH125B,SMT	PT1
273000990021	INDUCTOR;33uH,CDRH124,SMT	PL4
273000150106	INDUCTOR;4.7UH,10%,2012,SMT	L21
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346669900004	INSULATOR;INVERTER,7170	
346669900019	INSULATOR;MDC MB,94VO,7170	
531099990102	KBD OPTION;87,UK,7170	
531066990002	KBD;87,UK,K000918F,7170	
344669900007	KNOB;MIDDLE,TOUCHPAD,7170	
451669900092	LABEL KIT;N-B,7170	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669900008	LABEL;AGENCY,7170	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242669900012	LABEL;BAR CODE,32x11MM,7170	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	

Part Number	Description	Location(s)
242669900005	LABEL;LCD SIDE,7170	
242600000412	LABEL;PENTIUM,PWR SUITE 3 NOTE BIOS	
242668820022	LABEL;WINDOWS ME/2000,ORION-3	
441669900010	LCD ASSY;HYUNDAI,XGA,14.1",7170	
451669900034	LCD ME KIT;HYUNDAI,XGA,14.1",7170	
413000020236	LCD;HT14X13,TFT,14.1",XGA,HYUNDAI	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D10,D6,D7,D8,D9
294011200063	LED;RE/GR,H.6,L2.1,W1,12-215 VGC	D11
294011200064	LED;RE/GR,H.6,L2.1,W1,12-215 VRC	D15
561566990001	MANUAL KIT;EN,7170,N-B	
561566990101	MANUAL;USER'S,EN,7170,N-B	
416266990012	NB PF;HYUNDAI,TV-OUT,XGA,14.1",7170	
375102030010	NUT-HEX;M2,2,NIW	
461669900002	PACKING KIT;N-B,7170	
227669900006	PAD;LCD/KB,ANIT-STATIC,7170	
221669950004	PARTITION;A,PALLET,7170	
221669950001	PARTITION;AK BOX,7170	
221669950005	PARTITION;B,PALLET,7170	
412669900001	PCB ASSY;INVERTER BD,13",7170	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222667220003	PE BAG;L560XW345,CERES	
222670000001	PE BUBBLE BAG;BATTERY,7521	
411669900008	PWA;PWA-7170,ESB BD,SMT	

9. Spare Parts List-6

Part Number	Description	Location(s)
411669900007	PWA;PWA-7170,ESB BD,T/U	
411669900006	PWA;PWA-7170,T/P BD	
411669900013	PWA;PWA-7170,TV-OUT,D/D BD,SMT	
411669900012	PWA;PWA-7170,TV-OUT,D/D BD,T/U	
411669900014	PWA;PWA-7170,TV-OUT,MOTHER BD	
411669900016	PWA;PWA-7170,TV-OUT,MOTHER BD,SMT	
411669900015	PWA;PWA-7170,TV-OUT,MOTHER BD,T/U	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERICA	
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR15,PR16
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR1,PR2
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR1,PR14
271071000002	RES;0 ,1/16W,0603,SMT	PR519,PR514,R503
271071000002	RES;0 ,1/16W,0603,SMT	PR13,PR511,PR534,R102
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR504
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR2,R505,R532,R534,R5
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R117,R227,R575
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR507,R501
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR507,PR549,PR551,PR5
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR10,PR5,PR503,PR513,
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR529,PR558
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR4,PR7,R504
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR506,PR512,PR517,PR5
271071118211	RES;11.8K,1/16W,1% ,0603,SMT	PR540
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R28,R34

Part Number	Description	Location(s)
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR545
271071121311	RES;121K ,1/16W,1% ,0603,SMT	PR532
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R69
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R27,R29,R32,R36,R37,R5
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R156,R160,R164,R166,R
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR504,PR524
271071187211	RES;18.7K,1/16W,1% ,0603,SMT	PR518
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR505,PR533,PR537,R50
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR515,PR516
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R13,R16,R199,R222,R39,
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR547,R20
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR517
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R169,R523,R541,R57,R6
271034278301	RES;2.7 ,1/2W ,5% ,2010,SMT	R502
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR12,PR521
271071214101	RES;210K ,1/16W,1% ,0603,SMT	PR539
271071221302	RES;22 ,1/16W,5% ,0603,SMT	PR508,R135,R136,R157,
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R40,R44,R510
271071249811	RES;24.9 ,1/16W,1% ,0603,SMT	R246,R247,R70,R71
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR552
271071324012	RES;324K ,1/16W,1% ,0603,SMT	PR556
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR523,R11,R2
271071361101	RES;360 ,1/16W,1% ,0603,SMT	R670
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR544,R109,R115,R121,

9. Spare Parts List-7

Part Number	Description	Location(s)
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR11,R15
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR536,PR550
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR535
271071453311	RES;453K ,1/16W,1% ,0603,SMT	PR538
271071475211	RES;47.5K,1/16W,1% ,0603,SMT	PR510,PR557
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R209,R210,R211,R212,R
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR3,PR5
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR9,R506,R518,R60
271071475311	RES;475K ,1/16W,1% ,0603,SMT	PR548
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR6
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR526,R1,R104,R4,R580
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R128,R130
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R49,R53,R64
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R10,R17,R18,R22,R25,R3
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR530
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R19
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R193,R688,R690,R691,R
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R14,R24,R45,R65,R7,R9
271071806111	RES;8.06K,1/16W,1% ,0603,SMT	PR509,PR541
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP501,RP502,RP503,RP5
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP2,RP500,RP501,RP502
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SMT	RP508,RP509,RP510,RP5
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP23,RP27,RP28,RP40,R
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP29

Part Number	Description	Location(s)
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP54,RP59,RP61
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP30,RP33,RP38
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SMT	RP34,RP35,RP36,RP37,R
271611331301	RP;330*4 ,8P ,1/16W,5% ,0612,SMT	RP15,RP16
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP22,RP39,RP46,RP50,R
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT,TF	RP32,RP43,RP49,RP51,R
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP31,RP517
271621560301	RP;56*8 ,10P,1/16W,5% ,1206,SMT,TF	RP10,RP11,RP12,RP13,R
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP505
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP1
345669900004	RUBBER;LCD,DOWN,7170	
345669900003	RUBBER;LCD,TOP,7170	
565166990001	S/W;CD ROM,SYSTEM DRIVER,7170	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
323766990002	SDRAM MODULE;128M,8M*16,PC133,SPD	
323799990034	SDRAM OPTION;128MB,PC133,7170	
340669900024	SHIELDING ASSY;D/D,7170	
340669900004	SHIELDING ASSY;TOP CASE,7170	
343669900012	SHIELDING;EMI-3,TOP CASE,7170	
346669900008	SHIELDING;M/B,7170	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&LCD	
346667120001	SPACER;FC-PGA CPU,6133XN	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	

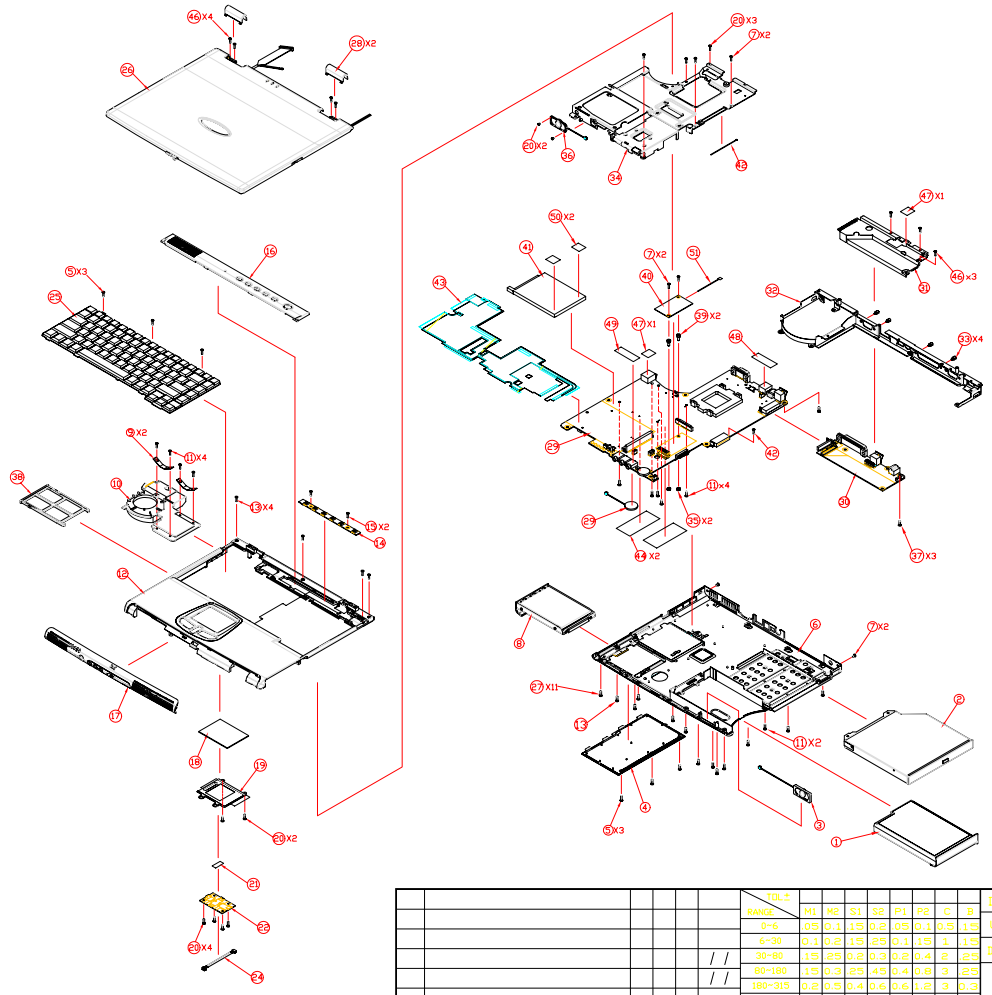
9. Spare Parts List-8

Part Number	Description	Location(s)
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010605	SPC-SCREW;M2L6,NIW,HDT=0.4,779	
370102010605	SPC-SCREW;M2L6,NIW,HDT=0.4,779	
370102010605	SPC-SCREW;M2L6,NIW,HDT=0.4,779	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340669900014	SPEAKER ASSY;L,7170	
340669900013	SPEAKER ASSY;R,7170	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	
344669600037	STOPPER;CUP SOCKET,RACE	
337120100006	SW;DIP,SPST,2P,24V,50MA,HDK632AR-ST	SW3
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS4S	SW1
297040105009	SW;PUSH BUTTOM,4P,SPST,12V/50MA,H2.5,W/	SW1,SW2,SW3,SW4,SW5

Part Number	Description	Location(s)
297040105009	SW;PUSH BUTTOM,4P,SPST,12V/50MA,H2.5,W/	SW10,SW7,SW8,SW9
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	SW4
340669900002	TILT UNIT;L,7170	
340669900001	TILT UNIT;R,7170	
442164900010	TOUCH PAD MODULE;TM41PD-350	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ501
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ501,PQ502,PQ506,PQ
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q501
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ5,Q10,Q13,Q14,Q15,Q
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ4,PQ503,Q4,Q7,Q8
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q12
288200302001	TRANS;FDV302P,P-CHANNEL,SOT23	Q11
288207811002	TRANS;IRF7811ATR,N-MOS,.01OHM,SO8	PU2,PU501
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ2
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	Q1
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236AB	PQ500,Q504
328202003001	TRANS;MTD20N03HDL,N-MOSFET,2A,30V	PQ1
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ504,PQ505
288214404001	trans;s14404DY,N-MOS,.008OHM,SO8	PU1,PU500,PU502
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ3,PQ6,Q2
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO8	PU1,PU2
288204816001	TRANS;SI4816DY,2 N-MOSFET,30V,SO8	PU3
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,SO8	PU3,PU4
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,SO8	PQ1

9. Spare Parts List-9

Part Number	Description	Location(s)
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,SO8	PU5,PU505
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU508
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,SO-8	Q500
273001050040	TRANSFORMER;10/100 BASE,H0011,SMT	U3
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-050	S500
271911103905	VR;10K ,20%,0.05W,RN101GAC10KPCJ-R	VR1
421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	
421669900001	WIRE ASSY;HYUNDAI 14.1",7170	
421669900006	WIRE ASSY;INVERTER,7170	
421669900013	WIRE ASSY;MDC,7170	
421669900014	WIRE ASSY;MICROPHONE,7170	
421669900012	WIRE ASSY;PATCH ANTENNA,7170	
421669900007	WIRE ASSY;TOUCHPAD,7170	
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,2P	X500,X502
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X501
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,2P	X1,X4
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X2
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X3



ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
(51)	421669900013	WIRE ASSY;MDC,7170	1	
(50)	345669600048	GASKET;FDD,SHORT,RACE	2	
(49)	345669600053	CONDUCTIVE TAPE;PCMCIA,RACE	1	
(48)	345669600033	GASKET;SUPPORT,EXT RAM,L,RACE	1	
(47)	345669600042	GASKET;USB,10X15X0.3,RACE	2	
(46)	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	7	
(45)	421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	1	
(44)	346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	2	
(43)	346669900008	SHIELDING;M/B,7170	1	
(42)	421669900014	WIRE ASSY;MICROPHONE,7170	1	
(41)	344600030002	IC CARD CON PART;68P,62601-22ROC,FCI	1	
(40)	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
(39)	341668300008	STANDOFF;MDC MODEM,NLK,HOPE	2	
(38)	344668900053	DUMMY-CARD;PCMCIA,M722	1	
(37)	370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	3	
(36)	340669900014	SPEAKER ASSY;L,7170	1	
(35)	375102030010	NUT-HEX;M2,2,NIW	2	
(34)	340669900027	SHIELDING ASSY-1;TOP CASE,7170	1	
(33)	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
(32)	340669900017	BRACK ASSY;I/O,7170	1	
(31)	340669900005	SHIELDING ASSY;HOUSUNG,7170	1	
(30)	411669900012	PWA;PWA-7170,TV-OUT,D/D BD,T/U	1	
(29)	411669900001	PWA;PWA-7170,MOTHER BD	1	
(28)	344669900003	COVER;HINGE,7170	2	
(27)	370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	11	
(26)	441669900009	LCD ASSY;UNIPAC,XGA,14.1",7170	1	OPTION
(25)	531066990001	KBD;86,US,K000918E,7170	1	
(24)	421669900007	WIRE ASSY;TOUCHPAD,7170	1	
(23)	343669900006	BRACKET;CD-ROM,7170	1	
(22)	411669900006	PWA;PWA-7170,T/P BD	1	
(21)	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
(20)	370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	11	
(19)	340669900033	BRACKET ASSY-1;TOUCHPAD,7170	1	
(18)	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
(17)	340669900008	COVER ASSY;SPEAKER COVER,7170	1	
(16)	340669900009	COVER ASSY;KEYBOARD COVER,7170	1	
(15)	370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	2	
(14)	316669900003	PCB;PWA-7170/QUICK KEY BD	1	
(13)	370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	5	
(12)	340669900029	COVER ASSY-1;7170	1	
(11)	370102010605	SPC-SCREW;M2L6,NIW,HDT=0.4,779	10	
(10)	340669900003	HEATSINK ASSY;CPU,7170	1	
(9)	341669900010	SPRING;HEATSINK,CPU,7170	2	
(8)	523466990011	HDD ASSY;20G,2.5",9.5MM,7170	1	OPTION
(7)	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	6	
(6)	340669900028	HOUSING ASSY-1;7170	1	
(5)	370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	6	
(4)	340669900015	COVER ASSY;RAM-MINIPCI COVER,7170	1	
(3)	340669900013	SPEAKER ASSY;R,7170	1	
(2)	523466990002	CD ROM ASSY;24X,224E-B92,TEAC,7170	1	OPTION
(1)	441999900051	BATT ASSY OPTION;LI,9-CELL,7170	1	OPTION

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/DAY

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	0.05	0.1	0.15	0.2	0.05	0.1	0.5	1.5
6~30	0.1	0.2	0.15	0.25	0.1	0.15	1	1.5
30~80	0.15	0.25	0.2	0.3	0.2	0.4	2	2.5
80~180	0.15	0.3	0.25	0.45	0.4	0.6	3	2.5
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	3.5
315~800	0.3	0.6	0.7	1.1	0.8	1.5	4	3.5

DATE	19-Jul-01	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	— —	DRAWING NAME	NB PF,UNIPAC,XGA,14.1",7170		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416266990003	R00

MiTAC International Corp.

SHEET NO. 1 OF 1

MODEL : 7170 Revision 0A

Contexts

Title	Page
Cover Sheet	1
System Block Diagram	2
Power Block Diagram	3
Central Processor Unit	4
CPU Decoupling Capacitor & VTT Termination Resistor	5
North Bridge (VIA TWISTER) Partial I	6
North Bridge (VIA TWISTER) Partial II	7
SO-DIMM Memory X 2	8
LCD & CRT&TV-OUT Interface	9
South Bridge (VIA VT8231) Partial I	10
South Bridge (VIA VT8231) Partial II	11
HDD, CDROM Connector	12
Audio Codec & Amplifier	13
PCMCIA/1394 Controller(PCI4410) & Socket	14
USBx2, BIOS,TOUCH PAD	15
Clock Generator,Screw holes	16
Micro Controller(H8)	17
LANPHY,MDC	18
MINIPCI	19
CPU Vcore/VTT	20
Battery Connector	21
DC-DC CONNECTOR,CHARGER	22

DRAW	DESIGN	CHECK	ISSUED

History of Schematics

Revision 00 (EVT)

1.Change S.B.VT8231
2.Del R518 Add R519.
3.Del R66
4.Del R106,Add R105.

Revision 0A (PreDVT)

POWER STATES

SIGNAL \ STATE	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSA	-	HIGH	LOW	LOW	LOW	
-SUSB	-	HIGH	LOW	LOW	LOW	
-SUSC	-	HIGH	HIGH	LOW	LOW	
DVMAIN	+18.5V	O	O	O	O	
VDCIN	+18.5V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
RTC_VCC	+3V	O	O	O	O	
VCC_CORE	+1.65V	O	O	X	X	
VTT	+1.5V	O	O	X	X	
VCC2.5	+2.5V	O	O	X	X	
5VALWAYS	+5V	O	O	O	O	
VDD5S	+5V	O	O	O	O	
VDD5	+5V	O	O	O	O	
AVDD	+5V	O	O	X	X	
VCC5	+5V	O	O	X	X	
5V_AMP	+5V	O	O	X	X	
VCC3	+3.3V	O	O	X	X	
VCC3_LAN	+3.3V	O	O	X	X	
VCC_LVDS	+3.3V	O	O	X	X	
VCC_CRT	+2.5V	O	O	X	X	
VGTLREF_CPU	+1V	O	O	X	X	
+12V	+12V	O	O	X	X	

Layout note:

Component side
Differential Signal 1
VCC 2
LCD_PIO 3
LVDS_VGA 4
GND 5
Differential Signal 6
Solder side

IDSEL

IDSEL	CHIP
AD18	VIA(S.B.)
AD11	VGA(N.B.)
AD22	LAN
AD17	MINI PCI
AD21	PCMCIA

BUSMASTER

REQ	CHIP
REQ0	PCMCIA
REQ1	NU
REQ2	VGA(N.B.)
REQ3	MINI PCI
REQ4	LAN

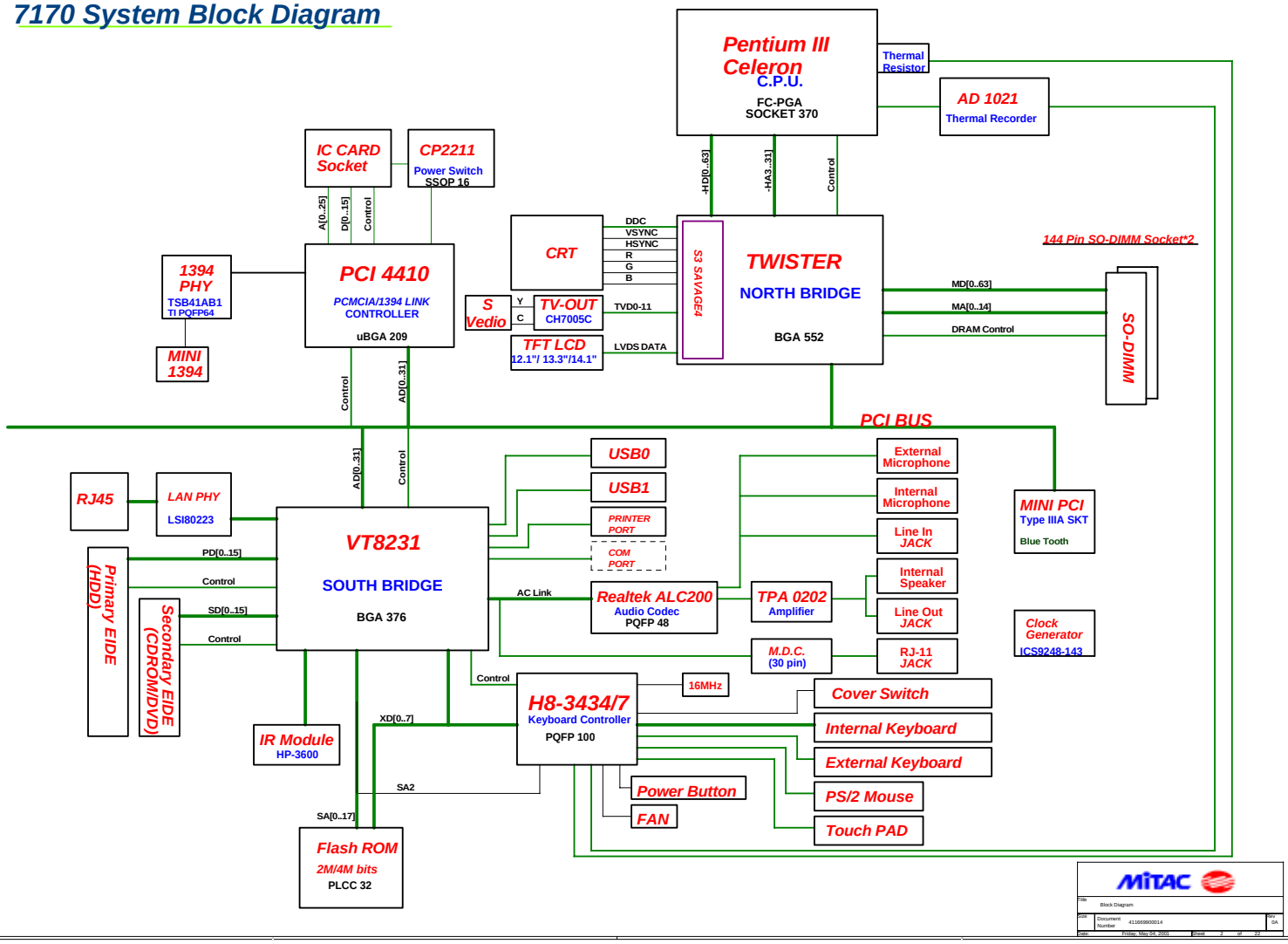
PCIINT

PCIINT	CHIP
INTA	PCMCIA
INTB	N.B.(VGA)
INTC	MINI PCI
INTD	USB /MINI PCI(REV)/1394/LAN

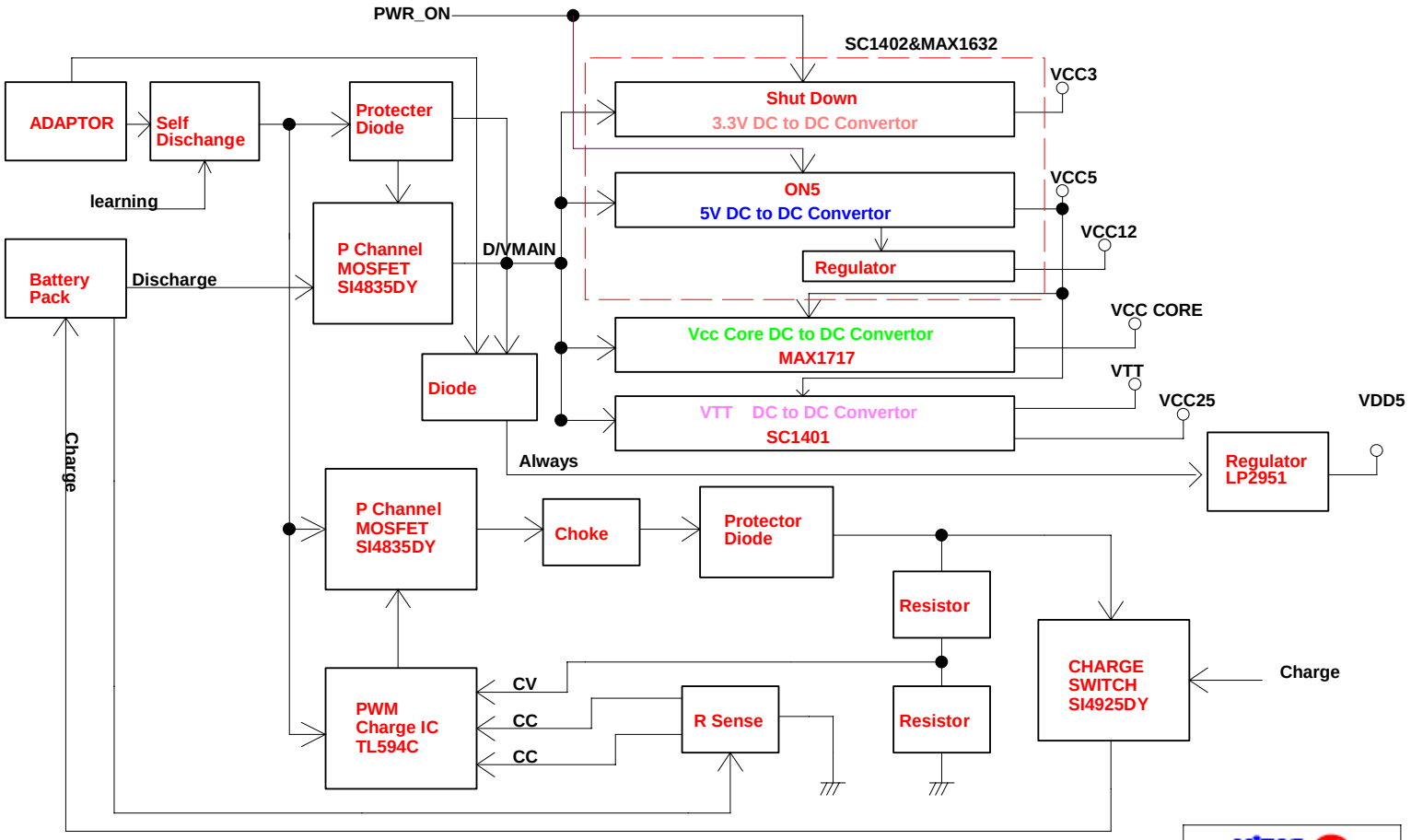
MiTAC

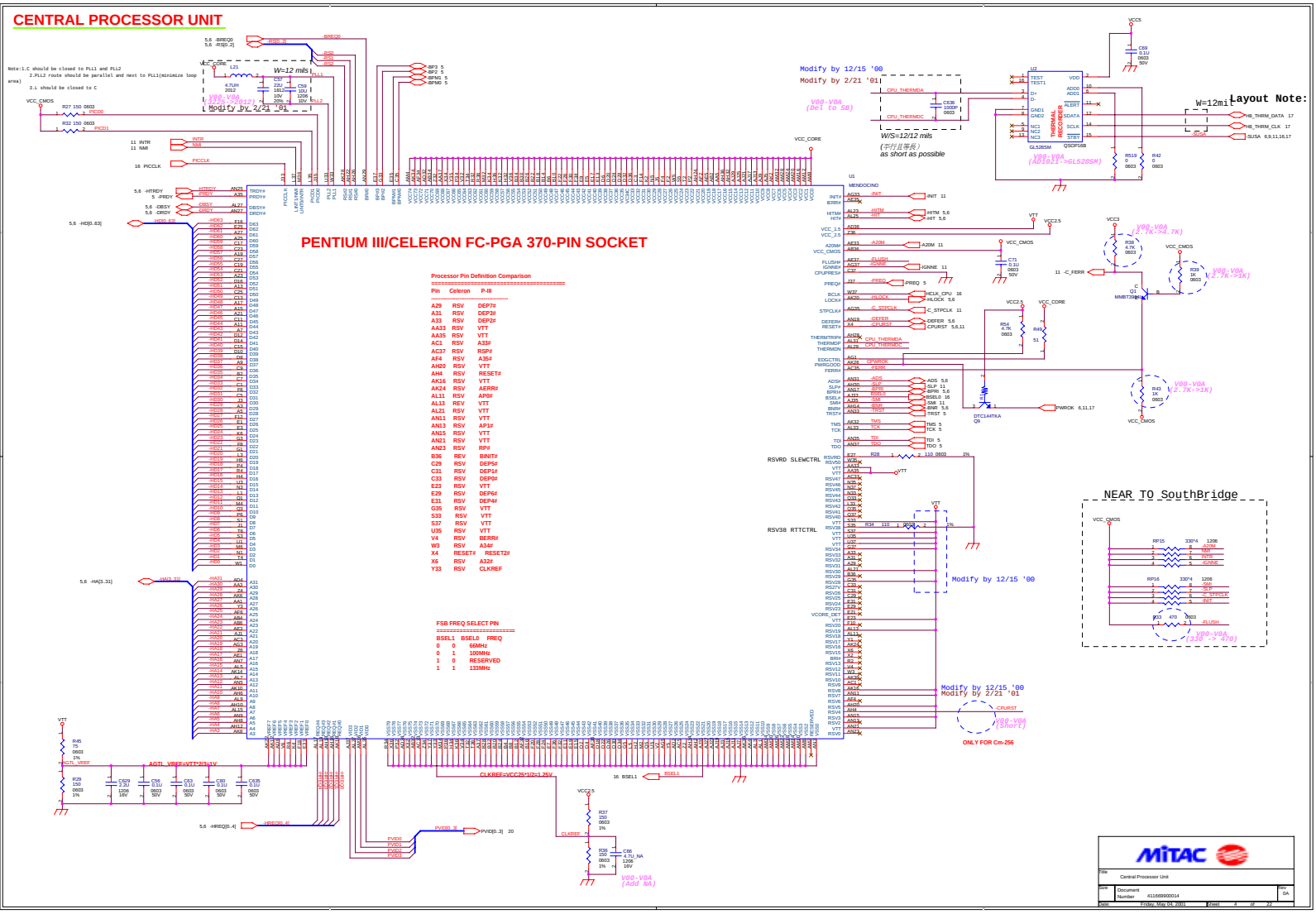
Title: Cover Sheet
Size: C
Document Number: 411669900014
Rev: 0A
Date: Friday, May 04, 2001
Sheet 1 of 22

7170 System Block Diagram

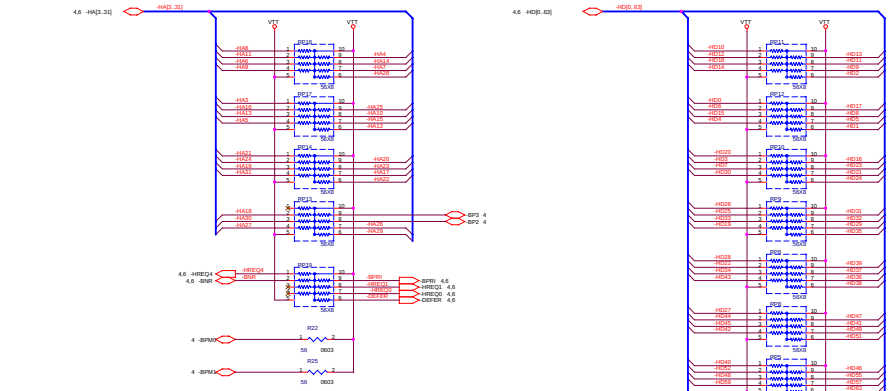


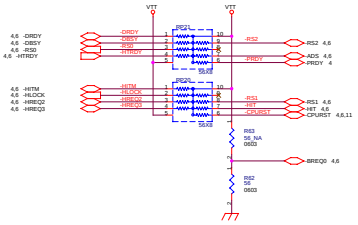
POWER DIAGRAM OF THE 7170

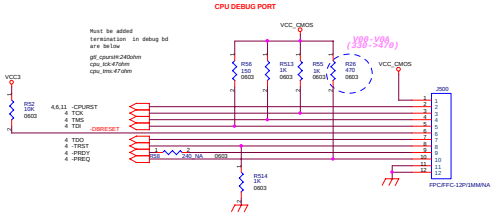


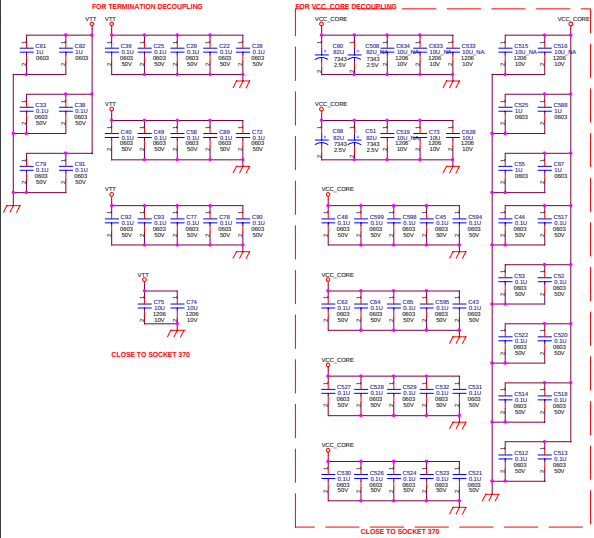


AGTL PLUS BUS TERMINATION

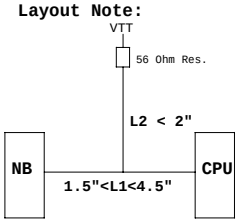






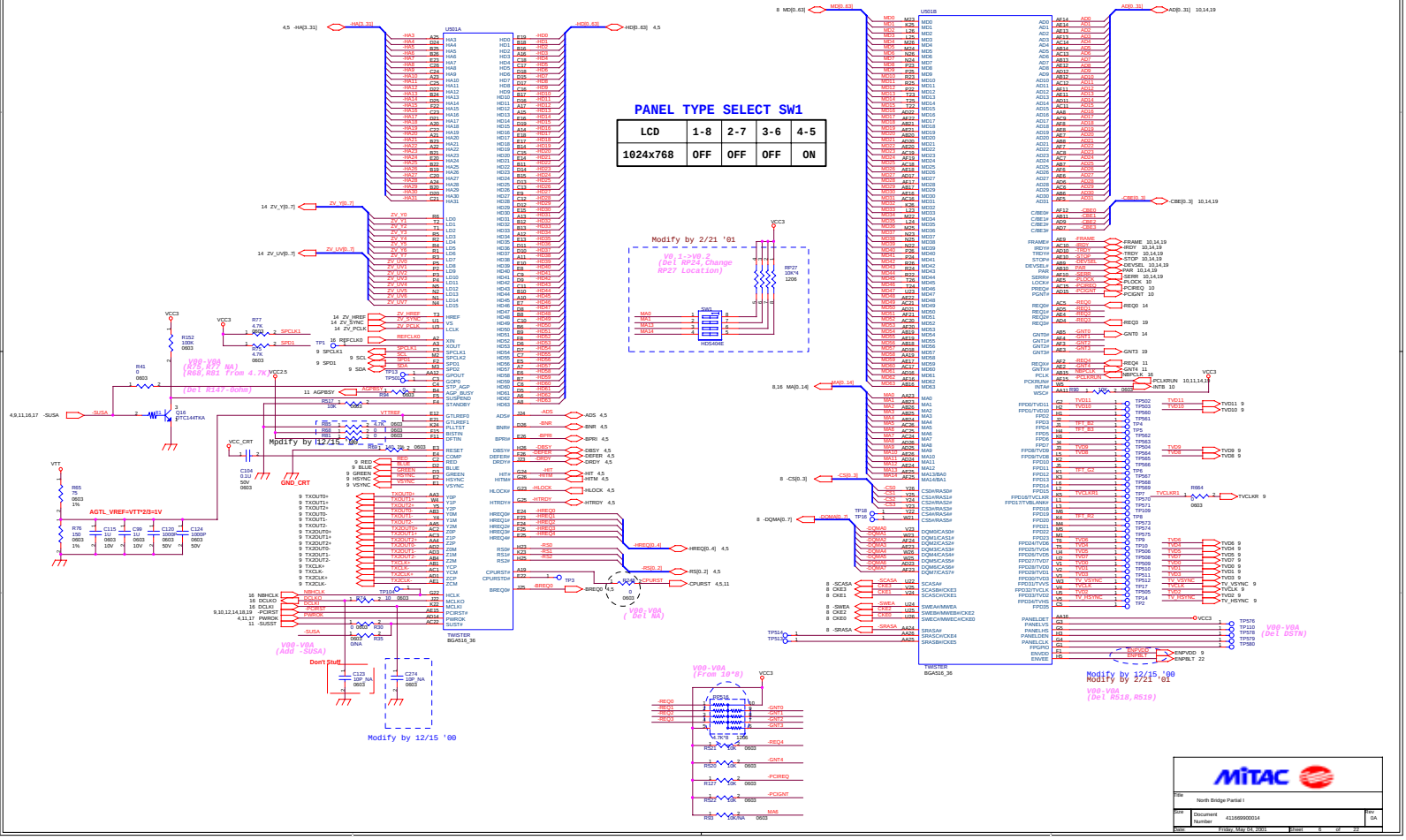


Layout Note:

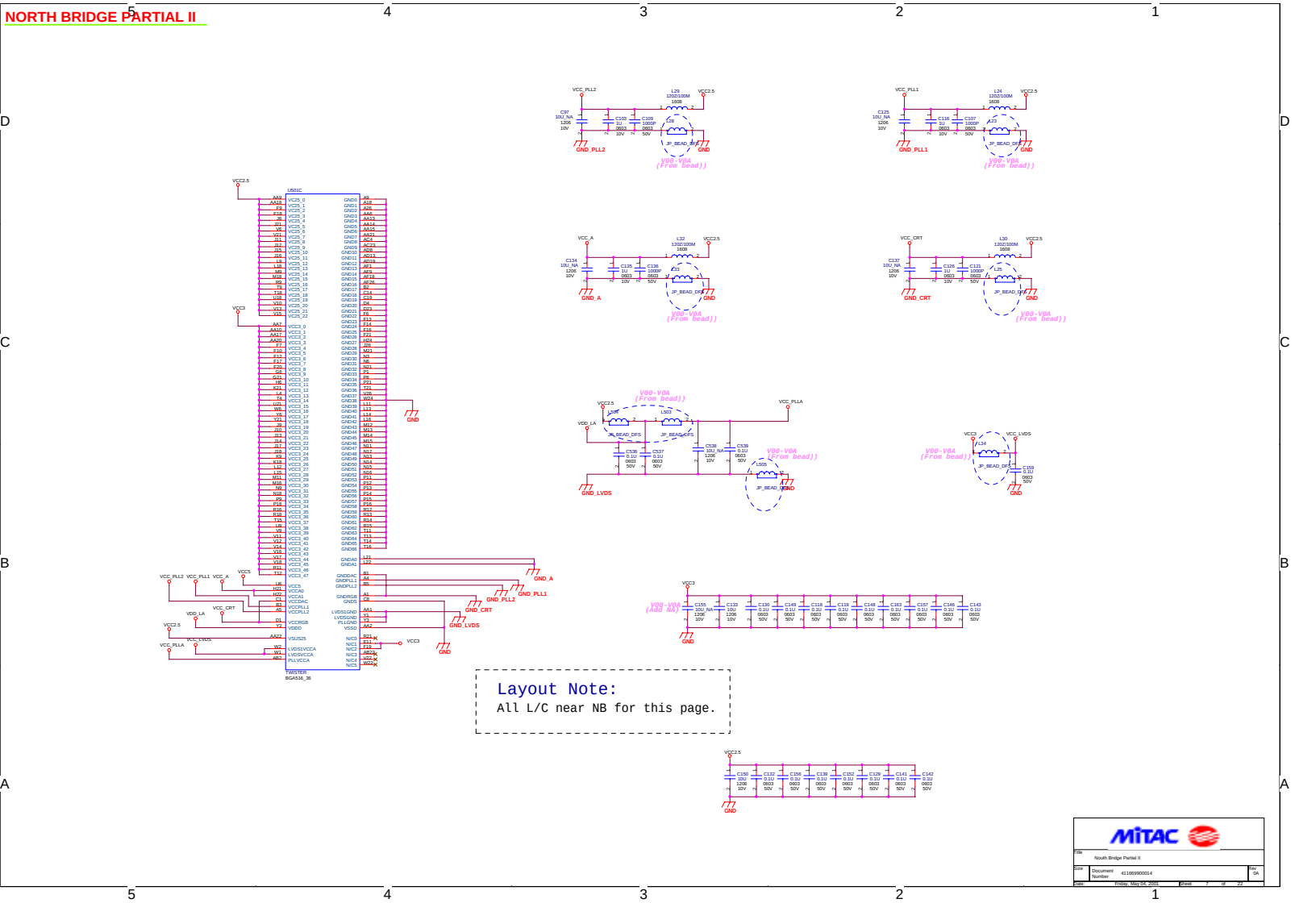


Title	VTT TERMINATION		
Size	Document Number	411669900014	Rev 0A
Date	Friday, May 04, 2001	Sheet 5 of 22	

NORTH BRIDGE PARTIAL I

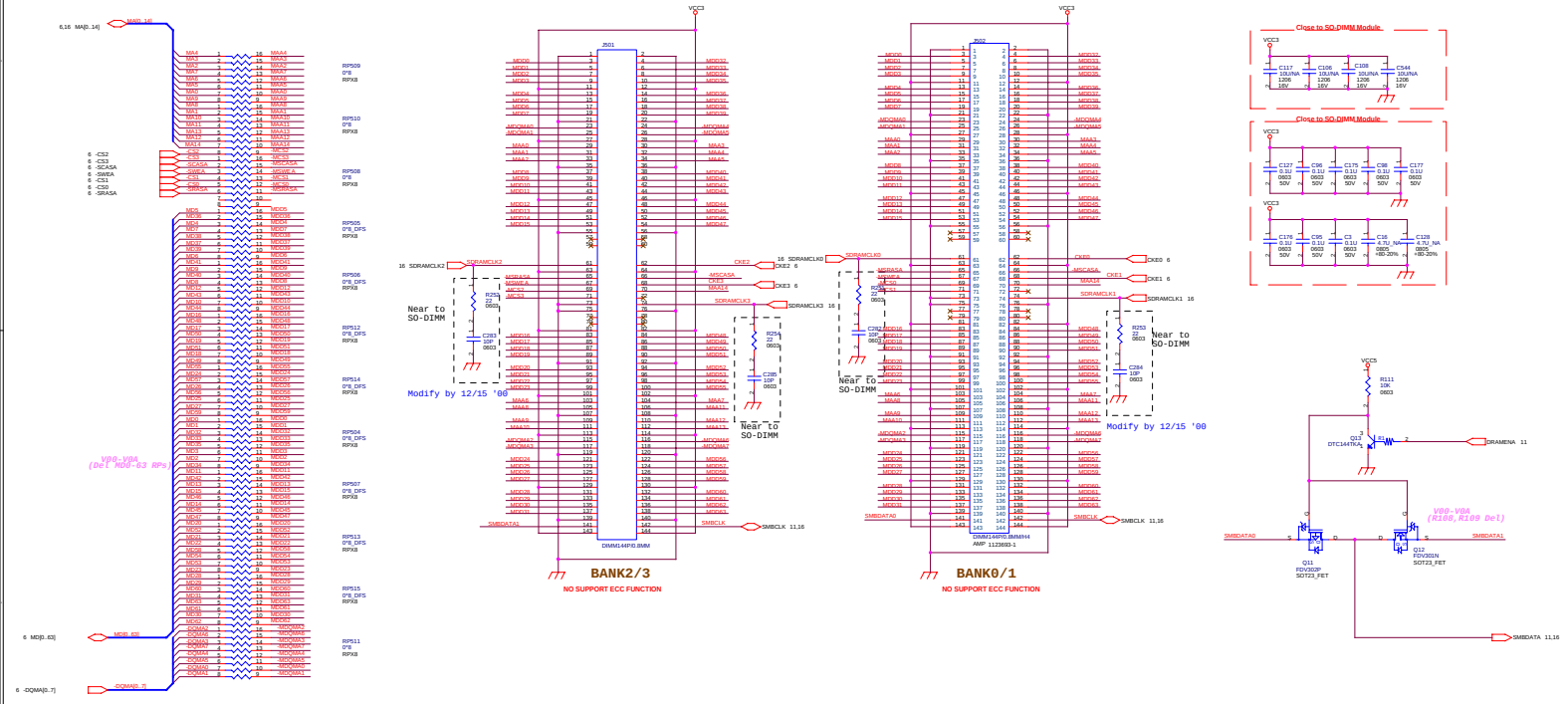


NORTH BRIDGE PARTIAL II



SYSTEM MEMORY

SO-DIMM Module



Layout Note:

NB	2.0"<L1<4.0"	DIMM1	0.4"<L2<0.5"	DIMM2

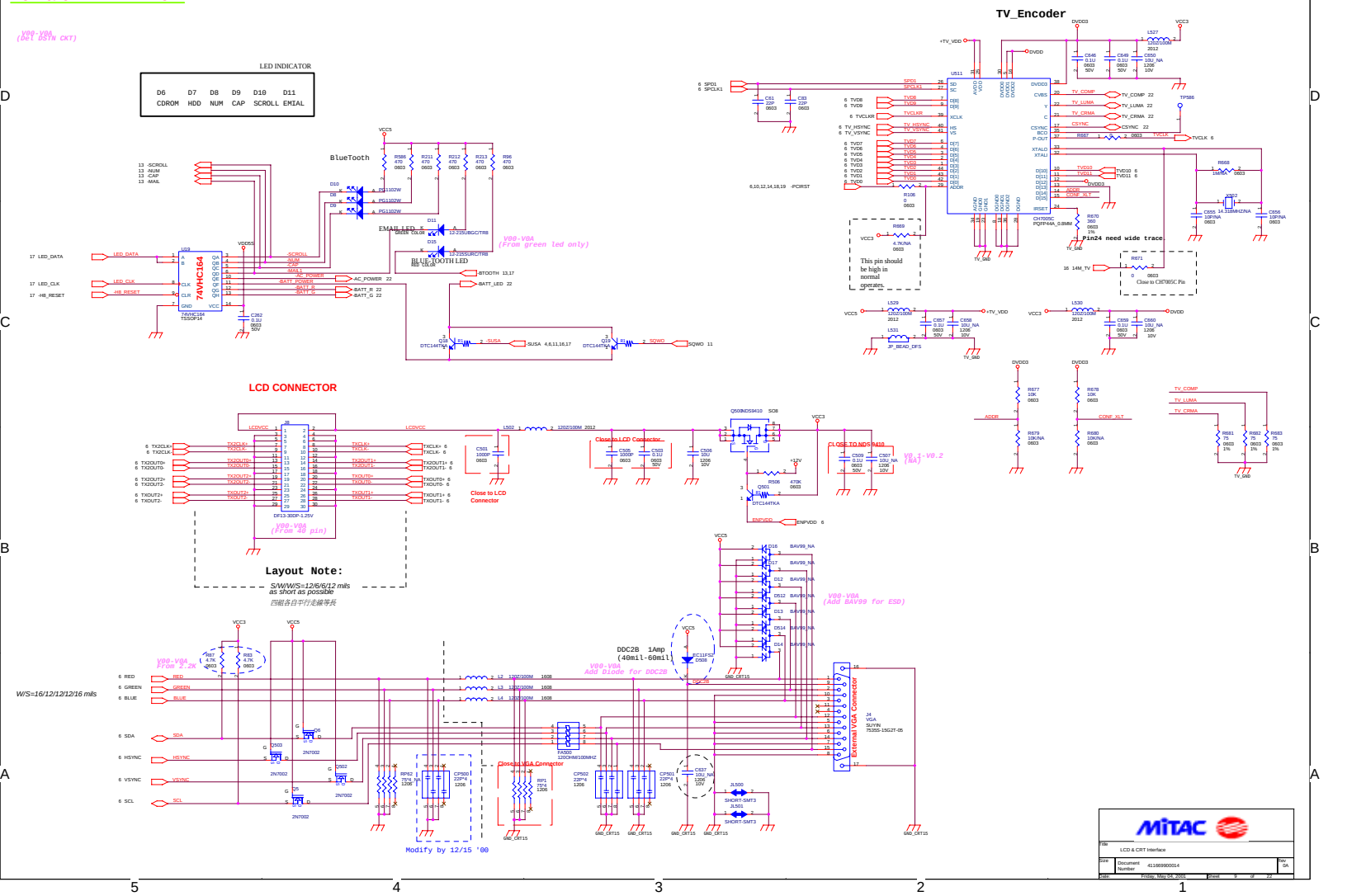
MiTAC

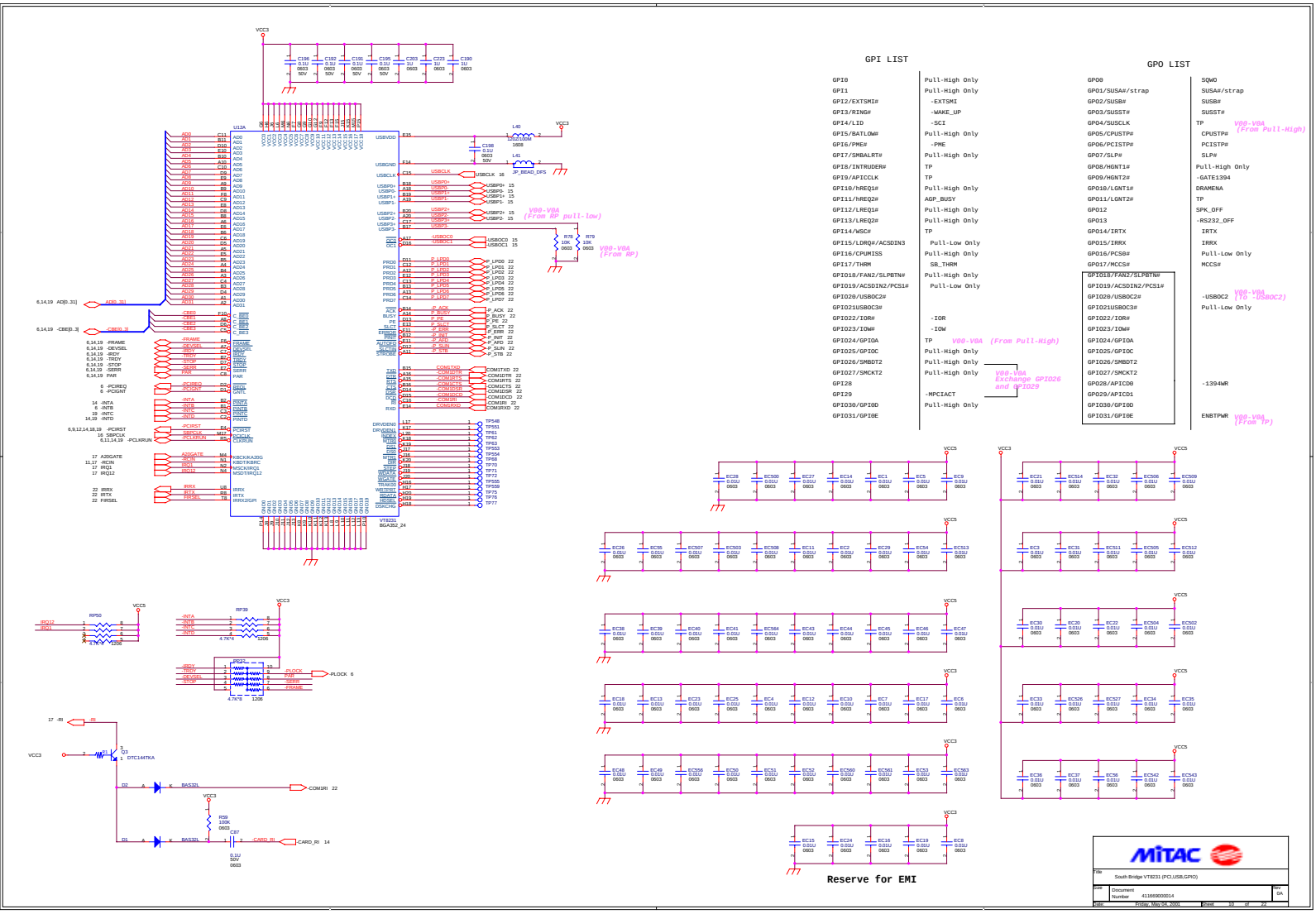
Title: System Memory

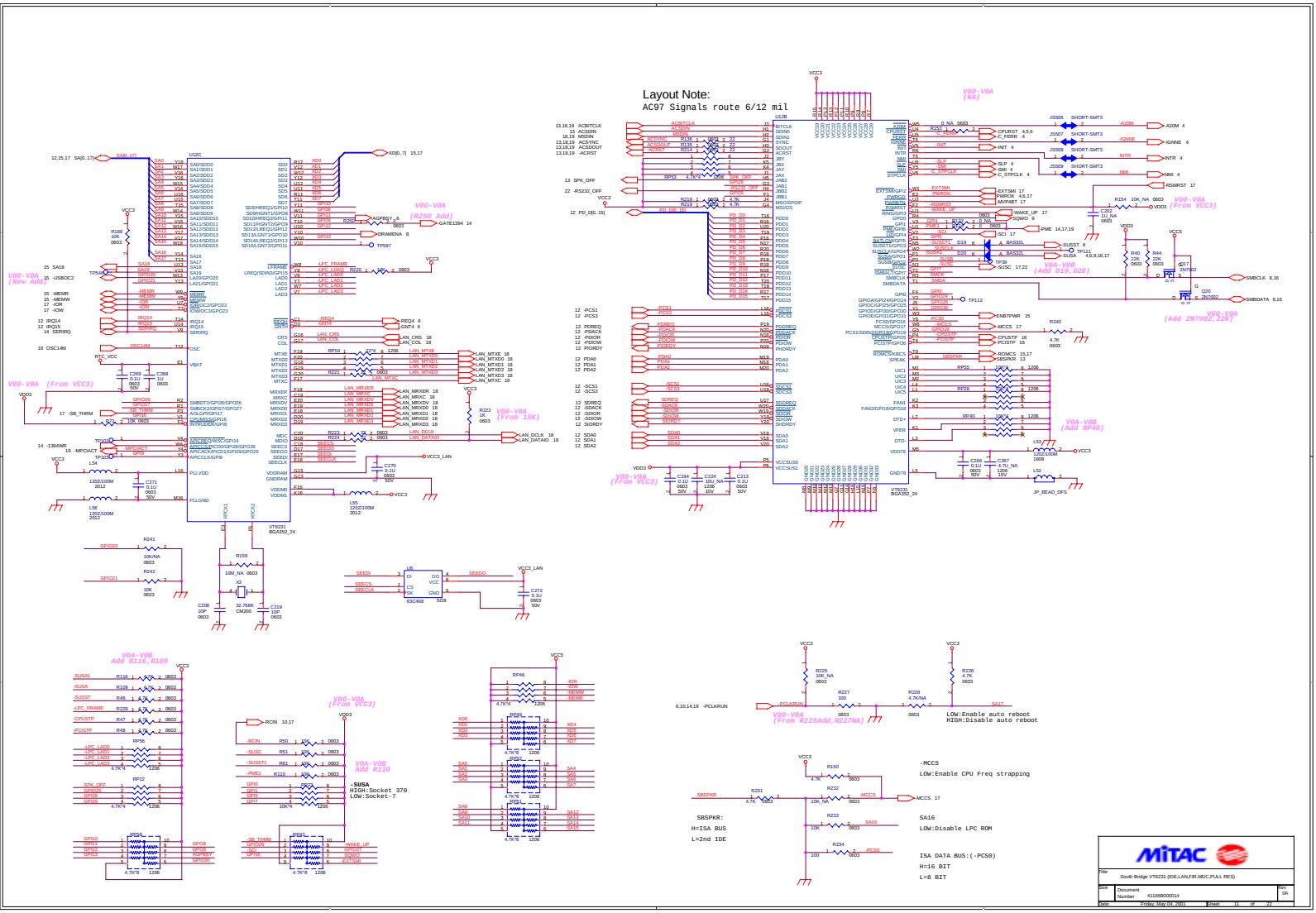
Size: Document Number: 411669900014 Rev: 0A

Date: Friday, May 04, 2001 Sheet 8 of 22

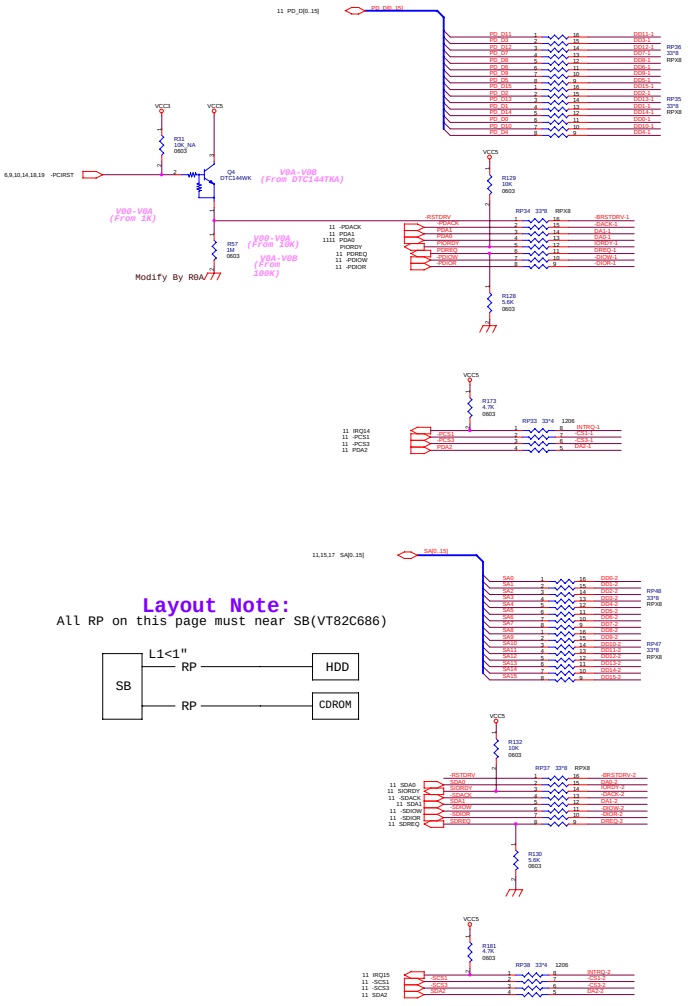
LCD & CRT INTERFACE



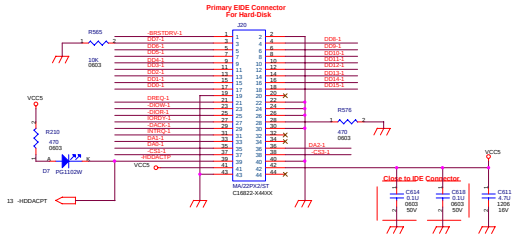


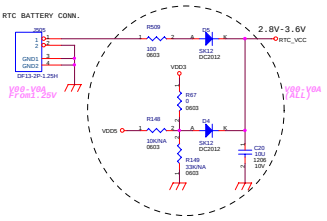


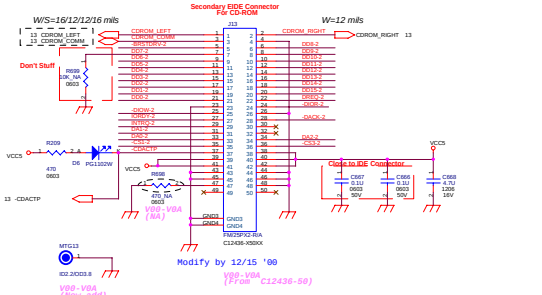
ENHANCED IDE



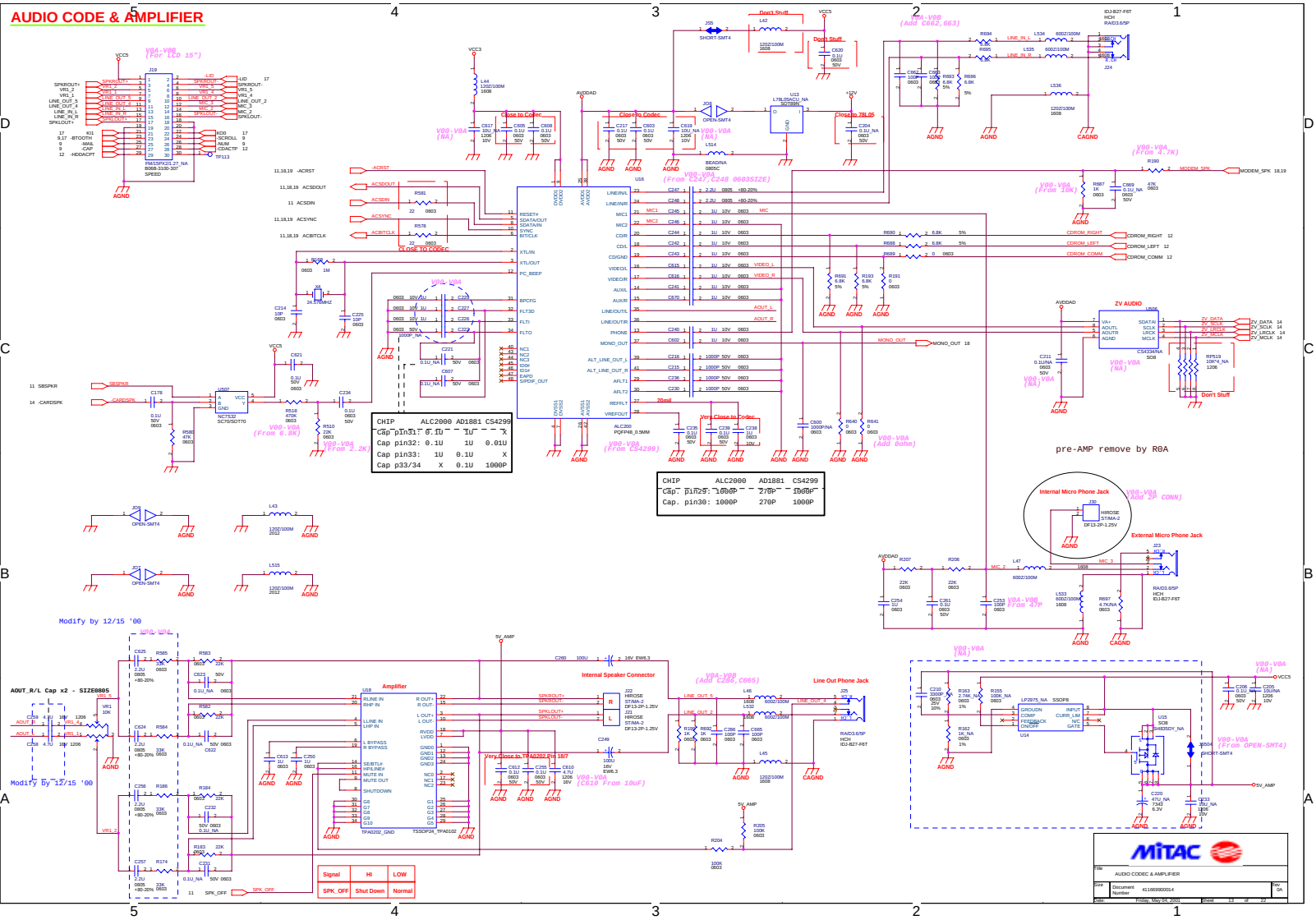
Layout Note:
All RP on this page must near SB(VT82C686)

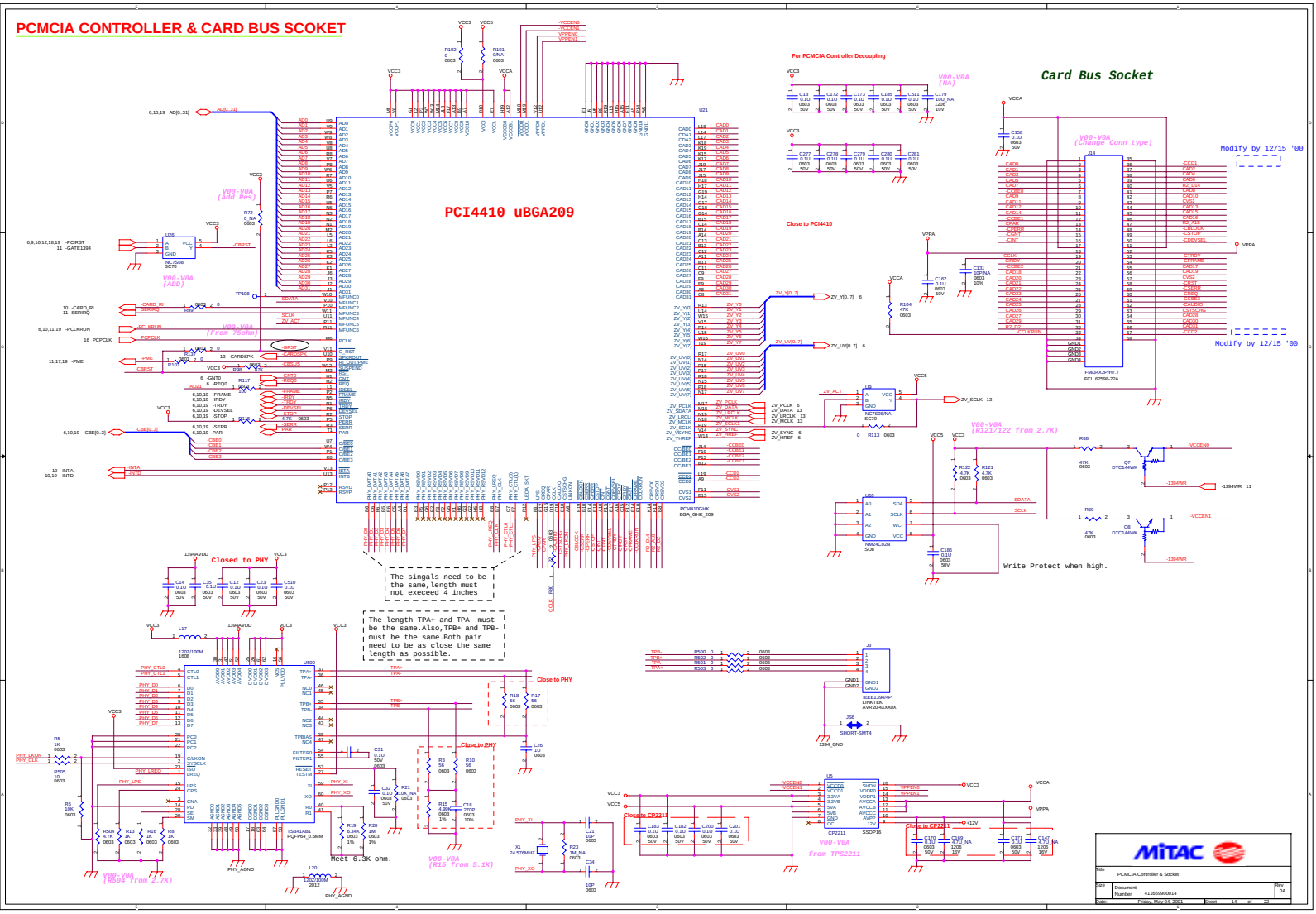


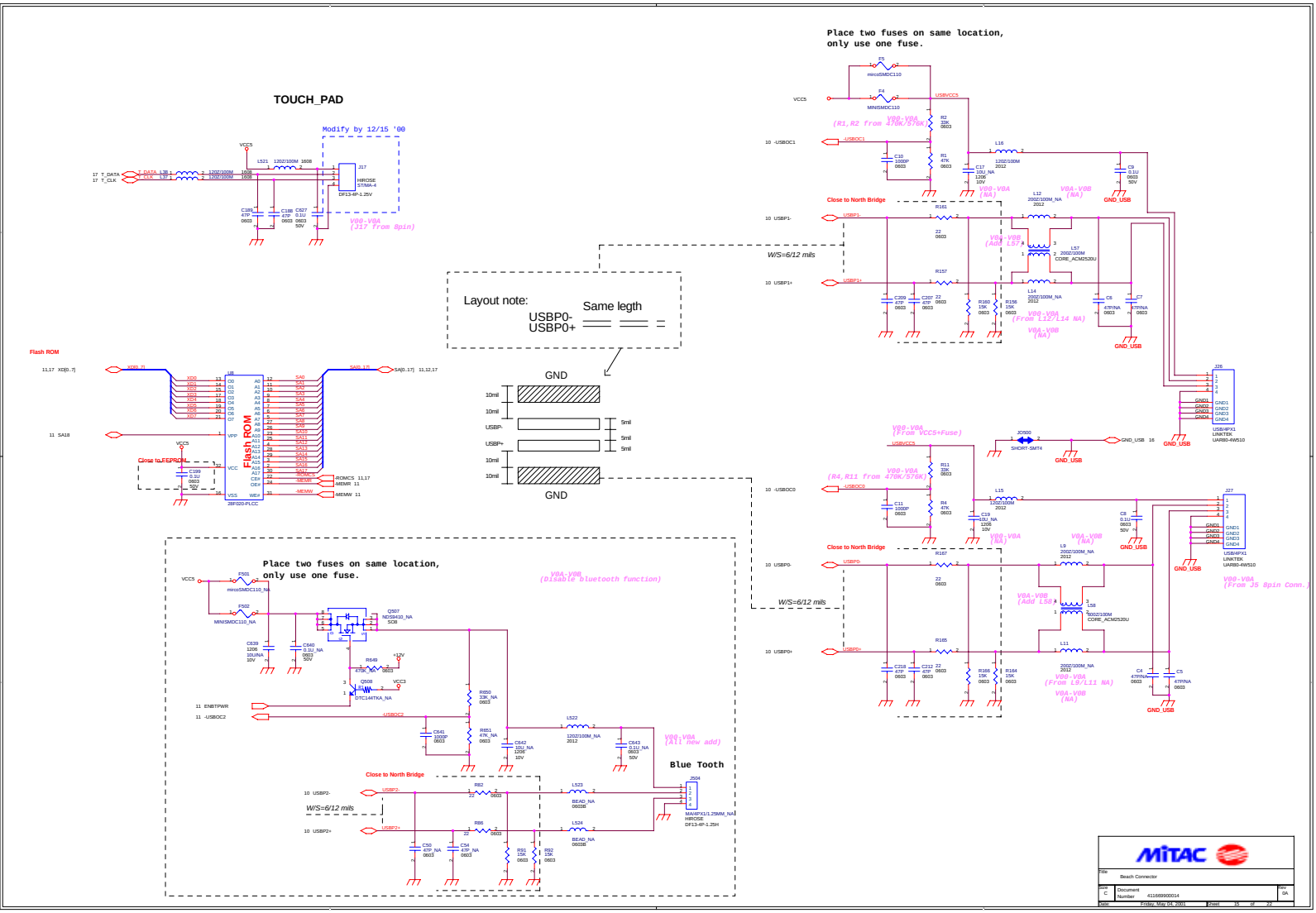




Title	EIDE & Floppy		
Size C	Document Number 411669900014		Rev 0A
Date: Friday, May 04, 2001	Sheet 12 of 22		





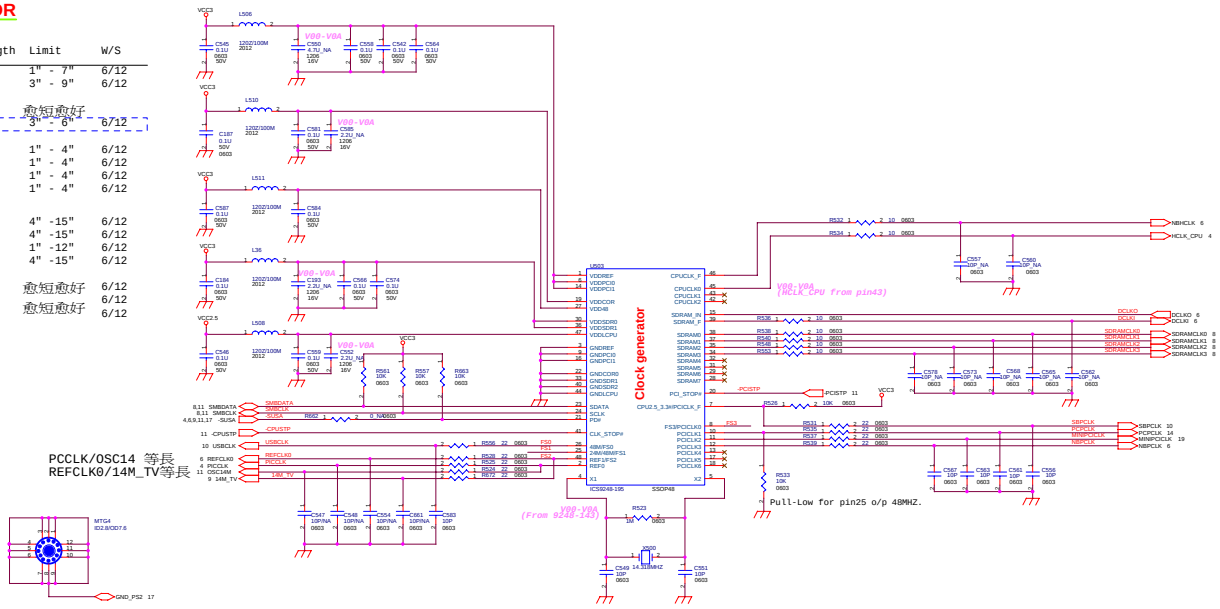


CLOCK GENERATOR

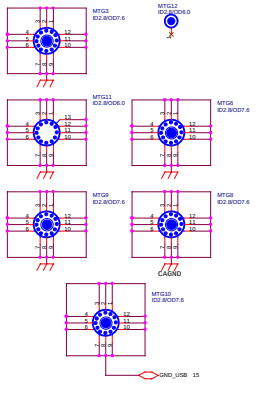
Layout Note:

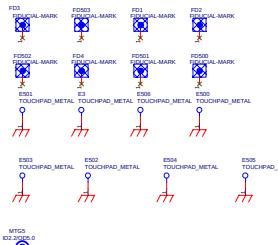
Signal Name	Trace Length	Limit	W/S
HCLK_CPU	Lcpu	1" - 7"	6/12
NBHCLK	Lcpu+2"	3" - 9"	6/12
DCLKO	Modify by 12/15 '00	愈短愈好	
DCLK1	Lsd+2"	3" - 6"	6/12
SDRAMCLK0	Lsd	1" - 4"	6/12
SDRAMCLK1	Lsd	1" - 4"	6/12
SDRAMCLK2	Lsd	1" - 4"	6/12
SDRAMCLK3	Lsd	1" - 4"	6/12
SBPCLK	Lpci	4" -15"	6/12
PCPCLK	Lpci	4" -15"	6/12
MINIPCCLK	Lpci-3"	1" -12"	6/12
NBPCLK	Lpci	4" -15"	6/12
REFCLK0		愈短愈好	6/12
PICCLK	L14m	愈短愈好	6/12
OSC14M	L14m	愈短愈好	6/12

PCCLK/OSC14 等長
REFCLK0/14M_TV等長



Screw Hole



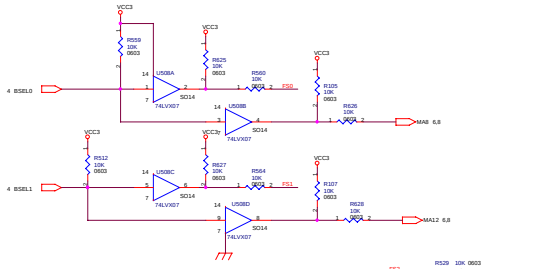


Configuration of Pin 10 will select the freq. of Pin 25. Verify the results with spec. Correcting to mount 10k pull-high or 0 pull-low.
H:24MHZ L:48MHZ

Frequency Select

FS3	FS2	FS1	FS0	CPU(MHZ)	PCI(MHZ)
0	0	0	0	66.67	33.33
0	0	0	1	100.00	33.33
0	0	1	0	100.00	33.33
0	0	1	1	133.33	33.33
0	1	0	0	105.00	35.00
0	1	0	1	133.37	33.34
0	1	1	0	137.00	34.25
0	1	1	1	75.00	37.50
1	0	0	0	100.00	33.33
1	0	0	1	95.00	31.67
1	0	1	0	97.00	32.33
1	0	1	1	133.33	33.33
1	1	0	0	90.00	30.00
1	1	0	1	96.22	32.07
1	1	1	0	66.82	33.41
1	1	1	1	91.50	30.50

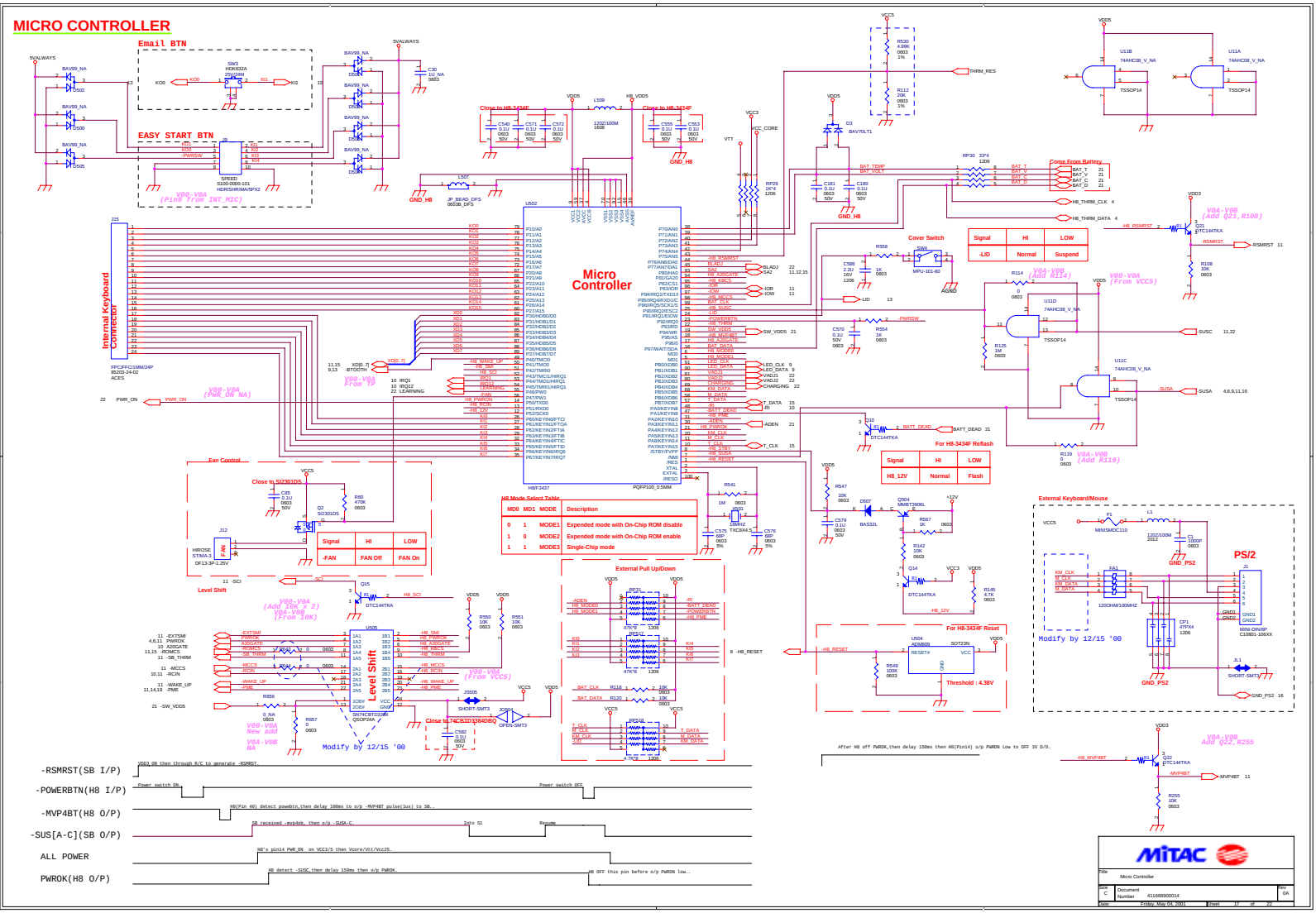
Internal Pull-Up 120Kohm

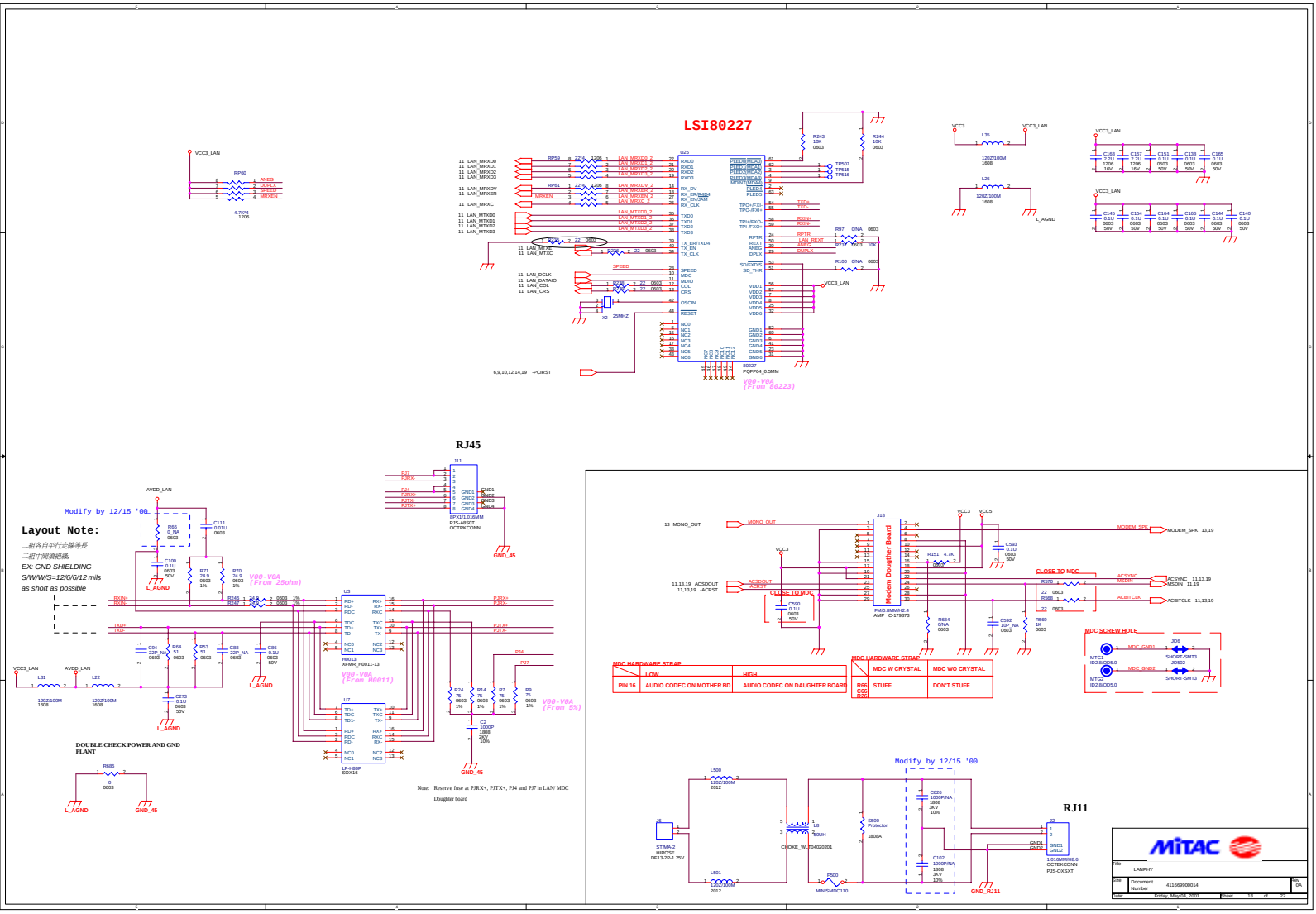


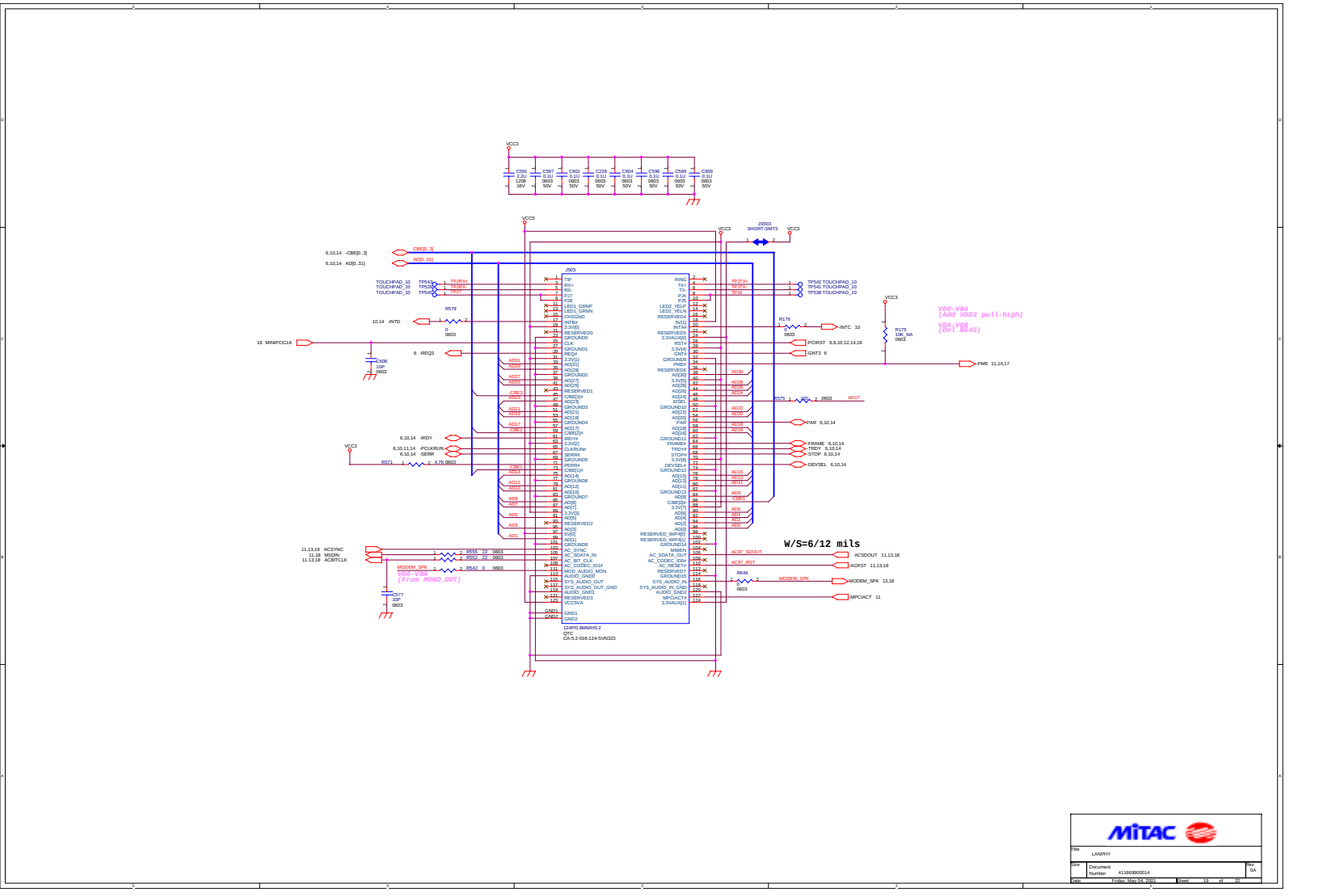
MA12	MA8	CPU(MHZ)
0	0	66.67
0	1	100.00
1	0	AUTO
1	1	133.33

MiTAC

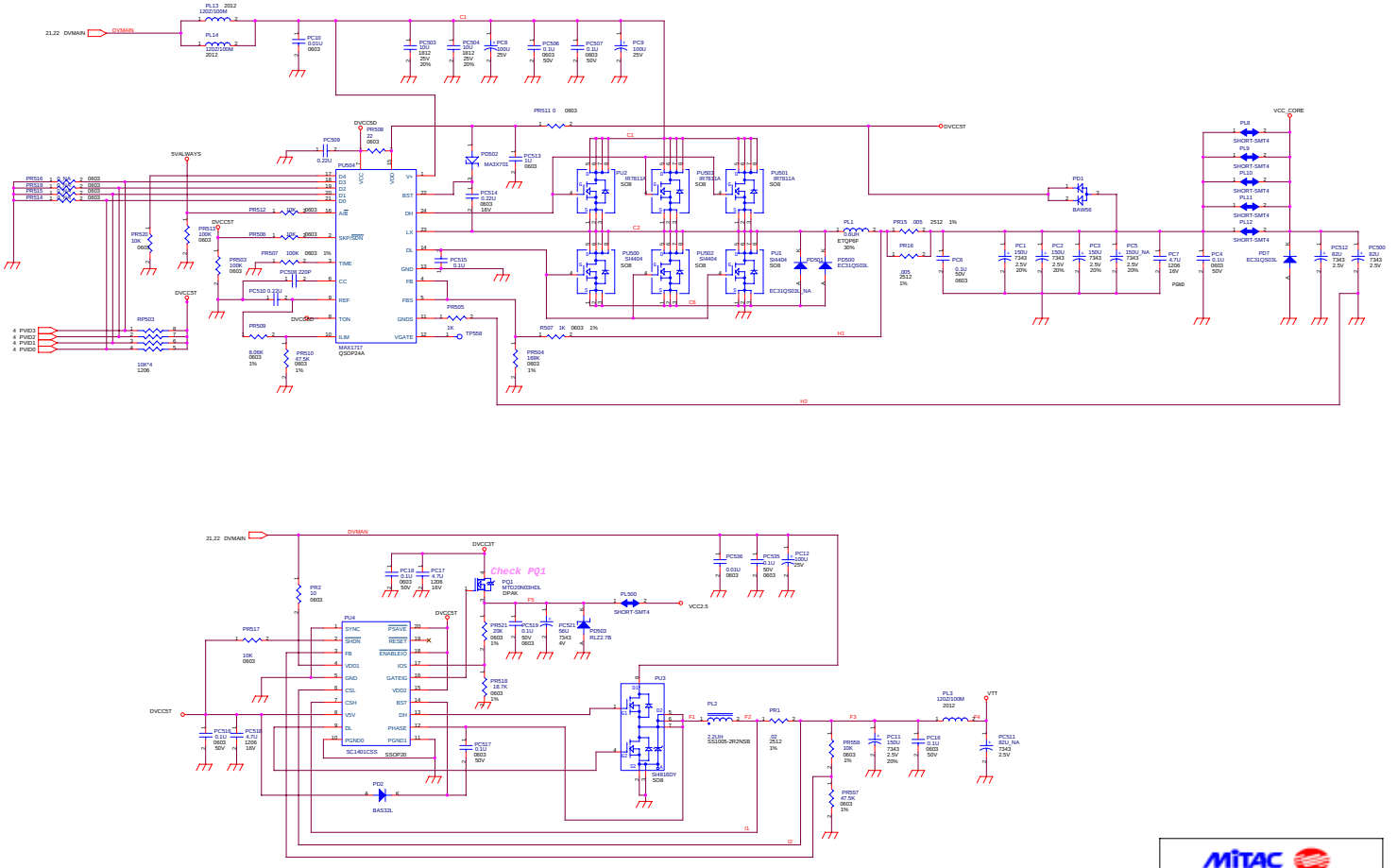
Title: CLOCK GENERATOR
Size: C | Document Number: 411669000014 | Rev: 0A
Date: Friday, May 04, 2001 | Sheet 16 of 22

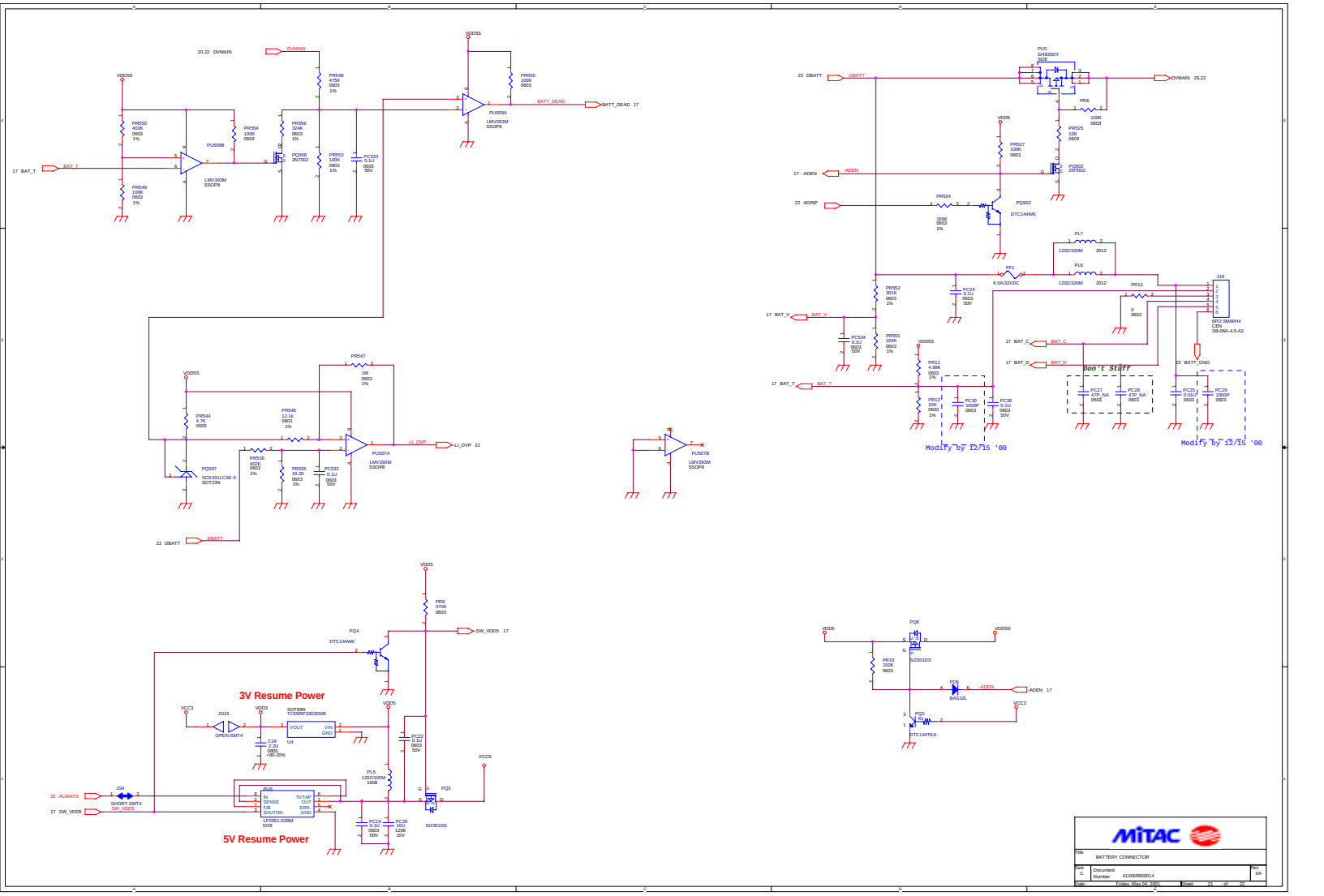


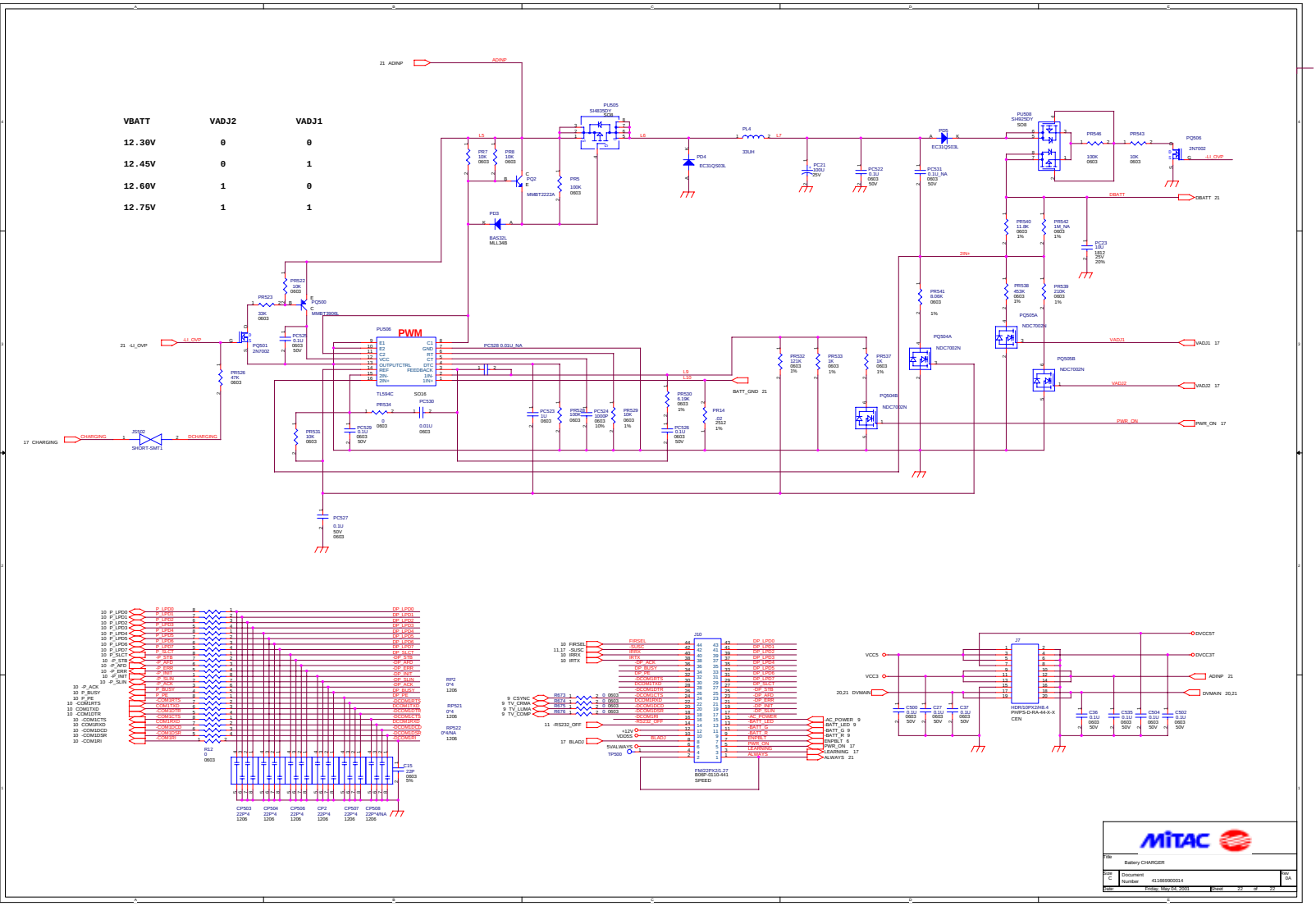




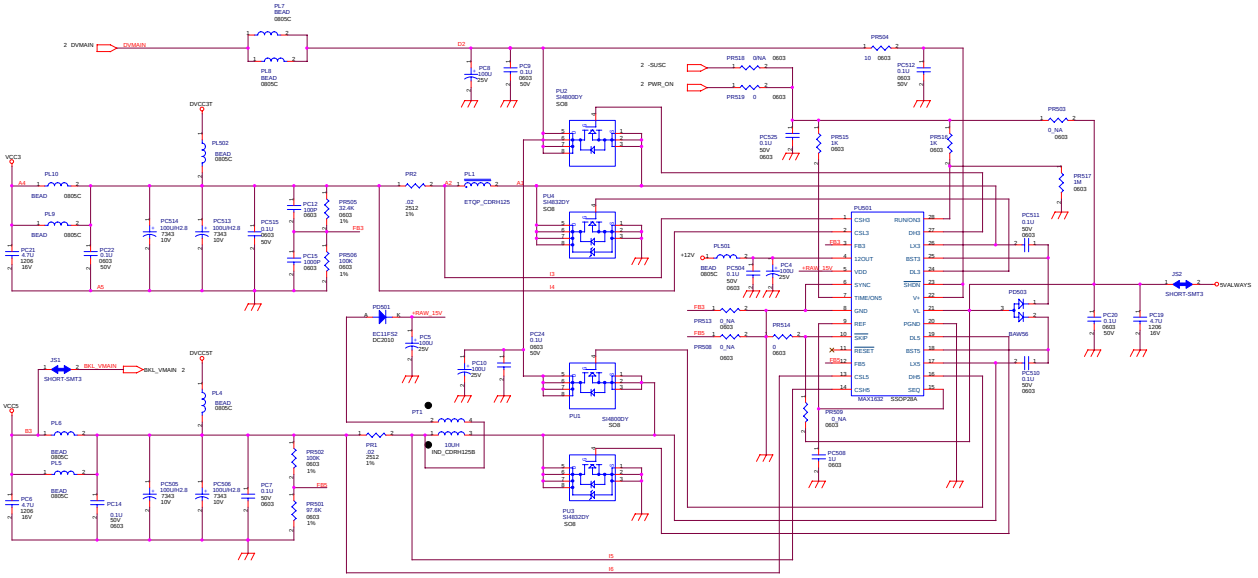
CPU Core POWER



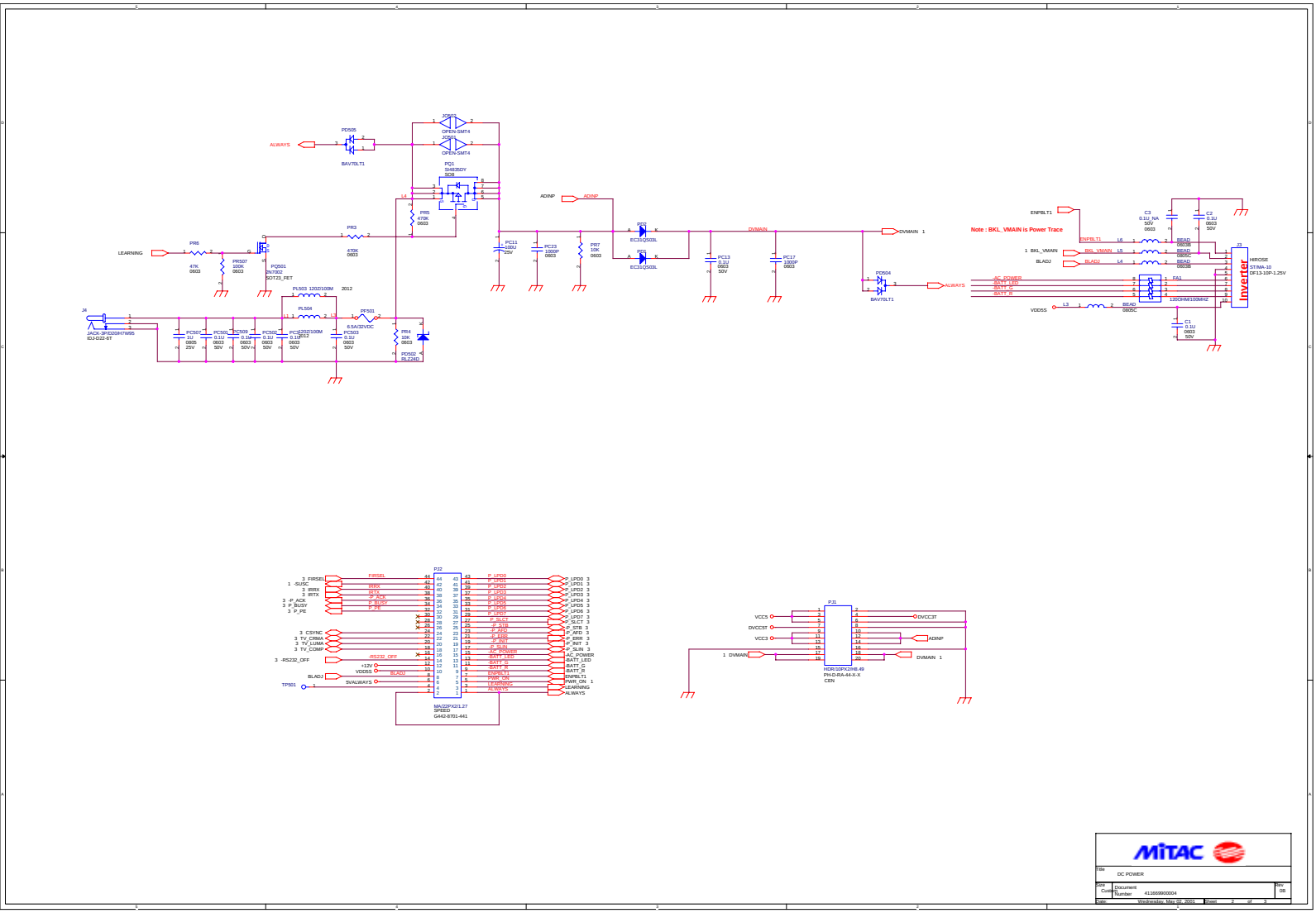


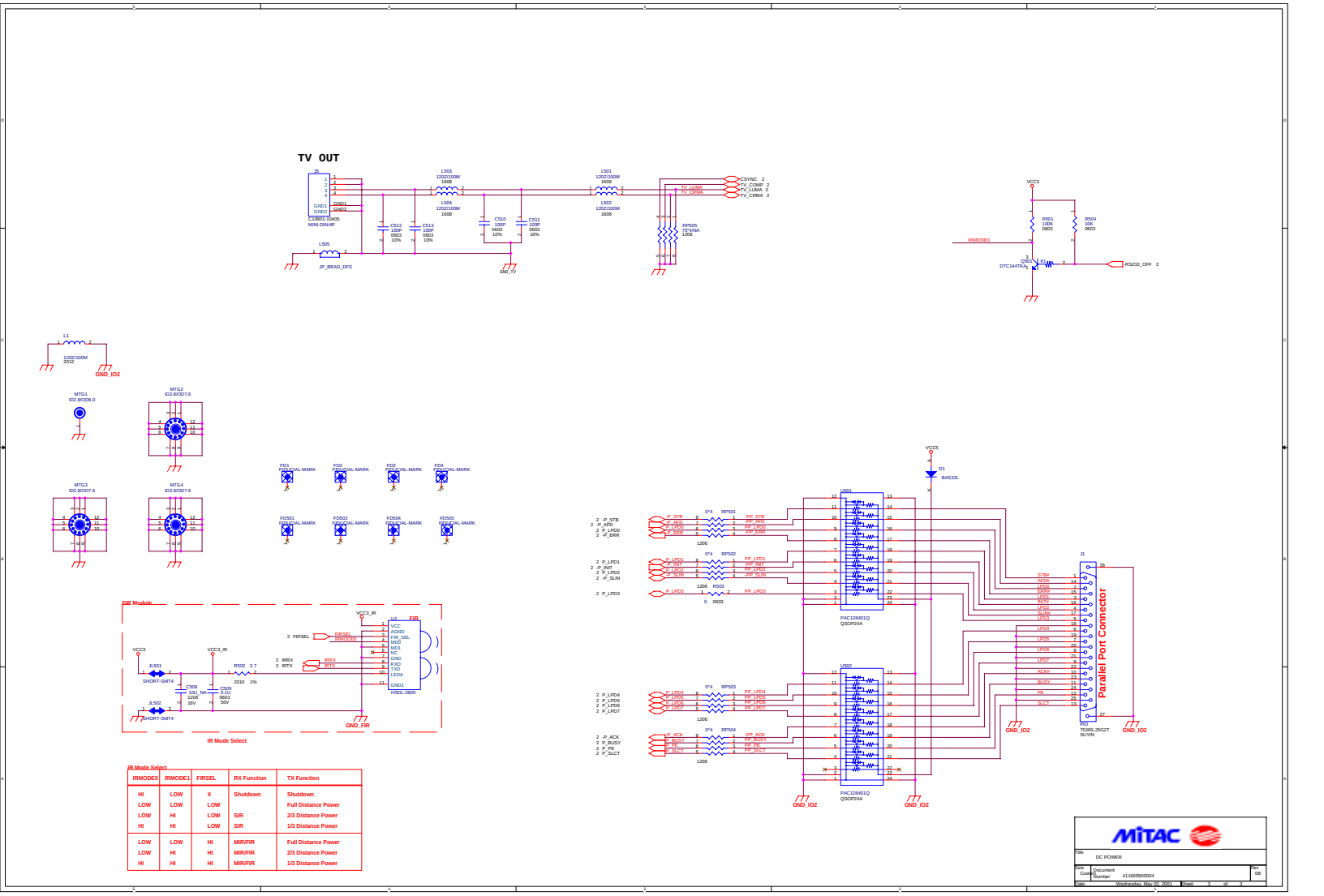


SYSTEM POWER (5V 3V 12V)

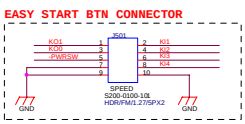


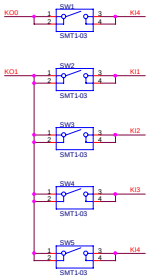
Title	SYSTEM POWER		
Size	Document Number	411660900004	Rev 09
Date	Wednesday, May 02, 2001	Sheet 1 of 3	

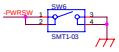


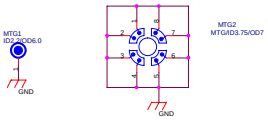


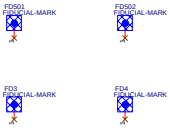
7170 ESB





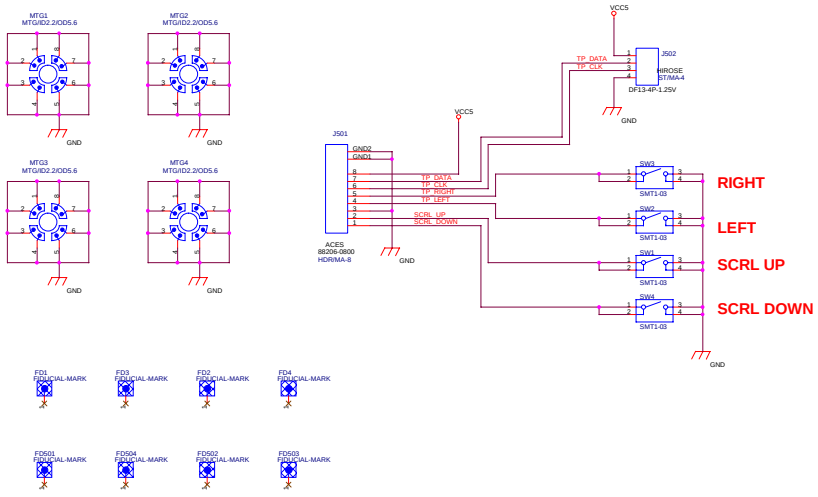






MiTAC		
Title	7170 EASY START BOARD	
Size C	Document Number 411669900007	Rev 00
Date: Wednesday, April 04, 2001	Sheet 1 of 1	

7170 TOUCH PAD BOARD



MiTAC		
Title	7170 T/P	
Size C	Document Number 411669900006	Rev 06
Date: Monday, May 07, 2001	Sheet 1 of 1	

SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR 7170

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