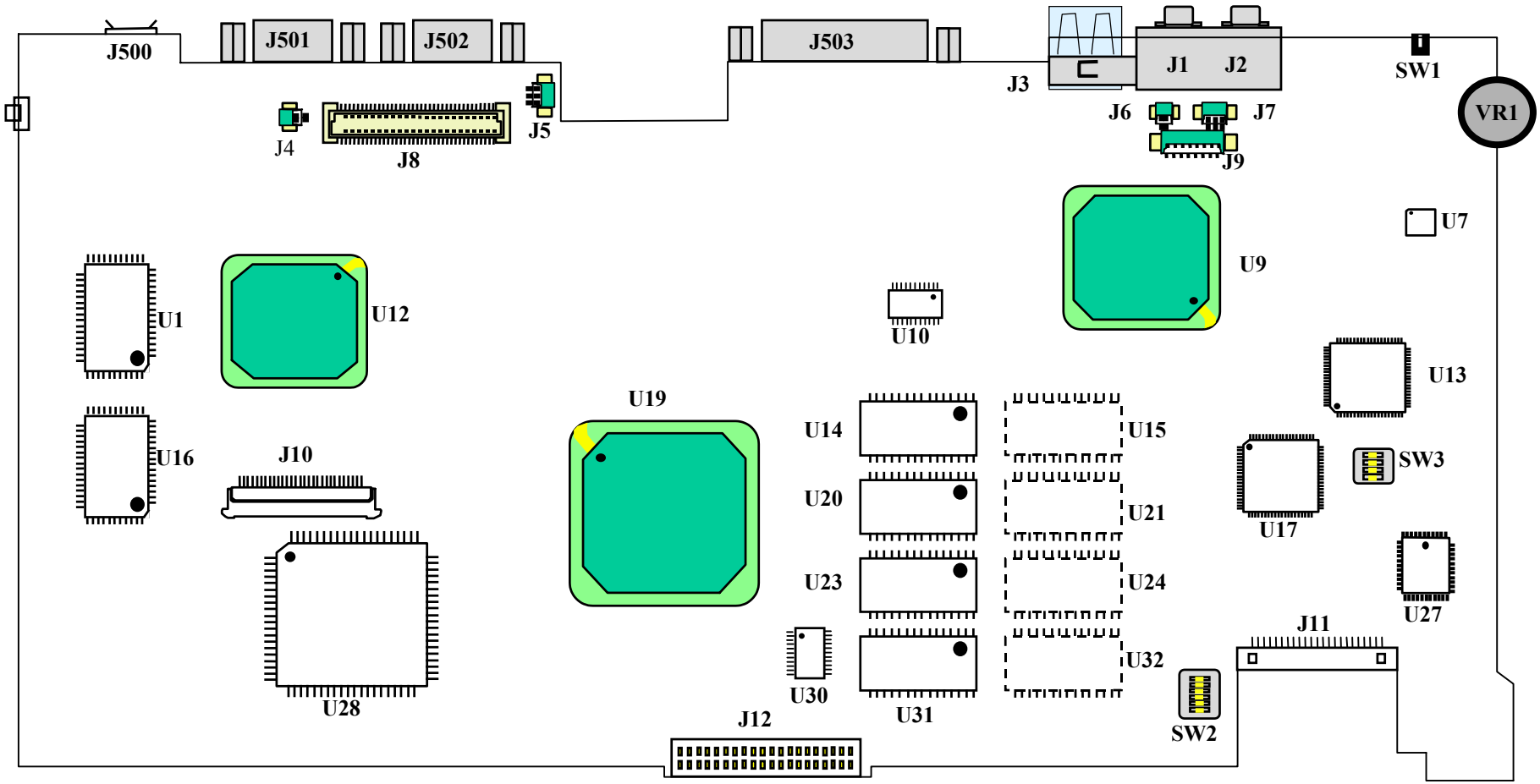
6233 N/B MAINTENANCE

6233 N/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS / SWITCHES (A)

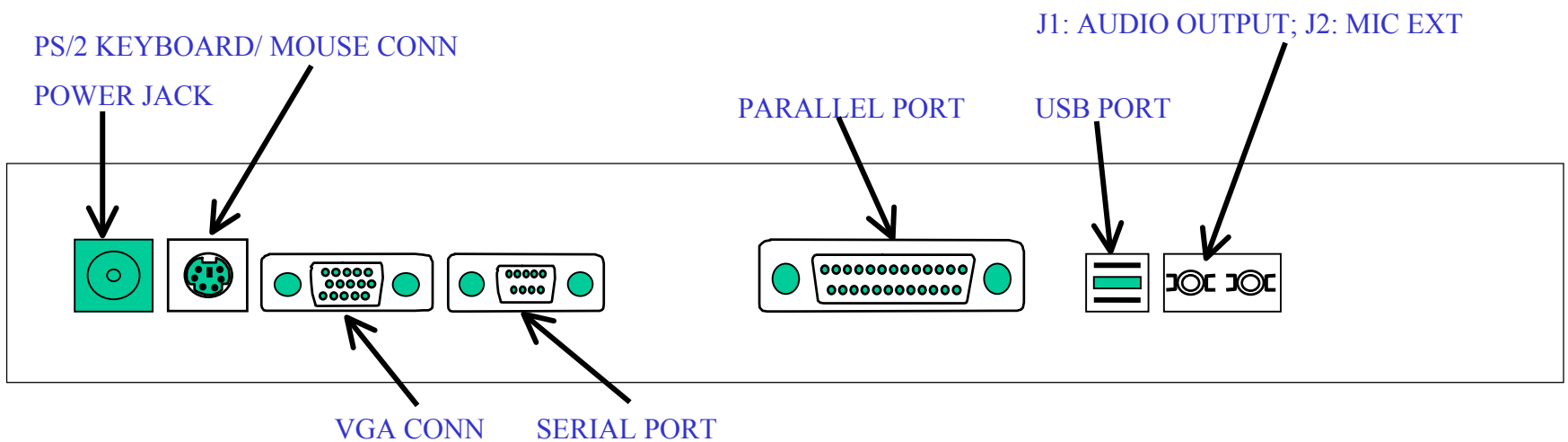
- J1: AUDIO OUTPUT.
- J2: MIC EXT.
- J3: USB PORT.
- J4,J6: R/L SPK CONN.
- J5: CPU FAN CONN.
- J7: INTERNAL MIC CONN.
- J8: LCD PANEL TRANS. BD CONNECTOR.
- J9: INVERTER BD CONN.
- J10: KEYBOARD CONN.
- J11: FDD CONN.
- J12: TOUCHPAD/ HDD CONN.
- SW1: SUSPEND SWITCH.
- SW2: LCD ID/ KEY MATRIX SELECT.
- SW3: CPU SPEED SEETING
- VR1: VOLUME CONTROL VR.
- U7:CS4297 AC 97 COMPLIANT AUDIO CODEC.
- U9: PIIX4E(82371EB) SOUTH BRIDGE.
- U10: ICS W137 FREQUENCY SYNTHESIZER.
- U11,U16:SGRAM.
- U12:ATI_RAGE_LTPRO VGA CTRL.
- U13:ESS-MAESTRO-2E AUDIO CTRL.
- U14,U20,U23,U31:32MB ON-BOARD MEMORY.
- U17: NS PC93338VJG SUPER I/O CONTROLLER.
- U19: FW82443ZXM HOST BRIDGE CONTROLLER.
- U27: 32P/PLCC/SMT SYSTEM BIOS.
- U28:TI 1225 PCI-PCMCIA/CARDBUS CONTROLLER.
- U30:W40S11-02 CLOCK BUFFER.

1. DEFINITION & LOCATION OF CONNECTORS / SWITCHES (A)

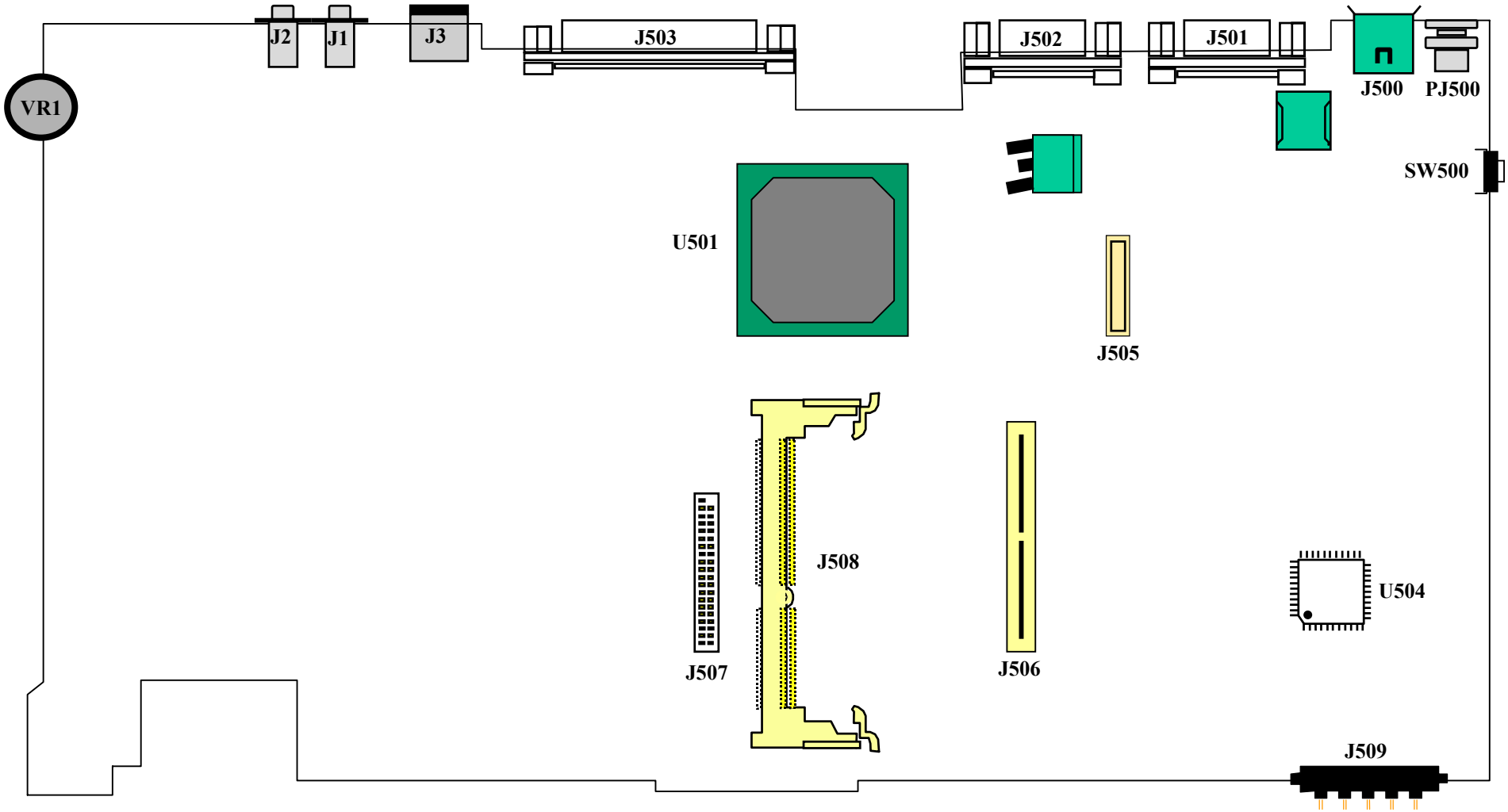


2. DEFINITION & LOCATION MAJOR COMPONENTS (SIDE B)

- PJ500: POWER JACK.
- J500: PS/2 KEYBOARD/ MOUSE CONN.
- J501: VGA CONN.
- J502: SERIAL PORT.
- J503: PARALLEL PORT.
- J505: FAX/MODEM CONNECTOR.
- J506: PCMCIA CONNECTOR.
- J507: CO-ROM CONNECTOR.
- J508: 144 PINS SODIMM SOCKET.
- J509: BATTERY CONNECTOR.
- SW500: POWER SWITCH.
- U501: CELERON CPU.
- U504: H8/F3434 KEYBOARD CONTROLLER.



2. DEFINITION & LOCATION MAJOR COMPONENTS (SIDE B)



3. PIN DESCRIPTIONS OF MAJOR COMPONENTS

3.1 INTEL CELERON PROCESSOR-1

Alphabetical Signal Reference (Sheet 1 of 8)

Signal	Type	Description
A[31:3]#	I/O	The A[35:3]# (Address) signals define a 2 36 -byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel ?Celeron?processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the Pentium II Processor Developer• Manual (Order Number 243502) for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.

(Sheet 2 of 8)

Signal	Type	Description
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. It must connect the appropriate pins of all Intel Celeron processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BSEL	I/O	This signal indicates the host bus frequency supported by the processor. A logic low indicates a host bus frequency of 66 MHz.
BR0#	I/O	The BR0# (Bus Request) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples it′ s BR0# pin on the active-to-inactive transition of RESET# to obtain it′ s symmetric agent ID. The processor asserts BR0# to request the system bus.
CPUPRES# (PPGA only)	O	The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.
D[63:0]#	I/O	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all Intel Celeron processor system bus agents.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
DRDY#	I/O	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all Intel Celeron processor system bus agents.
EDGCTRL	I	The EDGCTRL input provides GTL+ edge control and should be pulled up to VCC CORE with a 51 Ω ?% resistor.
EMI (S.E.P.P. only)	I	EMI pins should be connected to motherboard ground and/or to chassis ground through zero ohm (0Ω) resistors. The zero ohm resistors should be placed in close proximity to the Intel Celeron processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.

3.1 INTEL CELERON PROCESSOR-2

Alphabetical Signal Reference (Sheet 3 of 8)

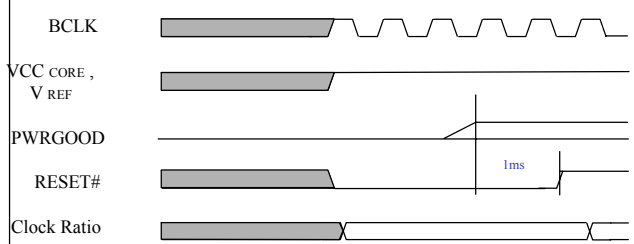
Signal	Type	Description
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration. See Pentium Pro Family Developer• Manual, Volume 1: Specifications (Order Number 242690) for details.
HIT#, HITM#	I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all Intel Celeron processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

(Sheet 4 of 8)

Signal	Type	Description
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium ?processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PPGA only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to VCC CORE through a low-pass filter that minimizes jitter.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

3.1 INTEL CELERON PROCESSOR-3

Alphabetical Signal Reference (Sheet 5 of 8)

Signal	Type	Description
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (VCC CORE , etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. Figure 23 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14 and Table 15, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must remain active for one microsecond for a • arm?Reset; for a power-on Reset, RESET# must stay active for at least one millisecond after VCC CORE and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Pentium Pro Family Developer• Manual, Volume 1: Specifications (Order Number 242690). The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.
SMI#	I	The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

(Sheet 6 of 8)

Signal	Type	Description
SLOTOCC# (S.E.P.P. only)	O	SLOTOCC# is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. This pin is not a signal; rather, it is a short to VSS. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.5), a system can determine if a SC242 connector is occupied, and whether a processor core is present. The states and values for determining the type of cartridge in the SC242 connector is shown below. **SC242 Occupation Truth Table** Signal / Value / Status SLOTOCC# 0, VID[4:0] Anything other than ?1111 — Processor with core in SC242 connector. SLOTOCC# 0, VID[4:0] 11111 — Terminator cartridge in SC242 connector (i.e., no core present). SLOTOCC# 1, VID[4:0] Any value — SC242 connector not occupied.
SLP#	I	The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.

3.1 INTEL CELERON PROCESSOR-4

Alphabetical Signal Reference (Sheet 7 of 8)

Signal	Type	Description
TESTHI (S.E.P.P. only)	I	Refer to Section 2.6 for implementation details.
THERMDN	O	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.
THERMDP	I	Thermal Diode p-n junction. Used to calculate core temperature. See Section 4.1.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 • . This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
VCC 1.5 (PPGA only)	I	The VCC CMOS pin provides the CMOS voltage for use by the platform. The 2.5V must be provided to the VCC 2.5 input and 1.5V must be provided to the VCC 1.5 input. The processor re-routes the 2.5V input to the VCC CMOS output via the package. Future processors requiring 1.5V CMOS voltage levels will route the 1.5V at the VCC 1.5 input to the VCC CMOS output.
VCC 2.5 (PPGA only)	I	The VCC CMOS pin provides the CMOS voltage for use by the platform. The 2.5V must be provided to the VCC 2.5 input and 1.5V must be provided to the VCC 1.5 input. The processor re-routes the 2.5V input to the VCC CMOS output via the package. Future processors requiring 1.5V CMOS voltage levels will route the 1.5V at the VCC 1.5 input to the VCC CMOS output.
VCC CMOS (PPGA only)	O	The VCC CMOS pin provides the CMOS voltage for use by the platform. The 2.5V must be provided to the VCC 2.5 input and 1.5V must be provided to the VCC 1.5 input. The processor re-routes the 2.5V input to the VCC CMOS output via the package. Future processors requiring 1.5V CMOS voltage levels will route the 1.5V at the VCC 1.5 input to the VCC CMOS output.

(Sheet 8 of 8)

Signal	Type	Description
VCORE DET (PPGA only)	O	The VCORE DET signal will float for 2.0 V core processors and will be grounded for future processors with a lower core voltage.
VID[4:0] (S.E.P.P.) VID[3:0] (PPGA)	O	The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 1 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V REF [7:0] (PPGA only)	I	These input signals are used by the GTL+ inputs as a reference voltage. GTL+ inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low.

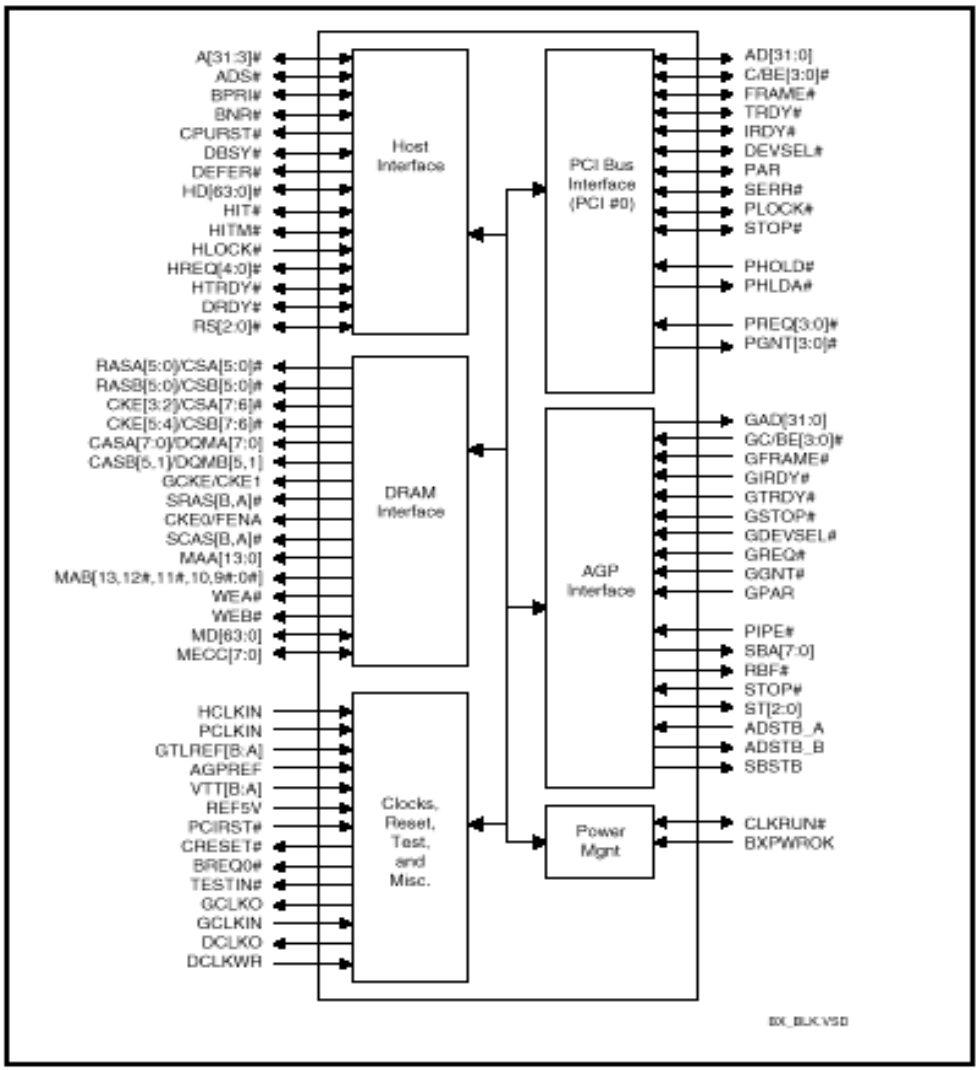
3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-1

•Intel 82443ZX Features:

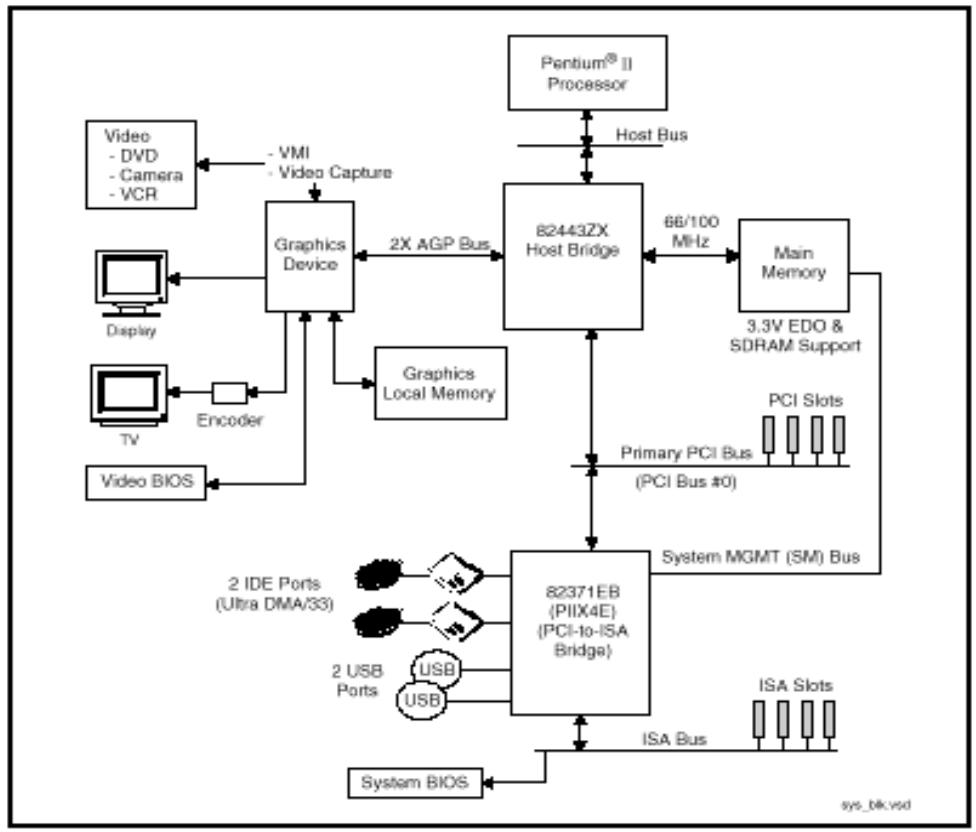
- Processor/host bus support
  - — Optimized for Pentium® II processor at 100 MHz system bus frequency; Support for 66 MHz
  - — In-order transaction and dynamic deferred transaction support
  - — Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power)
- Integrated DRAM controller
  - — 8 to 256Mbytes
  - — Supports 2 double-sided DIMMs (4 rows memory)
  - — 64-bit data interface
  - — Unbuffered SDRAM (Synchronous) DRAM Support (x-1-1-1 access @ 66 MHz, x-1-1-1 access @ 100 MHz)
  - — Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2k, 4k and 8k page sizes
- PCI bus interface
  - — PCI Rev. 2.1, 3.3V and 5V, 33MHz interface compliant
  - — PCI Parity Generation Support
  - — Data streaming support from PCI to DRAM
  - — Delayed Transaction support for PCI-DRAM Reads
  - — Supports concurrent CPU, AGP and PCI transactions to main memory
- AGP interface
  - — Supports single AGP compliant device (AGP-66/133 3.3V device)
  - — AGP Specification Rev 1.0 compliant
  - — AGP-data/transaction flow optimized arbitration mechanism
  - — AGP side-band interface for efficient request pipelining without interfering with the data streams
  - — AGP-specific data buffering
  - — Supports concurrent CPU, AGP and PCI transactions to main memory
  - — AGP high-priority transactions ("expedite") support
- Power Management Functions
  - — Stop Clock Grant and Halt special cycle translation (host to PCI Bus)
  - — Dynamic power down of idle DRAM rows
  - — Independent, internal dynamic clock gating reduces average power dissipationt
- Packaging/Voltage
  - — 492 Pin BGA
  - — 3.3V core and mixed 3.3V and GTL I/O
- Supporting I/O Bridge
  - — System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD)
  - — PCI-ISA Bridge (PIIX4E)
  - — 3.3V core and mixed 5V, 3.3V I/O and interface to the 2.5V CPU signals via open-drain output buffers

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-2

•Intel 82443ZX Simplified Block Diagram:



•Intel 440ZX AGPset System Block Diagram:



3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-3

Table 3.2.1. Host Interface Signals (Sheet 1 of 2)

Name	Type	Description
CPURST#	O GTL+	**CPU Reset.** The CPURST# pin is an output from the 82443ZX. The 82443ZX generates this signal based on the PCIRST# input (from PIIX4E) and also the SUSTAT# pin in mobile mode. The CPURST# allows the CPUs to begin execution in a known state.
A[31:3]#	I/O GTL+	**Address Bus:** A[31:3]# connect to the CPU address bus. During CPU cycles, the A[31:3]# are inputs.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.
ADS#	I/O GTL+	**Address Strobe:** The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O GTL+	**Priority Agent Bus Request:** The 82443ZX is the only Priority Agent on the CPU bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O GTL+	**Symmetric Agent Bus Request:** Asserted by the 82443ZX when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.
DBSY#	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	**Defer:** The 82443ZX generates a deferred response as defined by the rules of the 82443ZX? dynamic defer policy. The 82443ZX also uses the DEFER# signal to indicate a CPU retry response.
DRDY#	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HIT#	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI or AGP snoopable access to DRAM is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O GTL+	**Request Command:** Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 82443ZX Host Bridge are defined in the Host Interface section of this document.
HTRDY#	I/O GTL+	**Host Target Ready:** Indicates that the target of the CPU transaction is able to enter the data transfer phase.

Table 3.2.1. Host Interface Signals (Sheet 2 of 2)

Name	Type	Description
RS[2:0]#	I/O GTL+	**Response Signals:** Indicates type of response according to the following the table: **RS[2:0] Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by 82443ZX) 100 Hard Failure (not driven by 82443ZX) 101 No data response 110 Implicit Writeback 111 Normal data response

Table 3.2.2. Host Signals Not supported by the 82443ZX

Signal	Function	Not Supported By 82443ZX
A[35:32]#	Address	Extended addressing (over 4 GB)
AERR#	Address Parity Error	Parity protection on address bus
AP[1:0]#	Address Parity	Parity protection on address bus
BINIT#	Bus Initialization	Checking for bus protocol violation and protocol recovery mechanism
DEP[7:0]#	Data Bus ECC/Parity	Enhanced data bus integrity
IERR#	Internal Error	Direct internal error observation via IERR# pin
INIT#	Soft Reset	Implemented by PIIX4E, BIST supported by external logic.
BERR#	Bus Error	Unrecoverable error without a bus protocol violation
RP#	Request Parity	Parity protection on ADS# and PREQ[4:0]#
RSP#	Response Parity Signal	Parity protection on RS[2:0]#

Table 3.2.3. DRAM Interface Signals (Sheet 1 of 2)

Name	Type	Description
RASA[3:0]# /CSA[3:0]# RASB[3:0]# /CSB[3:0]#	O CMOS	**Row Address Strobe (EDO):** These signals are used to latch the row address on the MAxx lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. **Chip Select (SDRAM):** For the memory row configured with SDRAM these pins perform the function of selecting the particular SDRAM components during the active state. Note that there are 2 copies of RAS# per physical memory row to improve the loading.
CKE[3:2]	O CMOS	CKE is used to dynamically power down inactive SDRAM rows. Note that there are 2 copies of CS# per physical memory row to reduce the loading.
CASA[7:0]# /DQMA[7:0]	O CMOS	**Column Address Strobe A-side (EDO):** The CASA[7:0]# signals are used to latch the column address on the MA[13:0] lines into the DRAMs of the A half of the memory array. These are active low signals that drive the DRAM array directly without external buffering. **Input/Output Data Mask A-side (SDRAM):** These pins control the A half of the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-4

Table 3.2.3. DRAM Interface Signals (Sheet 2 of 2)

Name	Type	Description
GCKE/CKE1	O CMOS	**Global CKE (SDRAM):** Global CKE is normally used in an 82443BX 4 DIMM configuration requiring power down mode for the SDRAM. External logic must be used to implement this function in an 82443BX. This function is not supportrd in an 82443ZX. **SDRAM Clock Enable (CKE1):** In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. The combination of SDRAMPWR (SDRAM register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, ? RAMC? RAM Control Register (Device 0)?on page 3-19) for more details.
SRAS[A]#	O CMOS	**SDRAM Row Address Strobe (SDRAM):** The SRAS[A]# signal is a copy of the same logical SRASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
CKE0/FENA	O CMOS	**SDRAM Clock Enable 0 (CKE0).** In mobile mode, CKE0 SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. **FET Enable (FENA):** In a 4 DIMM configuration. FENA is used to select the proper MD path through the FET switches (refer to Section 4.3, ? RAM Interface on page 4-14 for more details). This function is not supported in the 82443ZX.
SCAS[A]#	O CMOS	**SDRAM Column Address Strobe (SDRAM):** The SCAS[A]# signal is a copy of the same logical SCASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
MAA[13:0] STRAP5 STRAP4 STRAP3 STRAP2 STRAP1 STRAP0	O CMOS	**Memory Address(EDO/SDRAM):** MAA[13:0] are used to provide the row and column address to DRAM. Each MAA[13:0] line has a programmable buffer strength to optimize for different signal loading conditions. STRAP[5:0] are described in Table 2-10, Strapping Options.
WEA#	O CMOS	**Write Enable Signal (EDO/SDRAM):** WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength to optimize for different signal loading conditions.
MD [63:0]	I/O CMOS	**Memory Data (EDO/SDRAM):** These signals are used to interface to the DRAM data bus.

Table 3.2.4. Primary PCI Interface Signals (Sheet 1 of 2)

Name	Type	Description
AD[31:0]	I/O PCI	**PCI Address/Data:** These signals are connected to the PCI address/data bus. Address is driven by the 82443ZX with FRAME# assertion, data is driven or received in the following clocks. When the 82443ZX acts as a target on the PCI Bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and input data (writes) or output data (reads) on subsequent clocks.
DEVSEL#	I/O PCI	**Device Select:** Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The 82443ZX asserts DEVSEL# based on the DRAM address range or AGP address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
FRAME#	I/O PCI	**Frame:** FRAME# is an output when the 82443ZX acts as an initiator on the PCI Bus. FRAME# is asserted by the 82443ZX to indicate the beginning and duration of an access. The 82443ZX asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the 82443ZX acts as a PCI target. As a PCI target, the 82443ZX latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	I/O PCI	**Initiator Ready:** IRDY# is an output when 82443ZX acts as a PCI initiator and an input when the 82443ZX acts as a PCI target. The assertion of IRDY# indicates the current PCI Bus initiator's ability to complete the current data phase of the transaction.
C/BE[3:0]#	I/O PCI	**Command/Byte Enable:** PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. PCI Bus command encoding and types are listed below. **C/BE[3:0]# Command Type** 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read 0011 I/O Write 0100 Reserved 0101 Reserved 0110 Memory Read 0111 Memory Write 1000 Reserved 1001 Reserved 1010 Configuration Read 1011 Configuration Write 1100 Memory Read Multiple 1101 Reserved (Dual Address Cycle) 1110 Memory Read Line 1111 Memory Write and Invalidate

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-5

Table 3.2.4. Primary PCI Interface Signals (Sheet 2 of 2)

Name	Type	Description
PAR	I/O PCI	**Parity:** PAR is driven by the 82443ZX when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the 82443ZX when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PLOCK#	I/O PCI	**Lock:** PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. The 82443ZX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
TRDY#	I/O PCI	**Target Ready:** TRDY# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.

Name	Type	Description
SERR#	I/O PCI	**System Error:** The 82443ZX asserts this signal to indicate an error condition. The SERR# assertion by the 82443ZX is enabled globally via SERRE bit of the PCICMD register. SERR# is asserted under the following conditions: In an ECC configuration, the 82443ZX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored. •The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated PCI cycle. •The 82443ZX can also assert SERR# when a PCI parity error occurs during the address or data phase. •The 82443ZX can assert SERR# when it detects a PCI address or data parity error on AGP. •The 82443ZX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperture Translation Table. •The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM). •The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture. •The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated AGP cycle.
STOP#	I/O PCI	**Stop:** STOP# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus.

Table 3.2.5. Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	**PCI Hold:** This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443ZX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.
PHLDA#	O PCI	**PCI Hold Acknowledge:** This signal is driven by the 82443ZX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.
PREQ[3:0]#	I PCI	**PCI Bus Request:** PREQ[3:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.
PGNT[3:0]#	O PCI	**PCI Grant: P**GNT[3:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

Table 3.2.6. AGP Interface Signals(Sheet 1 of 3)

Name	Type	Description
		AGP Sideband Addressing Signals 1
PIPE#	I AGP	**Pipelined Read:** This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. PIPE# is a sustained tri-state signal from masters (graphics controller) and is an input to the 82443ZX. Note that initial AGP designs may not use PIPE#.
SBA[7:0]	I AGP	**Sideband Address:** This bus provides an additional bus to pass address and command to the 82443ZX from the AGP master. Note that, when sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
		AGP Flow Control Signals
RBF#	I AGP	**Read Buffer Full.** This signal indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the 82443ZX is not allowed to return low priority read data to the AGP master on the first block. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal.

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-6

Table 3.2.6. AGP Interface Signals(Sheet 2 of 3)

Name	Type	Description
AGP Status Signals		
ST[2:0]	O AGP	**Status Bus:** This bus provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT# is asserted. When GGNT# is deasserted these signals have no meaning and must be ignored. 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously queued write command. 011 Indicates that the master is to provide high priority write data for a previously queued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the 82443ZX and an input to the master.
AGP Clocking Signals – Strobes		
ADSTB_A	I/O AGP	**AD Bus Strobe A:** This signal provides timing for double clocked data on the AD bus. The agent that is providing data drives this signal. This signal requires an 8.2K ohm external pull-up resistor.
ADSTB_B	I/O AGP	**AD Bus Strobe B:** This signal is an additional copy of the AD_STBA signal. This signal requires an 8.2K ohm external pull-up resistor.
SBSTB	I AGP	**Sideband Strobe:** THis signal provides timing for a side-band bus. This signal requires an 8.2K ohm external pull-up resistor.
AGP FRAME# Protocol SIgnals (similar to PCI)2		
GFRAME#	I/O AGP	**Graphics Frame:** Same as PCI. Not used by AGP. GFRAME# remains deasserted by its own pull up resistor.

Table 3.2.6. AGP Interface Signals(Sheet 3 of 3)

Name	Type	Description
GIRDY#	I/O AGP	**Graphics Initiator Ready:** New meaning. GIRDY# indicates the AGP compliant master is ready to provide all write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is never allowed to insert wait states during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. (There is no GFRAME# -- GIRDY# relationship for AGP transactions.)
GTRDY#	I/O AGP	**Graphics Target Ready:** New meaning. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP#	I/O AGP	**Graphics Stop:** Same as PCI. Not used by AGP.
GDEVSEL #	I/O AGP	**Graphics Device Select:** Same as PCI. Not used by AGP.
GREQ#	I AGP	**Graphics Request:** Same as PCI. (Used to request access to the bus to initiate a PCI or AGP request.)
GGNT#	O AGP	**Graphics Grant:** Same meaning as PCI but additional information is provided on ST[2:0]. The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority), it is to provide write data (high or normal priority), for a previously queued write command or has been given permission to start a bus transaction (AGP or PCI).
GAD[31:0]	I/O AGP	**Graphics Address/Data:** Same as PCI.
GC/BE[3:0] #	I/O AGP	**Graphics Command/Byte Enables:** Slightly different meaning. Provides command information (different commands than PCI) when requests are being queued when using PIPE#. Provide valid byte information during AGP write transactions and are not used during the return of read data.
GPAR	I/O AGP	**Graphics Parity:** Same as PCI. Not used on AGP transactions, but used during PCI transactions as defined by the PCI specification.

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-7

Table 3.2.7. Clocks,Reset,and Miscellaneous

Name	Type	Description
HCLKIN	I CMOS	**Host Clock In:** This pin receives a buffered host clock. This clock is used by all of the 82443ZX logic that is in the Host clock domain.
PCLKIN	I CMOS	**PCI Clock In:** This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 82443ZX logic that is in the PCI clock domain.
DCLKO	O CMOS	**SDRAM Clock Out:** 66 or 100 MHz SDRAM clock reference. It feeds an external buffer clock device that produces multiple copies for the DIMMs.
DCLKWR	I CMOS	**SDRAM Write Clock:** Feedback reference from the external SDRAM clock buffer. This clock is used by the 82443ZX when writing data to the SDRAM array. Note: See the Design Guide for routing constraints.
PCIRST#	I CMOS	**PCI Reset:** When asserted, this signal will reset the 82443ZX logic. All PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.
GCLKIN	I CMOS	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKOUT signal.
GCLKO	O CMOS	**AGP Clock Out:** The frequency is 66 MHz. The GCLKOUT output is used to feed both the reference input pin on the 82443ZX and the AGP compliant device.
CRESET#	O CMOS	**Delayed CPU Reset:** CRESET# is a delayed copy of CPURST#. This signal is used to control the multiplexer for the CPU strap signals. CRESET# is delayed from CPURST# by two host clocks. **Note:** This pin requires an external pull-up resistor. If not used, no pull up is required.
TESTIN#	I CMOS	**Test Input:** This pin is used for manufacturing, and board level test purposes. Note: This pin has an internal 50K ohm pull-up.

Table 3.2.8. Power Management Interface

Name	Type	Description
CLKRUN#	I/OD CMOS	**Primary PCI Clock Run:** The 82443ZX requests the central resource (PIIX4E) to start or maintain the PCI clock by the assertion of CLKRUN#. The 82443ZX tristates CLKRUN# upon deassertion of PCIRST# (since CLK is running upon deassertion of reset). If connected to PIIX4E an external 2.7K Ohm pull-up is required for Desktop, Mobile requires (8.2k?0K) pull-up. Otherwise, a 100 Ohm pull down is required.
BXPWROK	I CMOS	**BX Power OK:** BXPWROK input must be connected to the PWROK signal that indicates valid power is applied to the 82443ZX.

Table 3.2.9. Reference Pins

Name	Description
GTLREF[B:A]	GTL Buffer voltage reference input
VTT[B:A]	GTL Threshold voltage for early clamps
VCC	Power pin @ 3.3V
VSS	Ground
REF5V	PCI 5V reference voltage (for 5V tolerant buffers)
AGPREF	External Input Reference

Table 3.2.10. Strapping Options (Sheet 1 of 2)

Signal	Register Name[bit]	Description
MAB13#		**Reserved**.
STRAP5	NBXCFG[13]	**Host Frequency Select:** If STRAP5 is strapped to 0, the host bus frequency is 60/ 66 MHz. If STRAP5 is strapped to 1, the host bus frequency is 100 MHz. An internal pull-down is used to provide the default setting of 66 MHz.
STRAP4	NBXCFG[2]	**In-Order Queue Depth Enable.** If STRAP4 is strapped to 0 during the rising edge of PCIRST#, then the 82442BX will drive A7# low during the CPURST# deassertion. This forces the CPU bus to be configured for non-pipelined operation. If STRAP4 is strapped to 1 (default), then the 82443ZX does not drive the A7# low during reset, and A7# is sampled in default non-driven state (i.e. pulled-up as far as GTL+ termination is concerned) then the maximum allowable queue depth by the CPU bus protocol is selected (i.e., 8). Note that internal pull-up is used to provide pipelined bus mode as a default.
STRAP3	PMCR[3]	**Quick Start Select.** The value on this pin at reset determines which stop clock mode is used. STRAP3 = 0 (default) for normal stop clock mode. If STRAP3 = 1 during the rising edge of PCIRST#, then the 82443ZX will drive A15# low during CPURST# deassertion. This will configure the CPU for Quick Start mode of operation. Note that internal pull-down is used to provide normal stop clock mode as a default.
STRAP2	PMCR[1]	**AGP Disable:** When strapped to a 1, the AGP interface is disabled, all AGP Signals are tri-stated and isolated. When strapped to a 0 (default), the AGP Interface is enabled. When MMCONFIG is strapped active, we require that AGP_DISABLE is also strapped active. When MMCONFIG is strapped inactive, AGP_DISABLE can be strapped active or inactive but IDSEL_REDIRECT (bit 16 in NBXCFG register) must never be activated. This signal has an internal pull-down resistor.
MAB8#		**Reserved.**

3.2 INTEL 82443ZXM HOST BRIDGE CONTROLLER-8

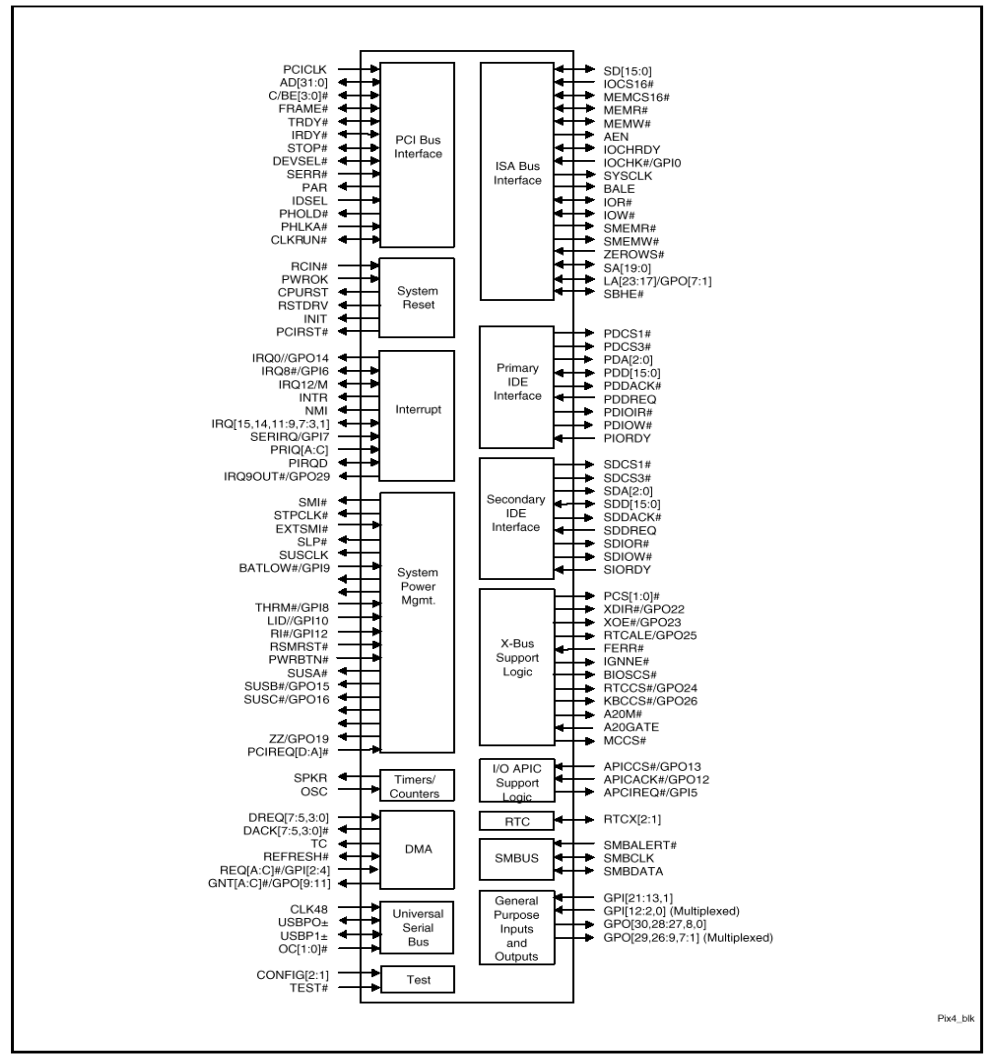
Table 3.2.10. Strapping Options (Sheet 2 of 2)

Signal	Register Name[bit]	Description
STRAP 1	DRAMC[5]	**Memory Module Configuration, MMCONFIG:** When strapped to a 1, the 82443ZX configures its DRAM interface in a 430-TX compatible manner. These unused inputs are isolated while unused outputs are tri-stated: RASB[3:0]#/ CSB[3:0]#, CKE[3:2], GCKE/CKE1, MAA[13:0], DCLKO. When strapped to a 0 (default), the 82443ZX DRAM signal are used normally. IDSEL_REDIRECT (bit 16 in NBXCFG register) is programmed by BIOS, before it begins with device enumeration process. The combination of SDRAMPWR (SDRAMC register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register for more details. Note that internal pull-down is used to set the DRAM interface to a normal Configuration, as a default.
STRAP 0	none	**Host Bus Buffer Mode Select:** When strapped 0, the desktop GTL+ 66 MHz or 100 MHz host bus buffers are used (default). When strapped ?? the mobile Low Power GTL+ 66 MHz host bus buffers are selected. Note that an internal pull-down is used to set the host bus buffers to a desktop configuration as a default in the 82443ZX. An external pull-up therefore is needed for mobile systems using the 82443BX or 82443DX.
A[15]#	none	**Quick Start Select.** The value on A15# sampled at the rising edge of CPURST# will reflect if the quick start/stop clock mode is enabled in the processors.
A7#	none	**In-order Queue Depth Status.** The value on A[7]# sampled at the rising edge of CPURST# reflects if the IOQD is set to 1 or maximum allowable by the CPU bus.

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-1

• 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4):

- Supported Kits for both Pentium™and Pentium™II Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA and EIO at 1/4 of PCI Frequency
- Supports both Mobile and Desktop Deep Green Environments
  - 3.3V Operation with 5V Tolerant Buffers
  - Ultra-low Power for Mobile Environments Support
  - Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-OFF System States
  - All Registers Readable and Restorable for Proper Resume from 0.V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend and Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management
- Integrated IDE Controller
  - Independent Timing of up to 4 Drives
  - PIO Mode 4 and Bus Master IDE Transfers up to 14 Mbytes/sec
  - Supports "Ultra DMA/33" Synchronous DMA Mode Transfers up to 33 Mbytes/sec
  - Integrated 16 x 32-bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-less "Swap-Bay" Option with Full Electrical Isolation
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA with 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Interrupt Controller Based on Two 82C59
  - 15 Interrupt Support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers Based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/sec
  - Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse
  - Supports UHCI Design Guide
- SMBus
  - Host Interface Allows CPU to Communicate Via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-byte Lockout Ranges
- Microsoft Win95* Compliant
- 324 mBGA Package



Simplified Block Diagram

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-2

PIIX4 Signals

3.3.1 PCI BUS INTERFACE (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described inthe PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.1 PCI BUS INTERFACE (Sheet 2 of 3)

Name	Type	Description
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by as serting DEVSEL# on the next cycle.
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4• ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PAR	O	**CALCULATED PARITY SIGNAL.** PAR is " even" parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. " Even" parity means that the number of " 1" within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-3

3.3.1 PCI BUS INTERFACE (Sheet 3 of 3)

Name	Type	Description
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4 ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.2. ISA BUS INTERFACE (Sheet 1 of 4)

Name	Type	Description
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/	I GPI0	**I/O CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purposeinput.
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# isan input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-4

3.3.2. ISA BUS INTERFACE (Sheet 2of 4)

Name	Type	Description
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000-00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

3.3.2. ISA BUS INTERFACE (Sheet 3 of 4)

Name	Type	Description
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 ownsthe ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SSD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-5

3.3.2. ISA BUS INTERFACE (Sheet 4 of 4)

Name	Type	Description
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000-00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then. ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

3.3.3. X-BUS INTERFACE(Sheet 1 of3)

Name	Type	Description
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High

3.3.3. X-BUS INTERFACE(Sheet 2 of3)

Name	Type	Description
PCS0# **PCS1#**	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch theappropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low/GPO
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

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3.3.3. X-BUS INTERFACE(Sheet 3 of3)

Name	Type	Description
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

3.3.4. DMA SIGNALS (Sheet 1 of 2)

Name	Type	Description
DACK[0,1,2,3]# DACK[55,66,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.

3.3.4. DMA SIGNALS (Sheet 2 of 2)

Name	Type	Description
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 1 of 3)

Name	Type	Description
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4 buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input.
INTR	OD	**INTERRUPT.** See CPU Interface Signals.

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3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 2 of 3)

Name	Type	Description
IRQ0/ GPO14	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO
IRQ1	I	**INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11, 14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ8#/ GPI6	I/O	**RQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its outputsignal.

3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 3 of 3)

Name	Type	Description
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.

3.3.6. CPU INTERFACE SIGNALS (Sheet 1 of 3)

Name	Type	Description
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**PU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.

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3.3.6. CPU INTERFACE SIGNALS (Sheet 2 of 3)

Name	Type	Description
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.6. CPU INTERFACE SIGNALS (Sheet 3 of 3)

Name	Type	Description
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI S tatus and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.7. CLOCKING SIGNALS (Sheet 1 of 2)

Name	Type	Description
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-9

3.3.7. CLOCKING SIGNALS (Sheet 2 of 2)

Name	Type	Description
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low

3.3.8. IDE SIGNALS (Sheet 1 of 6)

Name	Type	Description
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** PDA

3.3.8. IDE SIGNALS (Sheet 2 of 6)

Name	Type	Description
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H– –1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0– –3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** PDD
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High

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3.3.8. IDE SIGNALS (Sheet 3 of 6)

Name	Type	Description
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data I s latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High-Z

3.3.8. IDE SIGNALS (Sheet 4 of 6)

Name	Type	Description
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal s connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined [1]**During POS:** SDA
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H– –177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H– –377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-11

3.3.8. IDE SIGNALS (Sheet 5 of 6)

Name	Type	Description
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signalsare used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** SDD
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.

3.3.8. IDE SIGNALS (Sheet 6 of 6)

Name	Type	Description
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High

NOTES:

1. After reset, all undefined signals on the primary channel will default to the same values as the undefined signals on the secondary channel.

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3.3.9. UNIVERSAL SERIAL BUS SIGNALS

Name	Type	Description
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 1 of 4)

Name	Type	Description
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purposeinput.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used asa general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 2 of 4)

Name	Type	Description
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ [A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3 INTEL 82371EB PCI TO ISA/IDE XCELERATOR (PIIX4E)-13

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 3 of 4)

Name	Type	Description
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUSC#/ GPO16	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/ GPO20	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
SUS_STAT2#/ GPO21	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/ GPI8	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardw are can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 4 of 4)

Name	Type	Description
ZZ/ GPO19	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a cache data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.11. GENERAL PURPOSE INPUT AND OUTPUT SIGNALS

Some of the General Purpose Input and Output signals are multiplexed with other PIIX4 signals. The usage is determined by the system configuration.
The default pin usage is shown in Table 1 and Table 2. The configuration can be selected via the General Configuration register and X-Bus Chip Select register.

Name	Type	Description
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	**GENERAL PURPOSE OUTPUTS.** These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).

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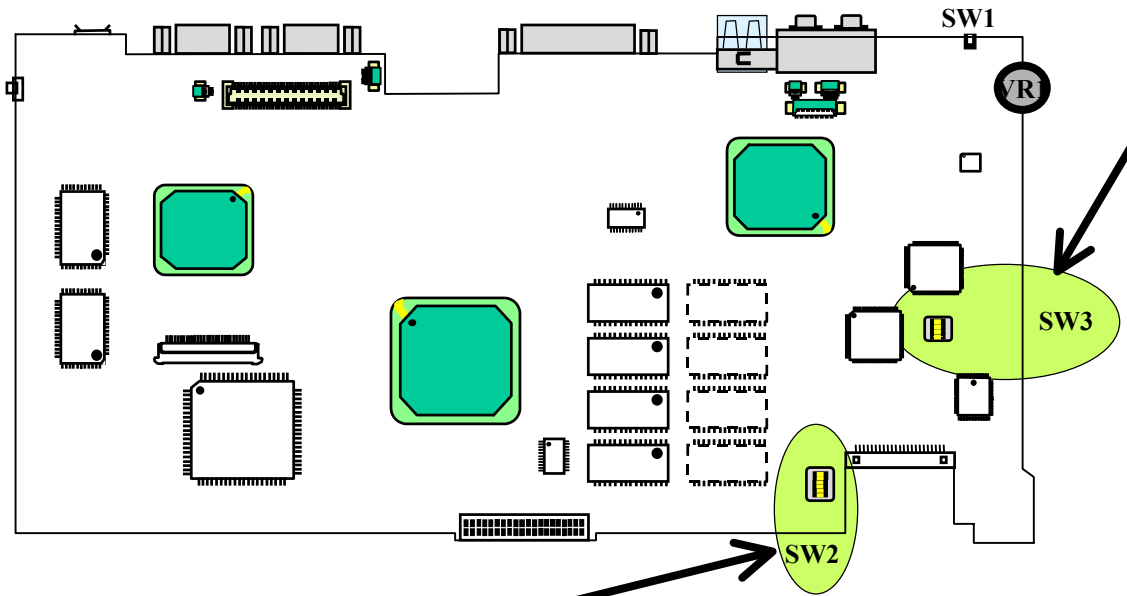
3.3.12. OTHER SYSTEM AND TEST SIGNALS

Name	Type	Description
CONFIG1	I	**CONFIGURATION SELECT 1.** This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	**CONFIGURATION SELECT 2.** This input signal is used to select the positive or subtractive decode of FFFF0000h-FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with sub tractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	**POWER OK.** When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	**SPEAKER.** The SPKR signal is the output of counter timer 2 and is internally " ANDed with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. **During Reset:** Low **After Reset:** Low **During POS:** Last State
TEST#	I	**TEST MODE SELECT.** The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

3.3.13. POWER AND GROUND PINS

Name	Type	Description
VCC	V	**CORE VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	**RTC WELL VOLTAGE SUPPLY.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	**SUSPEND WELL VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	**USB VOLTAGE SUPPLY.** This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	**VOLTAGE REFERENCE.** This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	**CORE GROUND.** These pins are the primary ground for PIIX4.
VSS (USB)	V	**USB GROUND.** This pin is the ground for the USB input/output buffers.

4.SWITCH SETTING



SW3 (CPU SPEED SETTING)

	1	2	3	4
300(1.6V)	OFF	ON	OFF	ON
333(1.6V)	OFF	OFF	ON	ON
366(1.6V)	OFF	OFF	OFF	ON
400(1.6V)	ON	ON	ON	OFF
433(1.9V)	ON	ON	OFF	OFF
466(1.9V)	ON	OFF	ON	OFF

SW2 (LCD AND CPU_CORE SETTING)

	SW2-1	SW2-2	SW2-3	SW2-4 K/B setting
HT13X13-201(HY)	On	On	On	X
AA121SJ03 (MI)	Off	On	On	X
TM121SV-02L01(SA)	Off	Off	On	X
SR1205-22NTR(SA-D)	Off	Off	Off	X

P.S : IF SW2-4 IS US THEN K/B SETTING X=OFF
IF SW2-4 IS JP THEN K/B SETTING X=ON

VCC_CORE	SW2-5	SW2-6
1.5V	ON	ON
1.6V	OFF	ON
1.8V	ON	OFF
1.9V	OFF	OFF

5.ASSEMBLY & DISASSEMBLY

5.1 SYSTEM VIEW

5.2 SYSTEM DISASSEMBLY

MODULAR COMPONENTS

LCD ASSEMBLY COMPONENTS

BASE UNIT COMPONENTS

5.ASSEMBLY & DISASSEMBLY

5.1 SYSTEM VIEW

5.1.1 RIGHT-SIDE VIEW

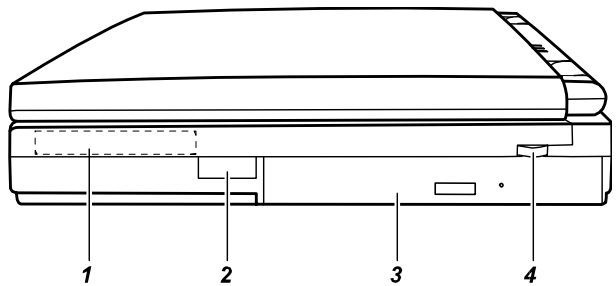


Figure 5-1. Right-Side View

1.**Hard Disk Drive.**
2.**IR Port.**
3.**CD-ROM/DVD-ROM Drive.**
4.**Volume Control.**

5.1.2 LEFT-SIDE VIEW

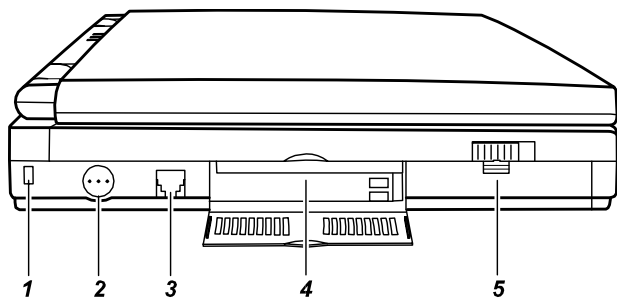
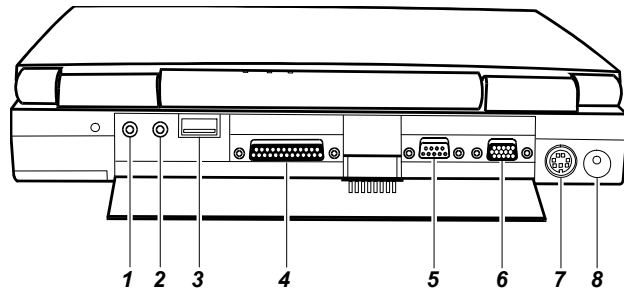


Figure 5-2. Left-Side View

1.**Kensington Lock Anchor.**
2.**Power Button.**
3.**Phone Line Connector** (optional).
4.**PC Card Slots.**
5.**Battery Pack.**

5.ASSEMBLY & DISASSEMBLY

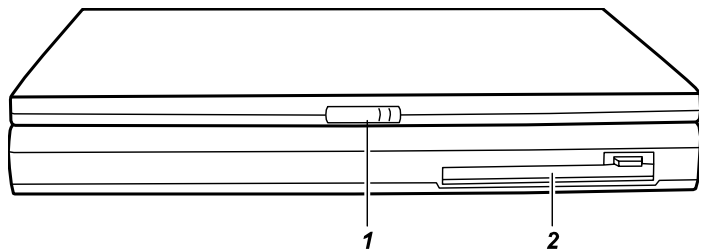
5.1.3 REAR VIEW



1. **Microphone Connector**
2. **Audio Output Connector**
3. **USB Port**
4. **Parallel Port**
5. **Serial Port**
6. **VGA Port**
7. **PS/2 Mouse/Keyboard Port**
8. **Power Connector**

Figure 5-3. Rear View

5.1.4 FRONT VIEW



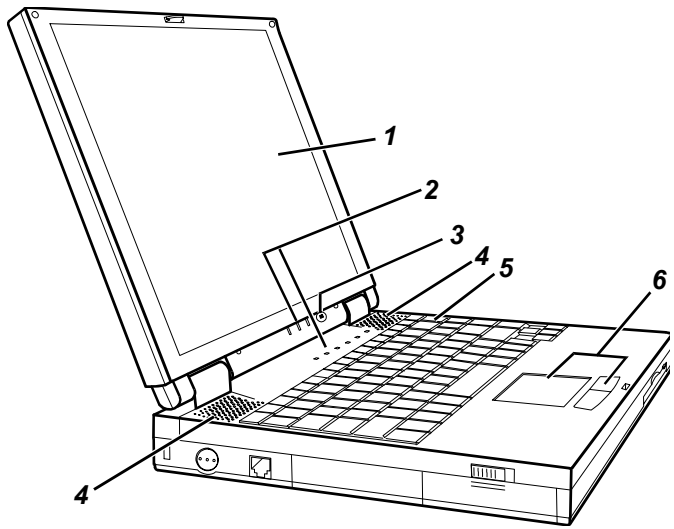
1.**Top Cover Latch.**
2.**Floppy Disk Drive**.

Figure 5-4. Front View

5.ASSEMBLY & DISASSEMBLY

5.1.5 TOP-OPEN VIEW

To open the cover, press the cover latch toward the right and lift the cover.



1.**LCD Display.**
2.**Indicators Panel.**
3.**Microphone.**
4.**Stereo Speaker Set.**
5.**Keyboard.**
6.**Touchpad.**

Figure 5-5. Top-Open View

5.ASSEMBLY & DISASSEMBLY

5.2 SYSTEM DISASSEMBLY

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

Modular Components

- 5.2.1 Battery Pack
- 5.2.2 CD-ROM/DVD-ROM Drive
- 5.2.3 CPU
- 5.2.4 Fax/Modem/Voice Card
- 5.2.5 SO-DIMM

LCD Assembly Components

- 5.2.6 LCD Assembly
- 5.2.7.1 12.1 Inch LCD Panel
- 5.2.7.2 13.3 Inch LCD Panel
- 5.2.8 Inverter Board/LED Board

Base Unit Components

- 5.2.9 Keyboard
- 5.2.10 Hard Disk Drive
- 5.2.11 Touchpad Board
- 5.2.12 System Board
- 5.2.13 Floppy Disk Drive

♦ You can also find details of each component on the exploded charts.

5.ASSEMBLY & DISASSEMBLY

5.2 SYSTEM DISASSEMBLY

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

5.2.1 BATTERY PACK

DISASSEMBLY

1.Place the notebook upside down.

2.First push away the small locking latch (❶) on the battery pack and then slide the locking latch (❷) on the side of the notebook to unlock and lift (❸) the battery pack out of the compartment.

REASSEMBLY

1.Fit the battery pack into the compartment.

Make sure the locking latch is in the locked position.

(Refer to Figure 5-6 earlier.)

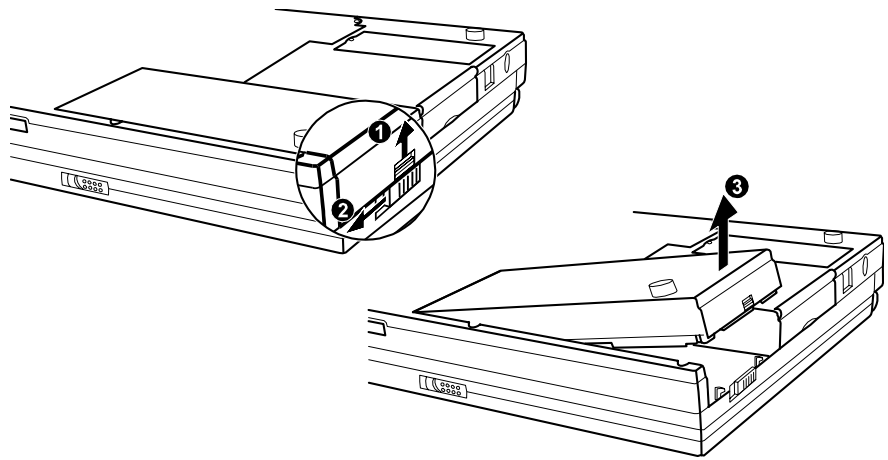


Figure 5-6. Removing the Battery Pack

5.ASSEMBLY & DISASSEMBLY

5.2.2 CD-ROM/DVD-ROM DRIVE

DISASSEMBLY

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (Refer to Figure 5-7)
3. Unplug the CD-ROM/DVD-ROM drive cable from the system board. (Refer to Figure 5-8)
4. Remove one screw and slide the CD-ROM/DVD-ROM drive out of the compartment. (Refer to Figure 5-9)

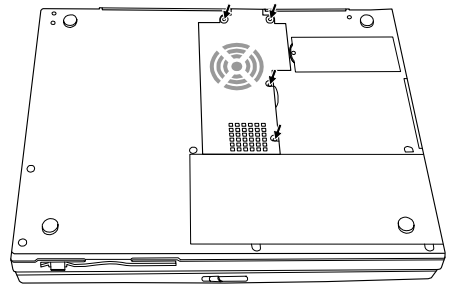


Figure 5-7. Removing the CPU Compartment Cover

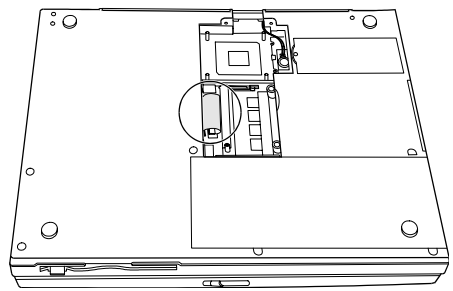


Figure 5-8. Unplugging the CD-ROM Drive Cable

REASSEMBLY

1. Connect one end of the cable to the CD-ROM/DVD-ROM drive.
2. Slide the CD-ROM/DVD-ROM drive into the compartment and secure with one screw. (Refer to Figure 5-9 earlier.)
3. Connect the CD-ROM/DVD-ROM drive cable to the system board. (Refer to Figure 5-8 earlier.)
4. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)

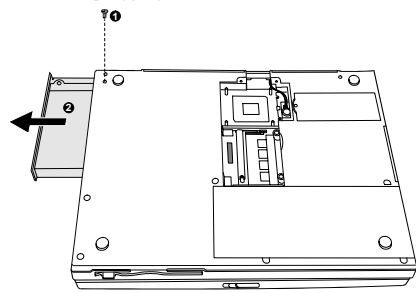


Figure 5-9. Removing the CD-ROM Drive

5.ASSEMBLY & DISASSEMBLY

5.2.3 CPU

DISASSEMBLY

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (See Figure 5-7.)
3. Remove four screws that fasten the fan assembly. Remove the bottom screws (❶) first and then the upper screws (❷).

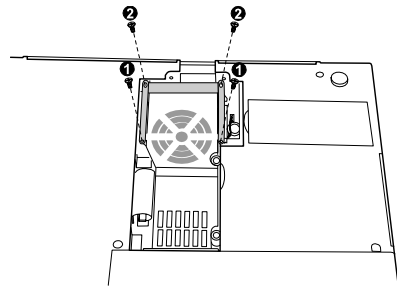


Figure 5-10. Removing the screws

4. Remove the metal plate. Unplug the power cord and remove the fan assembly.

> ***NOTE:*** When you remove the fan assembly, make sure that the thermal pad is not damaged. If it is damaged, you have to use a new thermal pad.

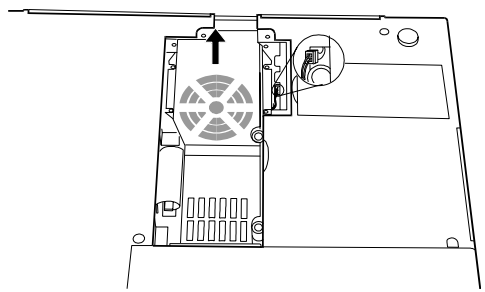


Figure 5-11. Removing the Fan Assembly

5.ASSEMBLY & DISASSEMBLY

5.2.3 CPU

DISASSEMBLY

5. Remove two screw standoffs.

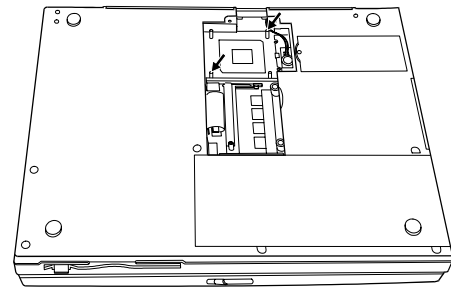


Figure 5-12. Removing Two Standoffs

6. Align the Actuation Slide with the arrowhead of the CPU. Place the Actuation Slide diagonally on top of the CPU.
7. Press the Actuation Slide with your fingers. Then use the lever to push the Slide to unlock the CPU.

> ***CAUTION:*** Push gently to lock/unlock the CPU, otherwise the CPU and socket might be damaged.

8. Remove the Actuation Slide and gently lift the CPU.

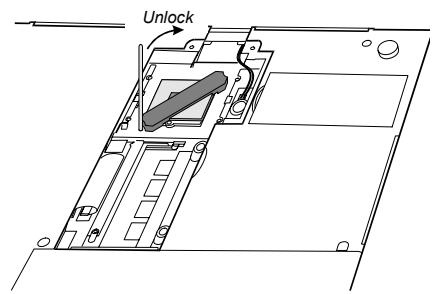


Figure 5-13. Unlocking the CPU

5.ASSEMBLY & DISASSEMBLY

5.2.3 CPU

REASSEMBLY

1. Align the arrowhead of the uPGA CPU with the arrowhead of the socket and insert the CPU pins into the holes.

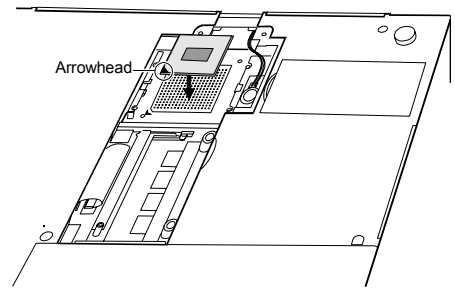


Figure 5-14. Placing the CPU

2. Place the Actuation Slide diagonally on top of the CPU. Press the Actuation Slide with your fingers. Then use the lever to push the Slide to lock the CPU.

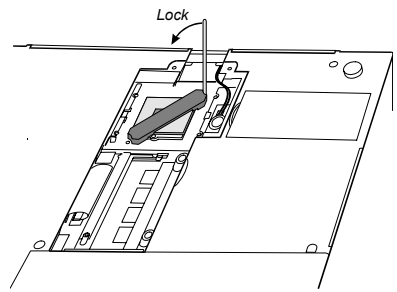


Figure 5-15. Securing the CPU

3. Replace two screw standoffs. Place the fan assembly on top of the CPU and plug the power cord. (Refer to Figure 5-12 and 5-11 earlier.)
4. Place the metal plate on top of the fan assembly. Secure the fan assembly with four screws, first the bottom screws (❶) and then the upper screws (❷). (Refer to Figure 5-10 earlier.)
5. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)

5.ASSEMBLY & DISASSEMBLY

5.2.4 FAX/ MODEM/DATA CARD

DISASSEMBLY

1. Place the notebook upside down.
2. To remove the compartment cover, remove one screw, then lift up the cover.

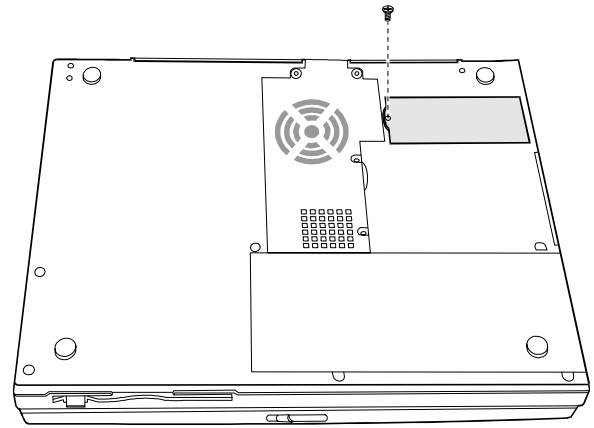


Figure 5-16. Removing the Fax/Modem/Voice Card Compartment Cover

3. Remove one screw. Then, lift up the inner edge of the card to remove the card.

REASSEMBLY

1. Hold the Fax/Modem/Voice Card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the phone line connector into the opening and press the other end to plug the other connector into the socket on the system board. Then, secure with one screw. (Refer to Figure 5-17 earlier.)
2. Replace the compartment cover and secure with one screw. (Refer to Figure 5-16 earlier.)

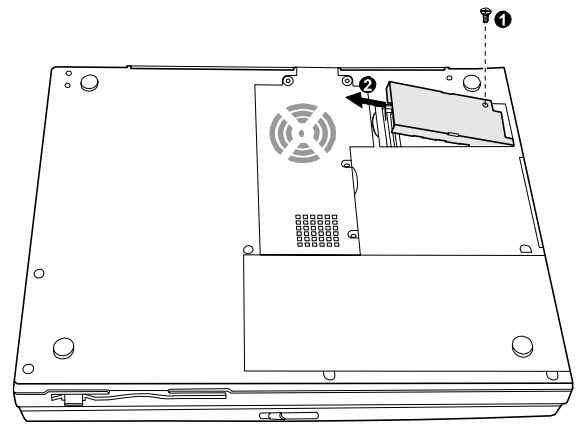


Figure 5-17. Removing the Fax/Modem/Voice Card

5.ASSEMBLY & DISASSEMBLY

5.2.5 SO-DIMM

DISASSEMBLY

1. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (See Figure 5-7.)
2. Pull the retaining clips outwards and remove the SO-DIMM.

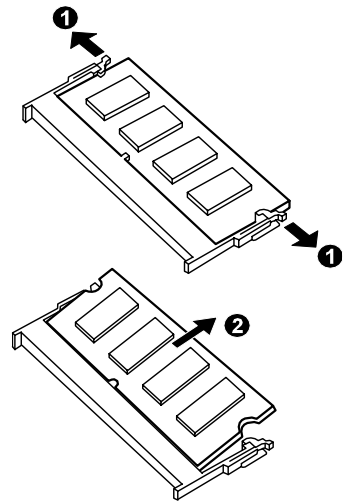


Figure 5-18. Removing the SO-DIMM

REASSEMBLY

1. To install the SO-DIMM, align the SO-DIMM's notched part with the socket's corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position. (Refer to Figure 5-18 earlier.)
2. Replace the compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)

5.ASSEMBLY & DISASSEMBLY

5.2.6 LCD ASSEMBLY

DISASSEMBLY

1. Remove six bottom screws.

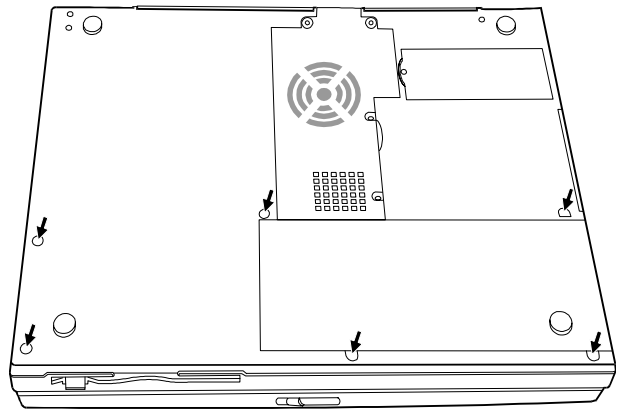


Figure 5-19. Removing Six Bottom Screws

2. Put the notebook back to the upright position and open the top cover. Remove the base unit cover.
3. Disconnect the keyboard cable form the system board.
4. Remove the shield plate by removing 12 screws.

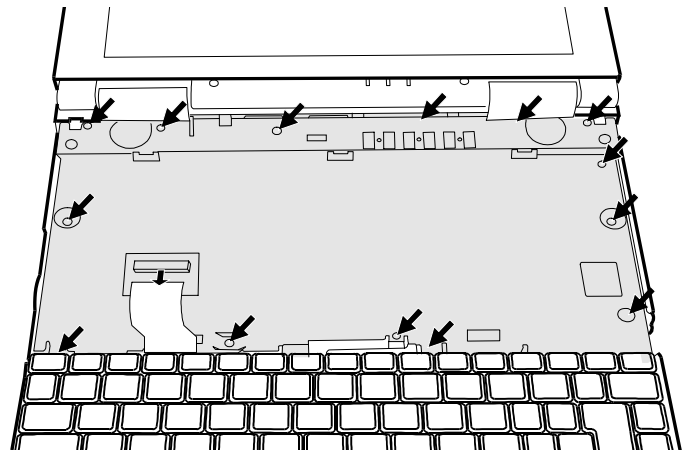


Figure 5-20. Removing the Shield Plate

5.ASSEMBLY & DISASSEMBLY

5.2.6 LCD ASSEMBLY

DISASSEMBLY

5. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. Repeat the same with the other hinge cover. Note the right and left hinges are not exchangeable.
6. Unplug the three cable connectors coming from the LCD assembly.
7. Remove four screws from the hinges. Now you can separate the LCD assembly from the base unit

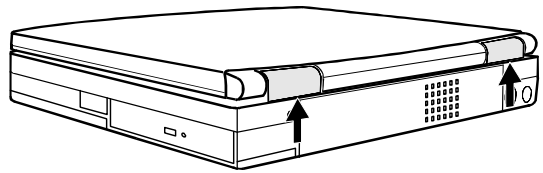


Figure 5-21. Removing the Hinge Covers

REASSEMBLY

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges. (Refer to Figure 5-22 earlier.)
2. Reconnect the LCD cable connectors to the system board. (Refer to Figure 5-22 earlier.)
3. Replace the two hinge covers. (Refer to Figure 5-21 earlier.)
4. Replace the shield plate and secure with 12 screws. (Refer to Figure 5-20 earlier.)
5. Connect the keyboard cable and replace the keyboard.
6. Replace the base unit cover.
7. Replace the six bottom screws. (Refer to Figure 5-19 earlier.)

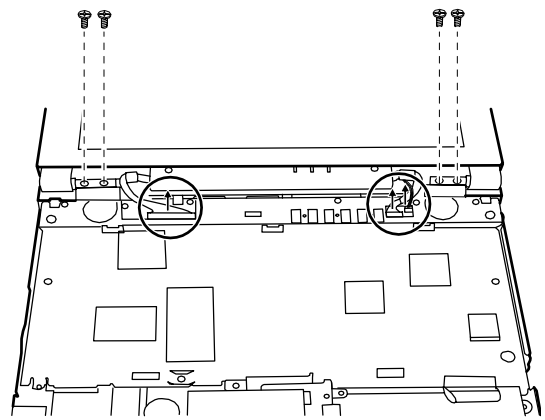


Figure 5-22. Unplugging the Cable Connectors and Removing Four Screws

5.ASSEMBLY & DISASSEMBLY

5.2.7.1 12.1 INCH LCD PANEL

DISASSEMBLY

1. Open the top cover.
2. Remove the four rubber pads and the four screws underneath. Then you can separate the LCD frame from the housing.

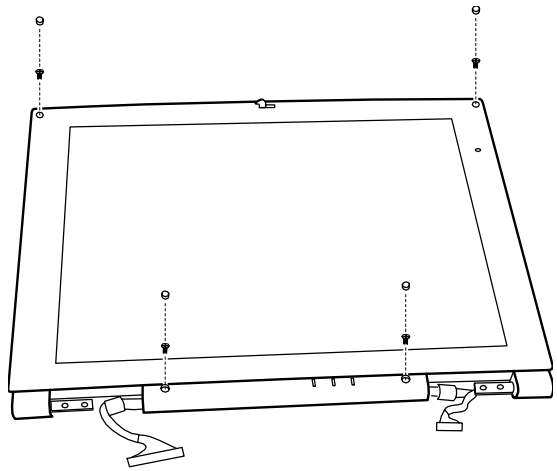


Figure 5-23. Removing the 12.1 Inch LCD Frame

3. To remove the LCD, remove four screws and unplug the cables.

REASSEMBLY

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with four screws. (Refer to Figure 5-24 earlier.)
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads. (Refer to Figure 5-23 earlier.)

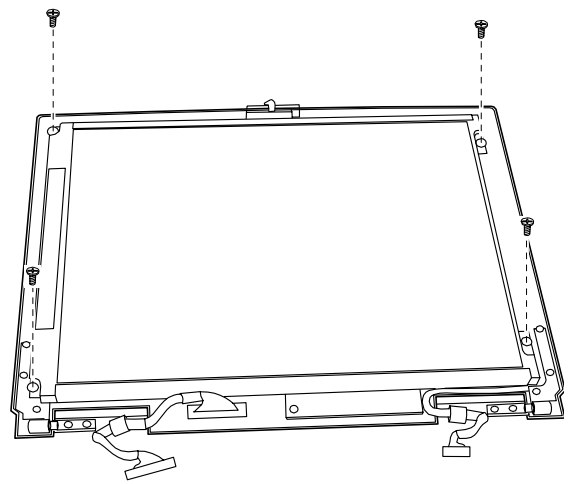


Figure 5-24. Removing the 12.1 Inch LCD

5.ASSEMBLY & DISASSEMBLY

5.2.7.2 13.3 INCH LCD PANEL

DISASSEMBLY

1. Open the top cover.
2. Remove the four rubber pads and two screws on the bottom side. Then slightly lift up the bottom part of the frame and gently separate the LCD frame from the housing.
3. To remove the LCD, remove six screws and unplug the cables.

REASSEMBLY

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with six screws. (Refer to Figure 5-26 earlier.)
2. Fit the LCD frame back to the housing and replace the two screws and four rubber pads. (Refer to Figure 5-25 earlier.)

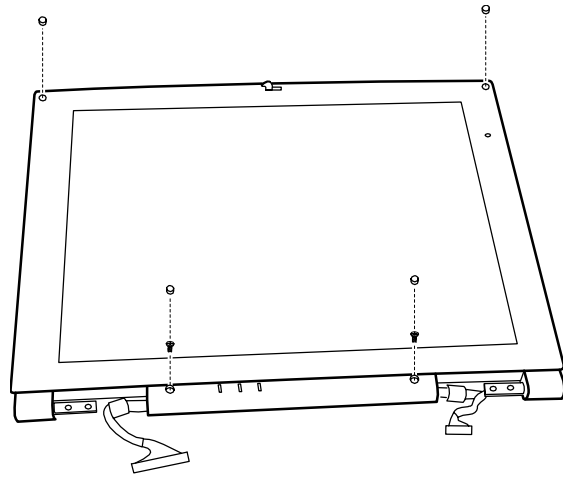


Figure 5-25. Removing the 13.3 Inch LCD Frame

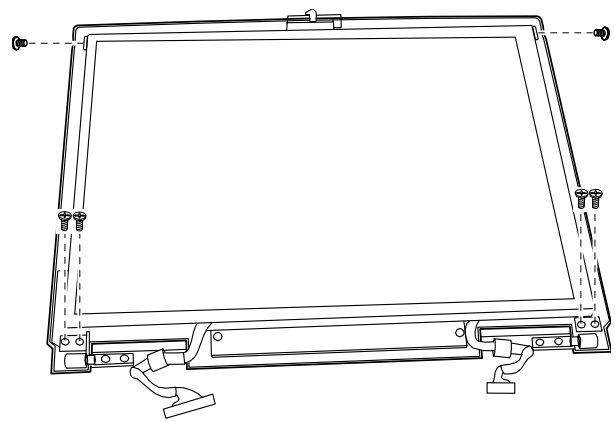


Figure 5-26. Removing the 13.3 Inch LCD

5.ASSEMBLY & DISASSEMBLY

5.2.8 INVERTER BOARD

DISASSEMBLY

1. Detach the LCD frame. (See steps 1 to 2 in section 5.2.7 Disassembly.)
2. For 12.1 inch LCD:
   To remove the LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board.
   To remove the inverter board at the right side of the LCD , remove two screws and unplug the connectors from the board.
3. For 13.3 inch LCD:
   To remove the inverter/LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board.

REASSEMBLY

1. Reconnect the connectors. Fit the inverter/LED board back into place and secure with according number of screws. (Refer to Figure 5-28 and 5-27 earlier.)
2. Place the LCD frame back to the housing. (Refer to Figure 5-25 and 5-23 earlier.)

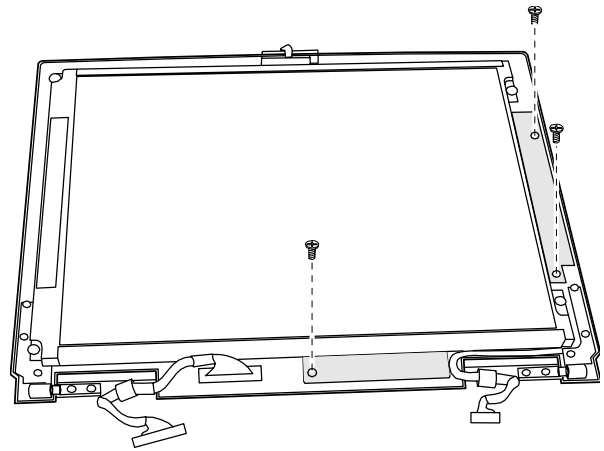


Figure 5-27. Removing the Inverter and LED Board for 12.1 Inch LCD

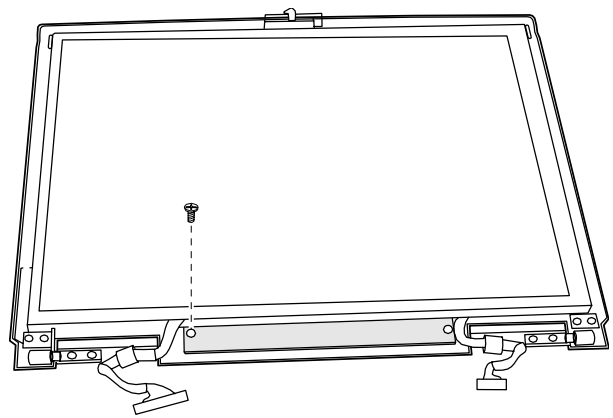


Figure 5-28. Removing the Inverter/LED Board for 13.3 Inch LCD

5.2.9 KEYBOARD

DISASSEMBLY

1. Remove the base unit cover. (See section 5.2.6 Disassembly steps 1 to 2.)
2. Lift the keyboard and unplug the keyboard cable from the system board.

REASSEMBLY

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the base unit cover. (See section 5.2.6 Reassembly steps 6 to 7.)

5.ASSEMBLY & DISASSEMBLY

5.2.10 HARD DISK DRIVE

DISASSEMBLY

1. Remove the base unit cover. (See section 5.2.6 Disassembly steps 1 to 2.)
2. Remove two top screws from the hard disk drive bracket and slide the hard disk drive outwards to unplug the connector.

To separate the hard disk drive from the bracket, remove four side screws from the bracket.

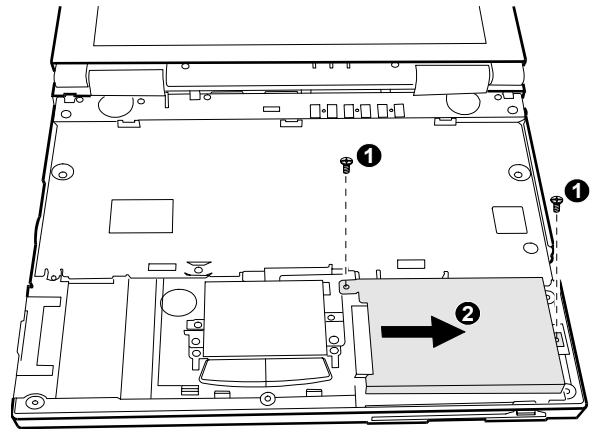


Figure 5-29. Removing the Hard Disk Drive

REASSEMBLY

1. Attach the bracket to the hard disk drive and secure with four screws on both sides. (Refer to Figure 5-30 earlier.)
2. Plug the hard disk drive connector to the touchpad board and secure the bracket in place with two screws. (Refer to Figure 5-29 earlier.)
3. Replace the base unit cover. (See section 5.2.6 Reassembly steps 6 to 7.)

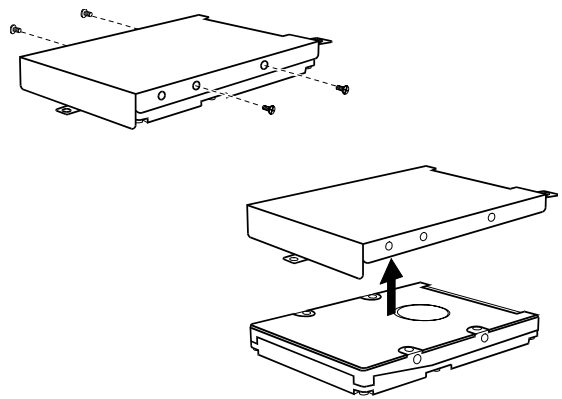


Figure 5-30. Removing the Hard Disk Drive Bracket

5.ASSEMBLY & DISASSEMBLY

5.2.11 TOUCHPAD BOARD

DISASSEMBLY

1. Remove the shield plate. (See section 5.2.6 Disassembly steps 1 to 4.)
2. Remove the hard disk drive. (See section 5.2.10.)
3. Lift the touchpad board free.

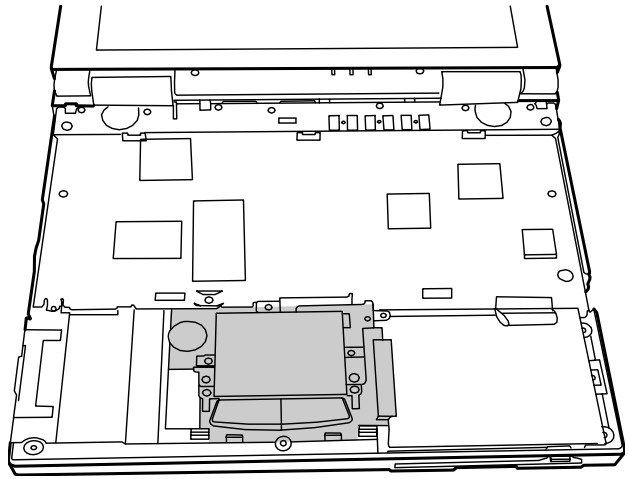


Figure 5-31. Removing the Touchpad Board

REASSEMBLY

1. Fit the touchpad board into place. (Refer to Figure 5-31 earlier.)
2. Replace the hard disk drive. (See section 5.2.10 Reassembly.)
3. Replace the shield plate. (See section 5.2.6 Reassembly steps 4 to 7.)

5.ASSEMBLY & DISASSEMBLY

5.2.12 SYSTEM BOARD

DISASSEMBLY

1. Remove all the bottom screws.
2. Remove the battery pack. (See section 5.2.1.)
3. Remove the CD-ROM drive. (See section 5.2.2.)
4. Remove the CPU and cooling fan assembly. (See section 5.2.3.)
5. Remove the Data/Fax/Modem Card if it exists. (See section 5.2.4.)
6. Remove the LCD assembly. (See section 5.2.6.)
7. Remove the hard disk drive. (See section 5.2.10.)
8. Remove the touchpad board. (See section 5.2.11.)
9. Unplug the speaker connectors from the system board.
10. Remove five screws fastening the rear frame.

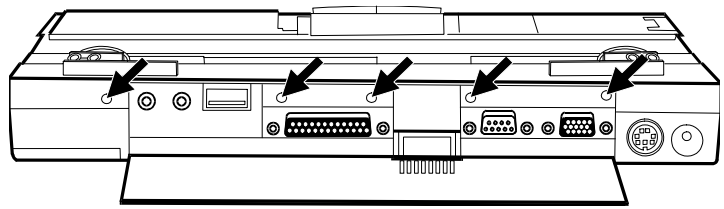


Figure 5-32. Removing Five Rear Screws

11. Gently lift the rear frame free from the housing.

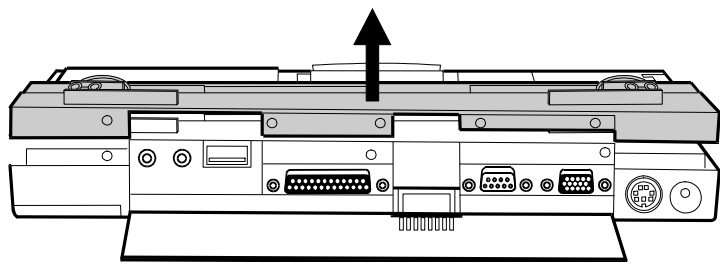


Figure 5-33. Removing the Rear Frame

5.ASSEMBLY & DISASSEMBLY

5.2.12 SYSTEM BOARD

DISASSEMBLY

12. Remove two bottom screws fastening the system board.

Unplug the floppy disk drive cable connector from the system board. Lift the system board free.

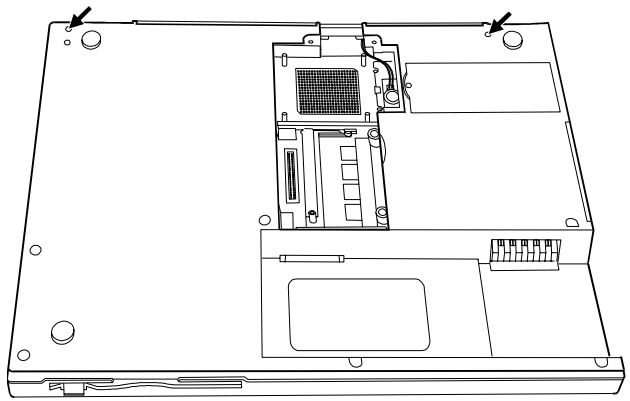


Figure 5-34. Removing Two Bottom Screws

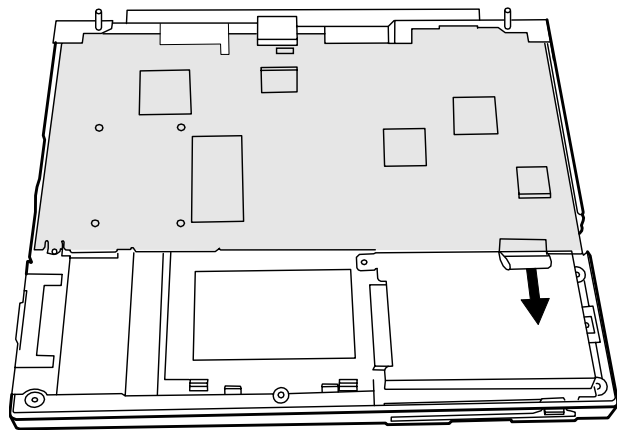


Figure 5-35. Unplugging the Floppy Disk Drive Cable

REASSEMBLY

1. Fit the system board into place.
2. Connect the floppy disk drive cable to the system board. (Refer to Figure 5-35 earlier.)
3. Replace two bottom screws fastening the system board. (Refer to Figure 5-34 earlier.)
4. Replace the rear frame and five rear screws. (Refer to Figure 5-33 and 5-32 earlier.)
5. Replace the touchpad board by plugging the connector. (Refer to Figure 5-31 earlier.)
6. Replace the hard disk drive with its bracket by plugging the connector to the touchpad board and securing with two screws. (Refer to Figure 5-29 earlier.)
7. Connect the speaker connectors.
8. Attach the LCD assembly to the base unit and secure with four screws. (Refer to Figure 5-22 earlier.)
9. Replace the two hinge covers. (Refer to Figure 5-21 earlier.)
10. Fit the shield plate back into place and secure with 12 screws. (Refer to Figure 5-20 earlier.)

5.ASSEMBLY & DISASSEMBLY

5.2.12 SYSTEM BOARD

REASSEMBLY

11. Connect the keyboard cable and replace the keyboard.
12. Fit the base unit cover into place and secure with six bottom screws. (Refer to Figure 5-19 earlier.)
13. Replace the CD-ROM drive by sliding it into the compartment, plugging the connector, and secure with one bottom screw. (Refer to Figure 5-9 and 5-8 earlier.)
14. Replace the CPU and fan assembly. (Refer to section 5.2.3 Reassembly.)
15. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)
16. Replace the Data/Fax/Modem Card and secure with one screw. (Refer to Figure 5-17 earlier.)
17. Replace the Data/Fax/Modem Card compartment cover and secure with one screw. (Refer to Figure 5-16 earlier.)
18. Replace the battery pack. (Refer to Figure 5-6 earlier.)

5.2.13 FLOPPY DISK DRIVE

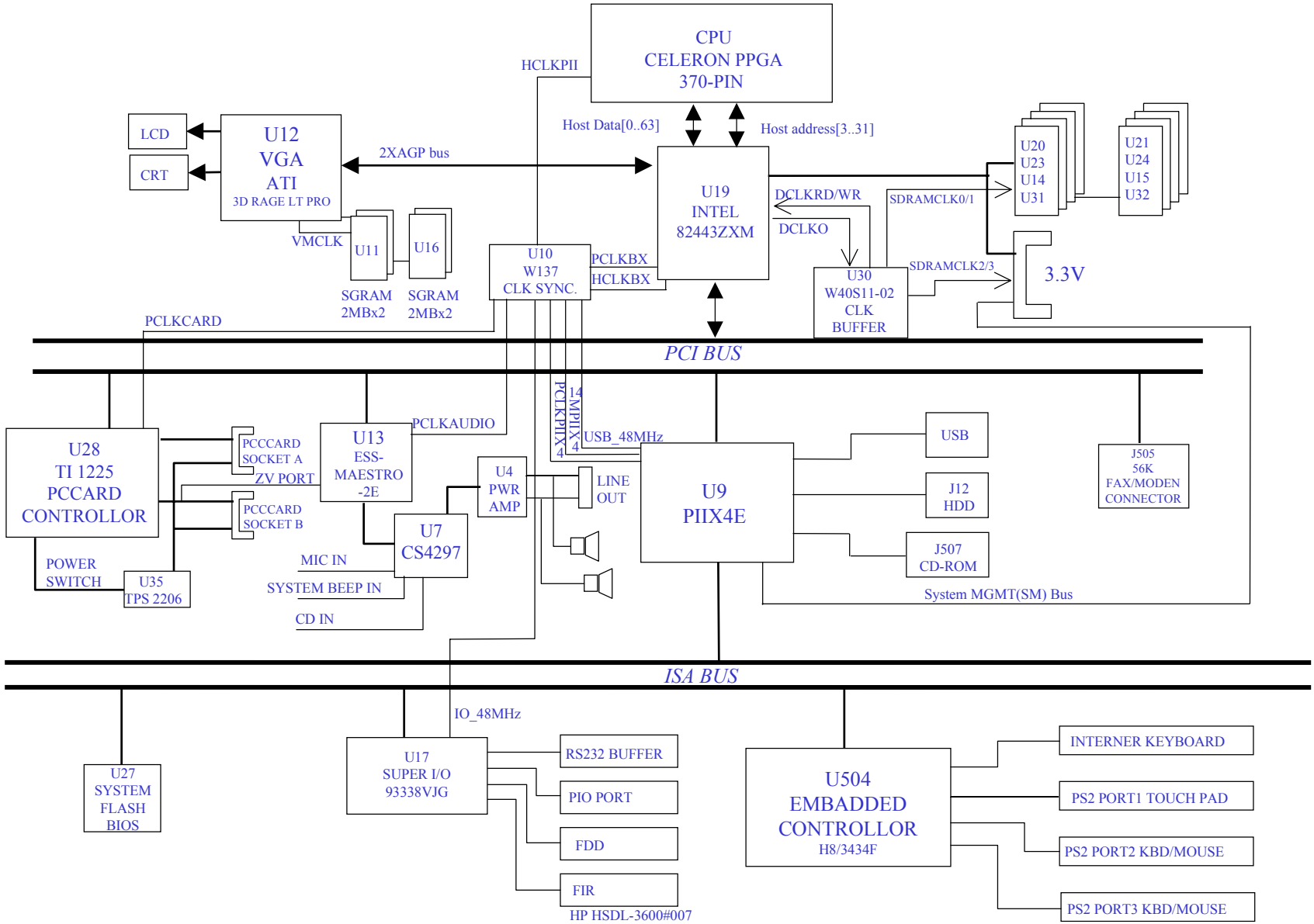
DISASSEMBLY

1. Remove the system board. (See section 5.2.12 Disassembly.)
2. Remove the floppy disk drive by first lifting the rear end of the floppy disk drive.

REASSEMBLY

1. Connect the floppy disk drive cable to the floppy disk drive and fit the floppy disk drive into place.
2. Replace the system board. (See section 5.2.12 Reassembly.)

6. 6233 BLOCK DIAGRAM



7. MAINTENANCE DIAGNOSTICS

7.1 INTRODUCTION

EVERY TIME THE COMPUTER IS TURNED ON ,THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY, THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC POST(378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE , IF THE TEST FAIL, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURS BY READING THE LAST VALUE WRITTEN TO POST 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

7. MAINTENANCE DIAGNOSTICS

7.2 ERROR CODES : FOLLOWING IS A LIST OF ERROR CODES IN SEQUENT DISPLAY ON THE PIO DEBUG BOARD.

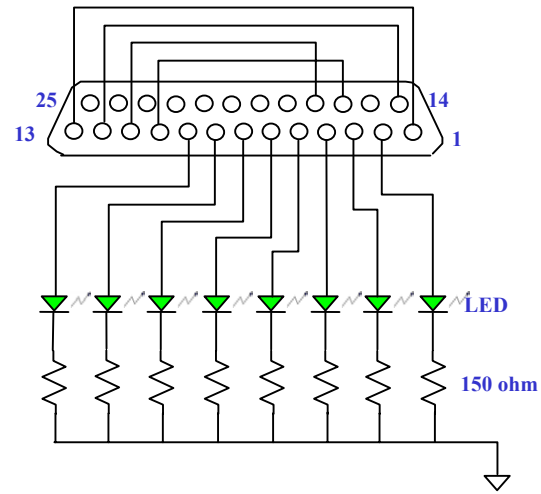
01h	Start of BootLoader sEQUence.
02h	Initialize ChipSet.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-pattern R/W.
05h	Move BootLoader to the RAM.
06h	Start point of execution of BootLoader in RAM.
07h	Shadow System BIOS.
08h	Initialize Clock Synthesizer
09h	Initialize Audio Controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with Normal Boot
0Ch	Proceed with Crisis Boot
0Fh	DRAM Sizing
10H	Initial L1,L2 cache, make stack and diagnose CMOS.
11H	Turn off FASTA20 for POST. Reset GDTs, 8259s guickly.
12H	Signal Power On Reset at COMS.
13H	Initialize the Chipset, (SDRAM).
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1, exite the RAM.
16H	user register config through CMOS
18H	Dispatch to 1st 64K RAM Test
19H	checksum the ROM
1AH	Reset PIC's(8259s)
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter

1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Perform Keyboard self test
21H	Test & Initialize Keyboard Controller
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Interrupt Vectors Table.
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Prepare To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter, VGA Initialize.
2FH	Signon messages displayed
30H	Special init of keyboard ctlr
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful

7. MAINTENANCE DIAGNOSTICS

38H	Update Keyboard output port to disable gate of A20
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	Initialize BIOS Data Area at 40:0.
3CH	Initialize the hardware interrupt vector table
3DH	Search and Init the Mouse
3EH	Update NumLock status
3FH	OEM initialization of COMM and LPT ports
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	OEM's init of PM with USB
44H	Initialize additional ROMs
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM's init of Power Management, (check SMI)
48H	OEM functions before boot (PCMCIA, CardBus)
49H	Dispatch To Operation System Boot
4AH	Jump Into Bootstrap Code

PIO PORT (378H) DIAGNOSTIC TOOLS



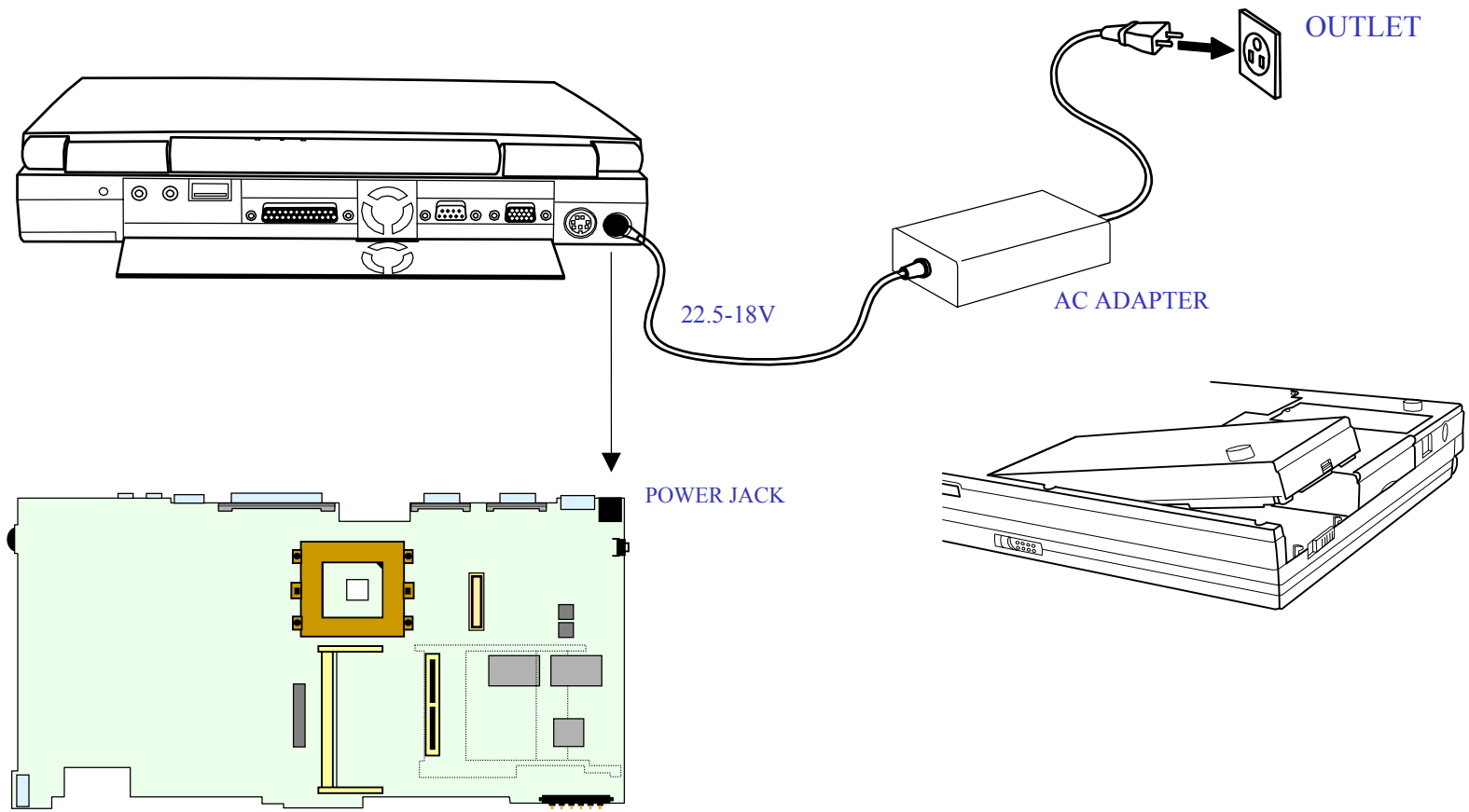
PIN1 : STROBE ⟷ PIN13: SLCT
PIN10: ACK# ⟷ PIN16: INT#
PIN11: BUSY ⟷ PIN17: SELIN#
PIN12:PTERR ⟷ PIN14: AUTOFD#
PIN[9:2]:PD[7:0]

8. TROUBLE SHOOTING

8.1 NO POWER:

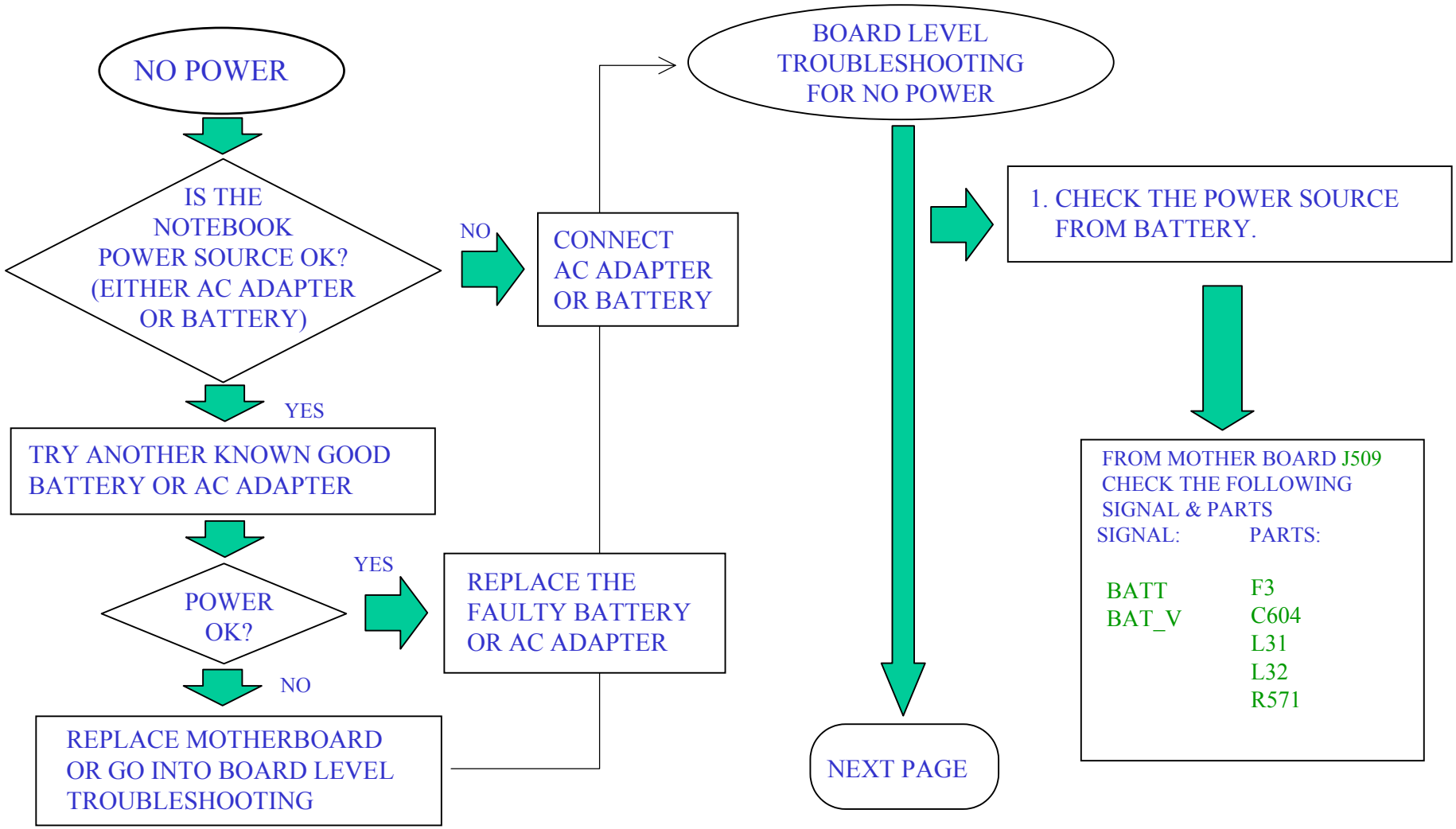
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR DOES NOT LIGHT UP.

1. CHECK AC ADAPTOR
2. CHECK BATTERY



8.1 NO POWER:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR DOES NOT LIGHT UP.



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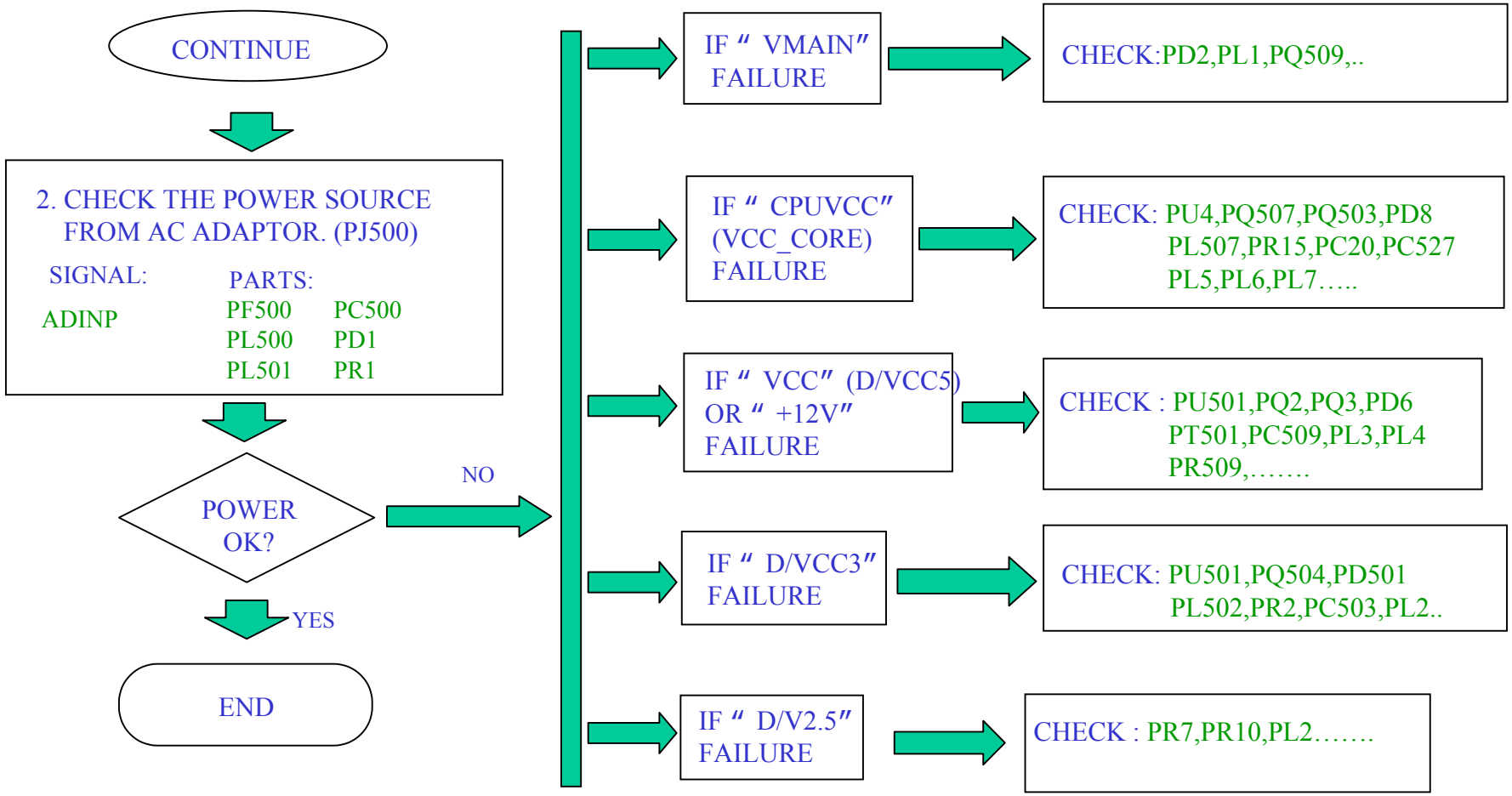
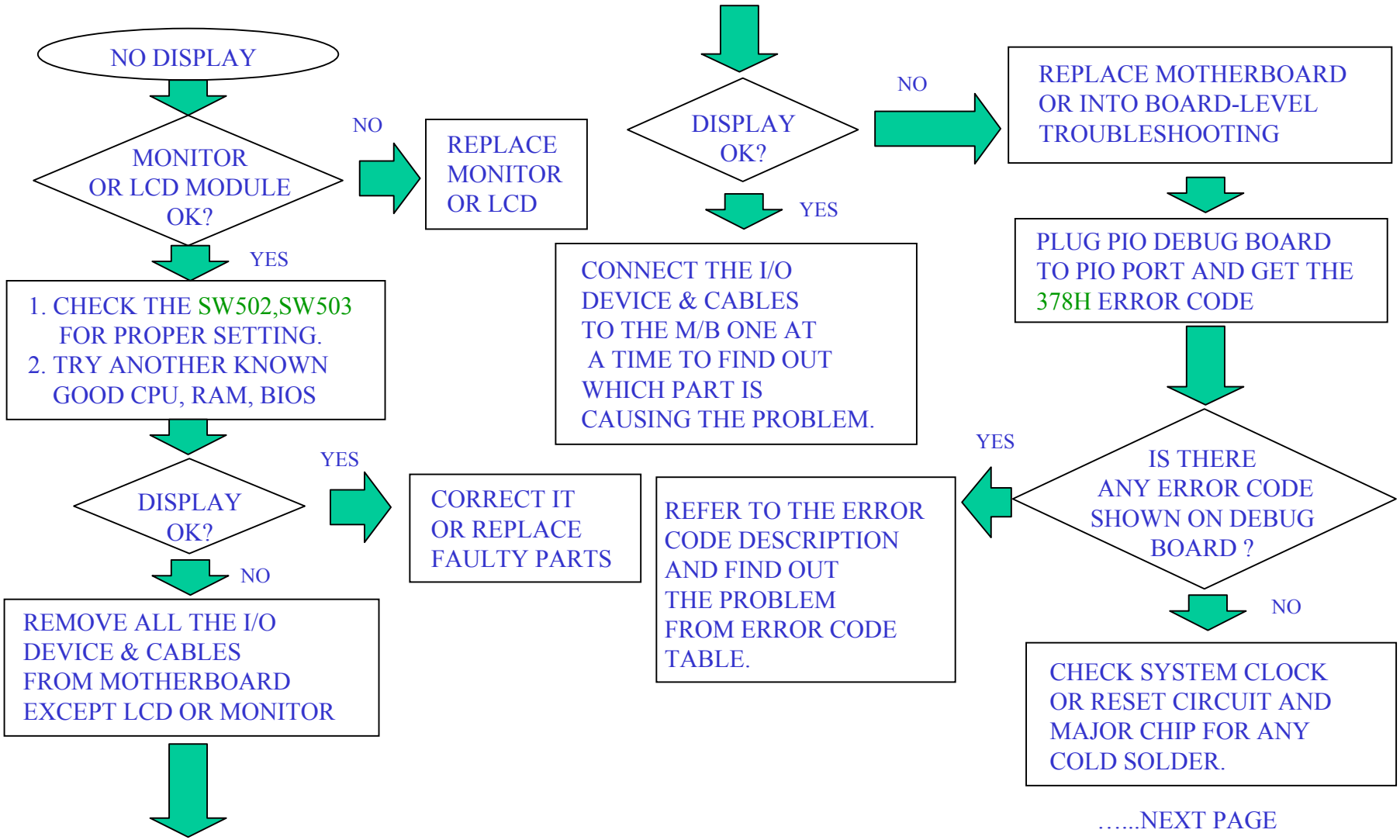


8.2 NO DISPLAY

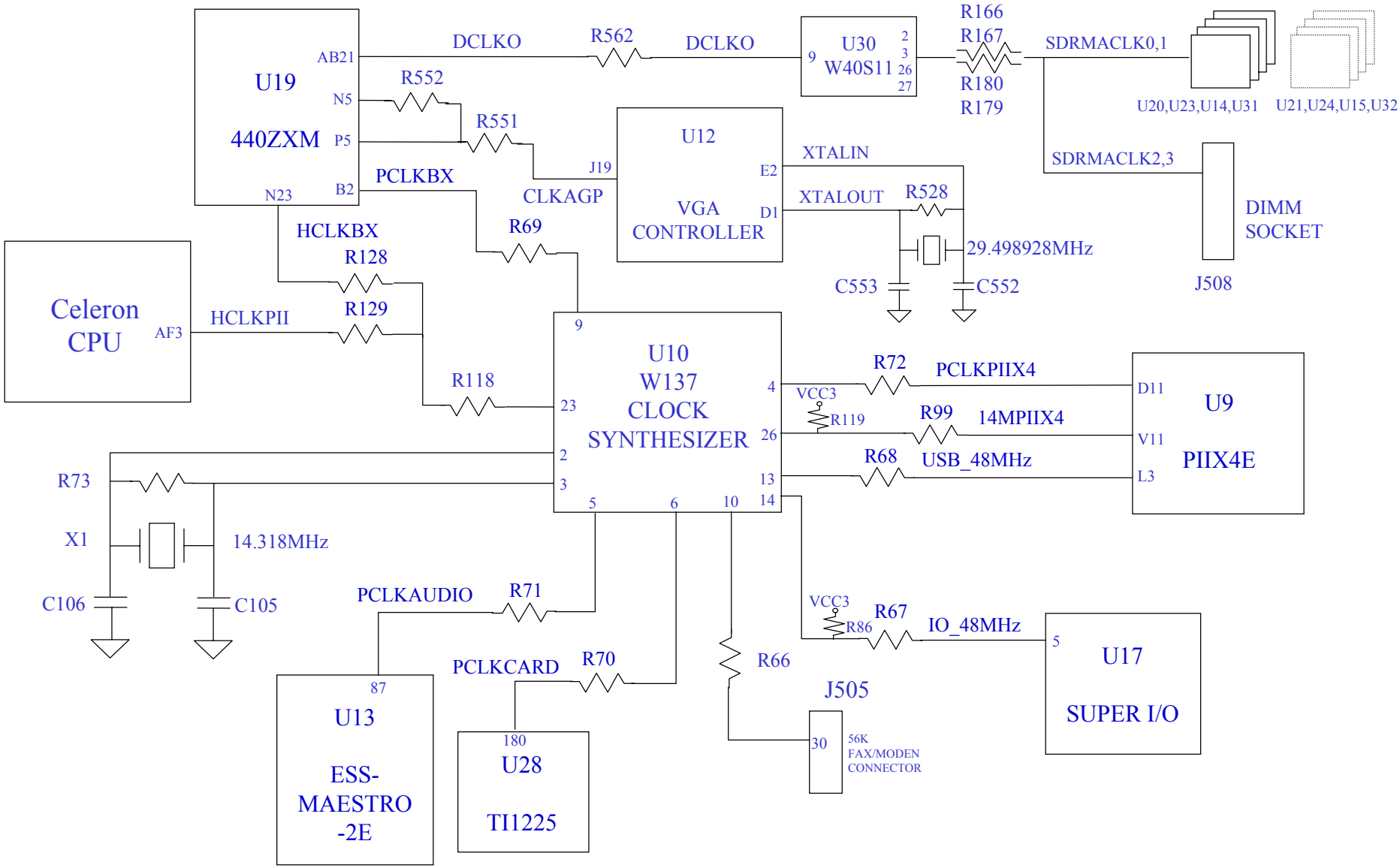
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR



……NEXT PAGE

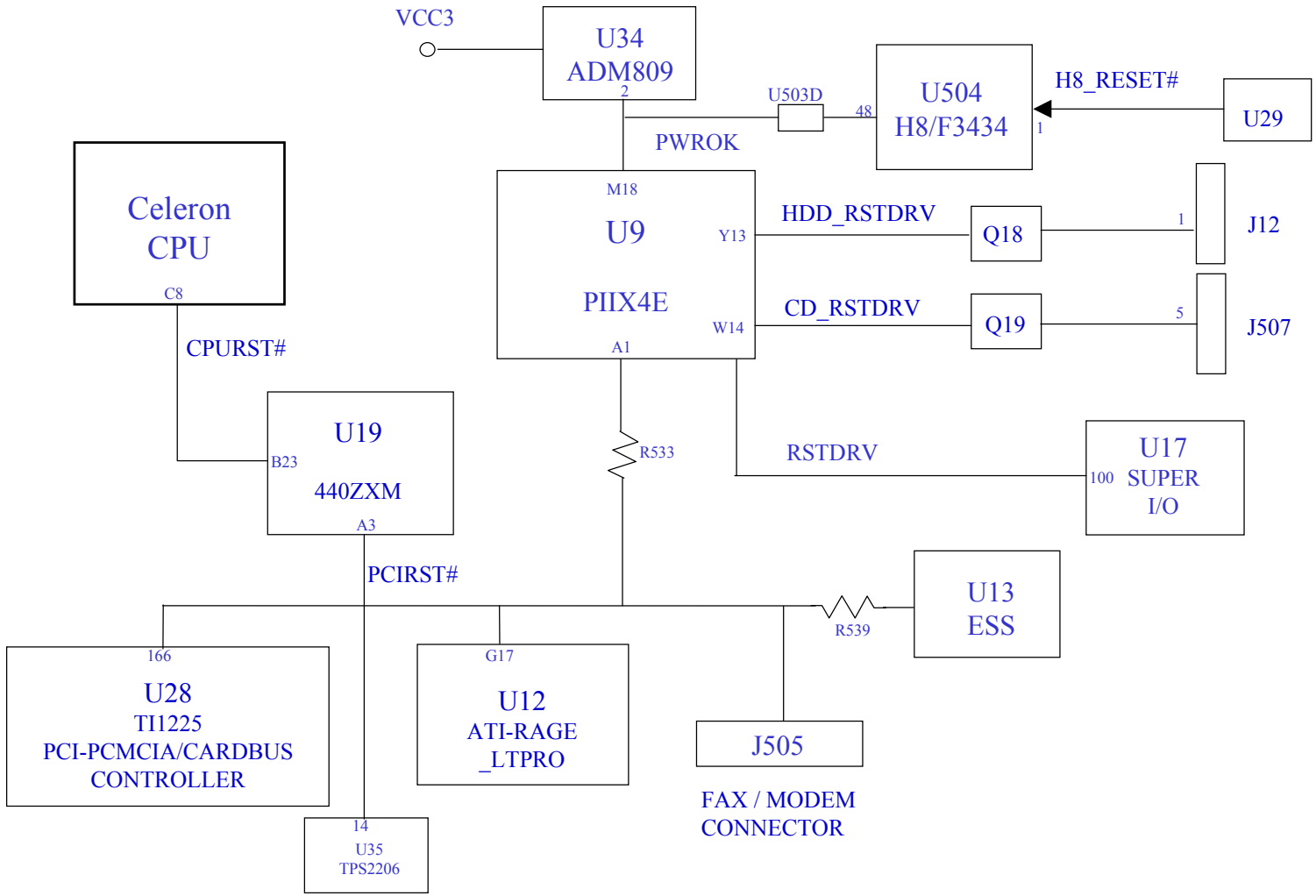
8.2 NO DISPLAY

******SYSTEM CLOCK CHECK ******



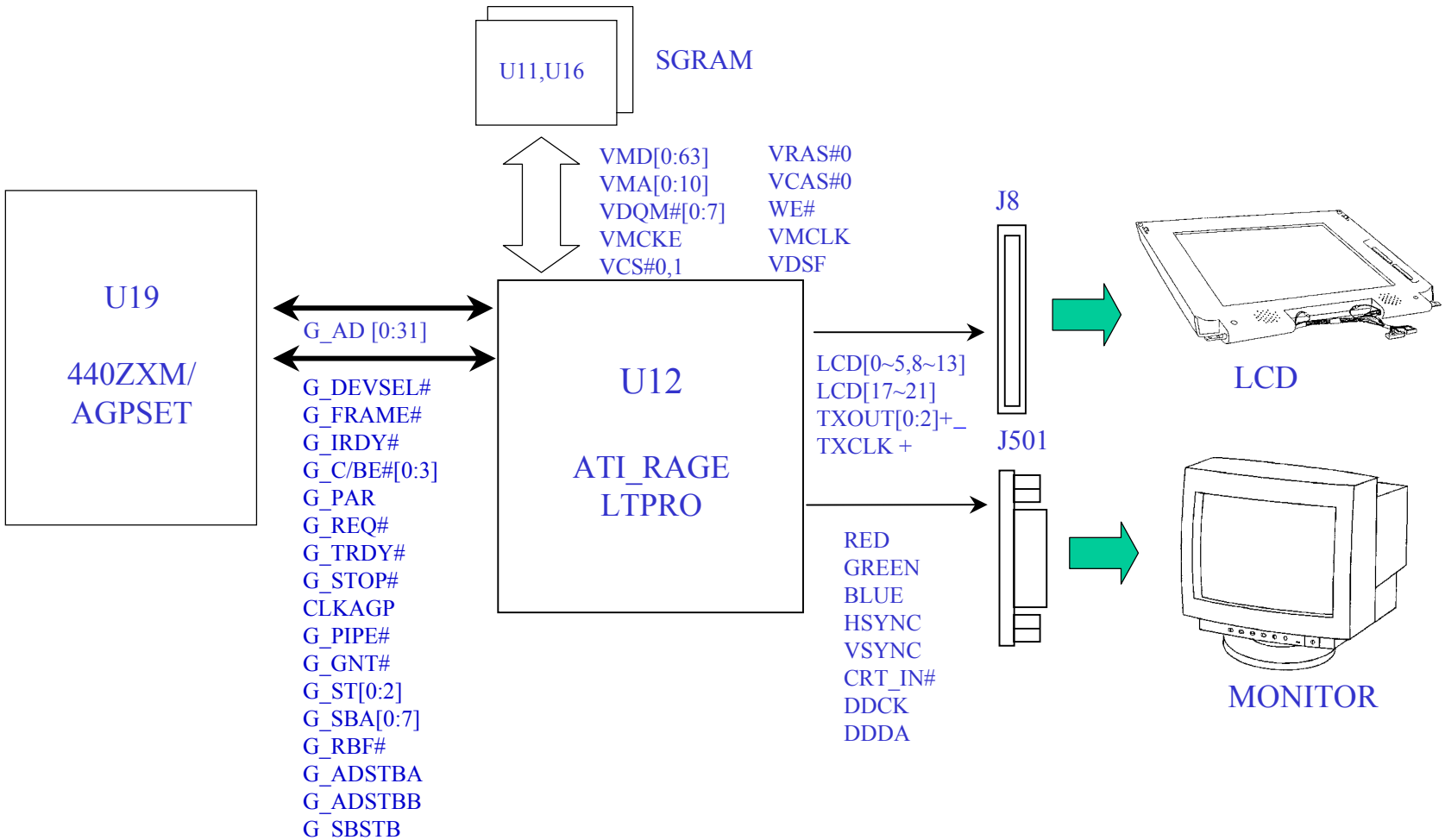
8.2 NO DISPLAY

****** RESET SYSTEM CHECK ******



8.3 VGA CONTROLLER FAILURE

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



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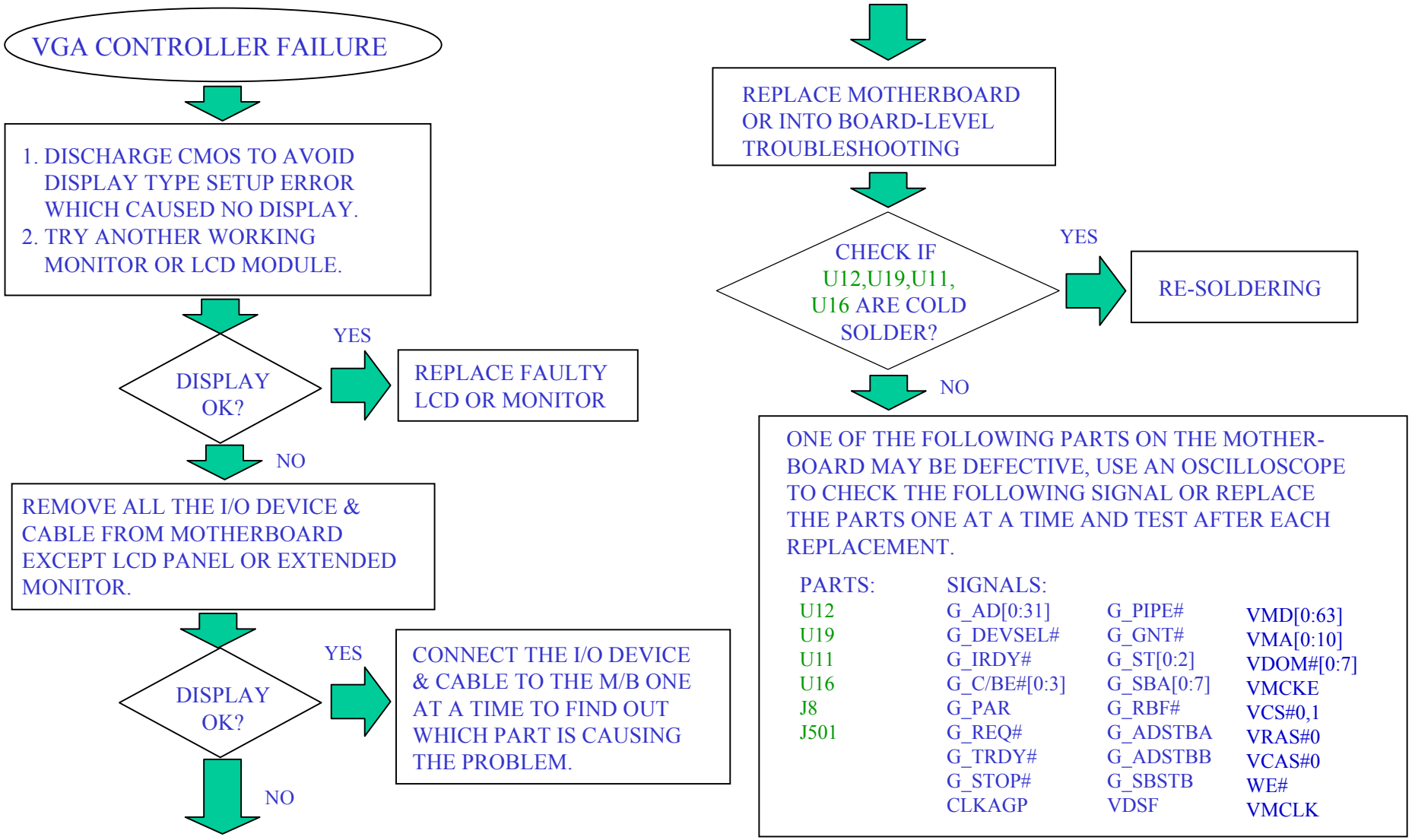
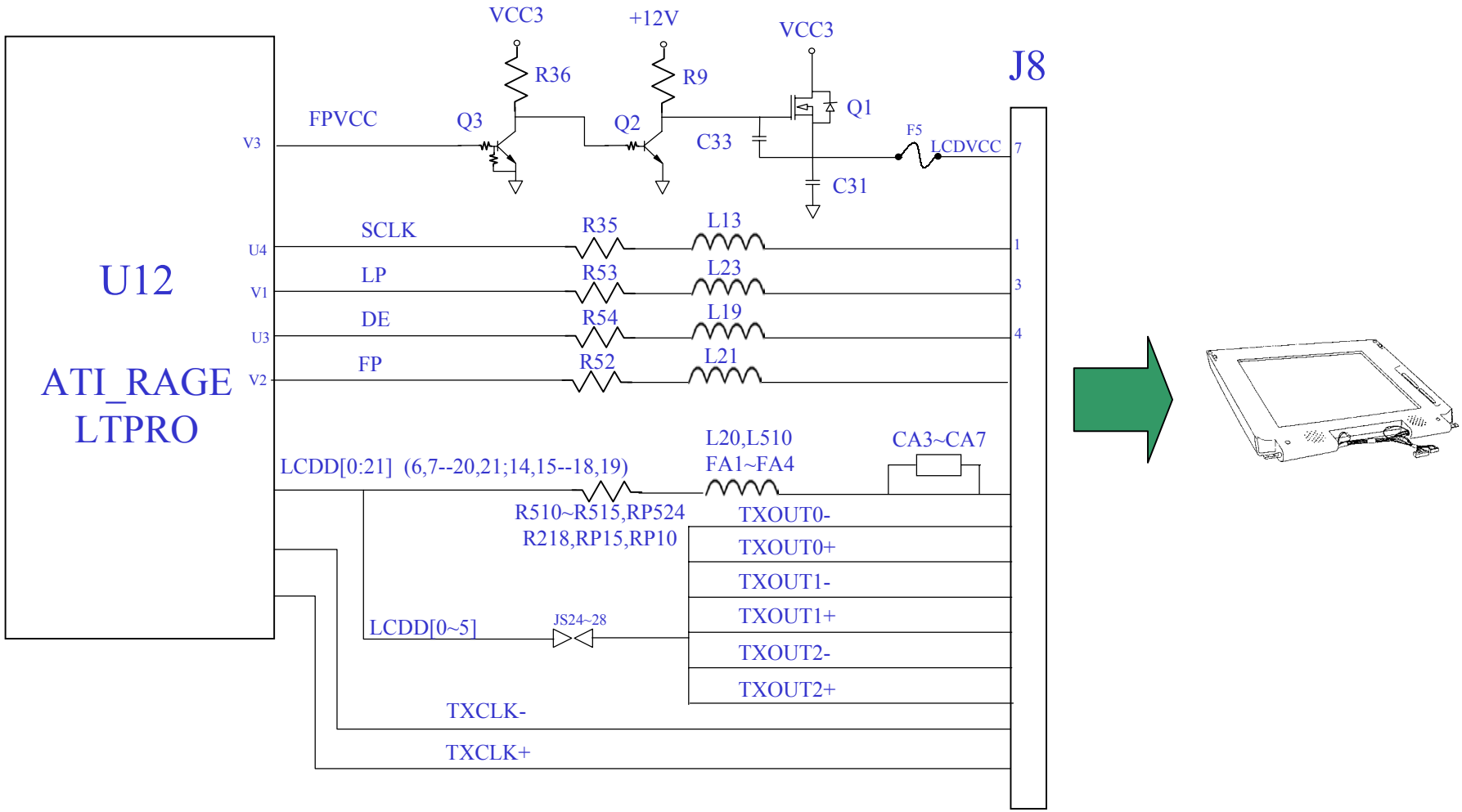


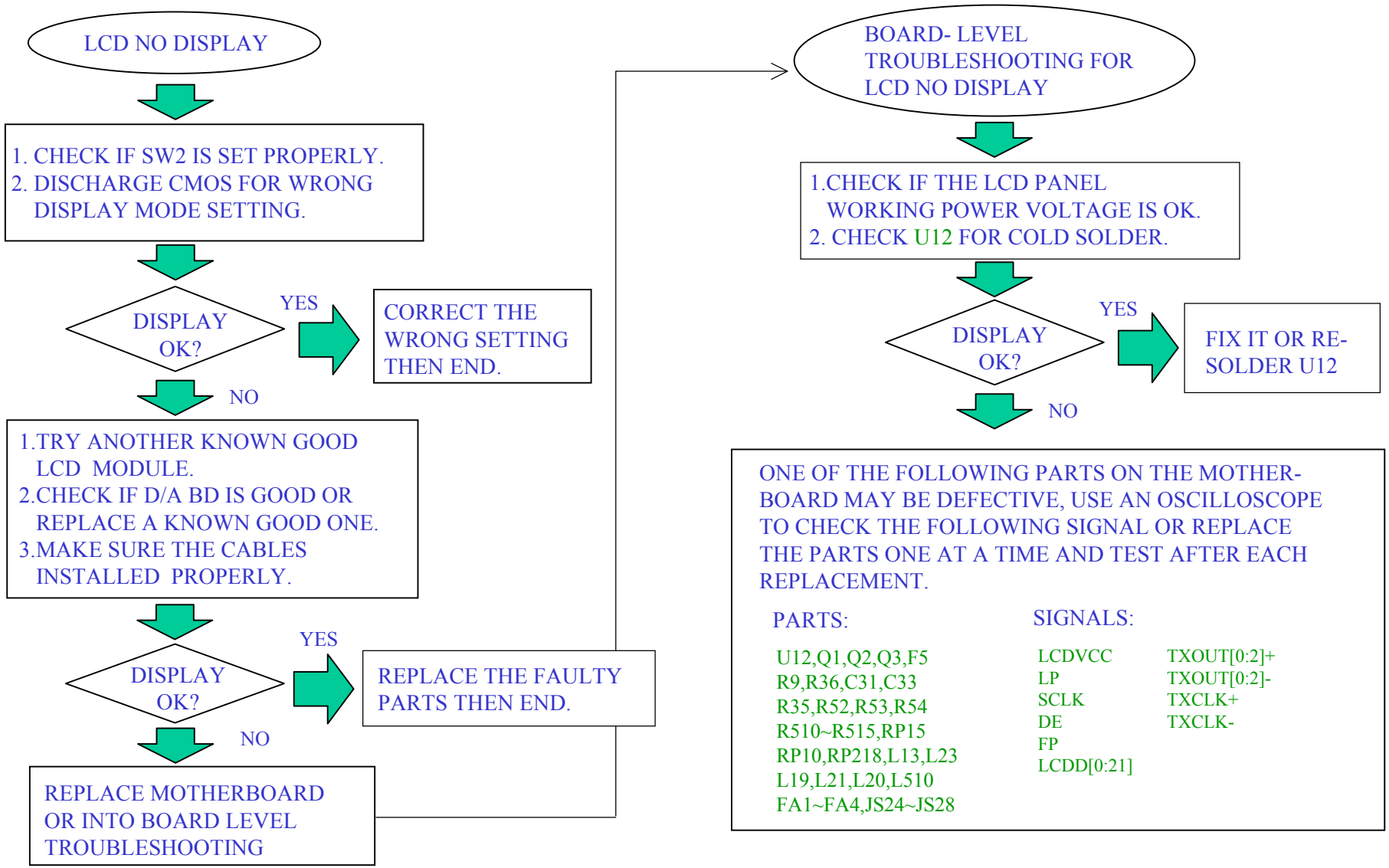
8.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



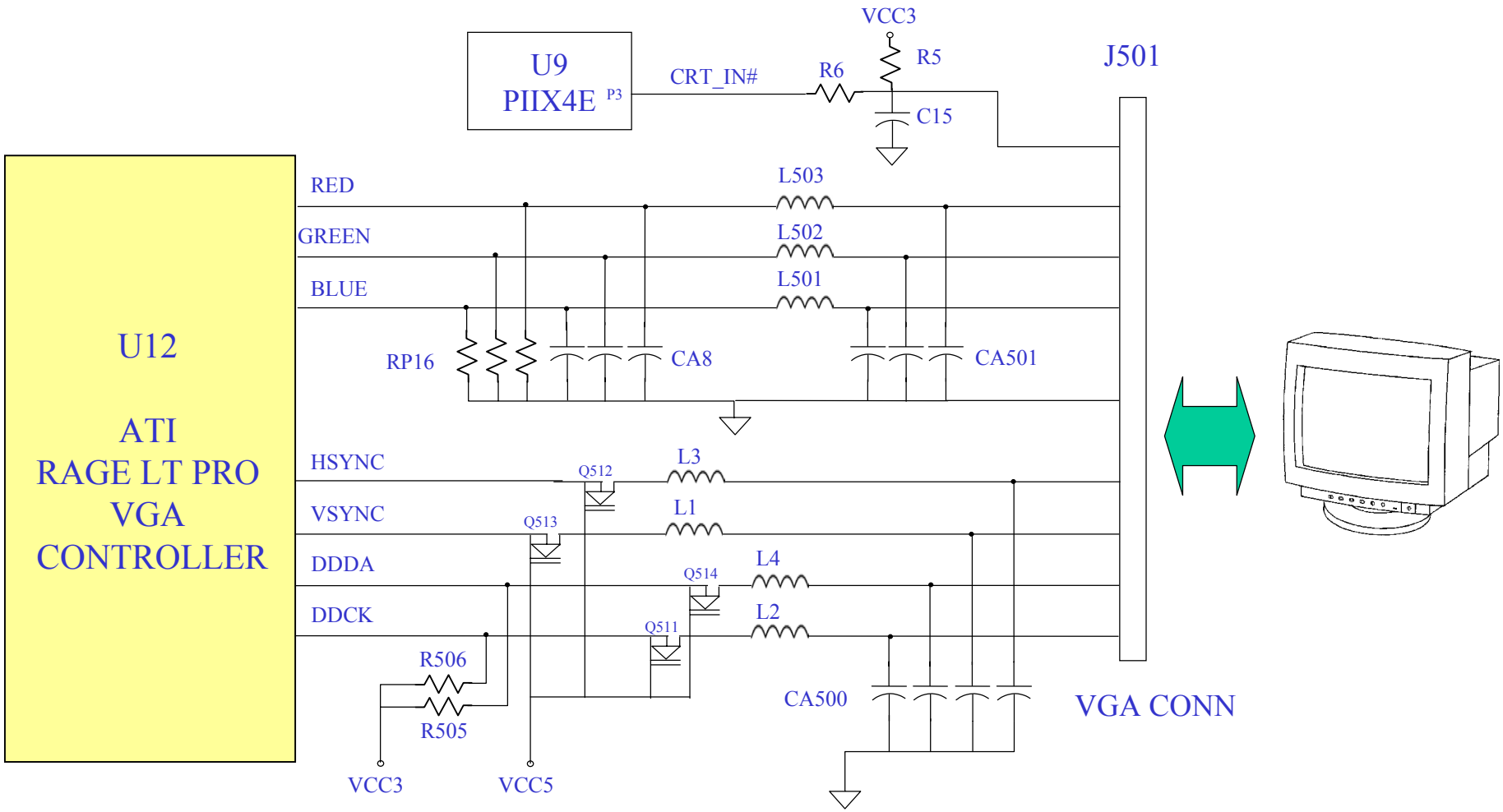
8.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



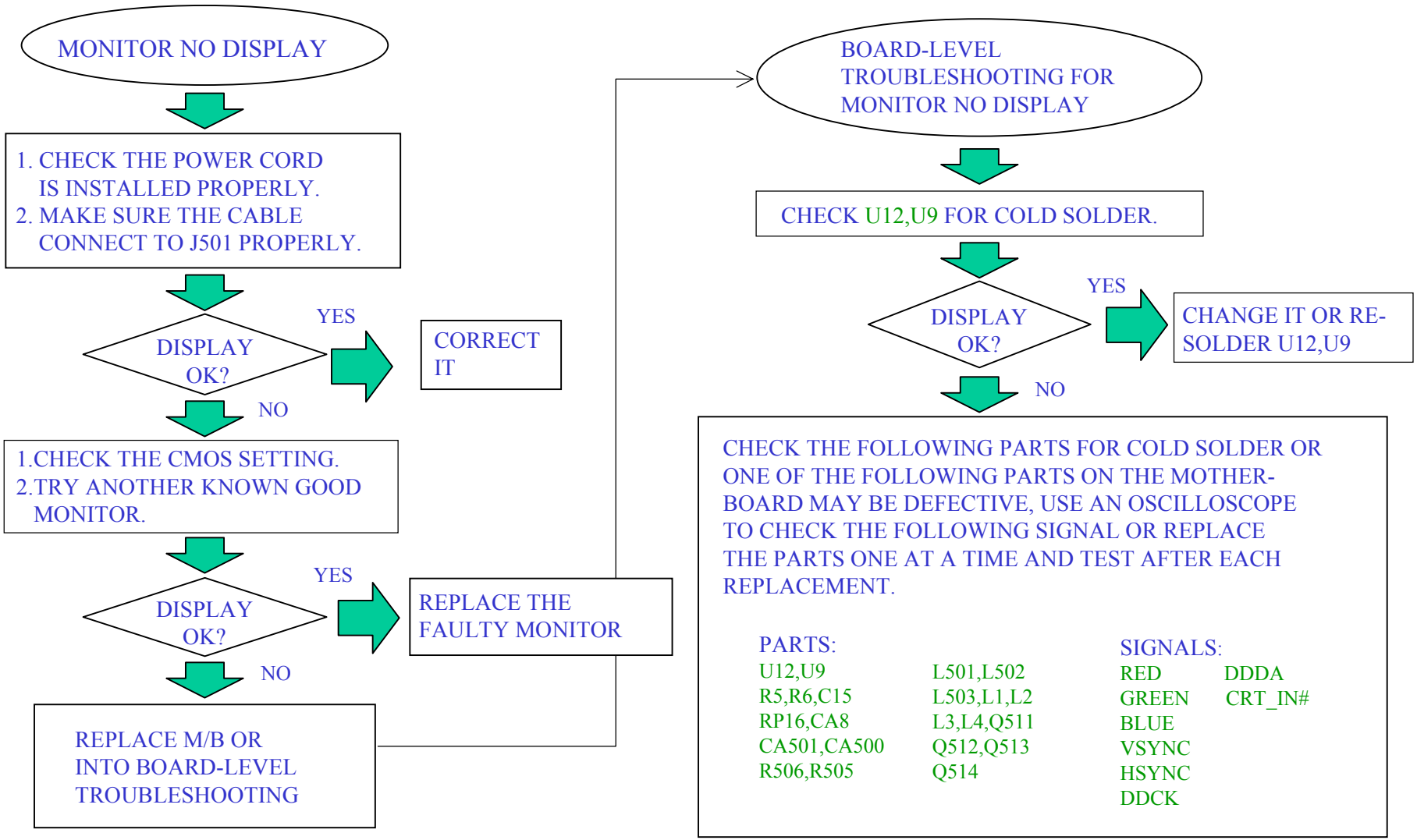
8.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



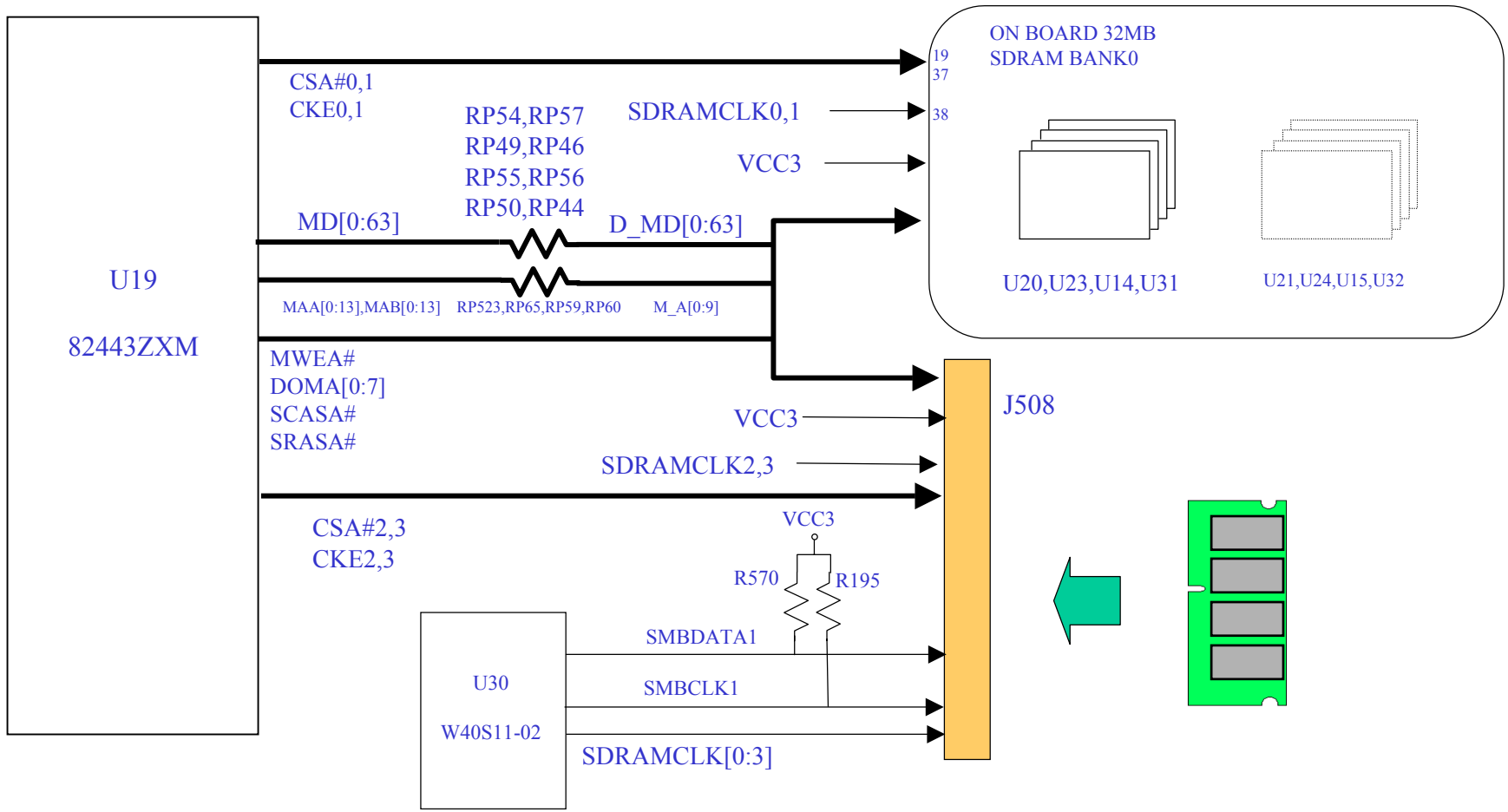
8.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



8.6 MEMORY TEST ERROR

EITHER ON BOARD OR EXTEND SDRAM ,THE ERROR CODE SHOWN
ON THE PIO DEBUG BOARD IS MEAN MEMORY ERROR AND SYSTEM HANGS UP.



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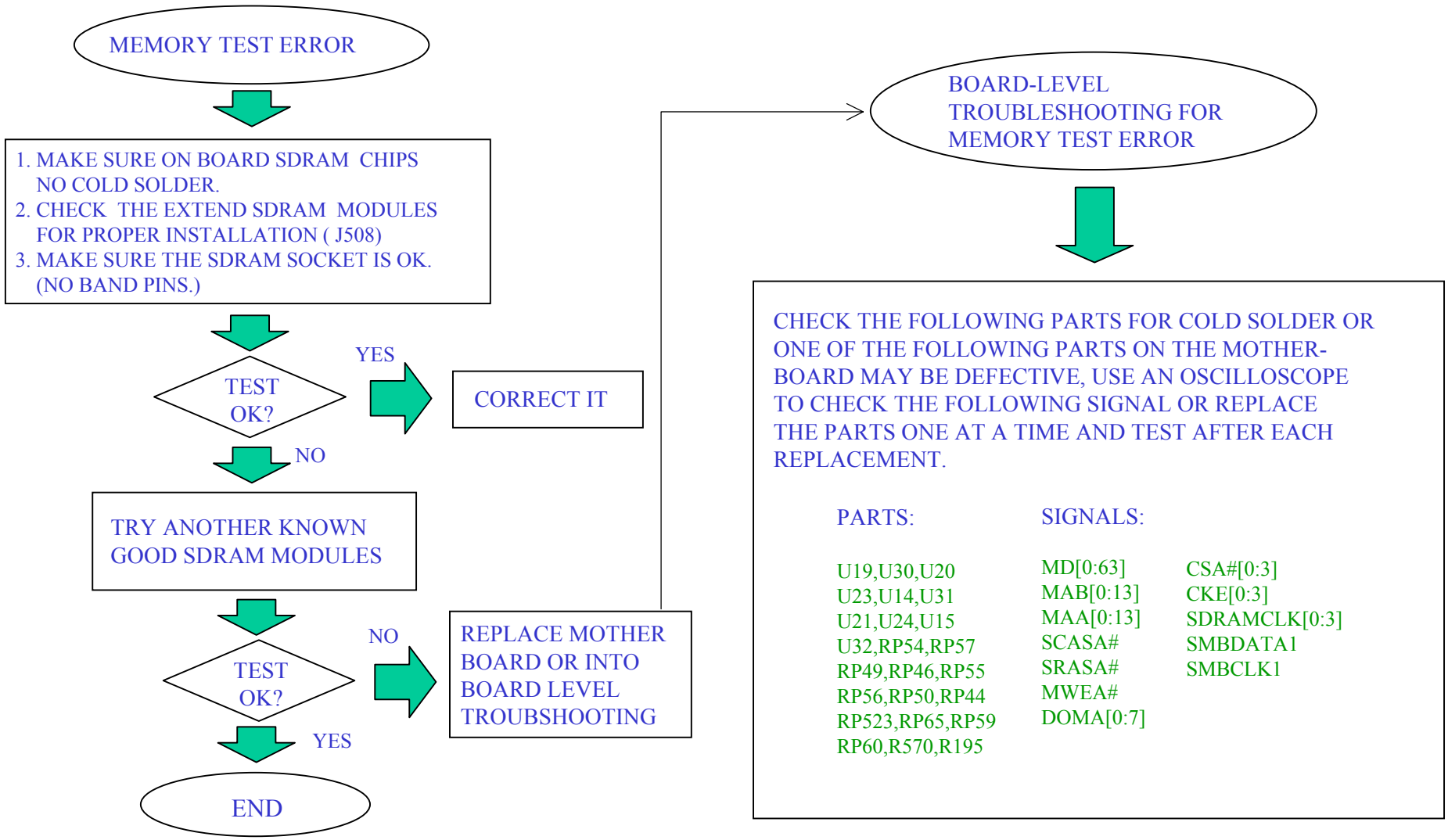
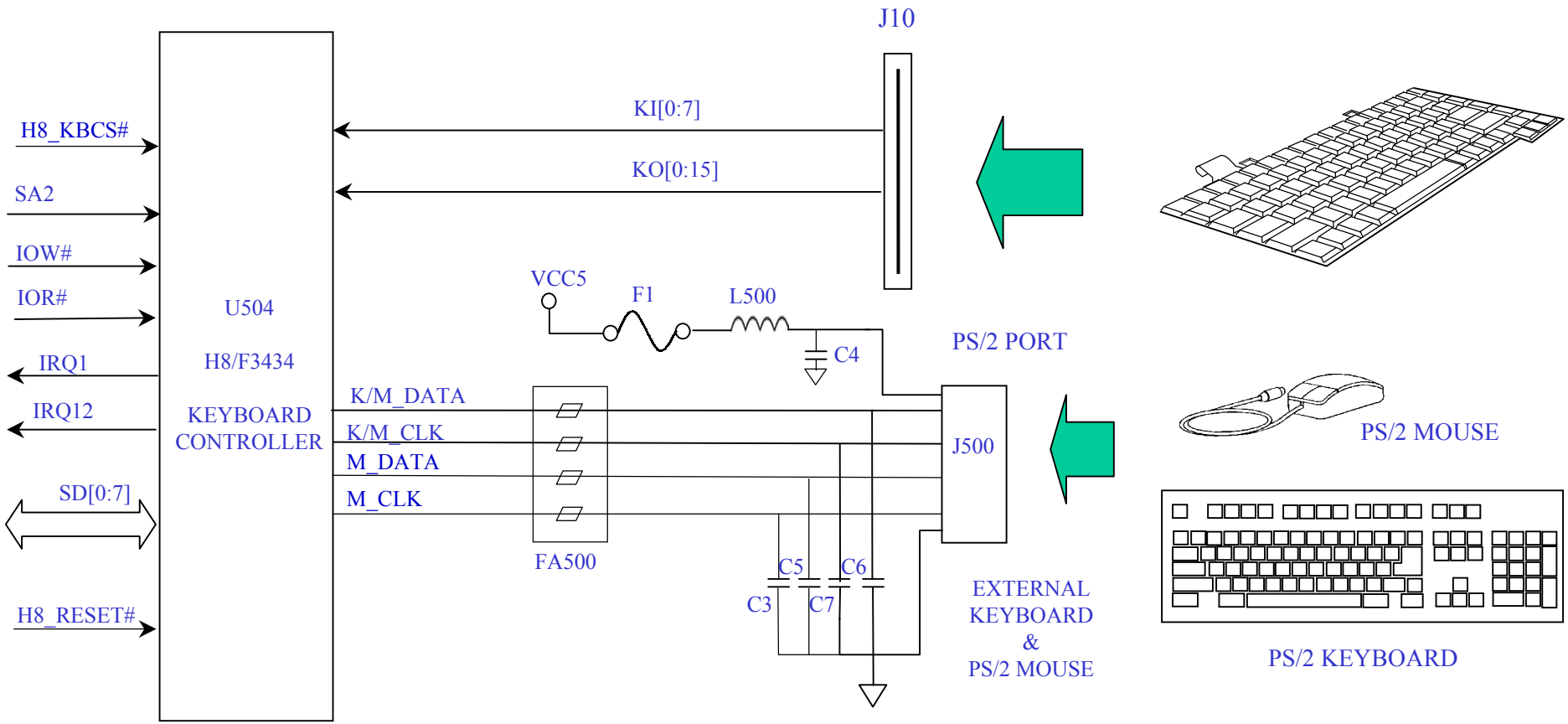


8.7 KEYBOARD TEST ERROR

ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.



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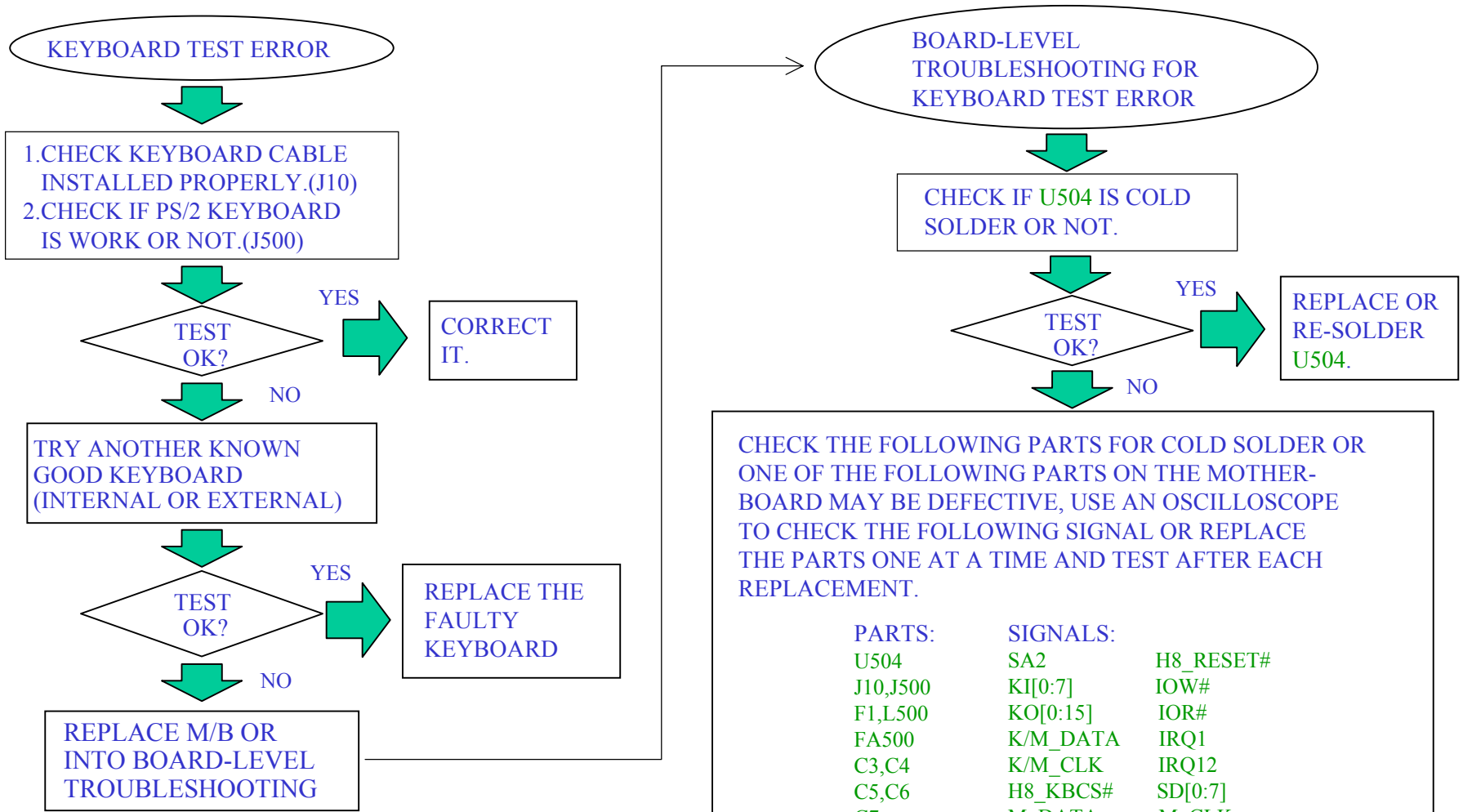
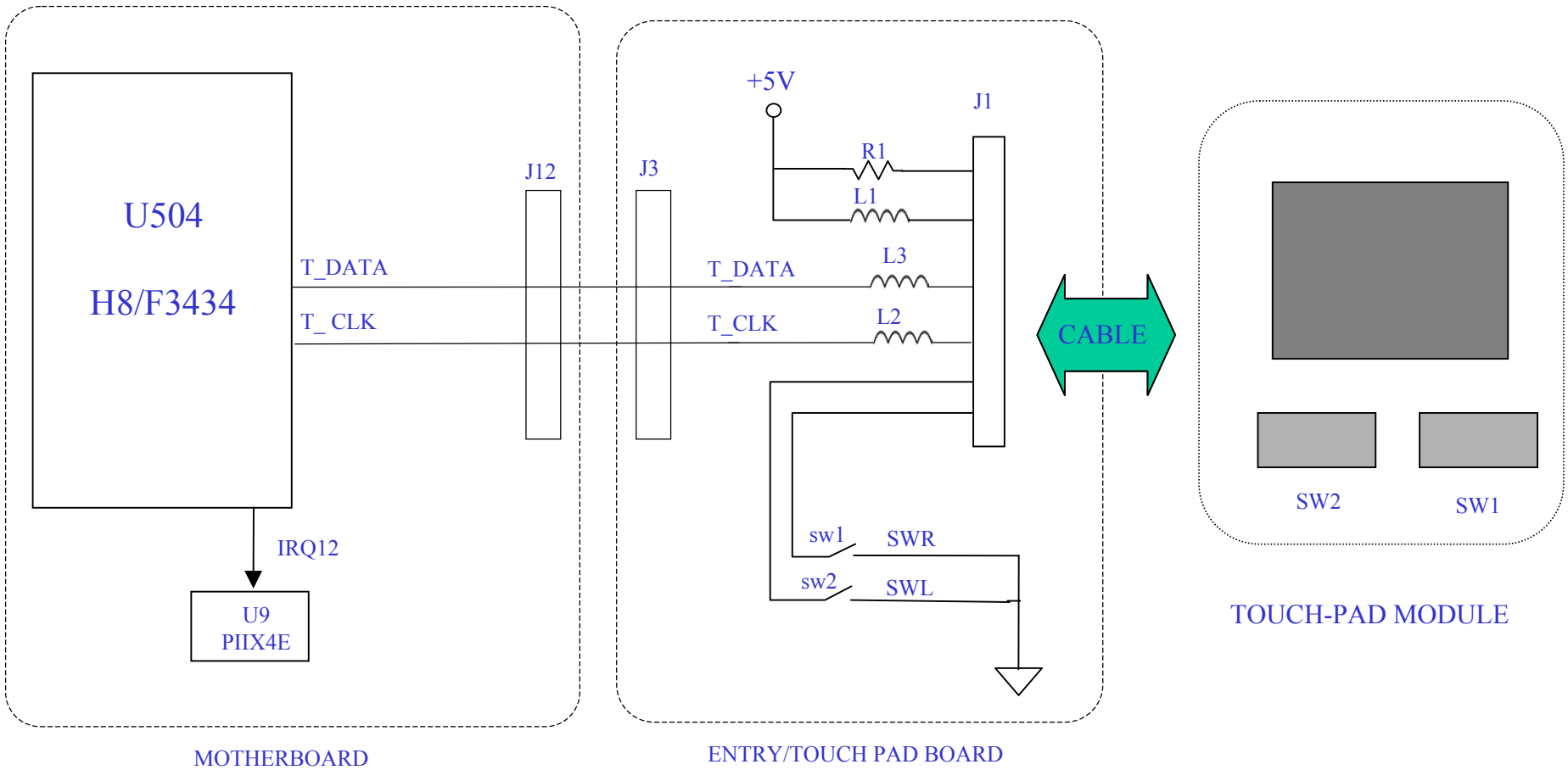


8.8 TRACK PAD TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



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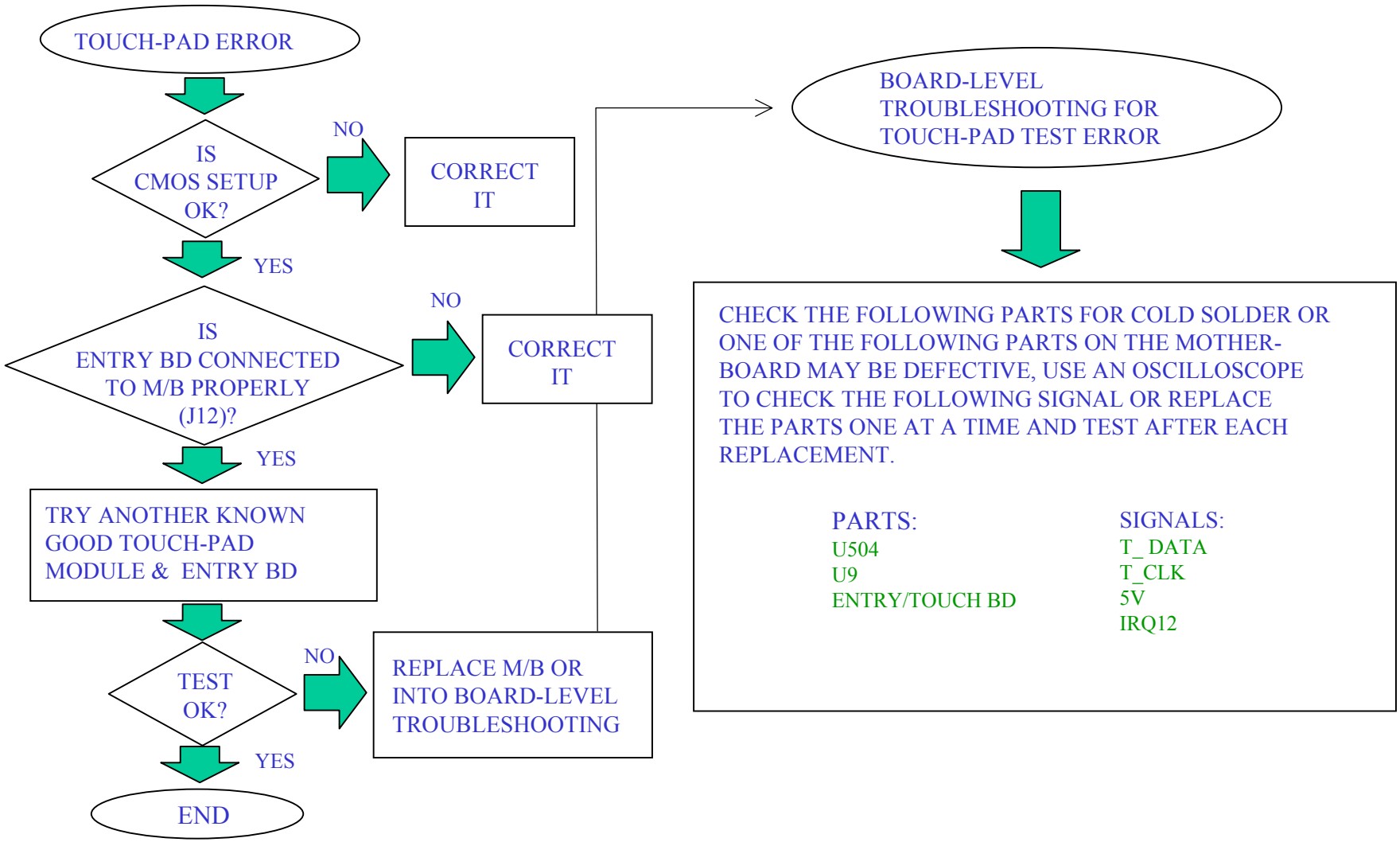
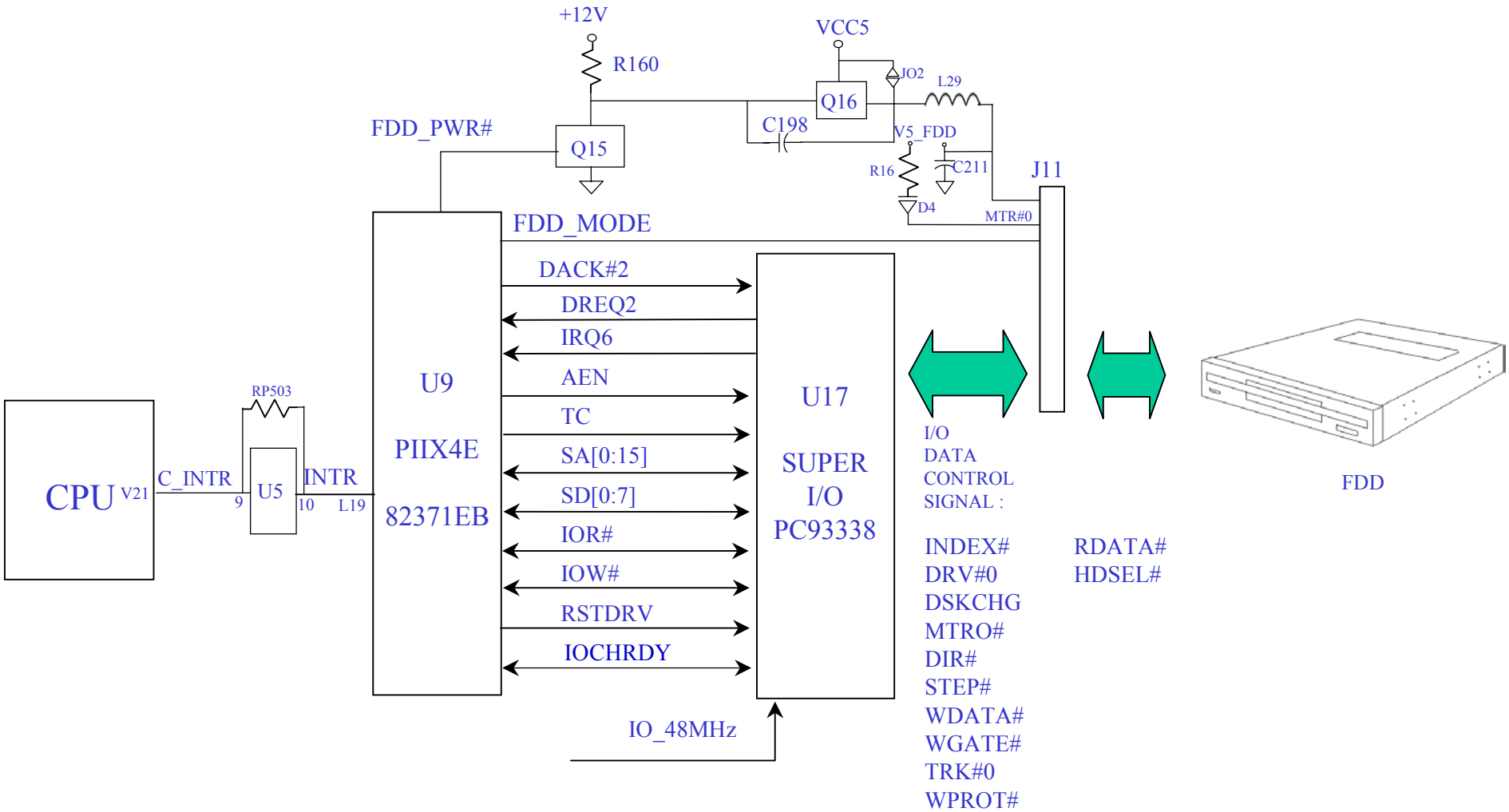
AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



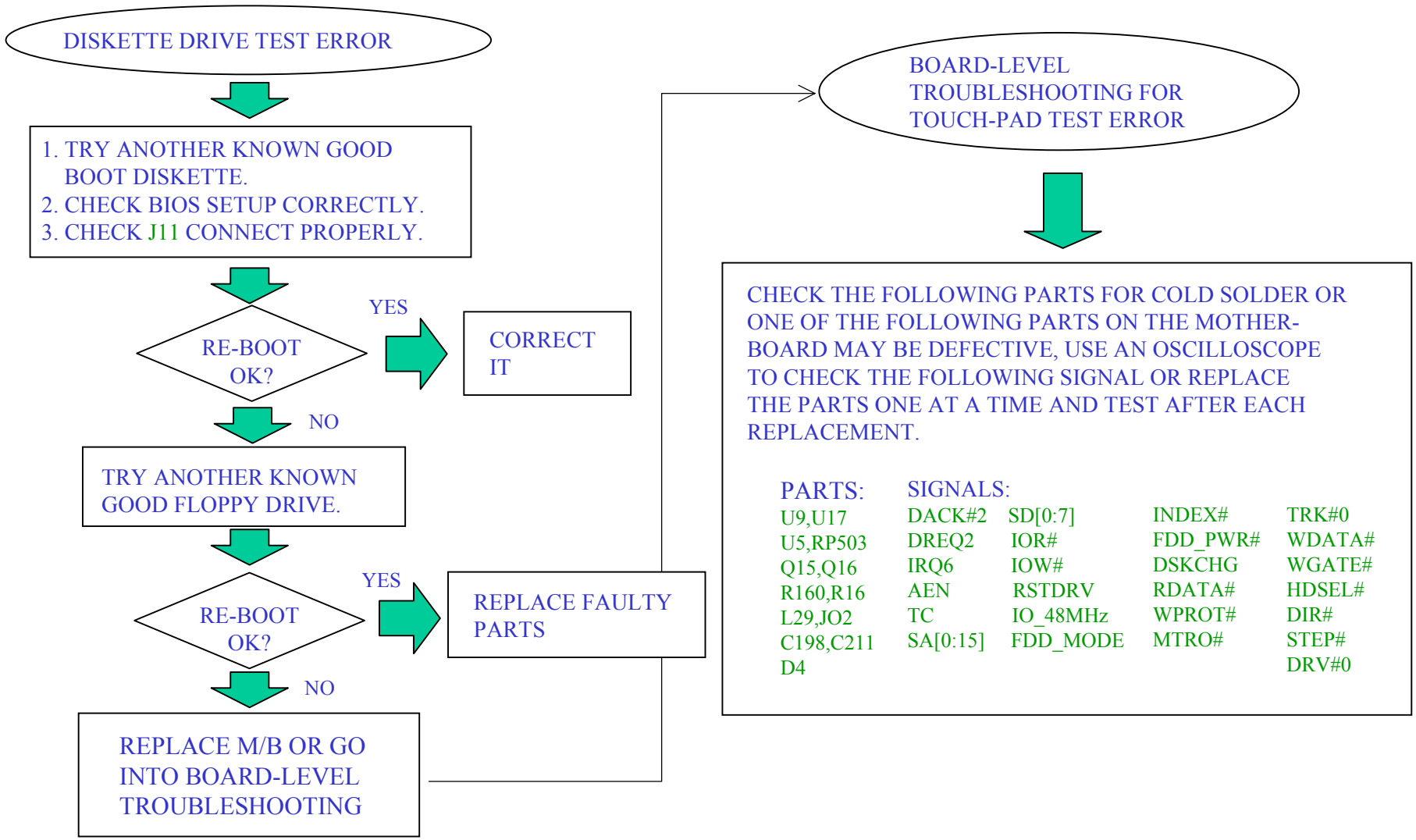
8.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



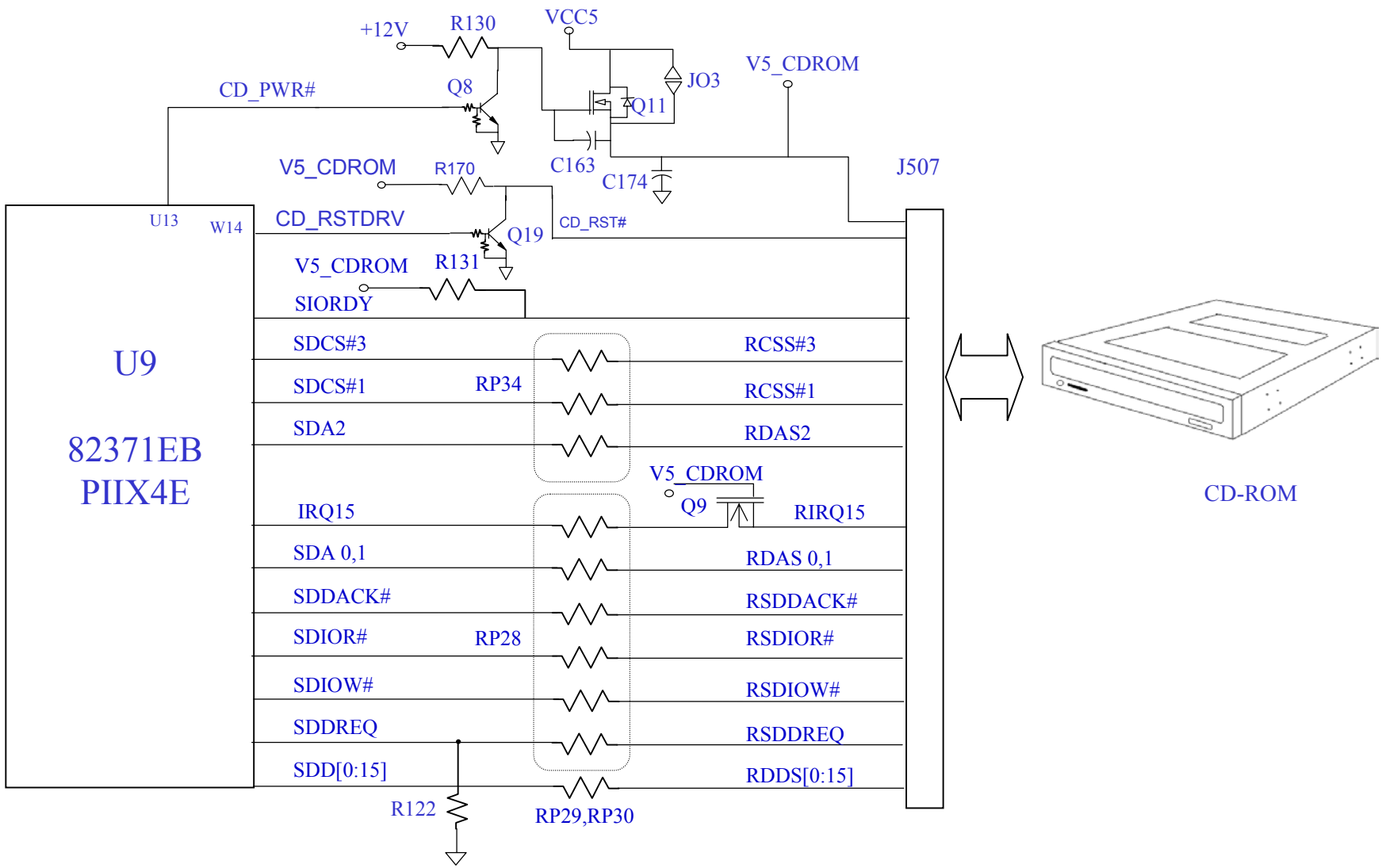
8.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



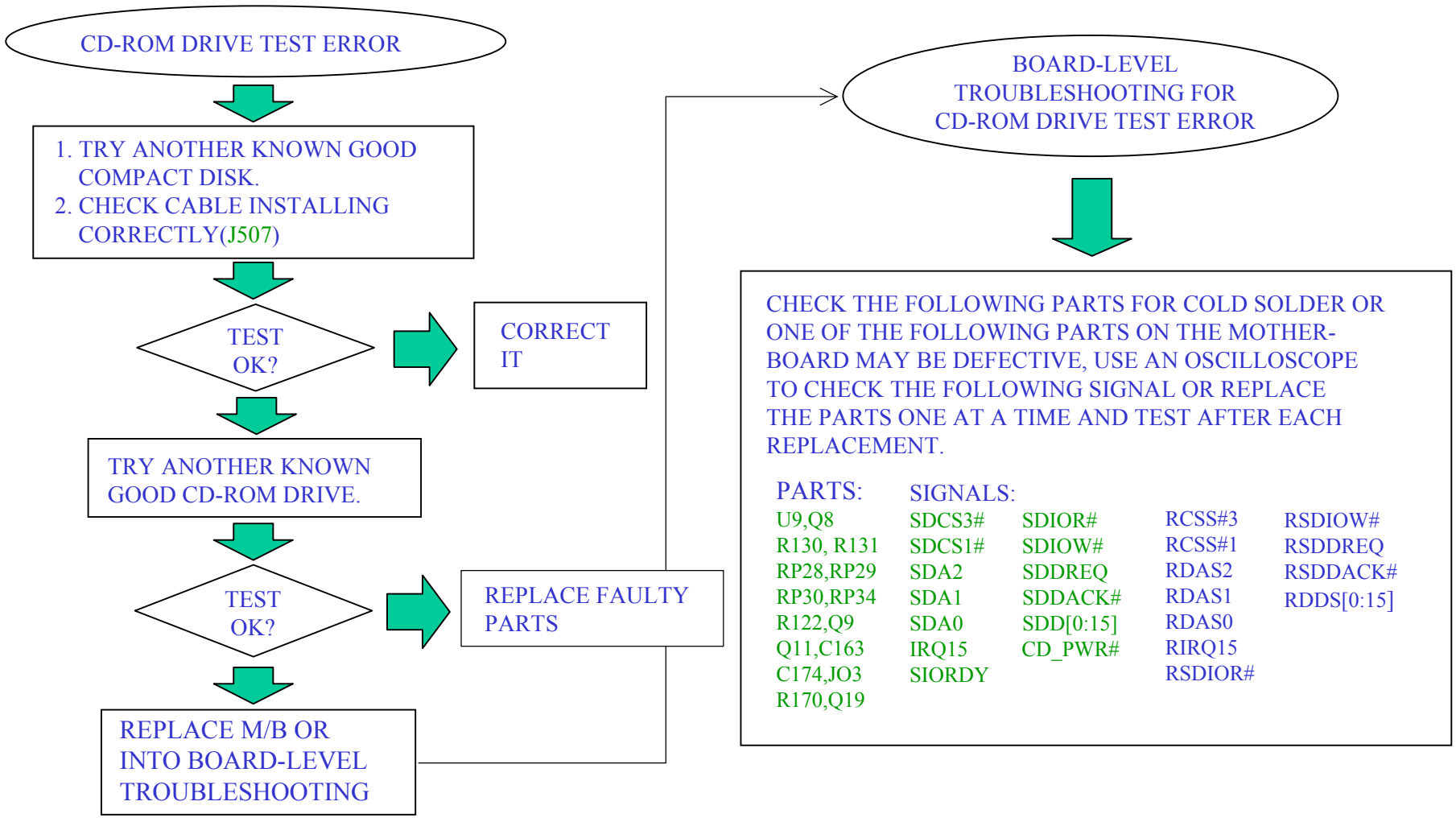
8.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING DATA FROM CD-ROM DRIVE.



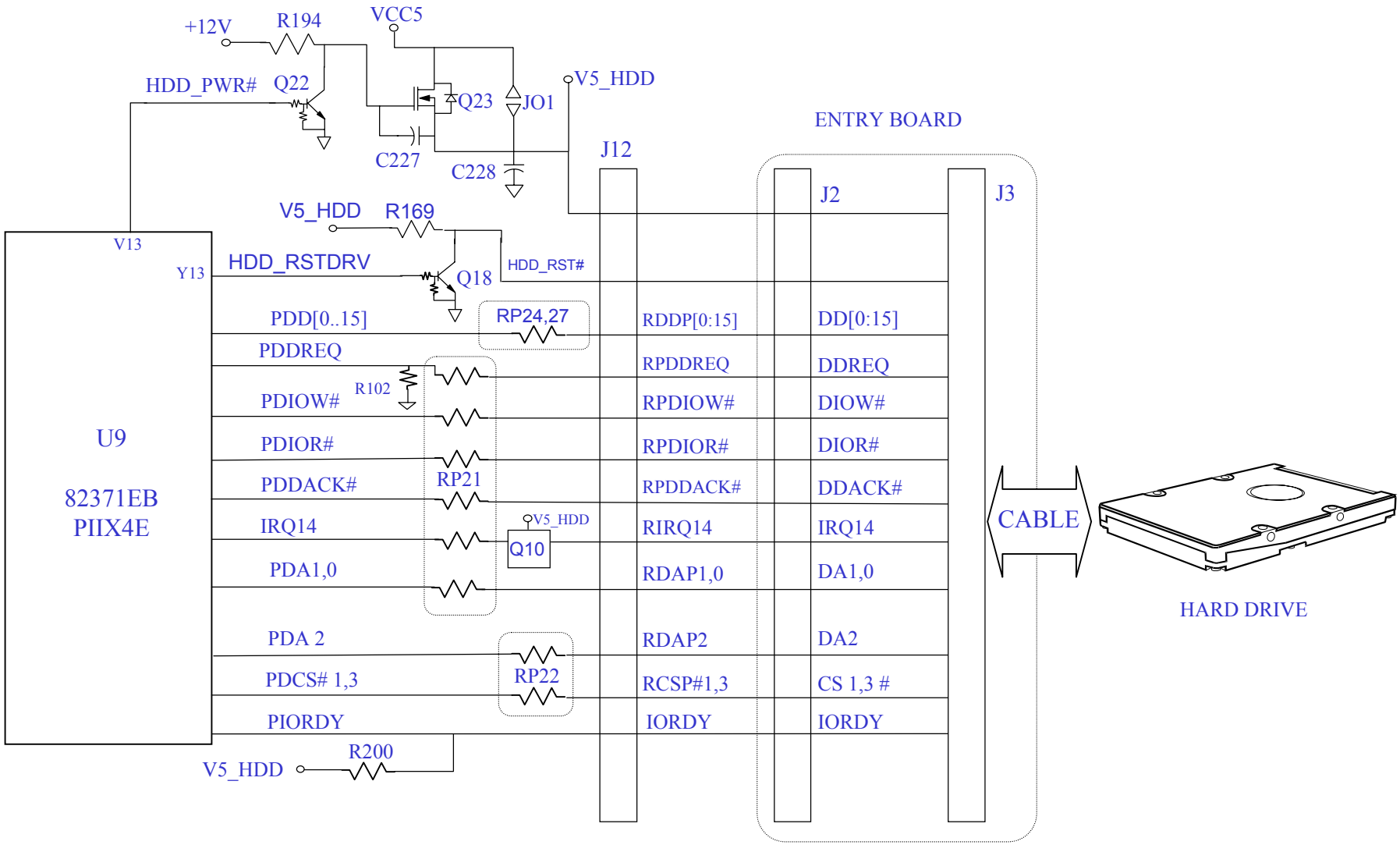
8.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING GATA FROM CD-ROM DRIVE.



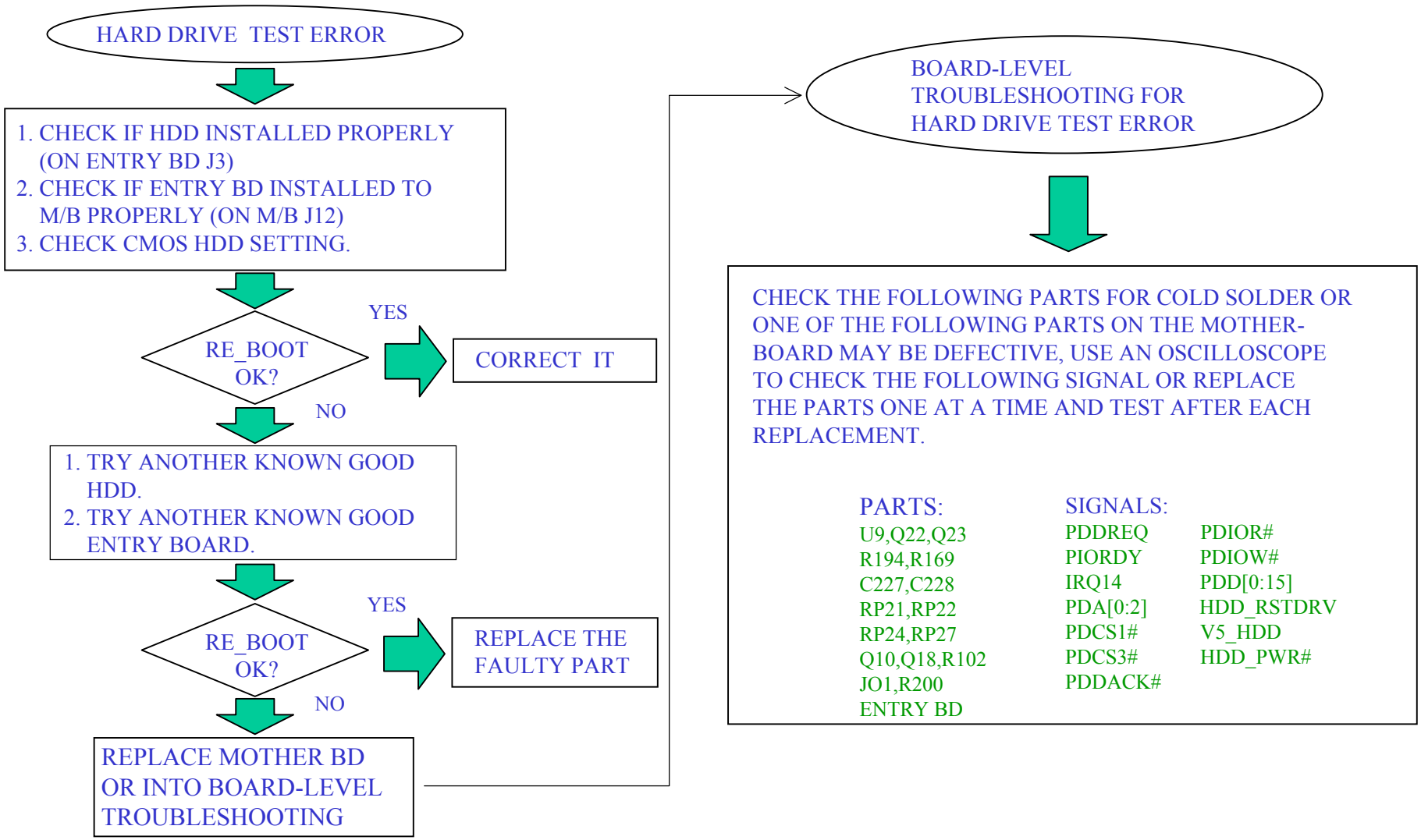
8.11 HARD DRIVE TEST ERROR

EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR CONTINUES SPINNING , WHILE READING DATA IS FROM OR WRITING DATA IS TO HARD DRIVE.



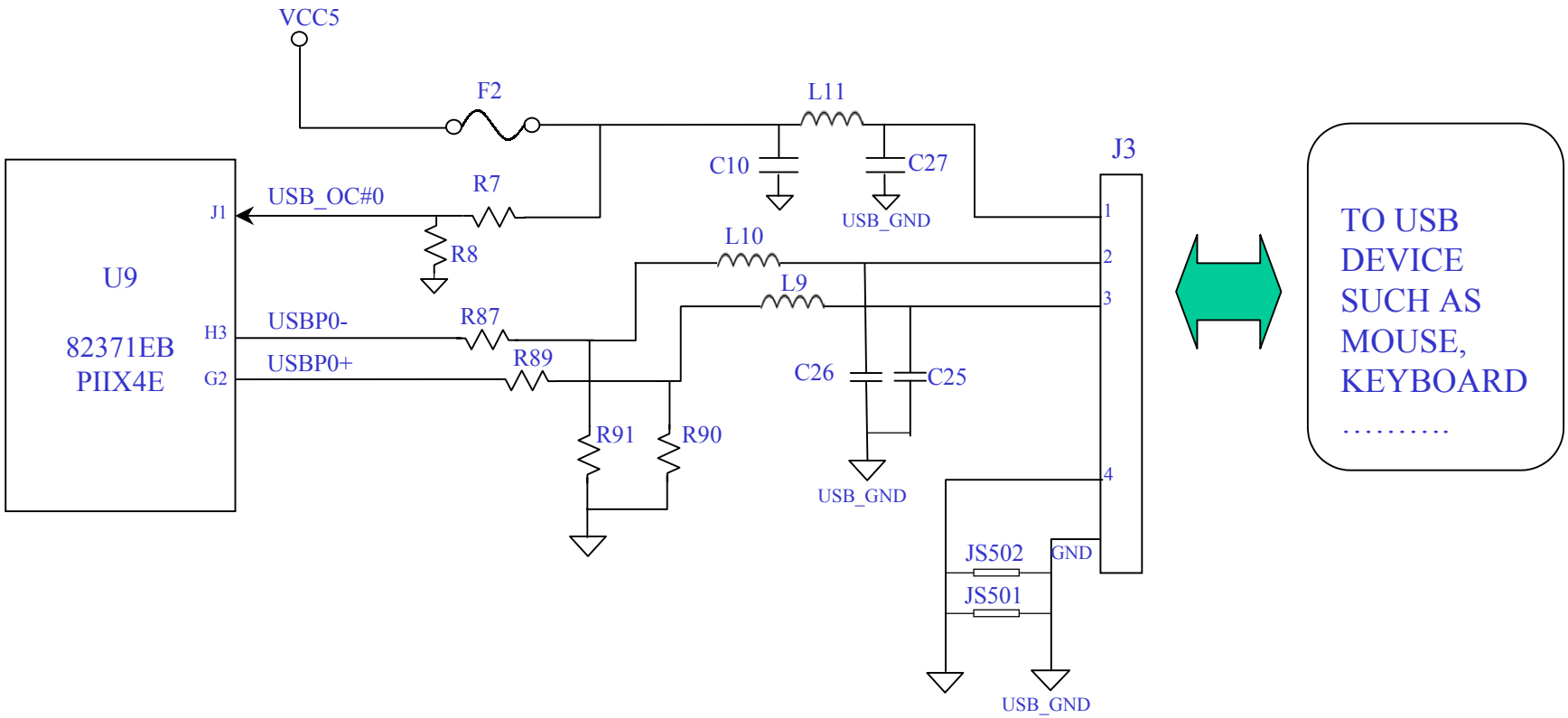
8.11 HARD DRIVE TEST ERROR

EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR CONTINUES SPINNING , WHILE READING DATA IS FROM OR WRITING DATA IS TO HARD DRIVE.



8.12 USB PORT TEST ERROR

AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



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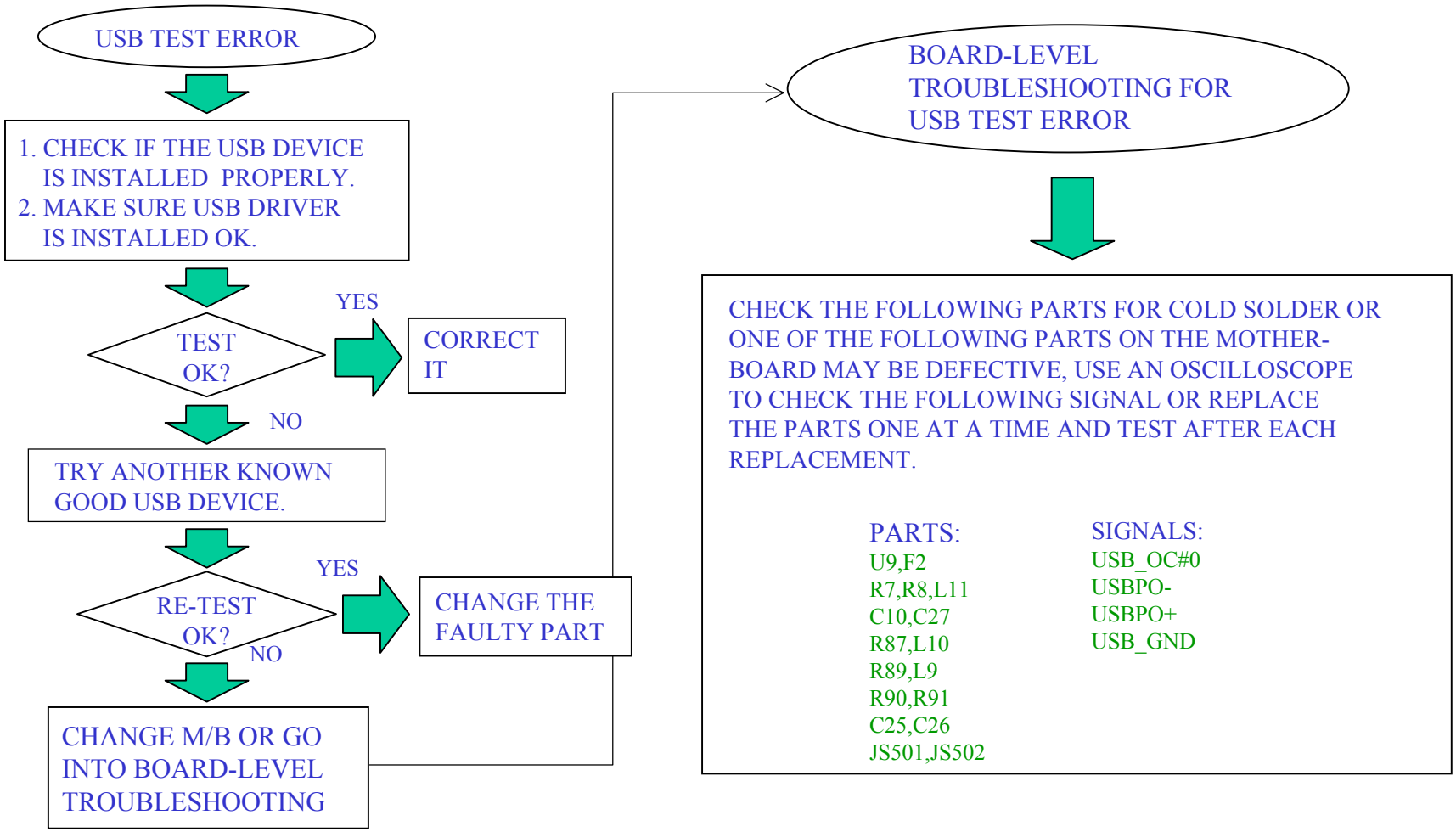
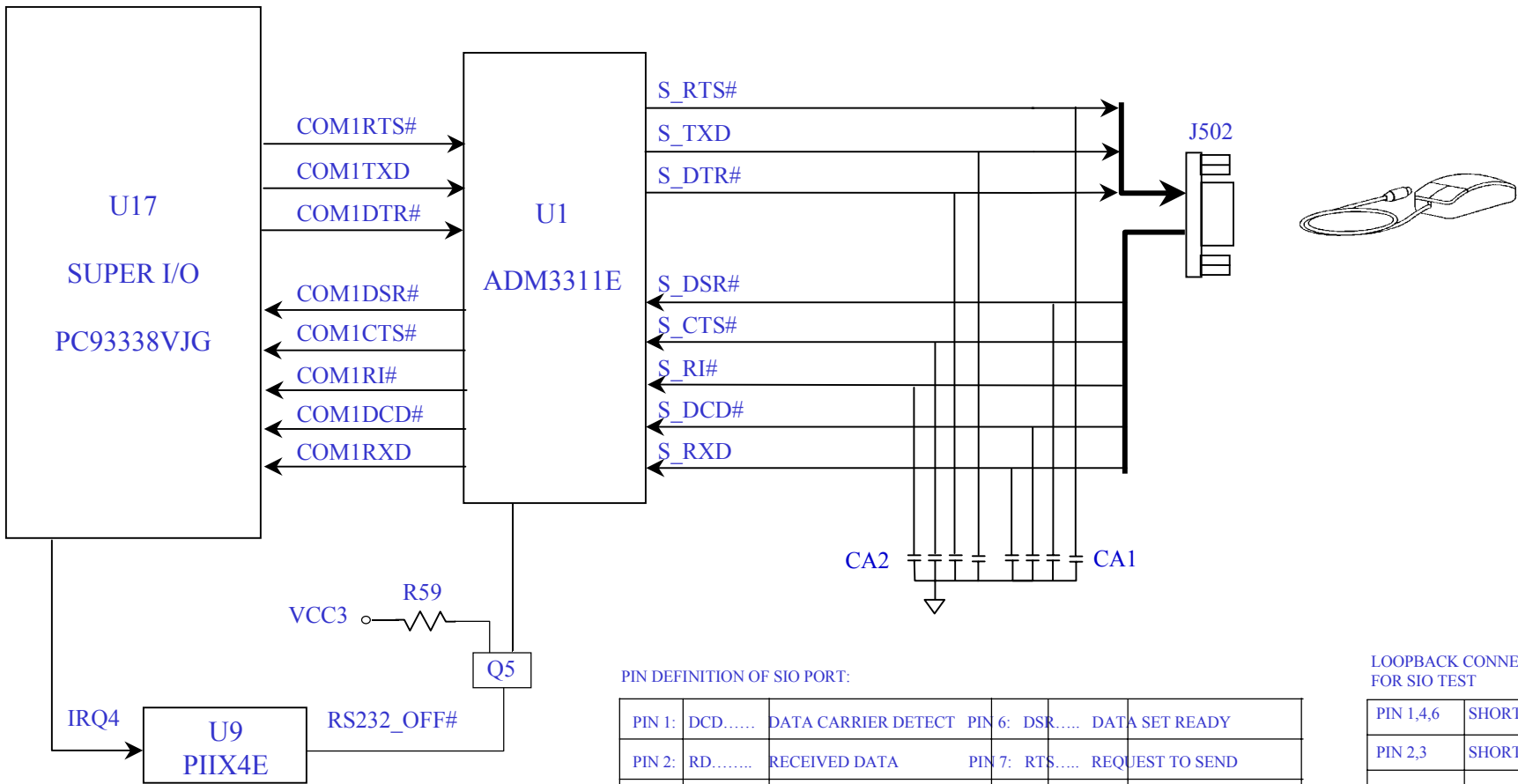


8.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

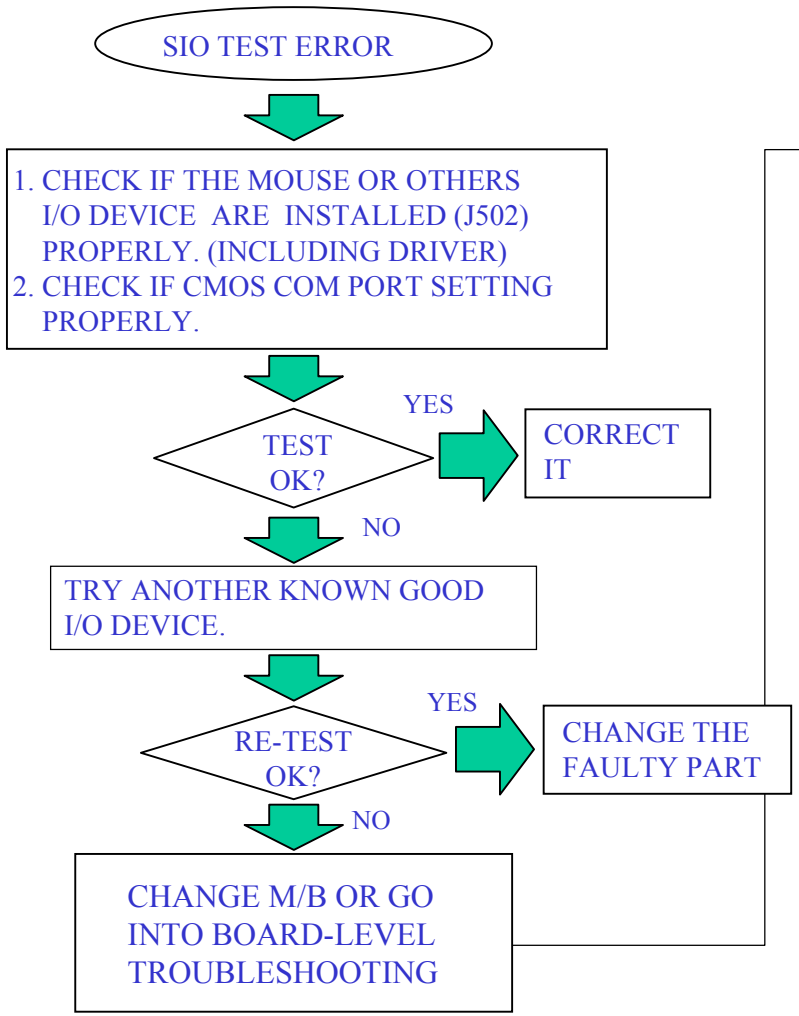
PIN 1:	DCD……	DATA CARRIER DETECT	PIN 6:	DSR…..	DATA SET READY
PIN 2:	RD……..	RECEIVED DATA	PIN 7:	RTS…..	REQUEST TO SEND
PIN 3:	TD……..	TRANSMIT	PIN 8:	CTS…..	CLEAR TO SEND
PIN 4:	DTR……	DATA TERMINAL READY	PIN9:	RI…….	RING INDICATOR
PIN 5:	SG……..	SIGNAL GROUND			

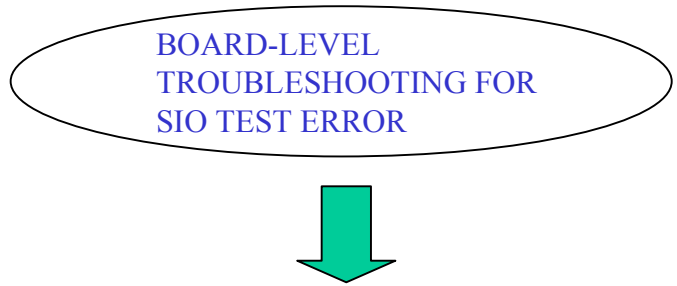
LOOPBACK CONNECTOR FOR SIO TEST

PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

8.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.





CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

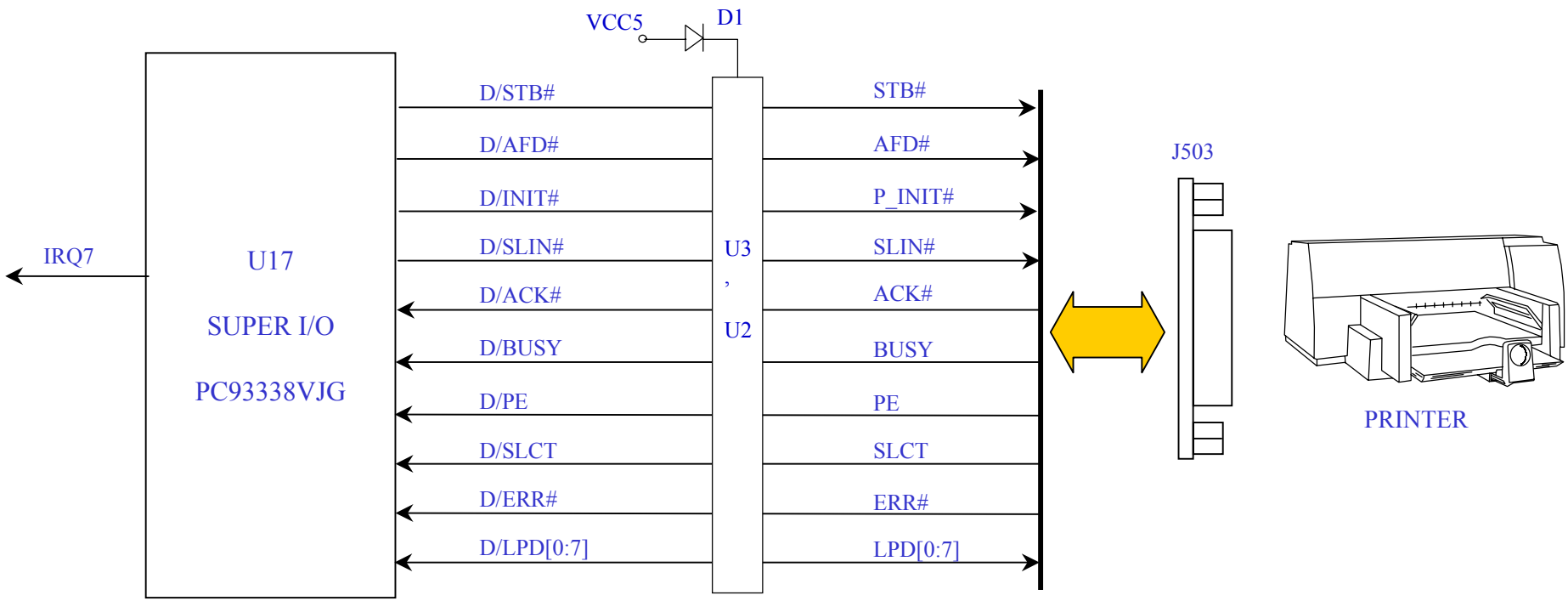
PARTS:
U17,U1
U9,Q5
R59
CA2,CA1

SIGNALS:

IRQ4	COM1DSR#	S_TXD
RS232_OFF#	COM1RI#	S_RXD
COM1RTS#	S_RTS#	
COM1TXD	S_DTR#	
COM1DTR#	S_DSR#	
COM1CTS#	S_CTS#	
COM1RXD	S_RI#	
COM1DCD#	S_DCD#	

8.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

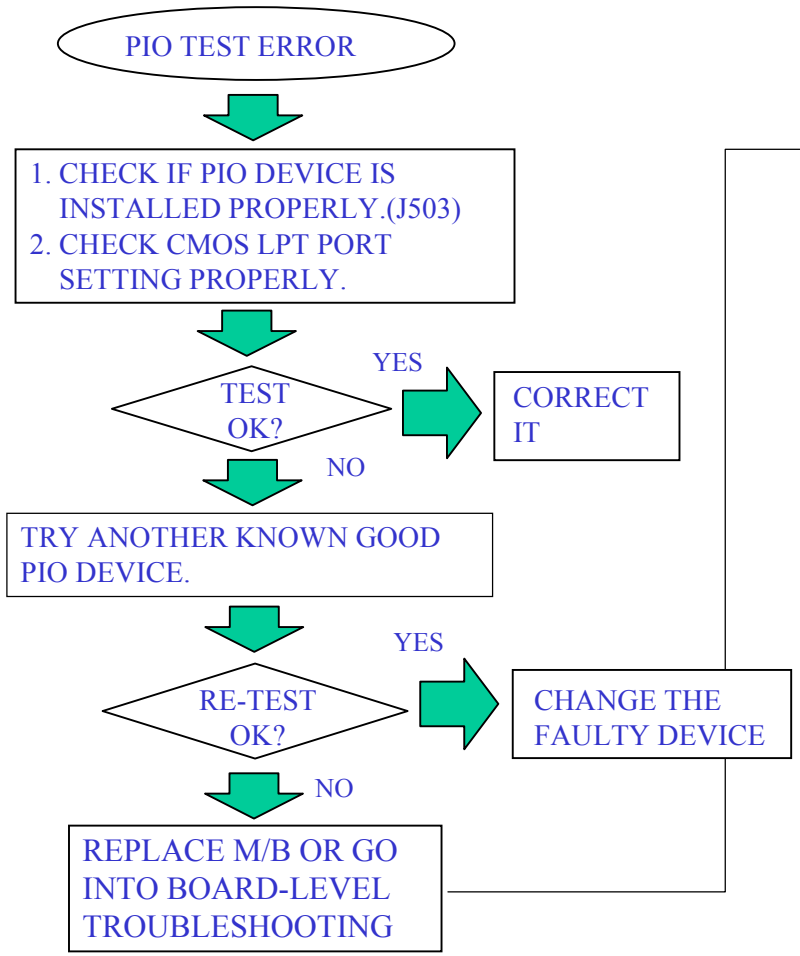
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

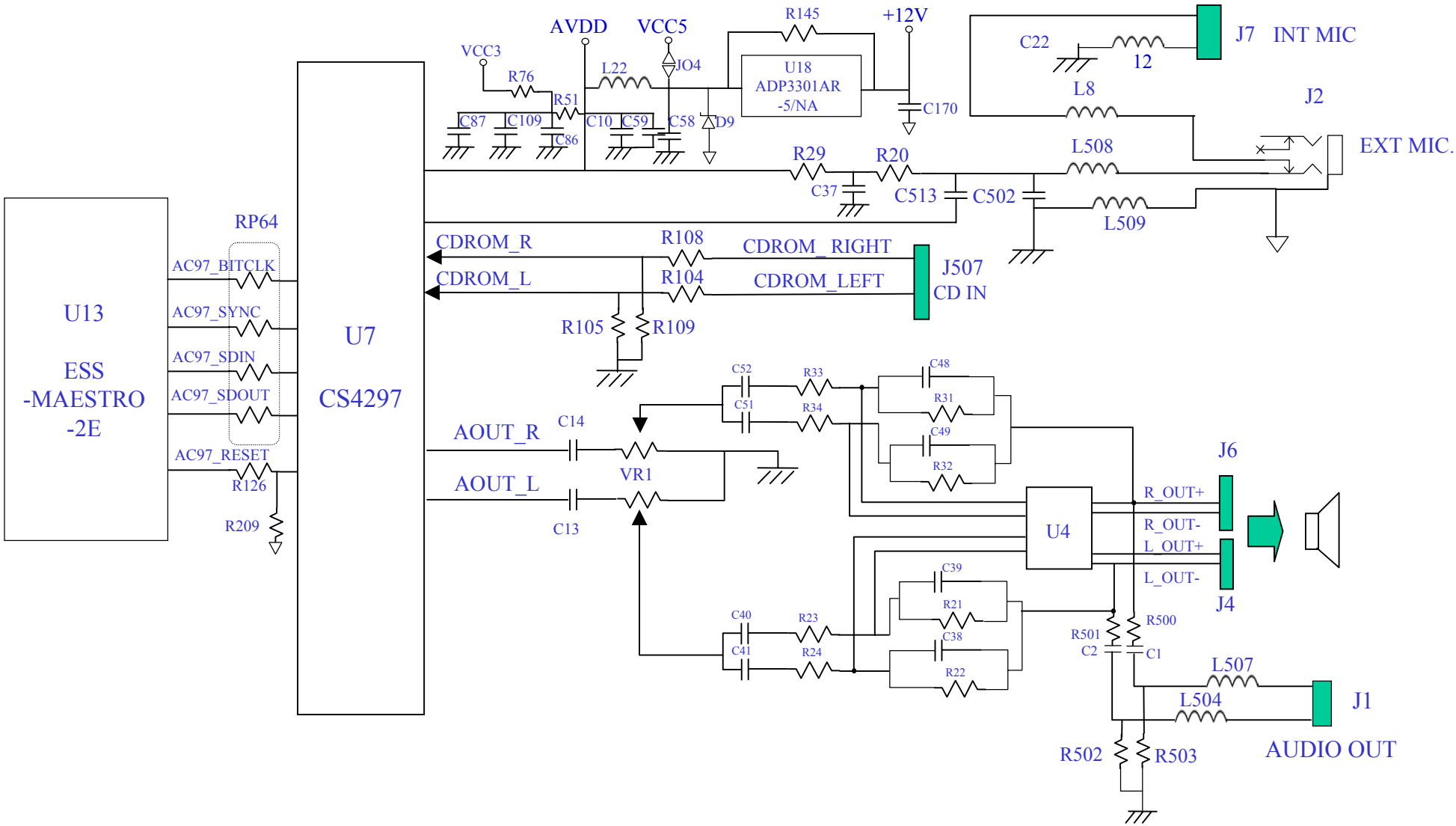
8.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



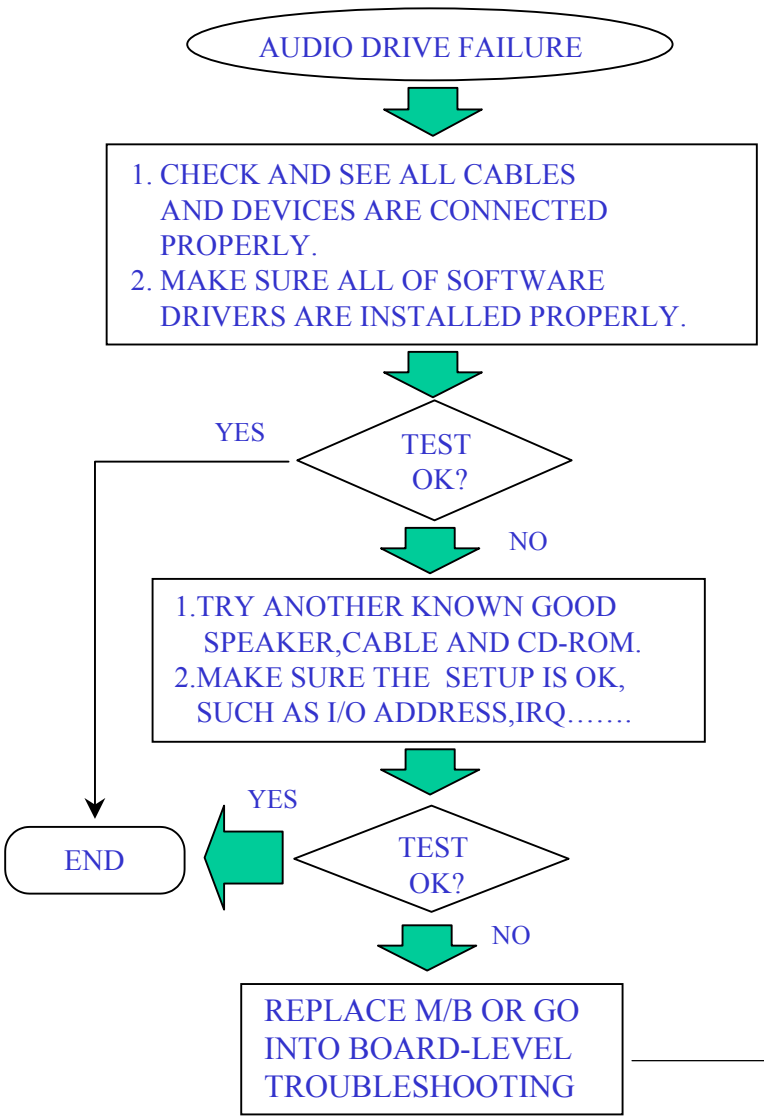
8.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



8.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



BOARD-LEVEL TROUBLESHOOTING FOR AUDIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

1.IF NO SOUND CAUSE OF LINE OUT, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
U13,U7	AOUT_R
LRP64	AOUT_L
R126,R209	
C87,C109	
R51,C86	
VR1	
C10,C59	
...	

2.IF NO SOUND CAUSE OF MIC, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
U13,U7	
U18,RP64	
R126,R209	
C87C109	
C86,R51	
L508,L8,C22	
J2,J7	
…….	

3.IF NO SOUND CAUSE OF CD-ROM, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
U13,U7	CDROM_R
RP64	CDROM_L
R126,R209	
R104,R105	
R108,R109	
J507	

9. SPARE PARTS LIST-1

Part Number	Description	Location(s)
272075103702	CAP;.01U ,50V ,+80-20% ,0603,SMT	C115,C137,C138,C147
272005103401	CAP;.01U ,CR,50V ,10% ,0805,X7R	PC8
272072104702	CAP;.1U ,16V ,+80-20% ,0603,SMT	C100,C101,C102,C103
272075104701	CAP;.1U ,50V ,+80-20% ,0603,SMT	C604,C605,PC1
272003104701	CAP;.1U ,CR,25V ,+80-20% ,0805,Y	C205,PC511,PC513
272072224701	CAP;.22U ,16V ,+80-20% ,0603,Y5V,	C513
272002474401	CAP;.47U ,CR,16V ,10% ,0805,X7R,S	C603
272075102701	CAP;1000P,50V ,+80-20% ,0603,SMT	C17,C27,C4,C42,C47
272075102403	CAP;1000P,CR,50V ,10% ,0603,X7R,SM	PC12,PC19
272075101701	CAP;100P ,50V ,+80-20% ,0603,SMT	C15,C16,C3
272075100701	CAP;10P ,50V ,+80-20% ,0603,SMT	C104,C105,C106
272021106501	CAP;10U ,10V ,20% ,1210,X7R,SMT	PC26
272011106701	CAP;10U ,10V ,+80-20% ,1206,Y5V,S	C173,C212,C58,C602
272022106701	CAP;10U ,16V ,+80-20% ,1210,Y5V,S	PC30,PC526,PC7
272023106501	CAP;10U ,25V ,20% ,1210,Y5U,SMT	PC38,39
272043106501	CAP;10U ,CR,25V ,20% ,1812,Y5U,S	PC29,PC36
272075122402	CAP;1200P,CR,50V ,10% ,0603,X7R,SM	PC519
272431157504	CAP;150U ,4V ,20% ,7343,POSCAP,SM	C120,C75,C93
272073180401	CAP;18P ,CR,25V ,10% ,0603,NPO,S	C108,C552,C553,C85
272071105701	CAP;1U ,CR,10V ,80-20% ,0603,Y5	C107,C135,C134,C136
272012105702	CAP;1U ,CR,16V ,+80-20% ,1206,Y	PC10,PC530
272013105501	CAP;1U ,CR,25V ,+80-20% ,1206,S	PC37
272002105701	CAP;1U ,CR,16V ,-20+80% ,0805,SM	PC15,13,27
272002225701	CAP;2.2U ,CR,16V ,+80-20% ,0805,Y	C14,C13

Part Number	Description	Location
272012225702	CAP;2.2U ,CR,16V ,+80-20% ,1206,Y	C153,18,214,216
272075200302	CAP;20P ,CR,50V ,5% ,0603,SMT	C145
272075222701	CAP;2200P,50V ,+80-20% ,0603,SMT	C99
272431227504	CAP;220U ,4V ,20% ,7343,POSCAP,SM	PC504,PC508
272075220701	CAP;22P ,50V ,+80-20% ,0603,SMT	C593,C594
272063226701	CAP;22U ,25V ,+80-20% ,2220,Y5U,	PC9
272041226501	CAP;22U ,CR,10V ,20% ,1812,X7R,S	C519
272075391301	CAP;390P ,CR,50V ,5% ,0603,NPO,SMT	C127
272012475701	CAP;4.7U ,CR,16V ,+80-20% ,1206,Y	C12,C124,C197,C231
272075470701	CAP;47P ,50V ,+80-20% ,0603,SMT	C25,C26,C560
272431566501	CAP;56U ,TT,4V ,20% ,SP-CON,7343,	PC18
342665500008	CFM-SUYIN,S-STANDOFF,#4-40H4.8,N	
273000500012	CHOKE COIL;10UH,4.7A,5.7MM,SMT	PL503
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	PT500
313000020110	CHOKE COIL;8uH,12.5TS,D0.8,55130	PL507
313000020148	CHOKE;15UH,D.7*16T/2*32,55130,T	PT501
313000020153	CHOKE;75uH,20% ,D0.6,55130,H=14MM	PL505
331000005001	CONN;BATTERY,5P,5MM,SPRING,50109	J509
331720015006	CONN;D-FM,15P,2.29,R/A,3ROW	J501
331720025005	CONN;D-FM,25P,2.775,R/A	J503
331720009004	CONN;D-MA,9P,2.775,R/A	J502
291000152401	CONN;FPC/FFC,24P,1MM,R/A,ELCO	J10
291000152602	CONN;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J11
291000016015	CONN;HDR,FM,30P*2,6MM,ST,SMT,613	J505

9. SPARE PARTS LIST-2

Part Number	Description	Location
291000011001	CONN;HDR,M A,10P*1,1.25,ST,SM T	J9
291000014003	CONN;HDR,M A,20P*2,1.25M M ,ST,SM T	J8
291000014802	CONN;HDR,M A,24P*2,1.27,ST,H 3.58,S	J12
291000014601	CONN;HDR,M A,46P,1.27,ST,H 1.5,SM T	J507
291000020404	CONN;HDR,SHROUD,4P*1,2,R/A,USB,BI	J3
291000251441	CONN;IC CARD,FM ,72P*2,.6M M ,H 3M M ,	J506
331870006011	CONN;M INIDIN,6P,R/A,W /GROUNDING	J500
331910003003	CONN;POW ER JACK,3P,16V DC/3A	PJ500
331840005002	CONN;STEREO JACK,5P,R/A,D 3.6,2 SW	J1,J2
291000410201	CONN;W FR,M A,2P,1.25,ST,SM T/M B	J4,J6
291000410301	CONN;W FR,M A,3P,1.25,ST,SM T/M B	J5,J7
345665400036	CONDUCTIVE TAPE;TOUCH PAD/166,VE	
272625101401	CP;100P*4,8P,50V ,10% ,1206,NPO,S	CA1,CA2
272625470401	CP;47P*4 ,8P,50V ,10% ,1206,NPO,S	CA500,CA501,CA8
Part Number	Description	Location
291000621445	DIMM SOCKET;144P,.8M M ,GOLD,SM T	J508
288100016001	DIODE;BAS16,75V ,250M A,SOT-23	D504,D505,D506,D508
288100032013	DIODE;BAS32L,VRRM 75V ,M ELF,SOD-	PD500,PD504,PD505
288100701002	DIODE;BAV70LT1,70V ,225M W ,SOT-23	D500,D507
288100099001	DIODE;BAV99,70V ,450M A,SOT-23	D501
288100056003	DIODE;BAW 56,70V ,215M A,SOT-23	D14,D503,D15,D16
288100202001	DIODE;DAN202K,80V ,SW ITCH,SM T	PD506
288101004024	DIODE;EC10QS04,RECT,40V ,1A ,CHIP,	PD5,PD501
288104148001	DIODE;RLS4148,200M A,500M W ,M ELF	D1,D11,D13,D17

Part Number	Description	Location
288100020002	DIODE;RLZ2.0B,ZENER,2.02-2.2,5%,	PD503
288100024002	DIODE;RLZ24D,ZENER,23.63V ,5% ,SM T	PD1
288100056001	DIODE;RLZ5.6B,ZENER,5.6V ,5% ,LL34	PD4
288100073002	DIODE;SFPJ-73,DC2010,30V ,3A ,SM T	PD2,PD3,PD6
288100056005	DIODE;UDZ5.6B,ZENER,5.6V ,UM D2,SI	D502,D9
312271006350	EC;100U ,25V ,20% ,RA ,6.3*7,-40~10	PC500,PC512,PC520
272602107501	EC;100U ,16V ,M ,6.3*5.5,-55+85℃,S	C1,C10,C2
312272206152	EC;220U ,4V ,M ,RA ,D8*5,OS-CON	PC503,PC529
312273306151	EC;330U ,6.3V ,20% ,RA ,D10,W /OS-CO	PC509,PC527,PC528
481666800002	F/W ASSY;KBD CTRL,6233	U504
481666800001	F/W ASSY;SYS/VGA BIOS,6233	U27
273000150002	FERRIET CHIP;1200 HM /100M HZ,2012,	L26,L28,L30,L33,L516
273000610008	FERRITE ARRAY;1200 HM /100M HZ,TK	FA5
273000130001	FERRITE CHIP;1200 HM /100M HZ,1608,	L1,L10,L3,L501,L502
273000150013	FERRITE CHIP;1200 HM /100M HZ,2012,	L31,L32,L5,PL1,PL2
273000150009	FERRITE CHIP;300 HM /100M HZ,2012,S	L11,L16,L22,L500
273000130006	FERRITE CHIP;6000 HM /100M HZ,2A ,1	L12,L15,L17,L2,L4
273000130002	FERRITE CHIP;800 HM /100M HZ,1608,S	L14,L18,L512,L513
288003600001	FIR;HSDL3600#007,FRONT VIEW ,10P,	U505
361200002001	FLUX ;3961-E,LOW SOLIDS,NO CLEAN	
295000010008	FUSE;1.1A ,POLY SW ITCH ,SM T	F1,F2
295000010105	FUSE;1A ,NORM AL,1206,SM T	F4
295000010016	FUSE;NORM AL,6.5A/32V DC ,3216,SM T	PF500
295000010020	FUSE;NORM AL,7A/24V DC ,1206,SM T	F3

9. SPARE PARTS LIST-3

Part Number	Description	Location
345666200012	GASKET;AUDIO-JACK,NV	
345665400013	GASKET;USB,VENUS	
344600000225	IC CARD CON PART;72P*2,6033	
291000616153	IC SOCKET;615P,ZIF,ZIFuPGA1,FOXC	U501
284500003007	IC;3D RAGE LT PRO,AGP,BGA,328P,J	U12
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U25
282674008001	IC;74AHCT08,2I/P AND GATE,TSSOP,	U503
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U22
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U26
284501021002	IC;ADM1021,TEMPERATURE MTR,SSC	U8
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U1
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,S	U29
284504297001	IC;CS4297,AUDIO CODEC,TQFP,48P	U7
284501978001	IC;ES1978S,AUDIO CHIP,TQFP,100P	U13
283420502004	IC;FLASH,256K*8-15,PLCC,32P,VENU	
284182371005	IC;FW82371EB,PIIX4E,PCI/ISA,BGA3	U9
284582443018	IC;FW82443ZXM,HOST BRIDGE,BGA,	U19
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
286317812001	IC;HA178L12UA,VOLT REGULATOR,S	PU2
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,	PU5,PU6
286302951015	IC;LP2951ACM,VOLTAGE REGULATO	U33
286302986001	IC;LP2986AIM-3.3,REGULATOR,SO8	PU3,PU500
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U34
284501284001	IC;PAC1284-01Q,TERM IN.NETWK,QS	U2,U3

Part Number	Description	Location
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100	U17
284501225001	IC;PCI1225PDV,PCI/CARDBUS,LQFP,2	U28
282153257001	IC;PI5C3257,BUS SWITCH QUAD,QSOI	U5
286303032001	IC;SB3032P,PWM CTLR,SO,16P	PU4
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU501
286300431011	IC;SC431CSK-5,.5%,ADJREG,SOT23	PQ4,PQ9
283766680001	IC;SDRAM,4M*16,TSOP,54P,6233	U14,U20
283866680001	IC;SGRAM,512K*32-100,TQFP,100P,6	U11,U16
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU1
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U4
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSO	U35
286500137001	IC;W137,CLOCK GENERATOR,SSOP,28	U10
284104011001	IC;W40S11-02,SDRAM BUFFER,SSOP,2	U30
273000051001	INDUCTOR,22UH,110mA,3225,SMT	L511
340666210016	INSULATOR ASSY;PCMCIA,MK-2,NV	
346666200007	INSULATOR;AUDIO-JACK,NV	
346665200036	INSULATOR;D/D CHOKE,PITCHING3	PL507
346665400009	INSULATOR;I/O PANEL,VENUS	
346665400025	INSULATOR;SW BD CON.,VENUS	
242600000380	LABEL,10*8MM,BIOS,HI-TEMP260	
242600000380	LABEL,10*8MM,BIOS,HI-TEMP260	
242662300009	LABEL,25*10MM,3020F	
242600000378	LABEL,27*7MM,HI-TEMP260℃	
242600000364	LABEL,BLANK,6*6MM,HI-TEMP	

9. SPARE PARTS LIST-4

Part Number	Description	Location
242600000172	LABEL;PCMCIA CARD WORKS/95,JP	
242600000195	LABEL;PENTIUM-BP,SYSTEM SOFT BIOS	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D2,D3,D4,D5,D6,D7
421666200031	MICROPHONE ASSY;LCD,NV	
316666800001	PCB;PWA-6233/MBD	R03
340666210015	PLATE ASSY-2;SUPPORT,CPU,MK-2,NV	
411666800004	PWA;PWA-6233,MB,13.3	
411666800006	PWA;PWA-6233,MB,13.3,SMT	
411666800005	PWA;PWA-6233,MB,13.3,TU	
271086057101	RES;.005,2W,1%,7520,SMT	PR15
271045207101	RES;.02,1W,1%,2512,SMT	PR509,6,2
271002000301	RES;0,1/10W,5%,0805,SMT	R76,R95
271071000002	RES;0,1/16W,0603,SMT	R104,106,108,211
271012000301	RES;0,1/8W,5%,1206,SMT	F5
271071152101	RES;1.5K,1/16W,1%,0603,SMT	R37
271071152302	RES;1.5K,1/16W,5%,0603,SMT	R110
271071187111	RES;1.87K,1/16W,1%,0603,SMT	R38
271071100302	RES;10,1/16W,5%,0603,SMT	R166,R167,R179,R180
271071101301	RES;100,1/16W,5%,0603,SMT	R123,R136,R559
271071104101	RES;100K,1/16W,1%,0603,SMT	PR19,PR25,PR30,PR500
271071104302	RES;100K,1/16W,5%,0603,SMT	PR23,PR24,PR3,PR5
271071103101	RES;10K,1/16W,1%,0603,SMT	PR14,PR514,PR503,PR8
271071103302	RES;10K,1/16W,5%,0603,SMT	PR31,R120,R185
271071118211	RES;11.8K,1/16W,1%,0603,SMT	PR39

Part Number	Description	Location
271071121211	RES;12.1K,1/16W,1%,0603,SMT	PR32
271071121301	RES;120,1/16W,5%,0603,SMT	R532,R98
271071121311	RES;121K,1/16W,1%,0603,SMT	PR13
271071124311	RES;124K,1/16W,1%,0603,SMT	PR501
271071151302	RES;150,1/16W,5%,0603,SMT	R536,R84
271071153301	RES;15K,1/16W,5%,0603,SMT	R103,R88,R90
271071180301	RES;18,1/16W,5%,0603,SMT	R118,R551,R552
271071102102	RES;1K,1/16W,1%,0603,SMT	PR505,PR507
271071102302	RES;1K,1/16W,5%,0603,SMT	R10,R100,R111,R12
271071105101	RES;1M,1/16W,1%,0603,SMT	PR33,R186
271071105301	RES;1M,1/16W,5%,0603,SMT	PR11,PR22,R142,R143
271071221111	RES;2.21K,1/16W,1%,0603,SMT	PR512
271071222302	RES;2.2K,1/16W,5%,0603,SMT	R505,R506
271071232111	RES;2.32K,1/16W,1%,0603,SMT	R214
271071249111	RES;2.49K,1/16W,1%,0603,SMT	R93
271071204101	RES;200K,1/16W,1%,0603,SMT	PR18,R563
271071205311	RES;205K,1/16W,1%,0603,SMT	PR36
271071203101	RES;20K,1/16W,1%,0603,SMT	R573
271071203302	RES;20K,1/16W,5%,0603,SMT	R94,206
271071221302	RES;22,1/16W,5%,0603,SMT	R178,R187,R66
271071221301	RES;220,1/16W,5%,0603,SMT	R107
271071224301	RES;220K,1/16W,5%,0603,SMT	R159
271071237311	RES;237K,1/16W,1%,0603,SMT	PR28
271071249211	RES;24.9K,1/16W,1%,0603,MST	PR506

9. SPARE PARTS LIST-5

Part Number	Description	Location(s)
271071267211	RES,26.7K,1/16W,1%,0603,SMT	PR511
271071261311	RES,261K,1/16W,1%,0603,SMT	PR21,PR29
271071270301	RES,27,1/16W,5%,0603,SMT	R87,R89
271071271301	RES,270,1/16W,5%,0603,SMT	R17,R18,R19
271071273301	RES,27K,1/16W,5%,0603,SMT	R21,R32
271071348111	RES,3.48K,1/16W,1%,0603,SMT	R213
271071365111	RES,3.65K,1/16W,1%,0603,SMT	PR513
271071301311	RES,301K,1/16W,1%,0603,SMT	R571
271071330302	RES,33,1/16W,5%,0603,SMT	PR12,27,508
271071334301	RES,330K,1/16W,5%,0603,SMT	PR7,PR518
271071333301	RES,33K,1/16W,5%,0603,SMT	R549
271071383211	RES,38.3K,1/16W,1%,0603,SMT	PR521
271071392211	RES,39.2K,1%,1/16W,0603,SMT	PR17
271071305301	RES,3M,1/16W,5%,0603,SMT	PR523,510
271013478301	RES,4.7,1/4W,5%,1206,SMT	R574,R575
271002472301	RES,4.7K,1/10W,5%,0805,SMT	PR1,PR4,PR515
271071472302	RES,4.7K,1/16W,5%,0603,SMT	R11,115,135,20,29
271071499111	RES,4.99K,1/16W,1%,0603,SMT	R196
271071402211	RES,40.2K,1/16W,1%,0603,SMT	PR504
271071402311	RES,402K,1/16W,1%,0603,SMT	PR26
271071412311	RES,412K,1/16W,1%,0603,SMT	PR35
271071422211	RES,42.2K,1/16W,1%,0603,SMT	PR502
271071442011	RES,442,1/16W,1%,0603,SMT	R520,R521
271071470301	RES,47,1/16W,5%,0603,SMT	R132,182

Part Number	Description	Location
271071471302	RES,470,1/16W,5%,0603,SMT	R198,558
271071474301	RES,470K,1/16W,5%,0603,SMT	R148,R190
271071473301	RES,47K,1/16W,5%,0603,SMT	PR16,R25,R554
271071511111	RES,5.11K,1/16W,1%,0603,SMT	PR34
271071562301	RES,5.6K,1/16W,5%,0603,SMT	R102,R122
271071510101	RES,51,1/16W,1%,0603,SMT	R538
271071511211	RES,51.1K,1/16W,1%,0603,SMT	PR9
271071549211	RES,54.9K,1/16W,1%,0603,SMT	PR10
271071564301	RES,560K,1/16W,5%,0603,SMT	R8
271071562311	RES,562K,1/16W,1%,0603,SMT	PR37
271071622301	RES,6.2K,1/16W,5%,0603,SMT	PR40
271071681301	RES,680,1/16W,5%,0603,SMT	R127,R15,R16,R537
271071909311	RES,909K,1/16W,1%,0603,SMT	PR20
271071976211	RES,97.6K,1/16W,1%,0603,SMT	PR38
271571000301	RP,0*8,16P,1/16W,5%,1606,SM	RP59,60
271571100301	RP,10*8,16P,1/16W,5%,1606,SM	RP44,RP46,RP49,RP50
271611103301	RP,10K*4,8P,1/16W,5%,0612,SMT	RP13,RP48,RP7
271621103303	RP,10K*8,10P,1/16W,5%,1206,SMT	RP12,RP19,RP25,RP33
271621103303	RP,10K*8,10P,1/16W,5%,1206,SMT	RP12,RP19,RP25,RP33
271621120301	RP,120*8,10P,1/16W,5%,1206,SMT	RP1,RP11,RP17,RP2
271611102301	RP,1K*4,8P,1/16W,5%,0612,SMT	RP9
271611220301	RP,22*4,8P,1/16W,5%,0612,SMT	RP47
271611330301	RP,33*4,8P,1/16W,5%,0612,SMT	RP18,RP22,RP34,RP521
271571330301	RP,33*8,16P,1/16W,5%,1606,SM	RP20,RP21,RP23,RP24

6233 N/B MAINTENANCE

9. SPARE PARTS LIST-6

PartNumber	Description	Location
271621472303	RP;4.7K*8,10P,1/16W,5%,1206,SMT	RP43,RP5,RP509,RP52
271621472303	RP;4.7K*8,10P,1/16W,5%,1206,SMT	RP43,RP5,RP509,RP52
271621433301	RP;43K*8,10P,1/16W,5%,1206,SMT	RP51,522,62,63
271621473301	RP;47K*8,10P,1/16W,5%,1206,SMT	RP41,RP53
271611750301	RP;75*4,8P,1/16W,5%,0612,SMT	RP14,RP16
271621822301	RP;8.2K*8,10P,1/16W,5%,1206,SMT	RP516,RP66,RP67
371102610401	SCREW,M2.6L4,FLT(+),NIW	
371102011001	SCREW,M2L10,FLT(+),NIW	
371102010010	SCREW,M2L4,FLT(+),NIW	
340666210001	SHIELD ASSY,BOTTOM,CASE KIT,MK-2	
341666200011	SHIELD;AUDIO,NV	
341666200013	SHIELD;PCMCIA,M/B,NV	
361400003028	SHIN-ETSU;KE45W S RTV SILICON,350	
365250000010	SOLDER BAR;63/37 ALLOY 1KG/BAR	
365350000002	SOLDER WIRE;63/37FLUX%1.2DIA.64	
370102610401	SPC-SCREW,M2.6L4,NIB,727,NLK	
370102010303	SPC-SCREW,M2L3,NIW,K-HD(+),NYLOK	
341666200012	SPRING,DC JACK,NV	
343666800003	STANDOFF;M2H12/M2.6,6233	
297120101008	SW;DIP,SPST,12P,50VDC,.1A,SMT,DH	SW2
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW500
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW3
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-8	SW1
225665500001	TAPE;INSULATION,AC04,25M*6MM,503	

PartNumber	Description	Location
346665400019	THERMAL PAD;20*20*.5,VENUS	
361200002002	THINNER;#111B,KESTER	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ10,PQ11,PQ12,PQ5
288200144002	TRANS;DTA144WK,PNP,SMT	PQ508,Q509
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-2	PQ505,PQ6,Q13,Q14
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ510,8,Q18
288206690001	TRANS;FDS6690A,N-MOSFET,.017OHM	PQ3
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ500
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO23	Q17,Q6,Q7
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q20,503,507
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q500
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM	PQ2,PQ507
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM	PQ509
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ1
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,	PQ501,PQ504,Q1
288204603001	TRANS;SPB46N03L,30V46A,N-CH,TO2	PQ503
271911103902	VR;10K,20%,.05W,XV0102GPH1N-93	VR1
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X1
274011600407	XTAL;16MHZ,30PPM,16PF,7*5,4P,SMT	X501
274012949401	XTAL;29.498928MHZ,30PPM,20PF,4P,	X500
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X2
274014915402	XTAL;49.152MHZ,30PPM,16PF,7*5,4P	X3
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