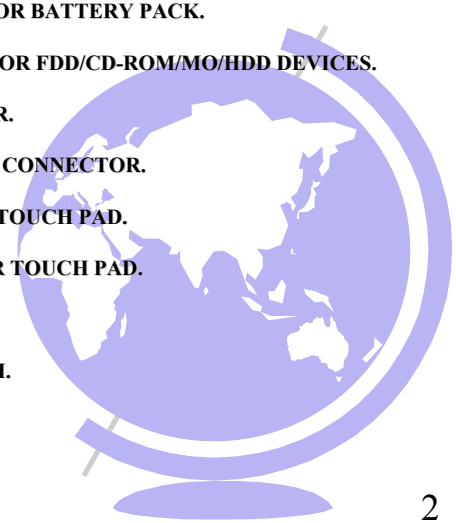
6031 N/B MAINTENANCE

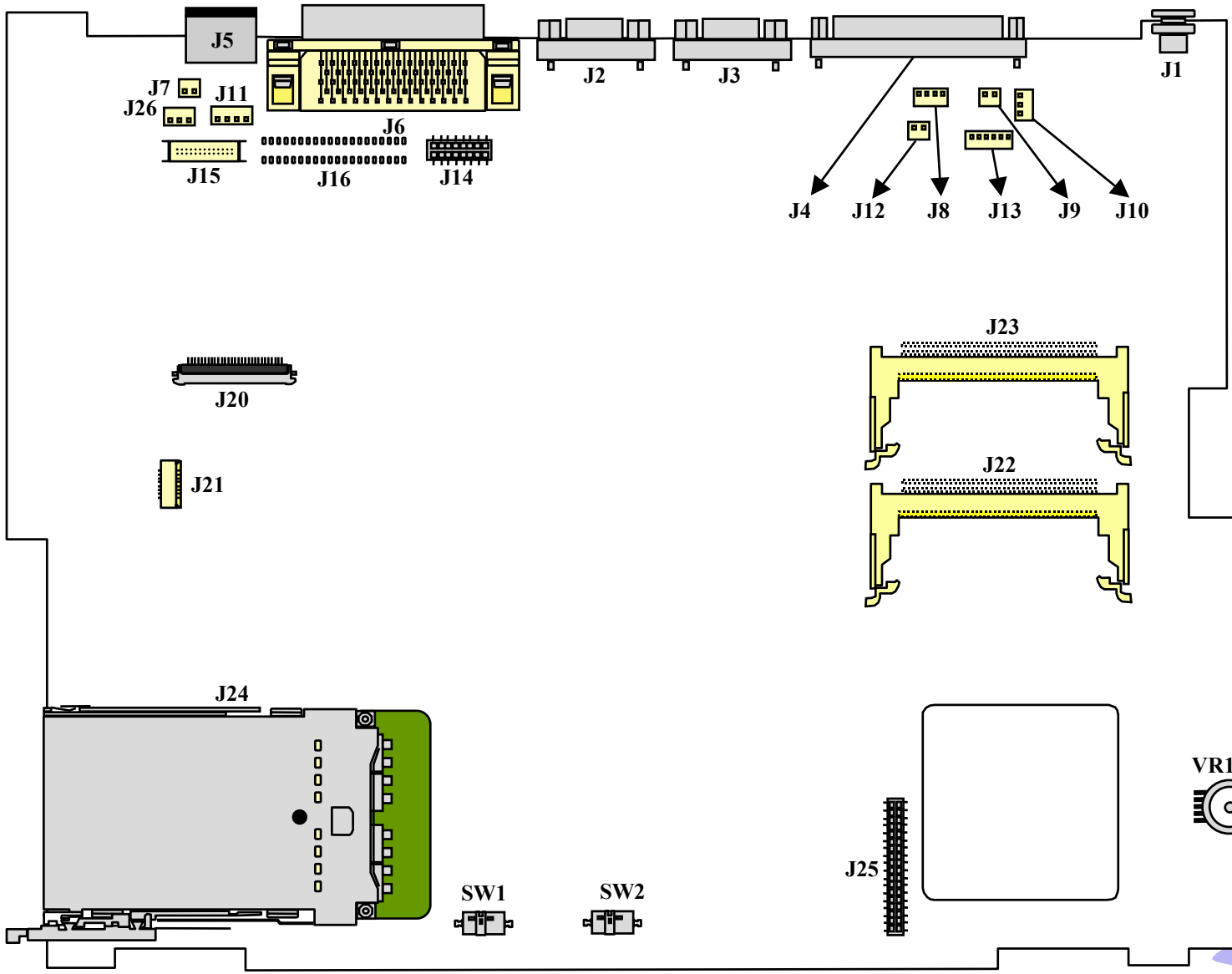
CONTENTS

1. DEFINITION OF CONNECTORS & SWITCHES

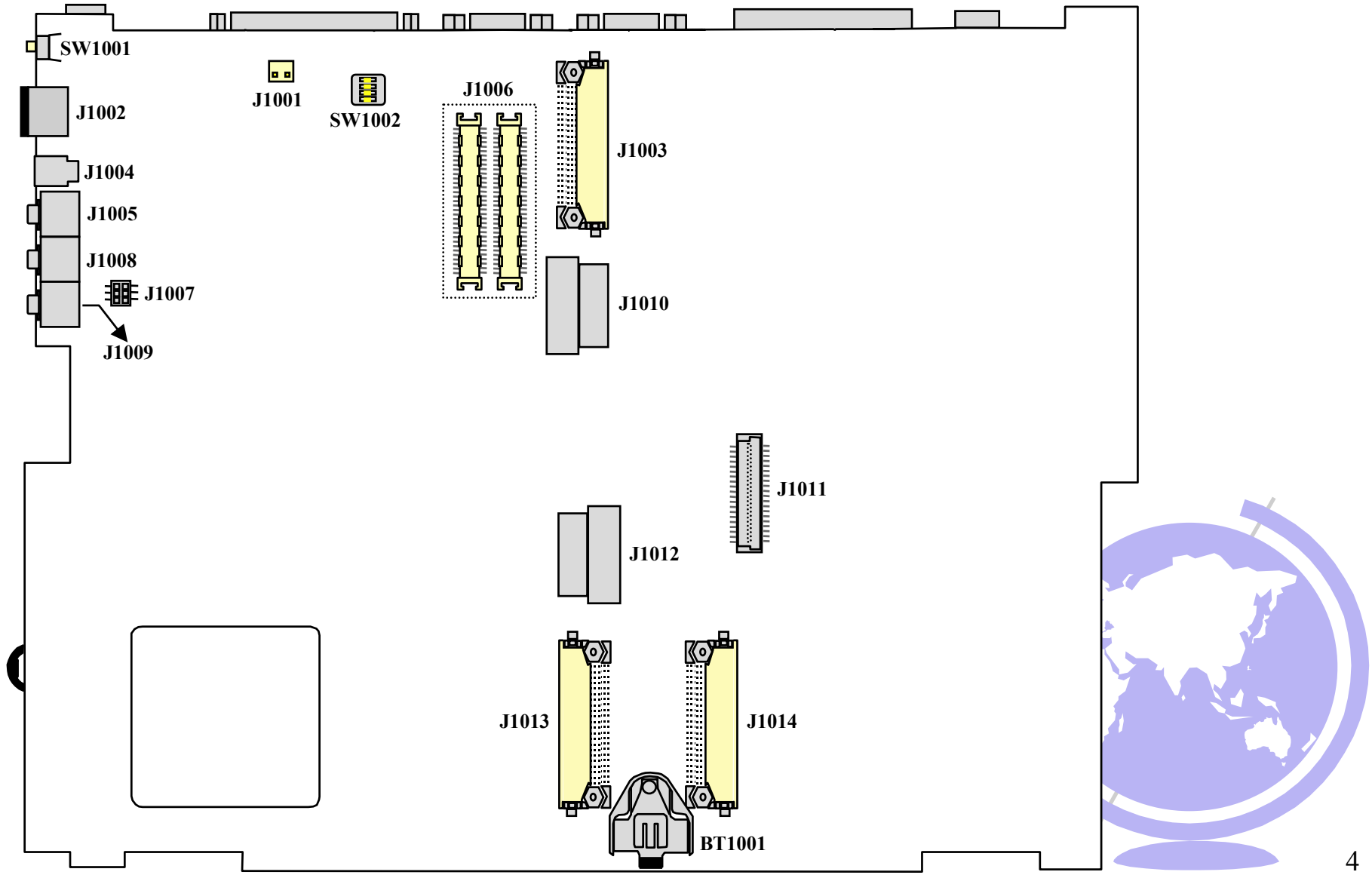
- J1 : POWER JACK.
- J2 : VGA CONNECTOR.
- J3 : SERIAL PORT (SIO).
- J4 : PARALLEL PORT(PIO).
- J5 : USB PORT CONNECTOR.
- J6 : DOCKING STATION CONNECTOR.
- J7 : INTERNAL LEFT CHANNEL SPEAKER CONNECTOR.
- J8 : INTERNAL CCD CAPTURE DEVICE CONNECTOR.
- J9 : INTERNAL RIGHT CHANNEL SPEAKER CONNECTOR.
- J10 : INTERNAL MICROPHONE CONNECTOR.
- J11 : UPPER LED BOARD CONNECTOR.
- J12 : COVER SWITCH CONNECTOR.
- J13 : BACKLIGHT CONNECTOR.
- J14 : LOWER LED BOARD CONNECTOR.
- J15 : LVDS LCD PANEL CONNECTOR.
- J16 : LEGACY LCD PANEL CONNECTOR (NO ASSEMBLY).
- J20 : INTERNAL KEYBOARD CONNECTOR.
- J21 : TOUCH PAD MODULE CONNECTOR.
- J22, J23 : 144 PIN 3.3V UNBUFFER DIMM SOCKETS.
- J24 : PCCARD CONNECTOR.
- J25 : DC/DC BOARD CONNECTOR.
- J1001 : COOL FAN CONNECTOR.
- J1002 : PS/2 KEYBOARD/MOUSE CONNECTOR.
- J1003 : LEFT BAY CONNECTOR FOR FDD/MO/HDD DEVICES.
- J1004 : POWER CONNECTOR FOR EXTERNAL CCD CAPTURE DEVICE.
- J1005 : EXTERNAL MICROPHONE CONNECTOR.
- J1006 : IMM/MMC-1 CPU MODULE CONNECTOR.
- J1007 : TV IN/OUT TRANSLATION BOARD CONNECTOR.
- J1008 : LINE-IN CONNECTOR.
- J1009 : LINE-OUT CONNECTOR.
- J1010 : LEFT BAY CONNECTOR FOR BATTERY PACK.
- J1011 : FAX/MODEM/VOICE CARD CONNECTOR.
- J1012 : RIGHT BAY CONNECTOR FOR BATTERY PACK.
- J1013 : RIGHT BAY CONNECTOR FOR FDD/CD-ROM/MO/HDD DEVICES.
- J1014 : PRIMARY HDD CONNECTOR.
- BT1001: CMOS BACK-UP BATTERY CONNECTOR.
- SW1: LEFT BUTTON SWITCH FOR TOUCH PAD.
- SW2: RIGHT BUTTON SWITCH FOR TOUCH PAD.
- SW1001: POWER SWITCH.
- SW1002: CONFIGURATION SWITCH.
- VR1: AUDIO VOLUME CONTROL.



2 . LOCATION OF CONNECTORS & SWITCHES (TOP SIDE)



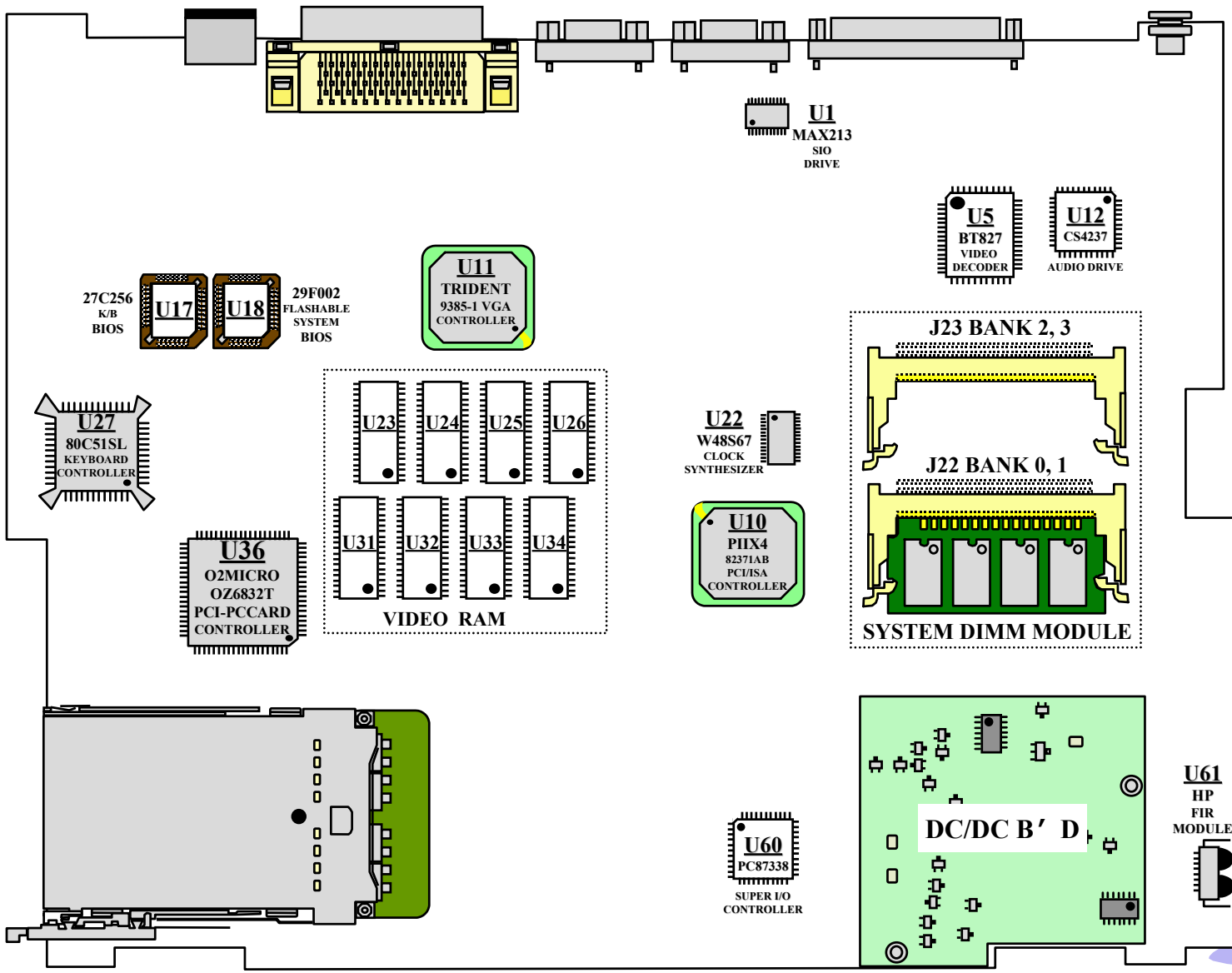
2 . LOCATION OF CONNECTORS & SWITCHES(BOTTOM SIDE)



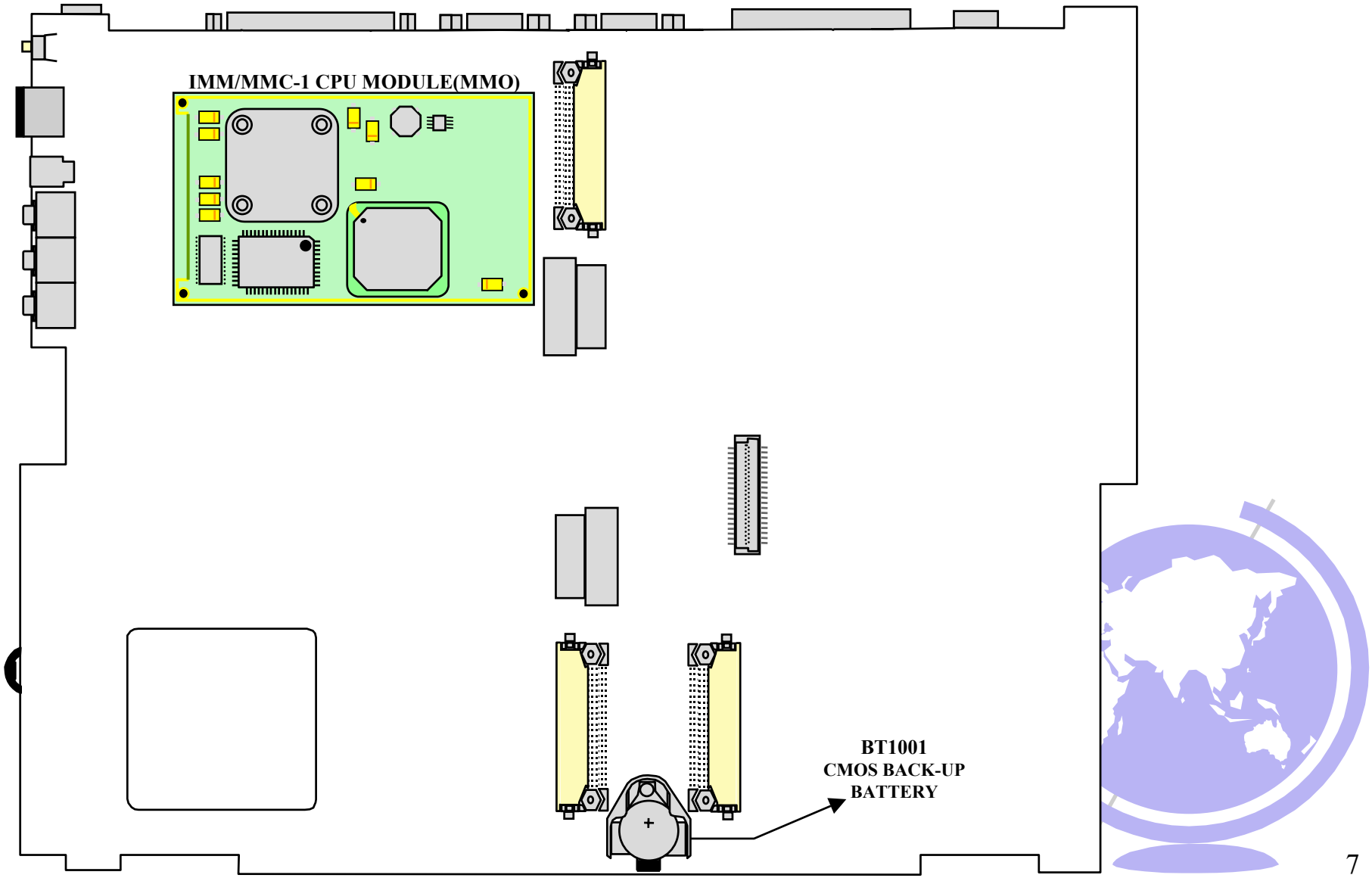
3. MAJOR COMPONENTS

- U1: MAX213 SIO DRIVE.
- U5: BT827 VIDEO DECODER.
- U10: INTEL PIIX4 FW82371AB PCI/ISA BRIDGE.
- U11: TRIDENT 9385-1 VGA CONTROLLER.
- U12: CS4237 AUDIO CONTROLLER.
- U17: 27C256 KEYBOARD BIOS.
- U18: 29F002 FLASHABLE SYSTEM BIOS.
- U22: W48S67 CLOCK SYNTHESIZER.
- U23~U26, U31~U34: 4MB VIDEO RAM.
- U27: 80C51SL KEYBOARD CONTROLLER.
- U36: O2MICRO OZ6832T PCI-PCCARD CONTROLLER.
- U60: PC87338 SUPER I/O CONTROLLER.
- U61: HP FIR MODULE.
- J22, J23: 144PIN 3.3V UNBUFFER SYSTEM DIMM MODULE.
- J25: DC/DC BOARD.
- J1006: IMM/MMC-1 CPU MODULE(MMO).
- BT1001: CMOS BACK-UP BATTERY.

4. LOCATION OF MAJOR COMPONENTS(TOP SIDE)



4. LOCATION OF MAJOR COMPONENTS(BOTTOM SIDE)



5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL MOBILE MODULE CONNECTOR 1 (IMM/MMC-1)

SIGNAL	TYPE	DESCRIPTION
RAS[5:0]# or CS[5:0]#	I/O	V_3 **Row Address Strobe (EDO):** These pins select the DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
CAS[7:0]# or DQM[7:0]	O	V_3 **Column Address Strobe (EDO):** These pins select the DRAM column. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MA[13:0]	O	V_3 **Memory Address (EDO/SDRAM):** This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB [13:0]. The Pentium® II processor mobile module supports only the MAB set of address lines.
MWE[A,B]#	O	V_3 **Memory Write Enable (EDO/SDRAM):** MWE[A,B]# should be used as the write enable for the memory data bus. Each copy is intended to support four rows, for loading purposes.
SRAS[A,B]#	O	V_3 **SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge. Each copy is intended to support four rows, for loading purposes.
SCAS[A,B]#	O	V_3 **SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Each copy is intended to support four rows, for loading purposes.
CKE[A,B]	O	V_3 **SDRAM Clock Enable (SDRAM):** When these signals are de-asserted, SDRAM enters power-down mode. Each copy is intended to support four rows, for loading purposes. CLKEB is NC and not used by the system electronics.
MD[63:0]	I/O	V_3 **Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the Intel Mobile Module. It is recommended that the system electronics provide series termination of 33Ω.
AD[31:0]	I/O	V_3 **Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
C/BE[3:0]#	I/O	V_3 **Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O	V_3 **Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfers are desired by the cycle initiator.
DEVSEL#	I/O	V_3 **Device Select:** This signal is driven by the 443BX Host Bridge when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O	V_3 **Initiator Ready:** Asserted when the initiator is ready for data transfer.
TRDY#	I/O	V_3 **Target Ready:** Asserted when the target is ready for a data transfer.
STOP#	I/O	V_3 **Stop:** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O	V_3 **Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed. The 443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[3:0]#	I	V_3 **PCI Request:** PCI master requests for PCI.
GNT[3:0]#	O	V_3 **PCI Grant:** Permission is given to the master to use PCI.
PHOLD#	I	V_3 **PCI Hold:** This signal comes from the expansion bridge; it is the bridge request for PCI. The 443BX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O	V_3 **PCI Hold Acknowledge:** This signal is driven by the 443BX Host Bridge to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.

SIGNAL	TYPE	DESCRIPTION
PAR	I/O	V_3 **Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	I/O	V_3 **System Error:** The 443BX asserts this signal to indicate an error condition.
CLKRUN#	I/O	V_3 **Clock Run:** An open-drain output and also an input. The 443BX Host Bridge requests the central resource (PIIX4) to start or maintain the PCI clock by asserting CLKRUN#. The 443BX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset.
PCI_RST#	I	V_3 **Reset:** When asserted, this signal asynchronously resets the 443BX Host Bridge. The PCI signals also tri-state, compliant with PCI Rev 2.1 specifications.
FERR#	O	V_CPUIO **Numeric Coprocessor Error:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4.
CPURST	N/C	V_CPUIO **Processor Reset:** The signal is not used in the Pentium® II Processor mobile module.
IGNNE#	ID	V_CPUIO **Ignore Error:** This open drain signal is connected to the ignore error pin on the processor and is driven by the PIIX4.
INIT#	ID	V_CPUIO **Initialization:** INIT# is asserted by the PIIX4 to the processor for system initialization. This signal is an open drain.
INTR	ID	V_CPUIO **Processor Interrupt:** INTR is driven by the PIIX4 to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open drain.
NMI	ID	V_CPUIO **Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4 ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open drain.
A20M#	ID	V_CPUIO **Address Bit 20 Mask:** When enabled, this open drain signal causes the processor to emulate the address wraparound at one Mbyte which occurs on the Intel 8086™ processor.
SMI#	ID	V_CPUIO **System Management Interrupt:** SMI# is an active low synchronous output from the PIIX4 that is asserted in response to one of many enabled hardware or software events. The SMI# open drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	ID	V_CPUIO **Stop Clock:** STPCLK# is an active low synchronous open drain output from the PIIX4 that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is de-asserted.
OEM_PU	I	V_3 **OEM Pull-Up:** this pull-up resistor is not required on the Intel Pentium II® processor mobile module. This signal is used by previous mobile module generations.
L2_ZZ	N/C	V_CPUIO **Low-Power Mode For Cache SRAM:** This signal is not used on the Intel Pentium® II Processor Mobile Module. It is a signal used by previous mobile module generations.
SUS_STAT#	I	V_3-ALWAYS **Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4. It provides information on host clock status and is asserted during all suspend states.
VR_ON	I	V_3S **VR_ON:** Voltage regulator ON. This 3.3V (5V tolerant) signal controls the operation of the Intel Mobile Module voltage regulator. VR_ON should be generated as a function of the PIIX4 SUSB# signal which is used for controlling the uspend State B voltage planes. This signal should be driven by a digital signal with a rise/fall time of less than or equal to 1us. .
VR_PWRGD	O	V_3S **VR_PWRGD:** This signal is driven high by the Intel Mobile Module to indicate the voltage regulator is stable and is pulled low using a 100K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
SM_CLK	I/O	V_3 **Serial Clock:** This clock signal is used on the SMBUS interface to the digital thermal sensor.
SM_DATA	I/O	V_3 **Serial Data:** Open-drain data signal on the SMBUS interface to the digital thermal sensor.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL MOBILE MODULE CONNECTOR 1 (IMM/MMC-1)

SIGNAL	TYPE	DESCRIPTION
ATF_INT#	O	V_3 **ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor.
OEM_PD	I	V_3 **OEM Pull-Down:** It is renamed from PCI_REF and this pull-down resistor is not required on the Intel Pentium® II processor mobile module. It is a signal used by previous mobile module generations.
PCLK	I	V_3S **PCI Clock In:** PCLK is an input to the module from the CKDM66-M clock source and is one of the system PCI clocks. This clock is used by all of the 443BX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4 PCI_STP# signal is asserted and/or during all suspend states.
HCLK[1:0]	I	V_CPUIO **Host Clock In:** These clocks are inputs to the module from the CKDM66-M clock source and are used by the processor and 443BX Host Bridge system controller. This clock is stopped when the PIIX4 CPU_STP# signal is asserted and/or during all suspend states.
SUSCLK	N/C	V_3 **Suspend Clock**: This signal is not used on the Intel Pentium® processor mobile module.
FQS[1:0]	O	V_3S **Frequency Status:** This signal provides status of the host clock frequency to the system electronics. These signals are static and are pulled either low or high to the V_3S voltage. **FQS1 FQS0 Frequency** 0 0 60 MHz 0 1 66 MHz 1 0 Reserved 1 1 Reserved
CPU3.3_2.5#	O	V_CPUIO **Clock Voltage Select:** Provides status to the system electronics about the voltage level at which the CKDM66-M clock generator should be operating. This signal is pulled low by the Intel Pentium® II processor mobile module.
V_DC	I	**DC Input:** 5 - 21V
V_3S	I	**SUSB# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff.
V_5	I	**SUSC# controlled 5V:** Power-managed 5V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_3	I	**SUSC# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_CPUIO	O	**Processor I/O Ring:** Driven by the Intel Mobile Module to power processor interface signals such as the PIIX4 open-drain pullups for the processor/PIIX4 sideband signals and the CKDM66-M clock source.
TDO	O	V_CPUIO **JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	V_CPUIO **JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_CPUIO **JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	V_CPUIO **JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_CPUIO **JTAG Test Reset:** Asynchronously resets the TAP controller in the processor.
ITP(1:0) ITP1 ITP0	O I	V_CPUIO **Debug Port Signals:** Currently defined for the generation of Pentium processors. These signals are not used in the Pentium® II processor mobile module, and should not be connected.
Module ID[3:0]	O	4 **Module Revision ID**: These pins track the revision level of the processor module. A 100K pull up resistor to V_3S is required on these signals and to be placed on the system electronics for these signals.

SIGNAL	TYPE	DESCRIPTION
PPP_PP#	O	**Pentium® II processor or Pentium processor present**: A high on this signal indicates to the PIIX4 ISA bridge CONFIG1 pin that the processor module used is based on the Pentium® Pro architecture; a low indicates that it is of the Pentium processor family. This signal is allowed to float onPentium II processor mobile modules and requires a 100K pull up resistor to V_3S on the system electronics. For the Pentium processor mobile modules, this signal is grounded on the module.
Ground	I	Ground Reserved RSVD 8 Unallocated Reserved pins and should not be connected.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits).During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4□ ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master.

SIGNAL	TYPE	DESCRIPTION
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle. **PAR O CALCULATED PARITY SIGNAL.** PAR is □ven?parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. □ven?parity means that the number of ?□ within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4□ ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/ GPI0	I	**I/O CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/ GPO[7:1]	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles.

SIGNAL	TYPE	DESCRIPTION
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z
SMEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High
PCS0# PCS1#	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/ GPO25	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output.
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

SIGNAL	TYPE	DESCRIPTION
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
DACK[0,1,2,3]# DACK[5,6,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4□ buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input. **INTR** OD **INTERRUPT.** See CPU Interface Signals.
IRQ0/ GPO14	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO **IRQ1** I **INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11,14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration.An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.

SIGNAL	TYPE	DESCRIPTION
IRQ8#/ GPI6	I/O	**IRQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**CPU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.

SIGNAL	TYPE	DESCRIPTION
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H– –1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0– –3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers.

SIGNAL	TYPE	DESCRIPTION
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H– –177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H– –377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0□	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0.
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1.
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.

SIGNAL	TYPE	DESCRIPTION
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ[A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUSC#/ GPO16	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/ GPO20	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output.

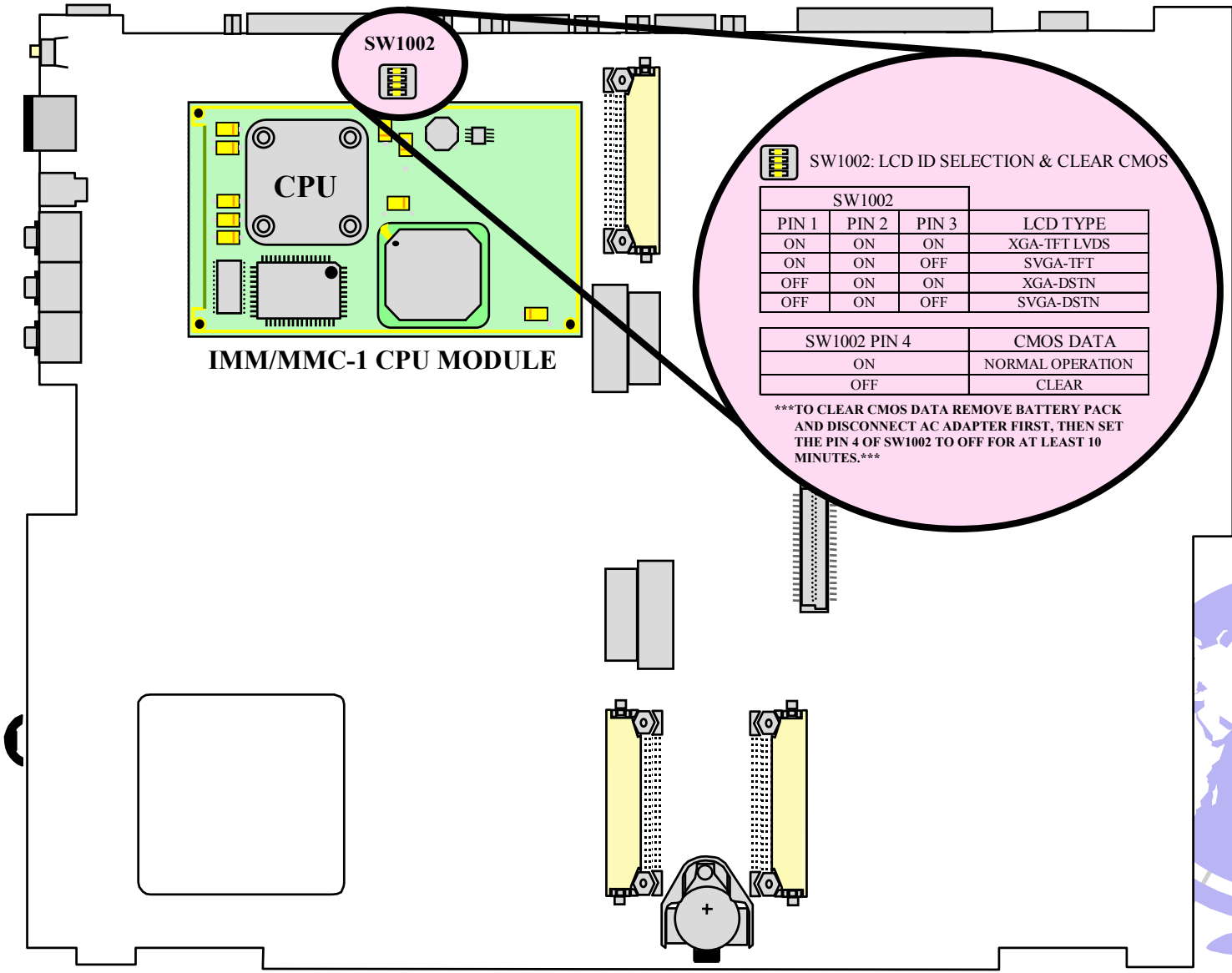
5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

INTEL 82371AB PCI-TO-ISA / IDE XCELERATOR (PIIX4).

SIGNAL	TYPE	DESCRIPTION
SUS_STAT2#/ GPO21	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/ GPI8	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/ GPO19	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a cache□ data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	**GENERAL PURPOSE OUTPUTS.** These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal□ state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).
CONFIG1	I	**CONFIGURATION SELECT 1.** This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	**CONFIGURATION SELECT 2.** This input signal is used to select the positive or subtractive decode of FFFF0000h□FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with subtractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	**POWER OK.** When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	**SPEAKER.** The SPKR signal is the output of counter timer 2 and is internally "ANDed" with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. **During Reset:** Low **After Reset:** Low **During POS:** Last State
TEST#	I	**TEST MODE SELECT.** The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

SIGNAL	TYPE	DESCRIPTION
VCC	V	**CORE VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	**RTC WELL VOLTAGE SUPPLY.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	**SUSPEND WELL VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	**USB VOLTAGE SUPPLY.** This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	**VOLTAGE REFERENCE.** This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	**CORE GROUND.** These pins are the primary ground for PIIX4.
VSS (USB)	V	**USB GROUND.** This pin is the ground for the USB input/output buffers.

6. SWITCH SETTING



7. SYSTEM VIEW AND DISASSEMBLY

- 7.1 SYSTEM VIEW

MODULAR COMPONENTS

- 7.2 LEFT AND RIGHT BAY DEVICES
- 7.3 PRIMARY HARD DISK DRIVE
- 7.4 CPU MODULE
- 7.5 FAX/MODEM/VOICE CARD
- 7.6 KEYBOARD
- 7.7 MEMORY MODULE

LCD ASSEMBLY COMPONENTS

- 7.8 LCD ASSEMBLY
- 7.9 LCD PANEL
- 7.10 INVERTER BOARD(D/A)

BASE UNIT COMPONENTS

- 7.11 BOTTOM CHASSIS
- 7.12 VIDEO-CAPTURE BOARD
- 7.13 SYSTEM BOARD
- 7.14 DC/DC BOARD
- 7.15 TOUCHPAD MODULE

7.1 SYSTEM VIEW

7.1.1 RIGHT-SIDE VIEW (FIGURE 7-1)

1. IR PORT.
2. VOLUME CONTROL.
3. AUDIO INPUT CONNECTOR.
4. AUDIO OUTPUT CONNECTOR.
5. MICROPHONE CONNECTOR.
6. CD-ROM DRIVE.
7. VIDEO OUT CONNECTOR.
8. VIDEO IN CONNECTOR.
9. 5V POWER CONNECTOR.
10. PS/2 MOUSE/KEYBOARD PORT.
11. POWER BUTTON.

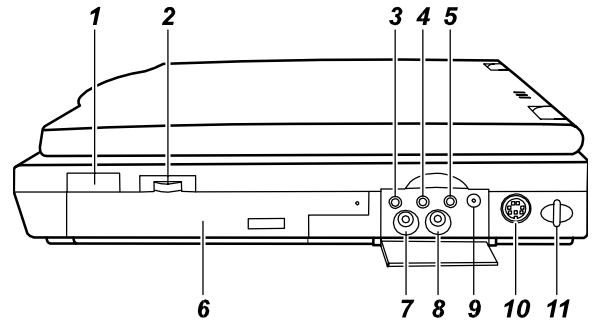


FIGURE 7-1. RIGHT-SIDE VIEW

7.1.2 LEFT-SIDE VIEW (FIGURE 7-2)

1. FLOPPY DISK DRIVE.
2. PHONE LINE CONNECTOR.
3. PC CARD SLOTS.
4. HARD DISK DRIVE.

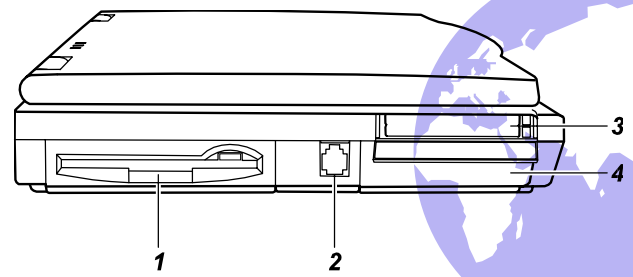


FIGURE 7-2. LEFT-SIDE VIEW

7.1.3 REAR VIEW (FIGURE 7-3)

1. POWER CONNECTOR.
2. PARALLEL PORT.
3. SERIAL PORT.
4. VGA PORT.
5. DOCKING STATION CONNECTOR.
6. USB PORT.
7. LEGS.
8. KENSINGTON LOCK ANCHOR.

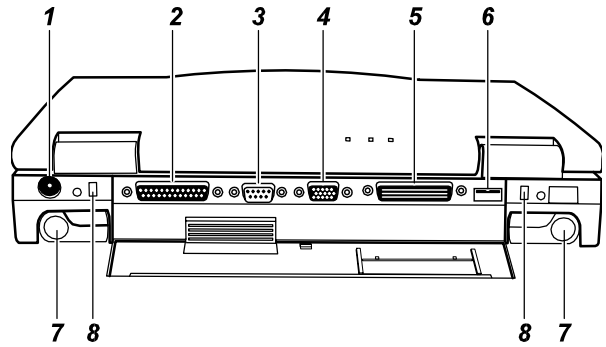


FIGURE 7-3. REAR VIEW

7.1.4 TOP-OPEN VIEW (FIGURE 7-4)

TO OPEN THE COVER, PRESS THE COVER LATCH AND LIFT THE COVER.

1. LCD DISPLAY.
2. MICROPHONE.
3. KEYBOARD.
4. TOUCHPAD.
5. INDICATORS PANEL.

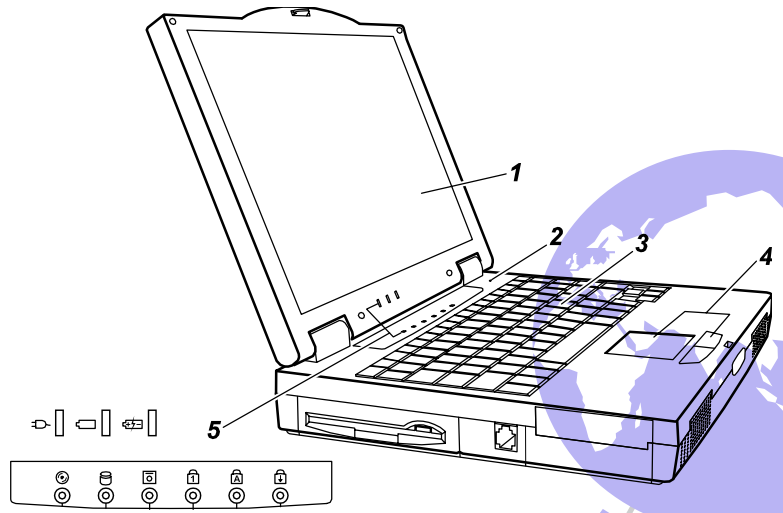


FIGURE 7-4. TOP-OPEN VIEW

7.1.5 FRONT VIEW (FIGURE 7-5)

1. CCD CAMERA CONNECTOR.
2. STEREO SPEAKER SET.
3. TOP COVER LATCH.

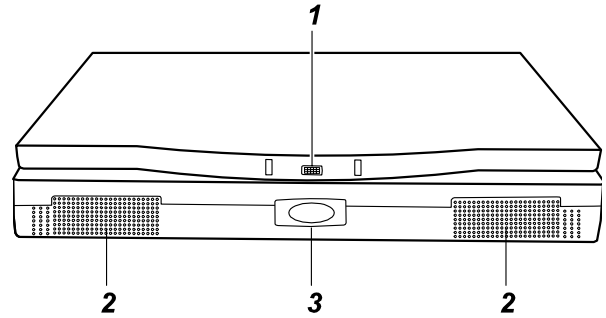


FIGURE 7-5. REAR VIEW

7.1.6 BOTTOM VIEW (FIGURE 7-6)

1. CPU COMPARTMENT COVER.
2. FAX/MODEM/VOICE CARD COMPARTMENT.

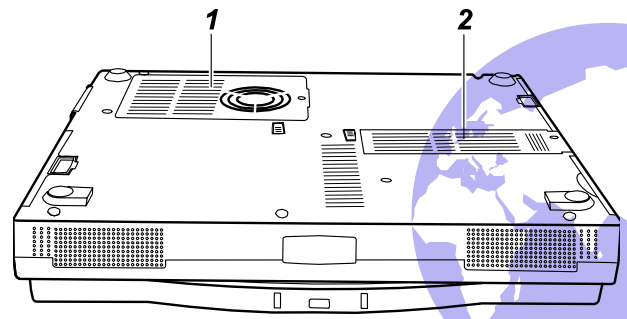


FIGURE 7-6. TOP-OPEN VIEW

7.2 LEFT AND RIGHT BAY DEVICES

THE LEFT AND RIGHT BAYS OF THE NOTEBOOK ARE DESIGNED FOR MULTIPLE OPTIONS.
THE LEFT BAY CAN ACCOMMODATE THE FOLLOWING DEVICES:

- ★ BATTERY PACK
- ★ AC ADAPTER
- ★ CARTRIDGE-REMOVABLE HARD DISK DRIVE
- ★ SECONDARY HARD DISK DRIVE
- ★ FLOPPY DISK DRIVE
- ★ MO DRIVE

THE RIGHT BAY CAN ACCOMMODATE THE FOLLOWING DEVICES:

- ★ FLOPPY DISK DRIVE (DEFAULT)
- ★ CD-ROM DRIVE
- ★ BATTERY PACK
- ★ CARTRIDGE-REMOVABLE HARD DISK DRIVE
- ★ SECONDARY HARD DISK DRIVE
- ★ MO DRIVE

DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. TO REMOVE THE LEFT BAY DEVICE AND RIGHT BAY DEVICE, PRESS THEIR LOCKING LATCHES TOWARD THE UNLOCKED POSITION AND PULL OUT THE MODULES.

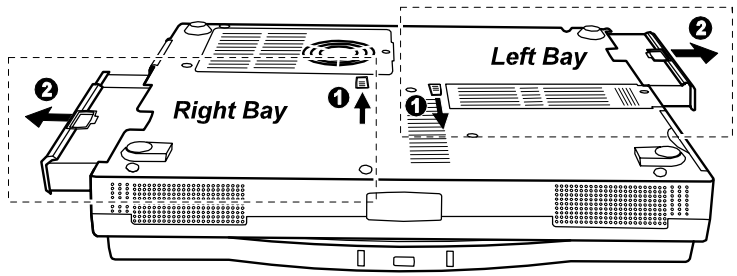


FIGURE 7-7. REMOVING THE LEFT AND RIGHT BAY DEVICES

REASSEMBLY

1. SLIDE THE DEVICE MODULE INTO THE BAY. MAKE SURE THE LOCKING LATCH IS IN THE LOCKED POSITION. (REFER TO FIGURE 7-7 EARLIER).

7.3 PRIMARY HARD DISK DRIVE DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. REMOVE THE BOTTOM SCREW AND PULL OUT THE HARD DISK DRIVE MODULE.

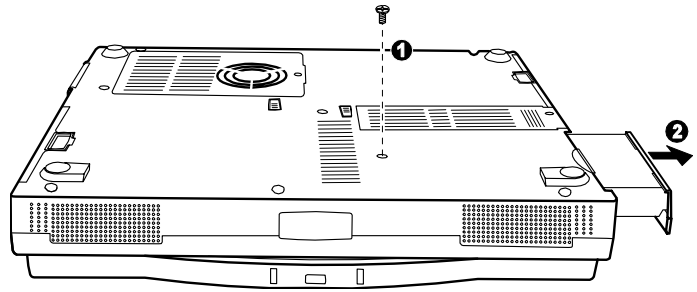


FIGURE 7-8. REMOVING THE HARD DISK DRIVE MODULE

3. REMOVE THE TOP COVER. REMOVE FOUR SIDE SCREWS AND TWO REAR SCRREWS AND DETACH THE HARD DISK DRIVE FROM THE BRACKET.

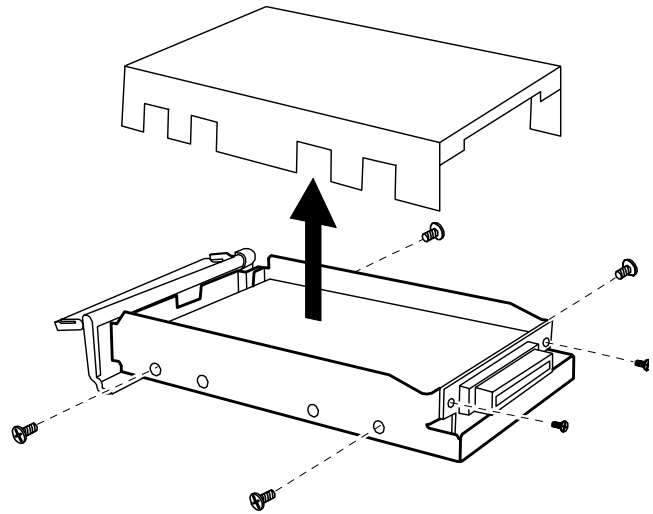


FIGURE 7-9. REMOVING THE HARD DISK DRIVE BRACKET SCREWS

4. UNPLUG THE CONNECTOR CARD.

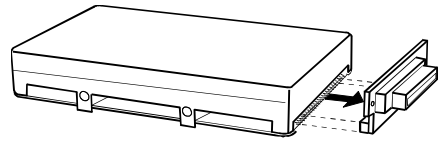


FIGURE 7-10. REMOVING THE HARD DISK DRIVE CONNECTOR CARD

REASSEMBLY

1. ALIGN THE CONNECTOR CARD WITH THE HARD DISK DRIVE CONNECTOR AND FIRMLY PLUG THE CONNECTOR. (REFER TO FIGURE 7-10 EARLIER).
2. ATTACH THE HARD DISK DRIVE TO THE BRACKET. SECURE WITH FOUR SCREWS ON BOTH SIDES AND TWO SCREWS ON THE REAR BRACKET. THEN FIT TOP COVER INTO PLACE. (REFER TO FIGURE 7-9 EARLIER).
3. SLIDE THE HARD DISK DRIVE MODULE INTO THE COMPARTMENT AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-8 EARLIER).

7.4 CPU MODULE DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. TO REMOVE THE CPU COMPARTMENT COVER. REMOVE ONE SCREW AND LIFT UP THE COVER.

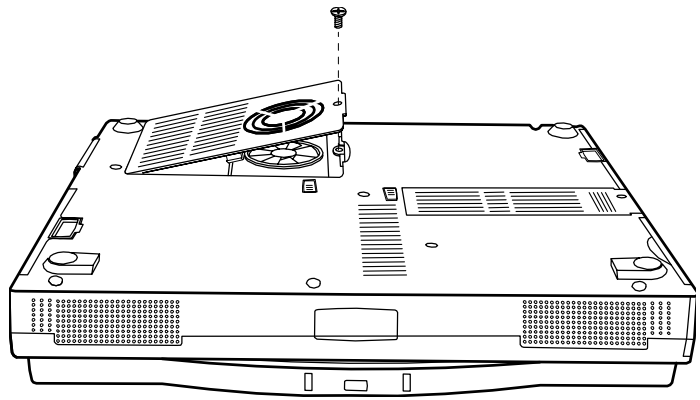


FIGURE 7-11. REMOVING THE CPU COMPARTMENT COVER SCREW

3. REMOVE TWO SCREWS FROM THE COOLING FAN ASSEMBLY.

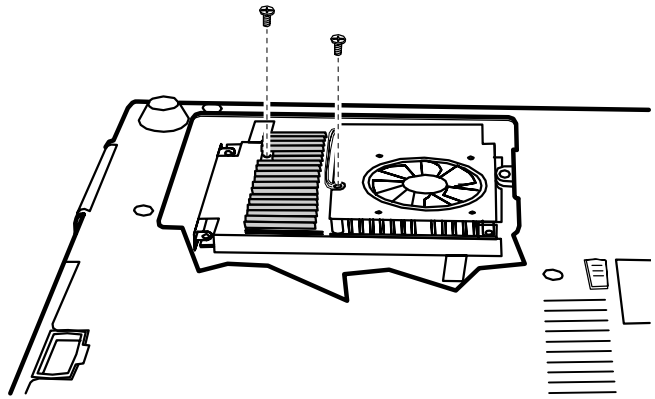


FIGURE 7-12. REMOVING TWO SCREWS FROM THE COOLING FAN ASSEMBLY

4. UNPLUG THE POWER CARD OF THE ASSEMBLY FROM J1001 ON THE SYSTEM BOARD.

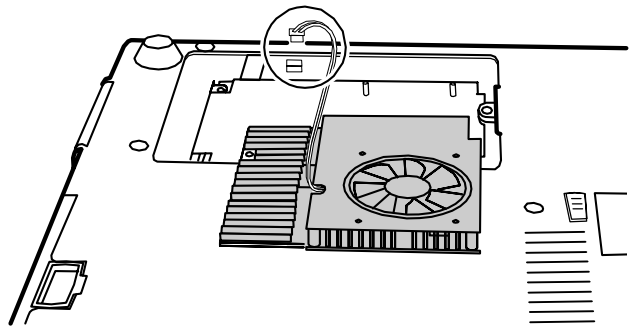


FIGURE 7-13. UNPLUG THE COOL FAN POWER CORD AND REMOVING COOL FAN.

5. REMOVE THE TWO HEXNUTS AND PULL UP THE RIBBONS TO LIFT THE IMM BRACKET AND UNPLUG THE CONNECTORS. (REFER TO FIGURE 7-14 ON NEXT PAGE).

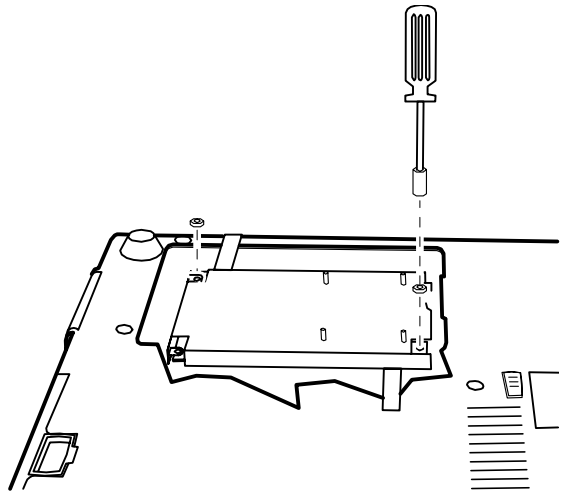


FIGURE 7-14. REMOVING THE CPU MODULE

6. SLIDE THE IMM OUT OF ITS BRACKET.

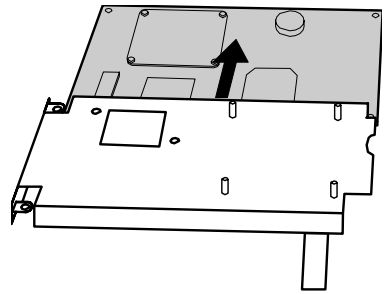


FIGURE 7-15. REMOVING THE CPU MODULE BRACKET

REASSEMBLY

1. INSERT THE CPU MODULE INTO THE BRACKET. (REFER TO FIGURE 7-15 EARLIER).
2. PLUG THE CONNECTORS ON THE CPU MODULE TO THE CORRESPONDING CONNECTORS ON THE SYSTEM BOARD. THEN REPLACE THE TWO HEXNUTS. (REFER TO FIGURE 7-14 EARLIER).
3. PLUG THE POWER CORD OF THE COOLING FAN ASSEMBLY TO J1001 ON THE SYSTEM BOARD.(REFER TO FIGURE 7-13 EARLIER).
4. ATTACH THE ASSEMBLY TO THE CPU BRACKET AND SECURE WITH TWO SCREWS (REFER TO FIGURE 7-12 EARLIER).
5. REPLACE THE COMPARTMENT COVER AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-11 EARLIER).

7.5 FAX/MODEM/VOICE CARD DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. TO REMOVE THE COMPARTMENT COVER, REMOVE ONE SCREW, THEN SLIDE THE COVER OUTWARDS AND LIFT UP.

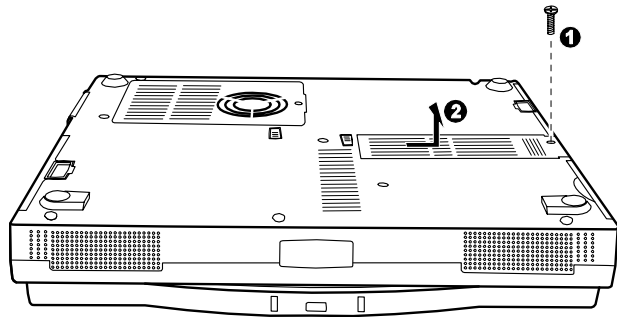


FIGURE 7-16. REMOVING THE FAX/MODEM/VOICE CARD COMPARTMENT COVER

3. LIFT UP THE INNER EDGE OF THE CARD AND REMOVE THE CARD.

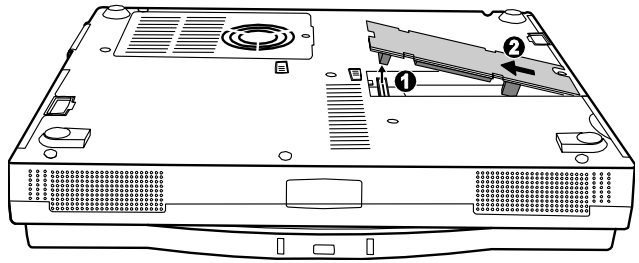


FIGURE 7-17. REMOVING THE FAX/MODEM/VOICE CARD

4. IF YOU WANT TO REINSTALL THE COMPARTMENT COVER AFTER THE CARD IS REMOVED, ATTACH THE PAD TO THE COVER.

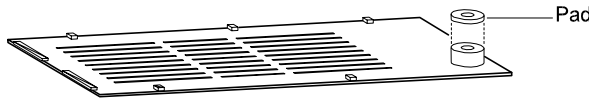


FIGURE 7-18. ATTACH THE PAD TO REINSTALL THE FAX/MODEM/VOICE COMPARTMENT COVER

REASSEMBLY

1. HOLD THE FAX/MODEM/VOICE CARD AT AN ANGLE SO THAT THE PHONE LINE CONNECTOR IS POINTED TOWARDS THE OPENING ON THE NOTEBOOK. INSERT THE PHONE LINE CONNECTOR INTO THE OPENING AND PRESS THE OTHER END TO PLUG THE OTHER CONNECTOR INTO THE SOCKET ON THE SYSTEM BOARD. (REFER TO FIGURE 7-17 EARLIER).
2. REINSTALL THE COMPARTMENT COVER (WITH THE PAD) AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-16 EARLIER).

7.6 KEYBOARD

DISASSEMBLY

1. OPEN THE TOP COVER. REMOVE THE INDICATORS PANEL COVER BY SLIDING IT DOWNWARDS AND LIFTING THE LOWER EDGE.

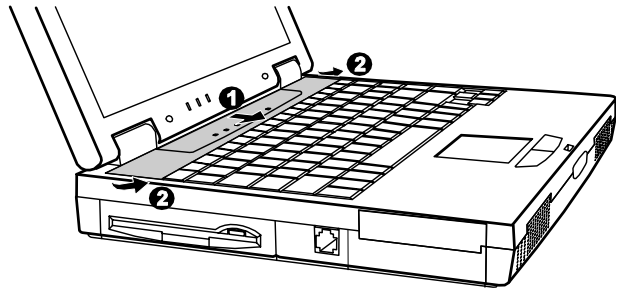


FIGURE 7-19. REMOVING THE INDICATOR PANEL

2. LIFT THE KEYBOARD AND UNPLUG THE KEYBOARD CABLE.

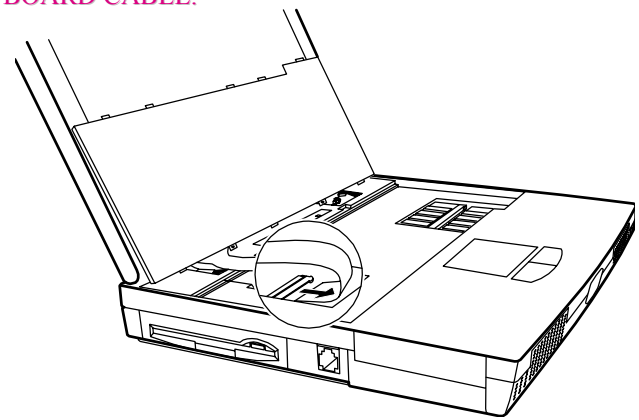


FIGURE 7-20. UNPLUGGING THE KEYBOARD CABLE

REASSEMBLY

1. RECONNECTOR THE KEYBOARD CABLE AND FIT THE KEYBOARD BACK INTO PLACE. (REFER TO FIGURE 7-20 EARLIER).
2. REINSTALL THE INDICATORS PANEL. (REFER TO FIGURE 7-19 EARLIER).

7.7 MEMORY MODULE

DISASSEMBLY

1. OPEN THE KEYBOARD WITHOUT UNPLUGGING THE KEYBOARD CABLE. (SEE SECTION 7.6 DISASSEMBLY).
2. PULL THE RETAINING CLIPS OUTWARDS AND REMOVE THE SO-DIMM.

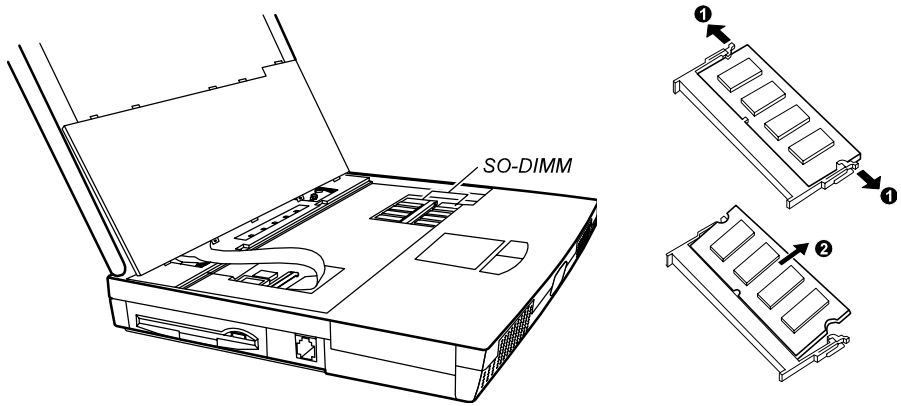


FIGURE 7-21. REMOING THE SO-DIMM

REASSEMBLY

1. TO INSTALL THE SO-DIMM, ALIGN THE SO-DIMM NOTCHED PART WITH THE SOCKET CORRESPONDING PART AND FIRMLY INSERT THE SO-DIMM INTO THE SOCKET AT A ANGLE. THEN PUSH DOWN UNTIL THE RETAINING CLIPS LOCK THE SO-DIMM INTO POSITION. (REFER TO FIGURE 7-21 EARLIER).
2. REINSTALL THE KEYBOARD. (SEE SECTION 7.6 REASSEMBLY).

7.8 LCD ASSEMBLY

DISASSEMBLY

1. OPEN THE TOP COVER. REMOVE THE INDICATORS PANEL COVER BY SLIDING IT DOWNWARDS AND LIFTING THE LOWER EDGE. (SEE FIGURE 7-19)
2. REMOVE THE TWO HINGE COVERS.(REFER TO FIGURE 7-22 ON THE NEXT PAGE).

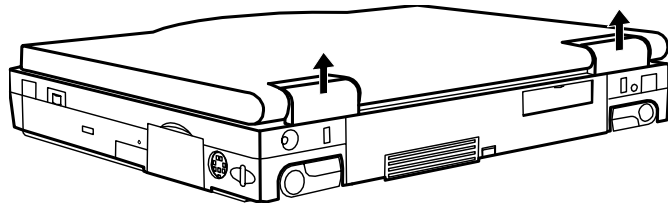


FIGURE 7-22. REMOVING THE HINGE COVERS

3. UNPLUG THE LCD CABLE CONNECTORS FROM THE SYSTEM BOARD. (SEE FIGURE 7-23)
4. REMOVE THE FOUR SCREWS FROM THE HINGES. NOW THE LCD ASSEMBLY FREE.

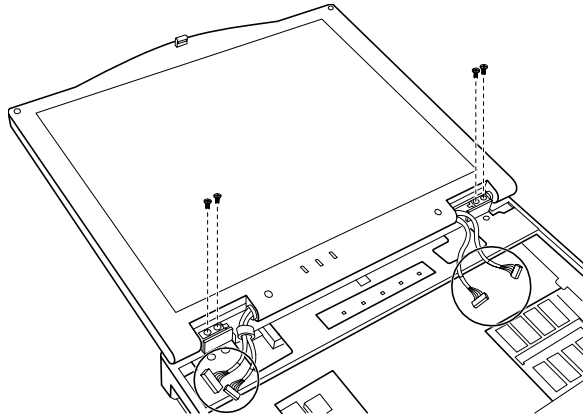


FIGURE 7-23. UNPLUGGING THE LCD CONNECTORS AND REMOVING THE HINGE SCREWS

REASSEMBLY

1. ATTACH THE LCD ASSEMBLY TO THE BASE UNIT AND SECURE WITH FOUR SCREWS ON THE HINGES. (REFER TO FIGURE 7-23 EARLIER).
2. RECONNECT THE LCD CABLE CONNECTORS TO THE SYSTEM BOARD. (REFER TO FIGURE 7-23 EARLIER).
3. REINSTALL THE TWO HINGE COVERS. (REFER TO FIGURE 7-22 EARLIER).
4. REINSTALL THE INDICATORS PANEL COVER.

7.9 LCD PANEL DISASSEMBLY

1. OPEN THE TOP COVER. REMOVE THE INDICATORS PANEL COVER BY SLIDING IT DOWNWARDS AND LIFTING THE LOWER EDGE. (SEE FIGURE 7-19 EARLIER).
2. UNPLUG THE LCD CABLE CONNECTORS FROM THE SYSTEM BOARD. (SEE FIGURE 7-24 ON NEXT PAGE).
3. REMOVE THE FOUR RUBBER PADS AND FOUR SCREWS UNDERNEATH. NOW YOU CAN SEPARATE THE LCD FRAME FROM THE HOUSING. (REFER TO FIGURE 7-24 ON NEXT PAGE).

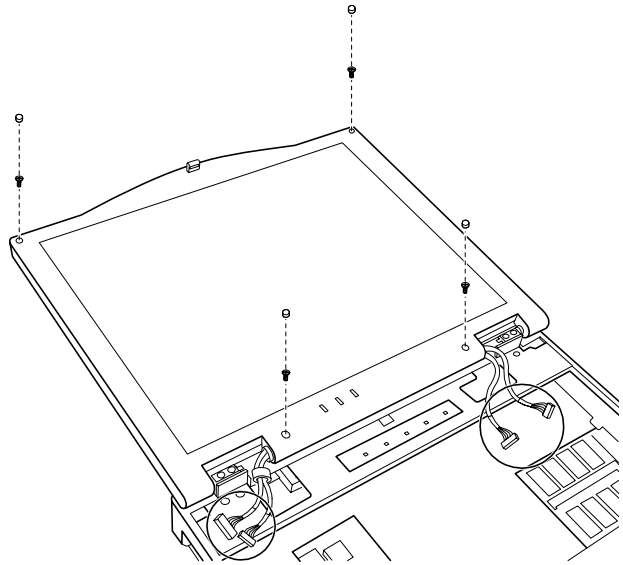


FIGURE 7-24. REMOVING THE LCD FRAME

4. TO REMOVE THE LCD, REMOVE FOUR SCREWS AND UNPLUG THE CABLES.

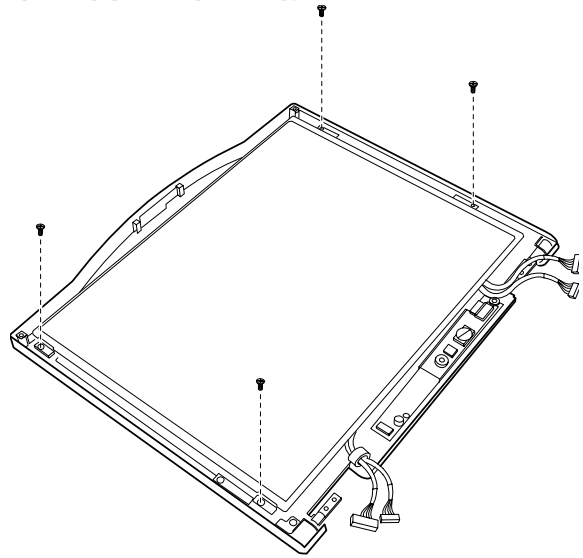


FIGURE 7-25. REMOVING THE FLAT PAANEL SCREEN

REASSEMBLY

1. RECONNECT THE CABLES TO THE LCD. FIT THE LCD BACK INTO PLACE AND SECURE WITH FOUR SCREWS. (REFER TO FIGURE 7-25 EARLIER).
2. FIT THE LCD FRAME BACK TO THE HOUSING AND REPLACE THE FOUR SCREWS AND RUBBER PADS. (REFER TO FIGURE 7-24 EARLIER).
3. RECONNECT THE LCD CABLE CONNECTORS TO THE SYSTEM BOARD. (REFER TO FIGURE 7-24 EARLIER).
4. REINSTALL THE TWO HINGE COVERS. (REFEER TO FIGURE 7-22 EARLIER).
5. REINSTALL THE INDICATORS PANEL COVER.

7.10 INVERTER BOARD

DISASSEMBLY

1. DETACH THE LCD FRAME. (SEE STEPS 1 TO 3 IN SECTION 7.9 DISASSEMBLY).
2. TO REMOVE THE INVERTER BOARD, REMOVE ONE SCREW AND UNPLUG THE CONNECTORS FROM THE BOARD.

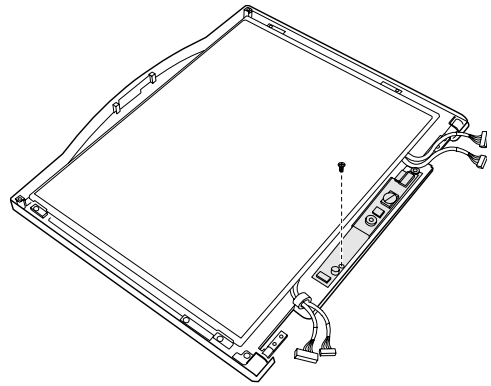


FIGURE 7-26. REMOVING THE INVERTER BOARD

REASSEMBLY

1. RECONNECT THE CONNECTORS. FIT THE INVERTER BOARD BACK INTO PLACE AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-26 EARLIER).
2. FIT THE LCD FRAME BACK TO THE HOUSING AND REPLACE THE FOUR SCREWS AND RUBBER PADS. (REFER TO FIGURE 7-24 EARLIER).

7.11 BOTTOM CHASSIS

DISASSEMBLY

1. REMOVE THE RIGHT AND LEFT BAY DEVICES. (SEE SECTION 7.2 DISASSEMBLY).
2. REMOVE THE HARD DISK DRIVE MODULE. (SEE SECTION 7.3 DISASSEMBLY).
3. REMOVE THE CPU COMPARTMENT COVER. (SEE SECTION 7.4 DISASSEMBLY).
4. REMOVE THE FAX/MODEM/VOICE CARD. (SEE FIGURE 7.5 DISASSEMBLY)
5. REMOVE TEN BOTTOM SCREWS TO SEPARATE THE BOTTOM CHASSIS FROM THE BASE UNIT. (REFER TO FIGURE 7-27 ON NEXT PAGE).

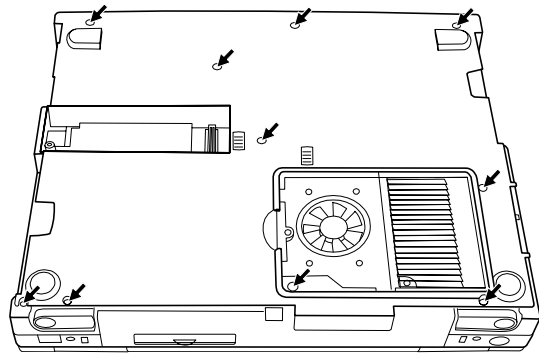


FIGURE 7-27. REMOVING THE BOTTOM CHASSIS

REASSEMBLY

1. REINSTALL THE BOTTOM CHASSIS AND SECURE WITH TEN SCREWS. (REFER TO FIGURE 7-27 EARLIER).
2. REINSTALL THE FAX/MODEM/VOICE CARD. (SEE SECTION 7.5 REASSEMBLY).
3. REINSTALL THE CPU COMPARTMENT COVER AND SECURE WITH ONE SCREW.
4. REINSTALL THE HARD DISK DRIVE MODULE. (SEE SECTION 7.3 REASSEMBLY).
5. REINSTALL THE RIGHT AND LEFT BAY DEVICES. (SEE SECTION 7.2 REASSEMBLY)

7.12 VIDEO CAPTURE BOARD

DISASSEMBLY

1. REMOVE THE BOTTOM CHASSIS. (SEE SECTION 7.11 DISASSEMBLY).
2. REMOVE THE VIDEO CAPTURE BOARD BY REMOVING ONE SCREW AND LIFTING IT UP.

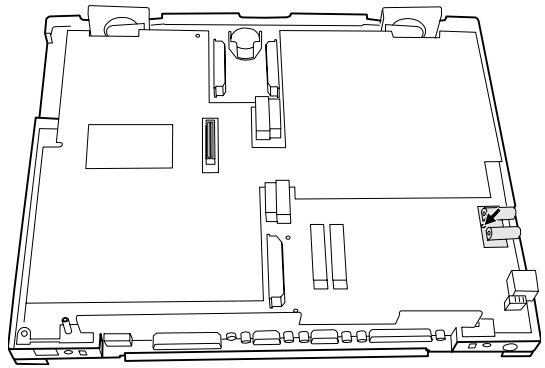


FIGURE 7-28. REMOVING THE VIDEO CAPTURE BOARD

REASSEMBLY

1. RECONNECT THE VIDEO CAPTURE CONNECTOR TO THE SYSTEM BOARD AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-28 EARLIER).
2. REINSTALL THE BOTTOM CHASSIS. (SEE SECTION 7.11 REASSEMBLY).

7.13 SYSTEM BOARD DISASSEMBLY

1. REMOVE TWO REAR PANEL SCREWS.

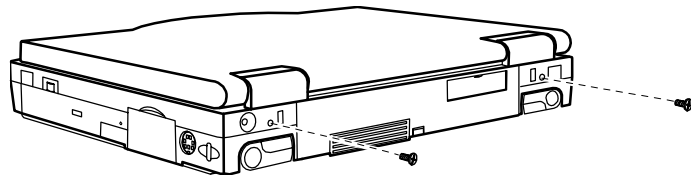


FIGURE 7-29. REMOVING TWO REAR PANEL SCREWS

2. REMOVE THE LCD ASSEMBLY. (SEE SECTION 7.8 DISASSEMBLY).
3. REMOVE THE KEYBOARD. (SEE SECTION 7.6 DISASSEMBLY).
4. UNPLUG THE TOUCHPAD CONNECTOR (J21) AND SPEAKER CONNECTORS(J7 AND J9) FROM THE SYSTEM BOARD.

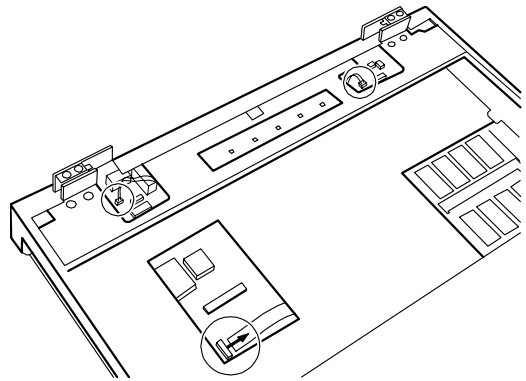


FIGURE 7-30. UNPLUGGING THE TOUCHPAD AND SPEAKER CONNECTORS

5. REMOVE THE FOUR SCREWS FROM NEAR THE HINGES. (REFER TO FIGURE 7-31 ON THE NEXT PAGE).

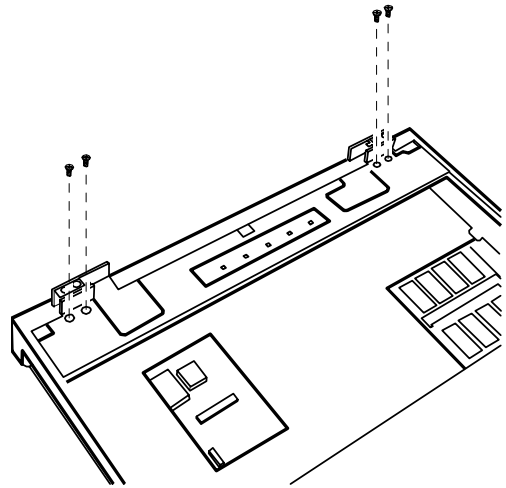


FIGURE 7-31. REMOVING FOUR SCREWS FROM NEAR THE HINGES

6. REMOVE THE BOTTOM CHASSIS. (SEE SECTION 7.11 DISASSEMBLY).
7. REMOVE THE IMM/MCC-1 CPU MODULE. (SEE SECTION 7.4 DISASSEMBLY).
8. UNPLUG ANY CONNECTORS THAT ARE STILL CONNECTED TO THE SYSTEM BOARD.
9. REMOVE THE REMAINING TWO SCREWS THAT SECURE THE SYSTEM BOARD TO THE BASE UNIT.

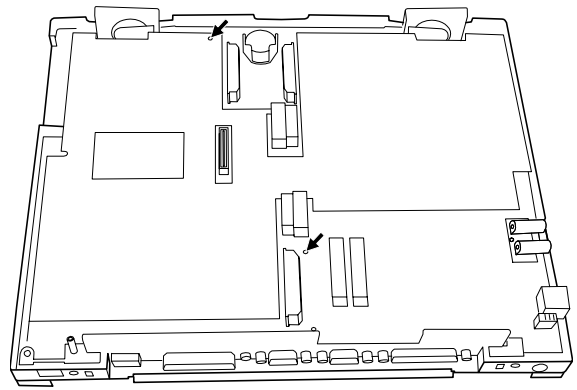


FIGURE 7-32. REMOVING THE SYSTEM BOARD SCREWS

11. LIFT THE SYSTEM BOARD FREE.

REASSEMBLY

1. FIT THE SYSTEM BOARD INTO BASE UNIT AND SECURE WITH TWO SCREWS. (SEE FIGURE 7-32 EARLIER).
2. REINSTALL THE IMM/MCC-1 CPU MODULE. (SEE SECTION 7.4 REASSEMBLY).
3. REINSTALL THE BOTTOM CHASSIS. (SEE SECTION 7.11 REASSEMBLY).
4. REPLACE THE FOUR SCREWS NEAR THE HINGES. (REFER TO THE FIGURE 7-30 EARLIER).
5. CONNECT THE SPEAKER AND TOUCHPAD CONNECTORS TO THE SYSTEM BOARD.
6. REINSTALL THE KEYBOARD. (SEE SECTION 7.6 REASSEMBLY).
7. REPLACE THE TWO REAR PANEL SCREWS. (REFER TO FIGURE 7-28 EARLIER).
8. REINSTALL THE LCD ASSEMBLY. (SEE SECTION 7.8 REASSEMBLY).

7.14 DC/DC BOARD DISASSEMBLY

1. REMOVE THE SYSTEM BOARD. (SEE SECTION 7.13 DISASSEMBLY).
2. REMOVE THE PLATE ON THE DC/DC BOARD BY REMOVING TWO SCREWS.

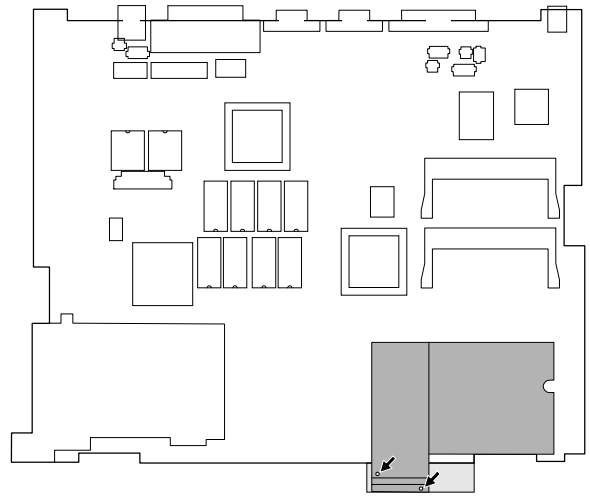


FIGURE 7-33. REMOVING THE DC/DC BOARD PLATE

3. REMOVE THE DC/DC BOARD BY REMOVING ONE SCREW AND LIFTING UP. (REFER TO FIGURE 7-34 ON THE NEXT PAGE).

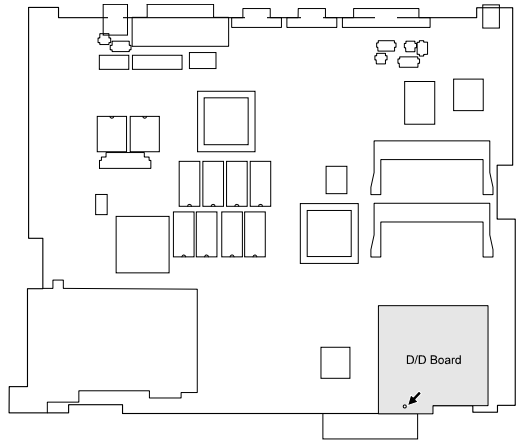


FIGURE 7-34. REMOVING THE DC/DC BOARD

REASSEMBLY

1. RECONNECT THE DC/DC BOARD CONNECTOR TO THE SYSTEM BOARD AND SECURE WITH ONE SCREW. (REFER TO FIGURE 7-34 EARLIER).
2. REINSTALL THE DC/DC BOARD PLATE AND SECURE WITH TWO SCREWS. (REFER TO FIGURE 7-33 EARLIER).
3. REINSTALL THE SYSTEM BOARD. (SEE SECTION 7.11 REASSEMBLY).

7.15 TOUCHPAD MODULE DISASSEMBLY

1. REMOVE THE SYSTEM BOARD. (SEE SECTION 7.14DISASSEMBLY).
2. REMOVE THE TOUCHPAD HOLDER BY REMOVING THREE SCREWS. (SHOWN AS FIGURE 7-35).
3. SLIDE THE TOUCHPAD MODULE OUT.

REASSEMBLY

1. FIT THE TOUCHPAD MODULE BACK INTO PLACE.
2. FIT THE TOUCHPAD HOLDER BACK INTO PLACE AND SECURE WITH THREE SCREWS. (REFER TO FIGURE 7-35 EARLIER).
3. REINSTALL THE SYSTEM BOARD. (SEE SECTION 7.14 REASSEMBLY).

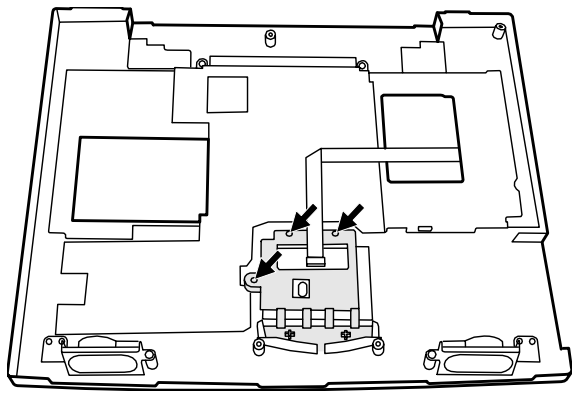


FIGURE 7-35. REMOVING THE TOUCHPAD HOLDER

8. MAINTENANCE DIAGNOSTICS

8.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON, THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED,THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC PORT (378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE, IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO PORT 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

8. MAINTENANCE DIAGNOSTICS

8.2 ERROR CODES

FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

CODE	BEEP	Description
00H		START OF BOOT LOADER SECQUENCE.
01H		DISABLE A20 THROUGH A20, NOT SEND.
02H	.._.	INITIALIZE CHIPSET OR BIOS NOT SHADOWED.
03H		PERFORM CONVENTIONAL RAM TEST WITH CROSSED-PATTERN R/W.
04H	._..	MOVE BOOT LOADER TO THE RAM OR BIOS CHECKSUM BAD.
05H		START POINT OF EXECUTION OF BOOT LOADER IN RAM.
06H		PERFORM PNP INITIALIZATION FOR CRYSTAL AUDIO CHIP OR CHECK
		OVERRIDE OPTION, NOT SEND.
07H		SHADOW SYSTEM BIOS.
08H		CHECKSUM SYSTEM BIOS ROM, NOT SEND.
09H		PROCEED WITH NORMAL BOOT.
0AH		PROCEED WITH CRISIS BOOT.
0FH	——	NO RAM OR DRAM SIZING.
10H		INITIAL L1, L2 CACHE, MAKE STACK AND DIAGNOSE CMOS.
11H		TURN OFF FAST A20 FOR FOR POST. RESET GDTS, 8259S QUICKLY.
12H		SIGNAL POWER ON RESET AT CMOS.
13H		INITIALIZE THE CHIPSET, (SDRAM).***SOLUTION: TRY TO CLEAR CMOS***
14H		SEARCH FOR ISA BUS VGA ADAPTER.
15H		RESET COUNTER/TIMER 1.
16H		USER REGISTER CONFIG THROUGH CMOS.
18H		DISPATCH TO 1ST 64K RAM TEST.
19H		CHECKSUM THE ROM.
1AH		RESET PIC'S(8259).
1BH		INITIALIZE VIDEO ADAPTER(S).
1CH		INITIALIZE VIDEO (6845 REGS).
1DH		INITIALIZE COLOR ADAPTER.
1EH		INITIALIZE MONOCHROME ADAPTER.
1FH		TEST 8237A PAGE REGISTERS.
20H		PERFORM KEYBOARD SELF TEST.
21H		TEST & INITIALIZE KEYBOARD CONTROLLER.
22H		CHECK IF CMOS RAM VALID.
23H		TEST BATTER FAIL & CMOS X-SUM.
24H		TEST THE DMA CONTROLLER.
25H		INITIALIZE 8237A CONTROLLER.
26H		INITIALIZE INTERRUPT VECTORS TABLE.
27H		RAM QUICK SIZING.

CODE	BEEP	Description
28H		PROTECTED MODE ENTERED SAFELY.
29H		RAM TEST COMPLETED.
2AH		PROTECTED MODE EXIT SUCCESSFUL .
2BH		SETUP SHADOW.
2CH		PREPARE TO INITIALIZE VIDEO.
2DH		SEARCH FOR MONOCHROME ADAOTER.
2EH		SEARCH FOR COLOR ADAPTER, VGA INITIALIZE.
2FH		SIGN-ON MESSAGES DISPLAYED.
30H		SPECIAL INIT OF KEYBOARD CONTROLLER.
31H		TEST IF KEYBOARD PRESENT.
32H		TEST KEYBOARD INTERRUPT.
33H		TEST KEYBOARD COMMAND BYTE.
34H		TEST, BLANK AND COUNT ALL RAM.
35H		PROTECTED MODE ENTERED SAFELY(2).
36H		RAM TEST COMPLETED.
37H		PROTECTED MODE EXIT SUCCESSFUL .
38H		UPDATE KEYBOARD OUTPUT PORT TO DISABLE GATE OF A20.
39H		SETUP CACHE CONTROLLER.
3AH		TEST IF 18.2HZ PERIODIC WORKING.
3BH		INITIALIZE BIOS DATA AREA AT 40:0.
3CH		INITIALIZE THE HARDWARE INTERRUPT VECTOR.
3DH		SEARCH AND INIT THE MOUSE.
3EH		UPDATE NUMLOCK STATUS.
3FH		OEM INITIALIZATION OF COMM AND LPT PORTS.
40H		CONFIGURE THE COMM AND LPT PORTS.
41H		INITIALIZE THE FLOPPIES.
42H		INITIALIZE THE HARD DISK.
43H		INITIALIZE ADDITIONAL ROMS.
44H		OEM'S INIT OF POWER MANAGEMENT, (CHECK SMI).
45H		UPDATE NUMLOCK STATUS.
46H		TEST FOR COPROCESSOR INSTALLED.
47H		OEM FUNCTIONS BEFORE BOOT(PCMCIA, CARDBUSS).
48H		DISPATCH TO OPERATION SYSTEM BOOT.
49H		JUMP INTO BOOTSTRAP CODE.
4AH		OEM'S INIT OF PM WITH USB.
FO~F1H	....	RMA TEST FAILED.

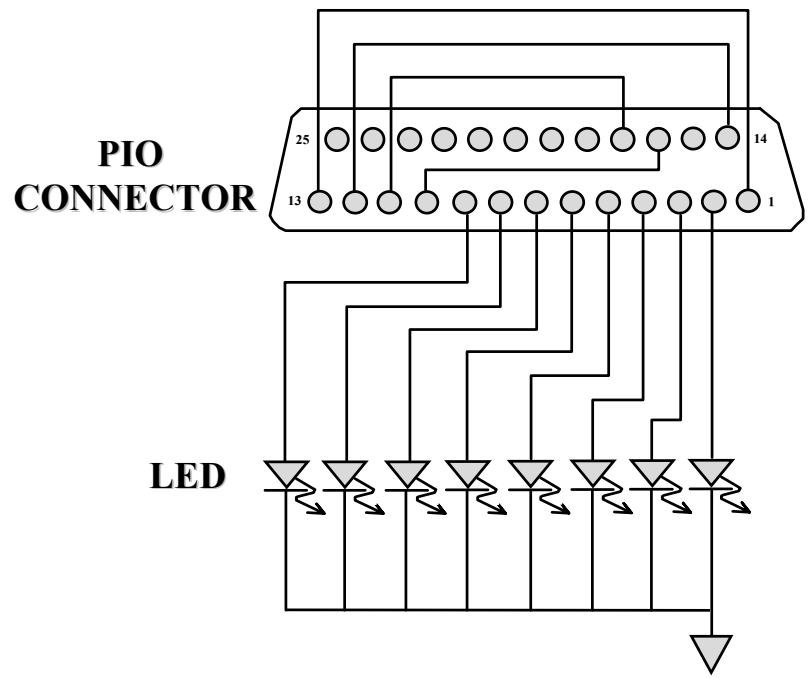
8. MAINTENANCE DIAGNOSTICS

8.3 PIO PORT (378H) DIAGNOSTIC TOOLS

A. PARTS USED:

- LED * 8
- PIO CONNECTOR * 1

B. CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

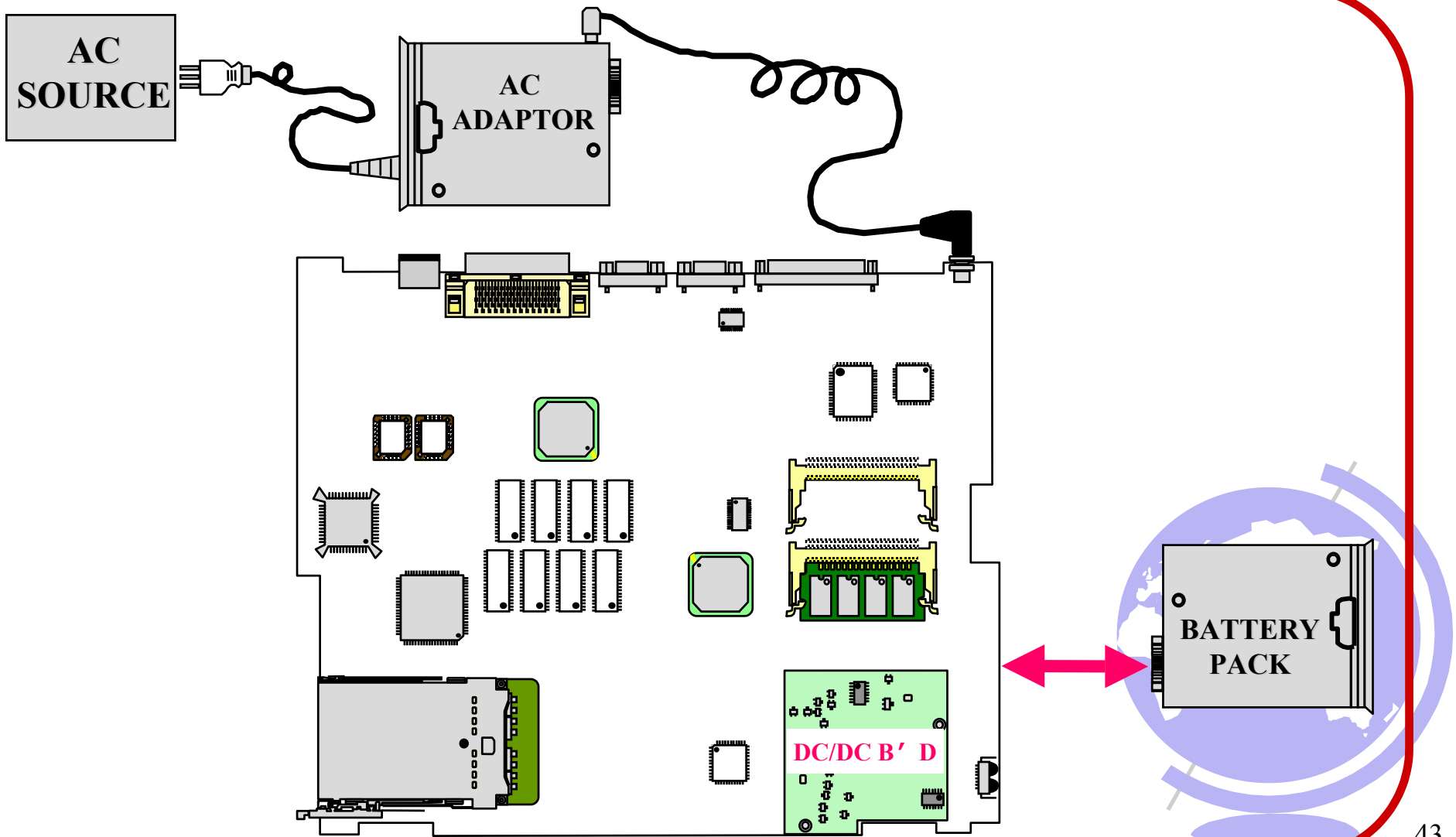
PIN{9:2}: PD{7:0}

9. TROUBLE SHOOTING

9.1 NO POWER

SYMPTOM:

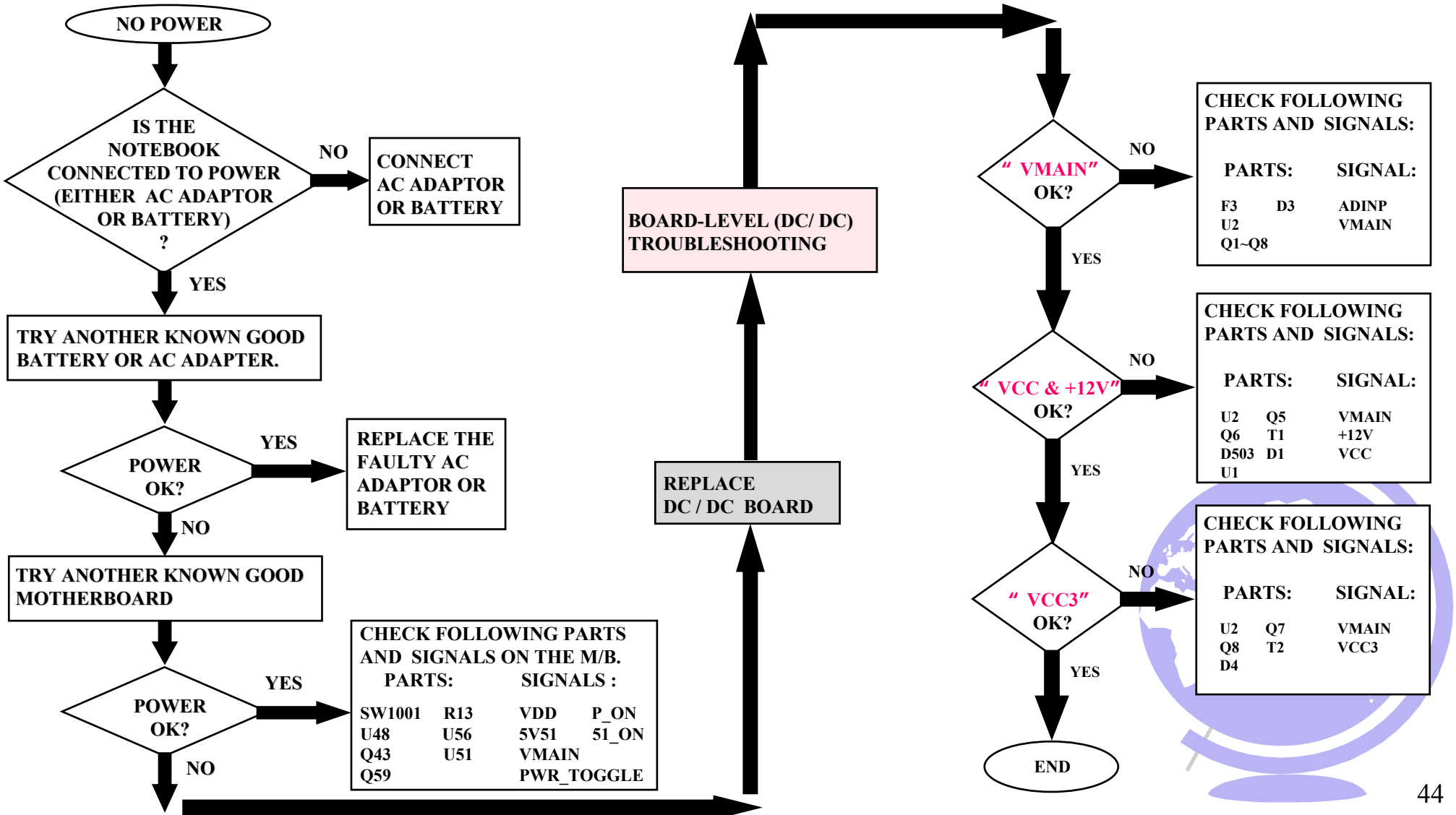
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



9.1 NO POWER

SYMPTOM:

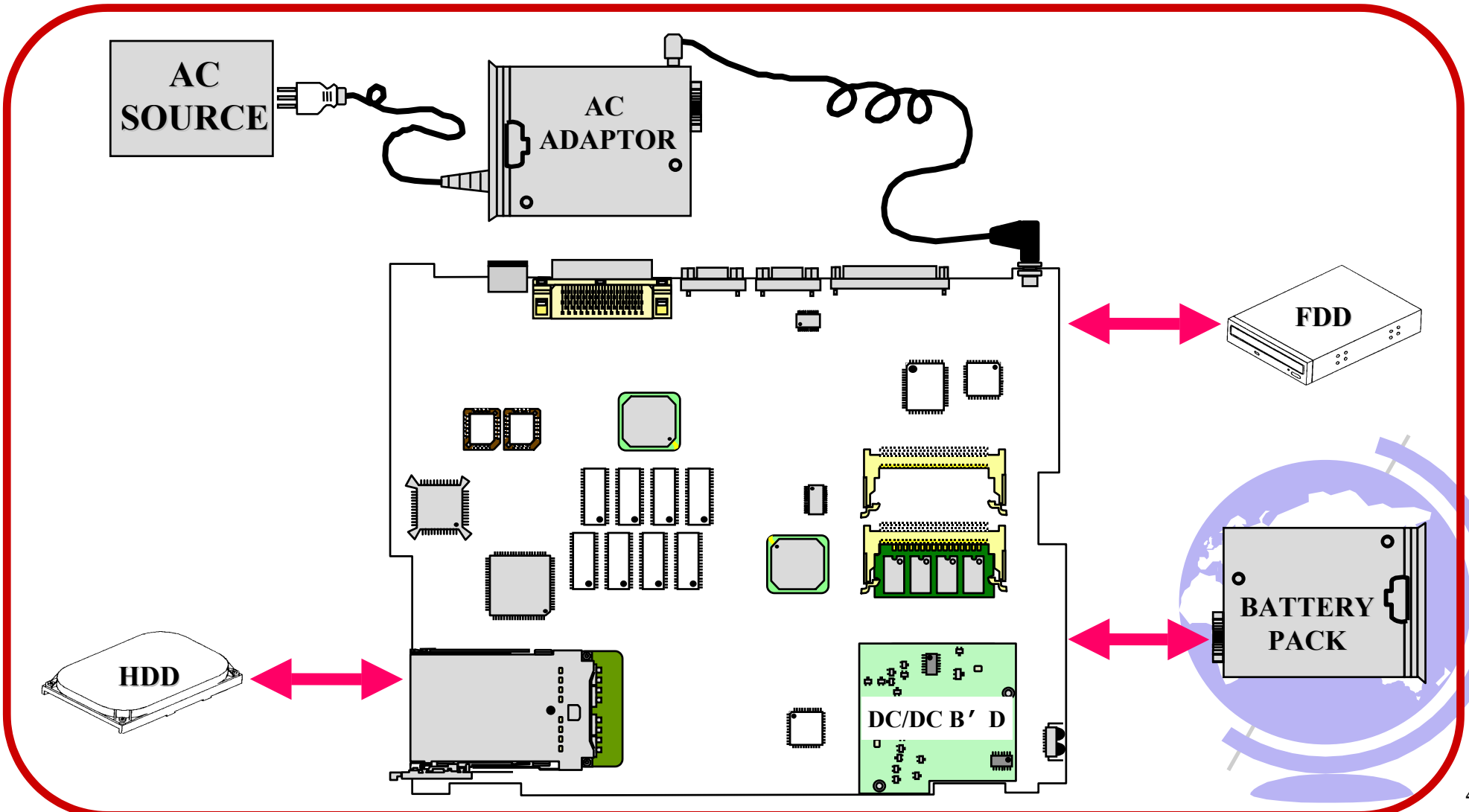
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



9.2 NO DISPLAY (SYSTEM FAILURE)

SYMPTOM:

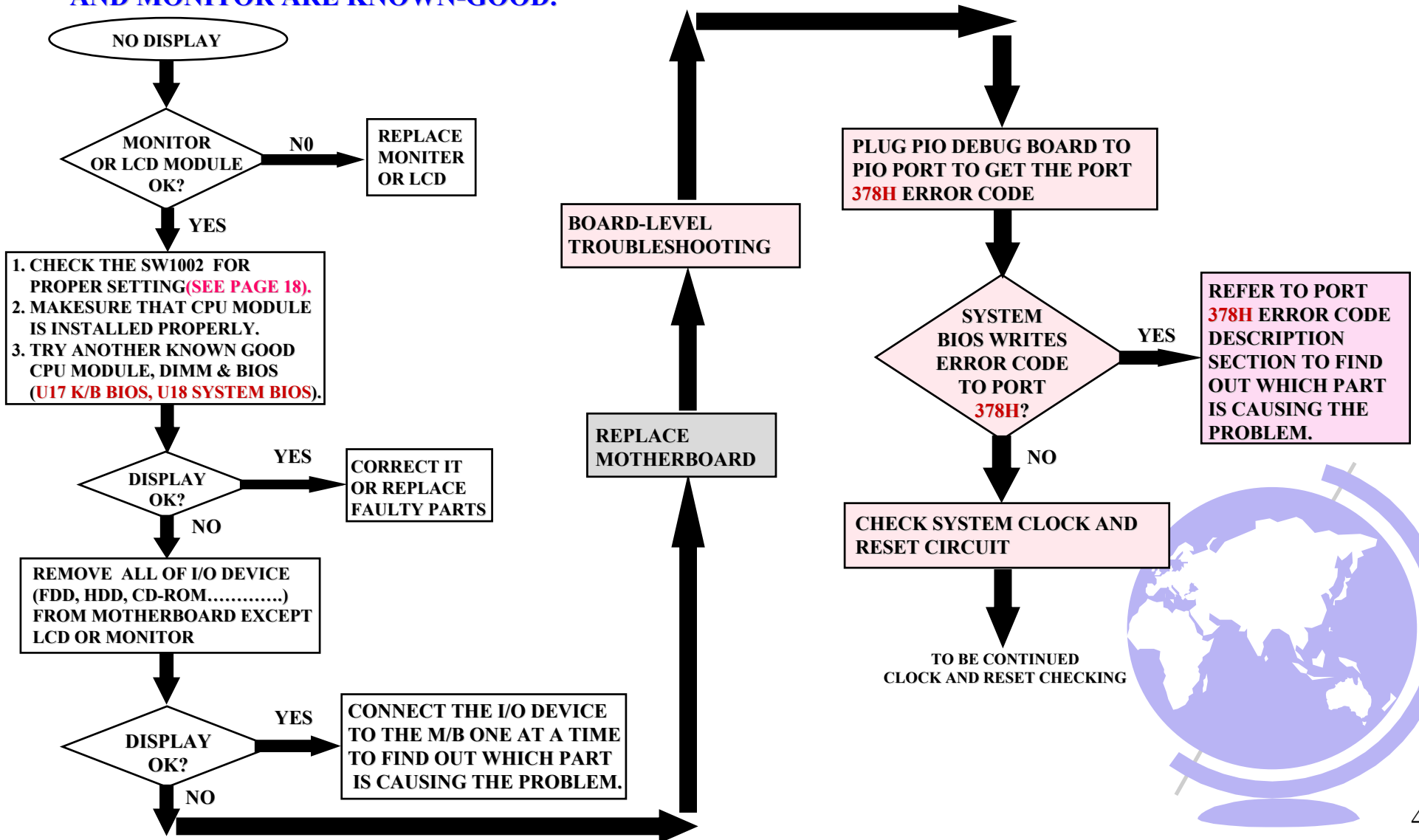
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



9.2 NO DISPLAY (SYSTEM FAILURE)

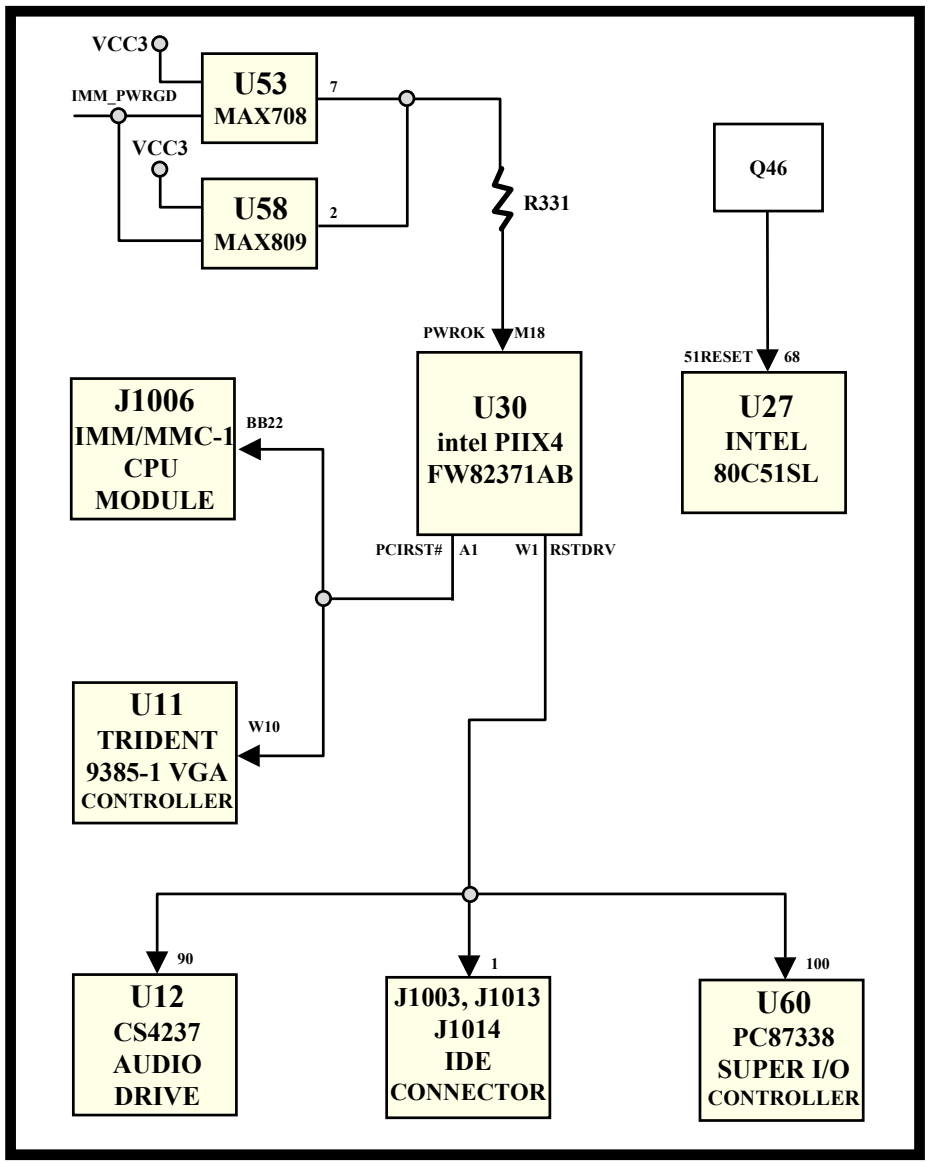
SYMPTOM:

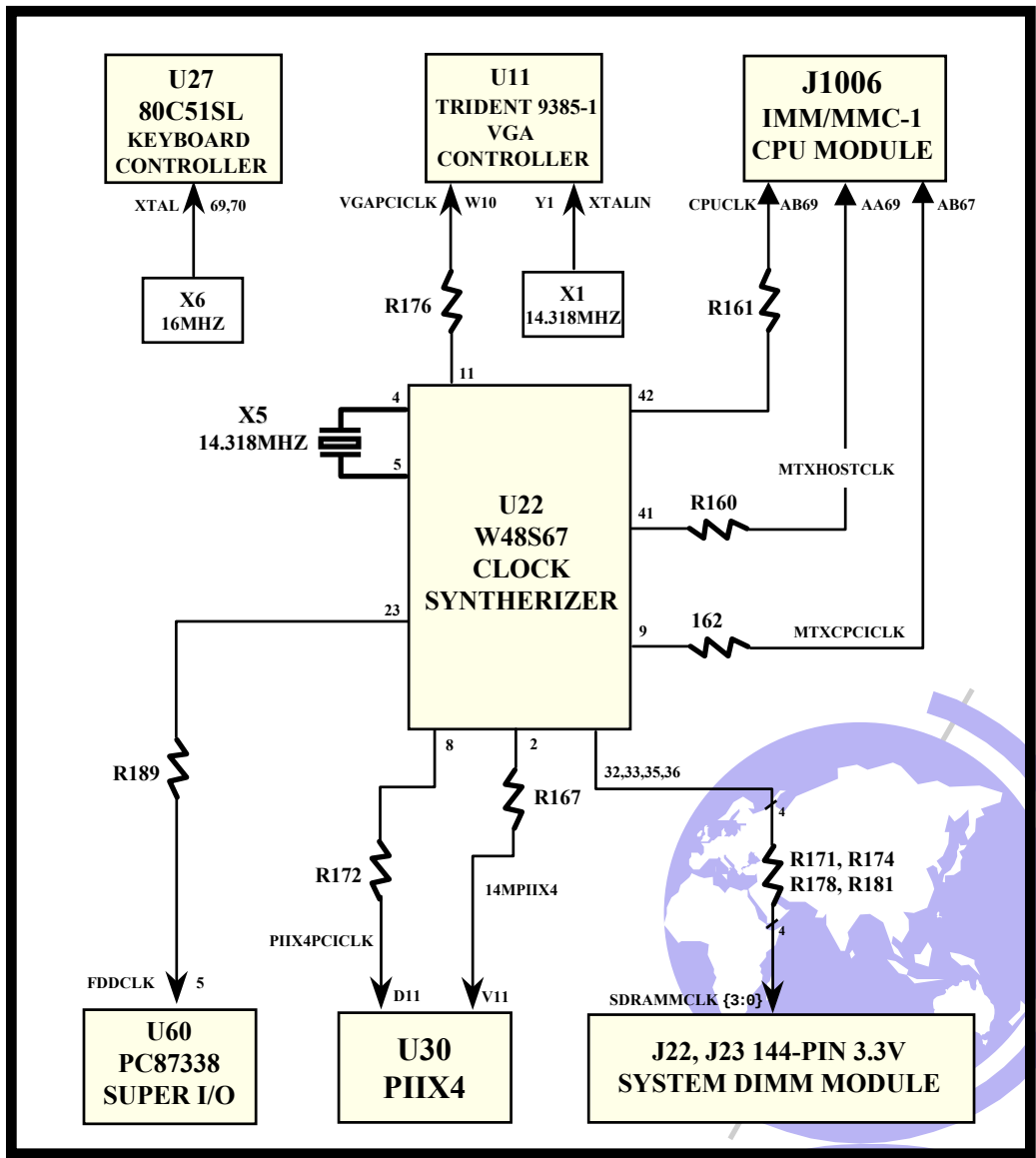
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



9.2 NO DISPLAY (SYSTEM FAILURE)

*********CLOCK AND RESET CIRCUIT CHECKING*********

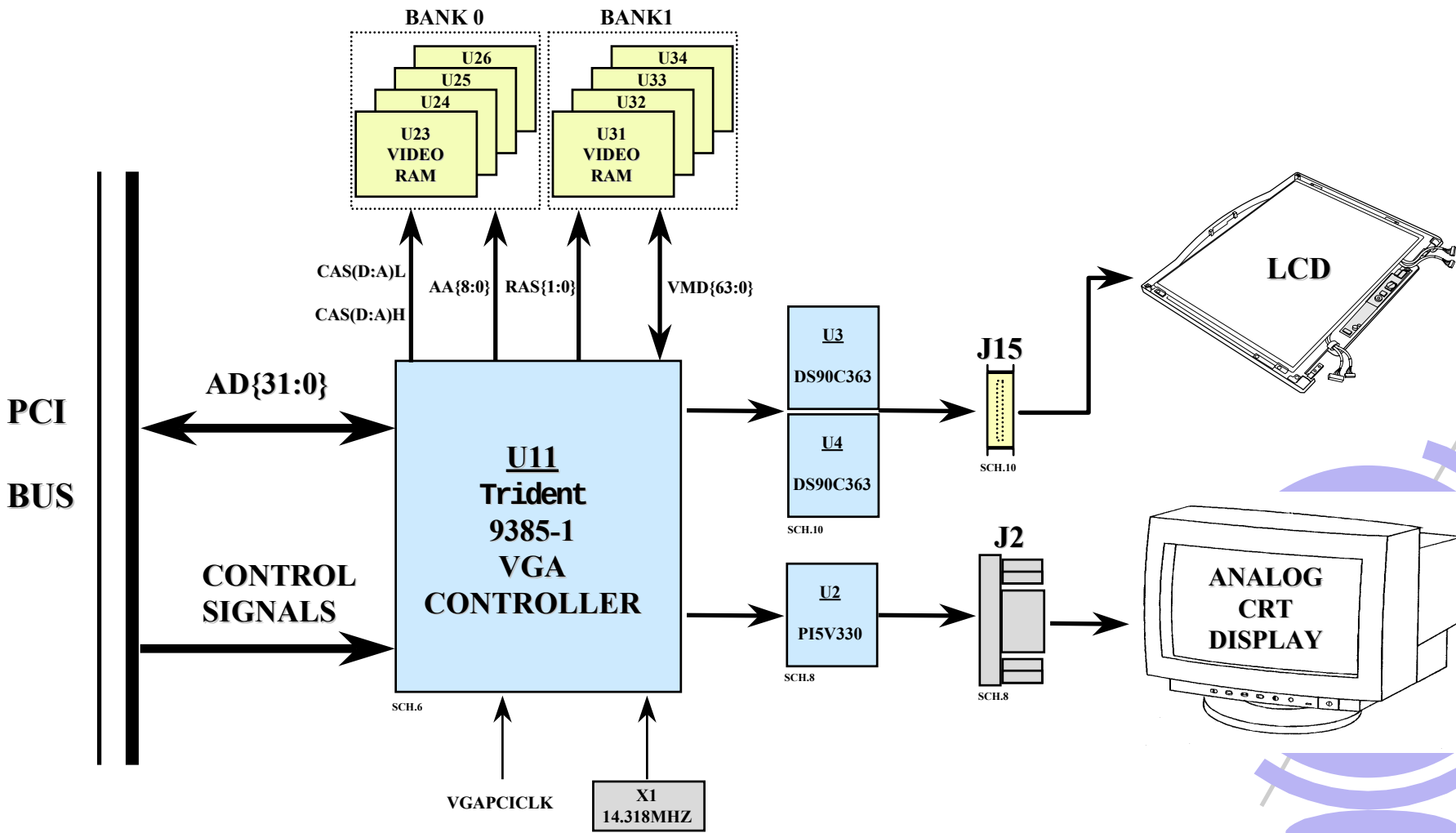




9.3 VGA CONTROLLER FAILURE

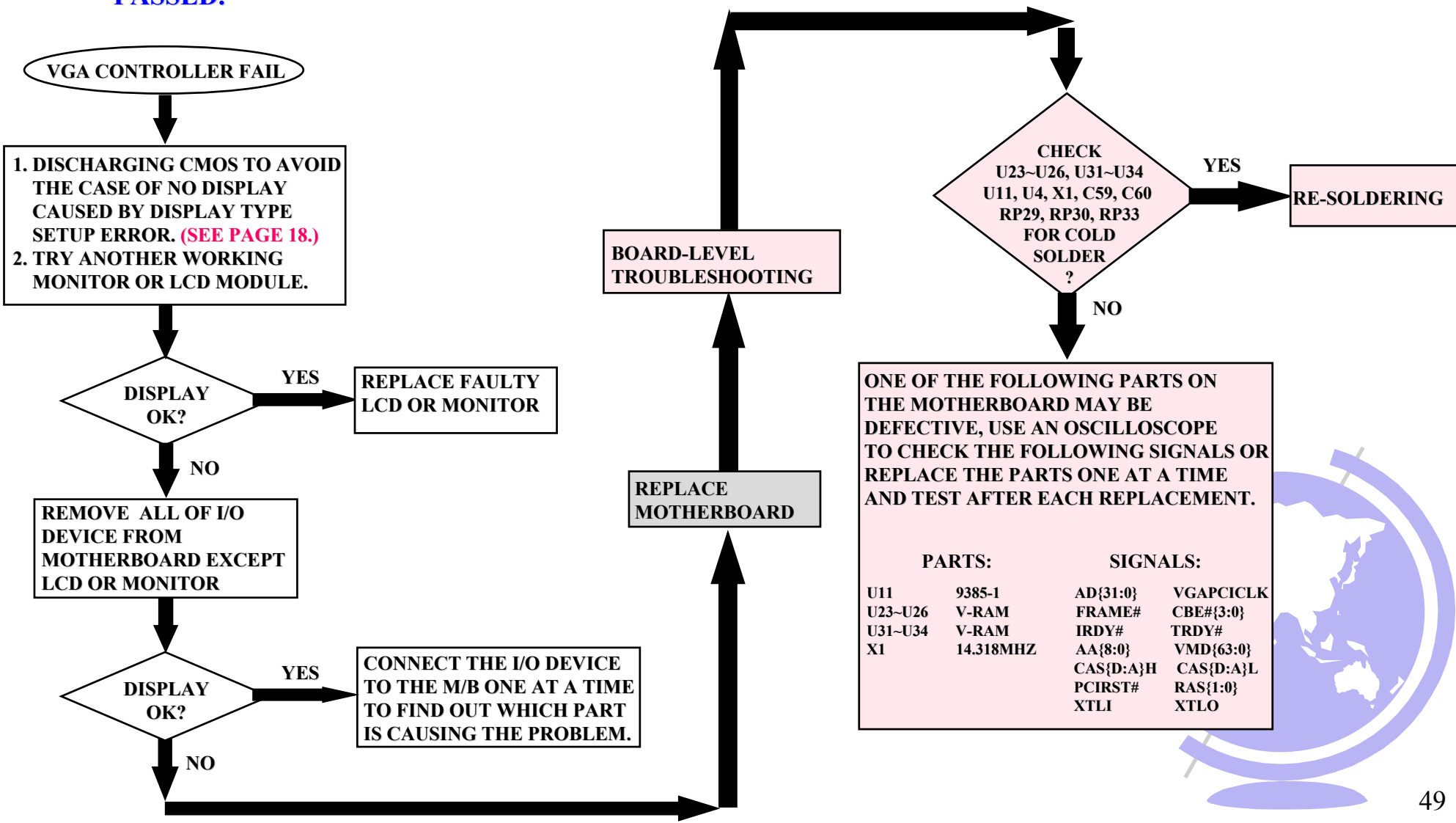
SYMPTOM:

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



9.3 VGA CONTROLLER FAILURE

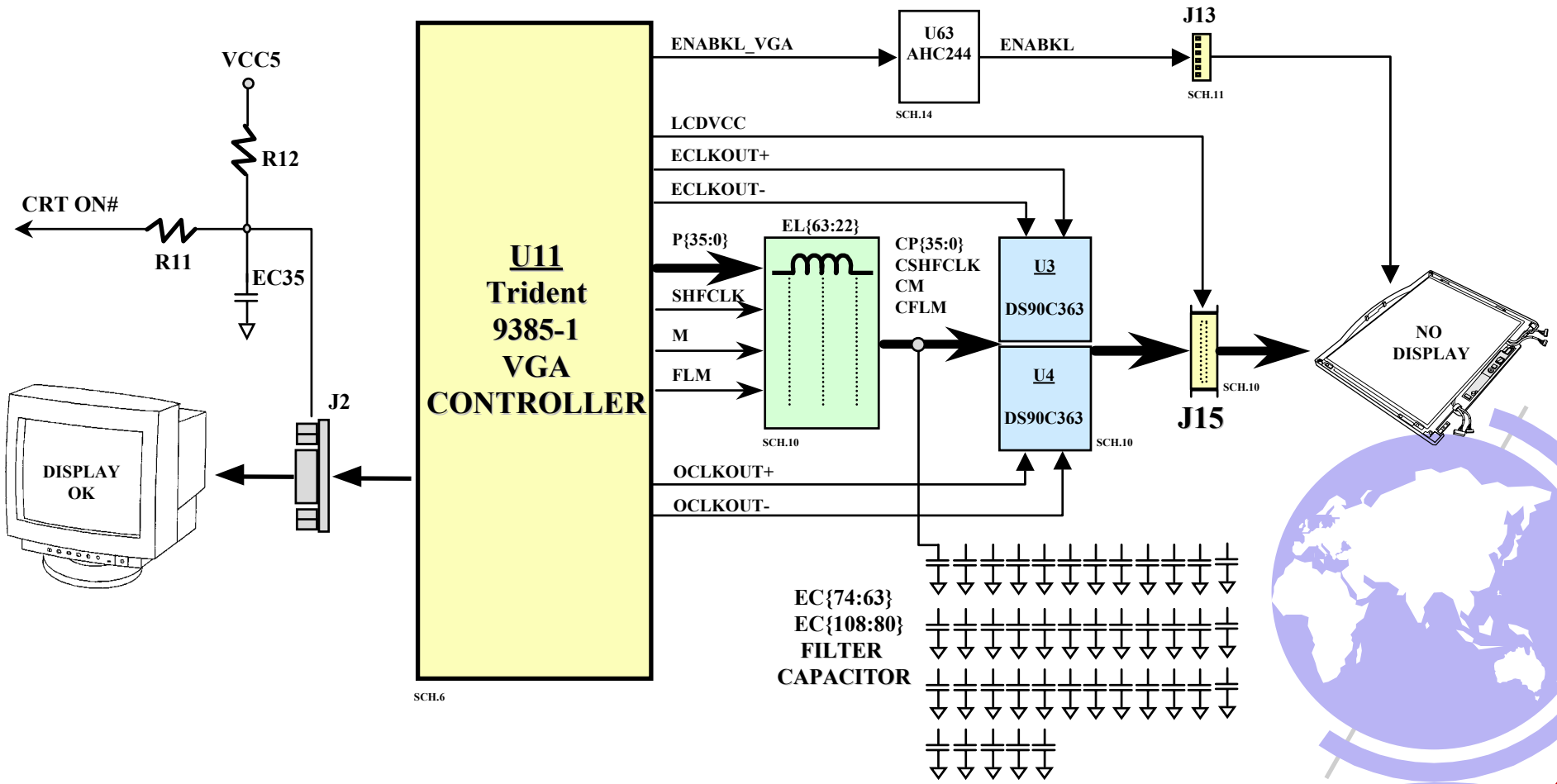
SYMPTOM:
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

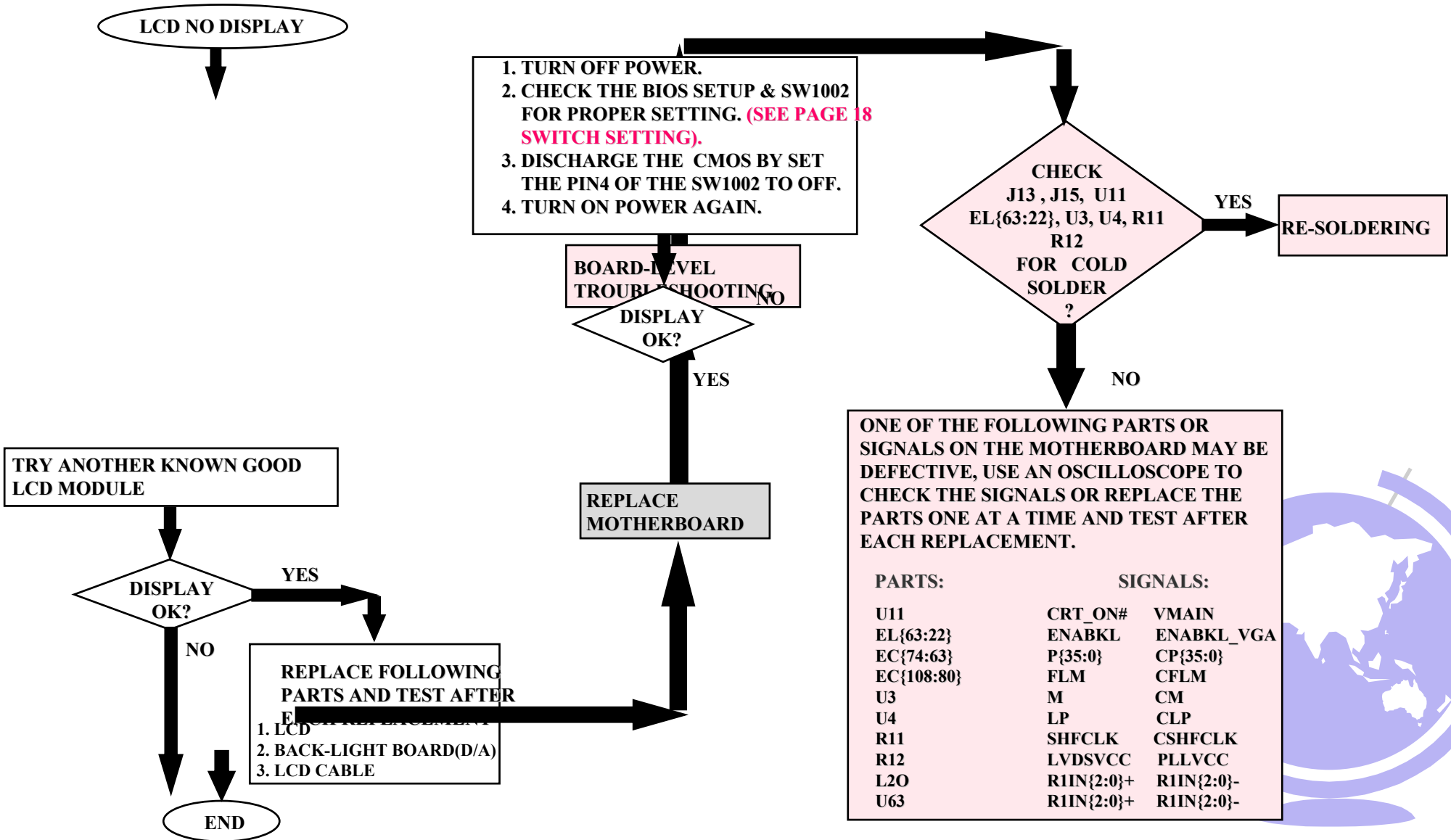
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

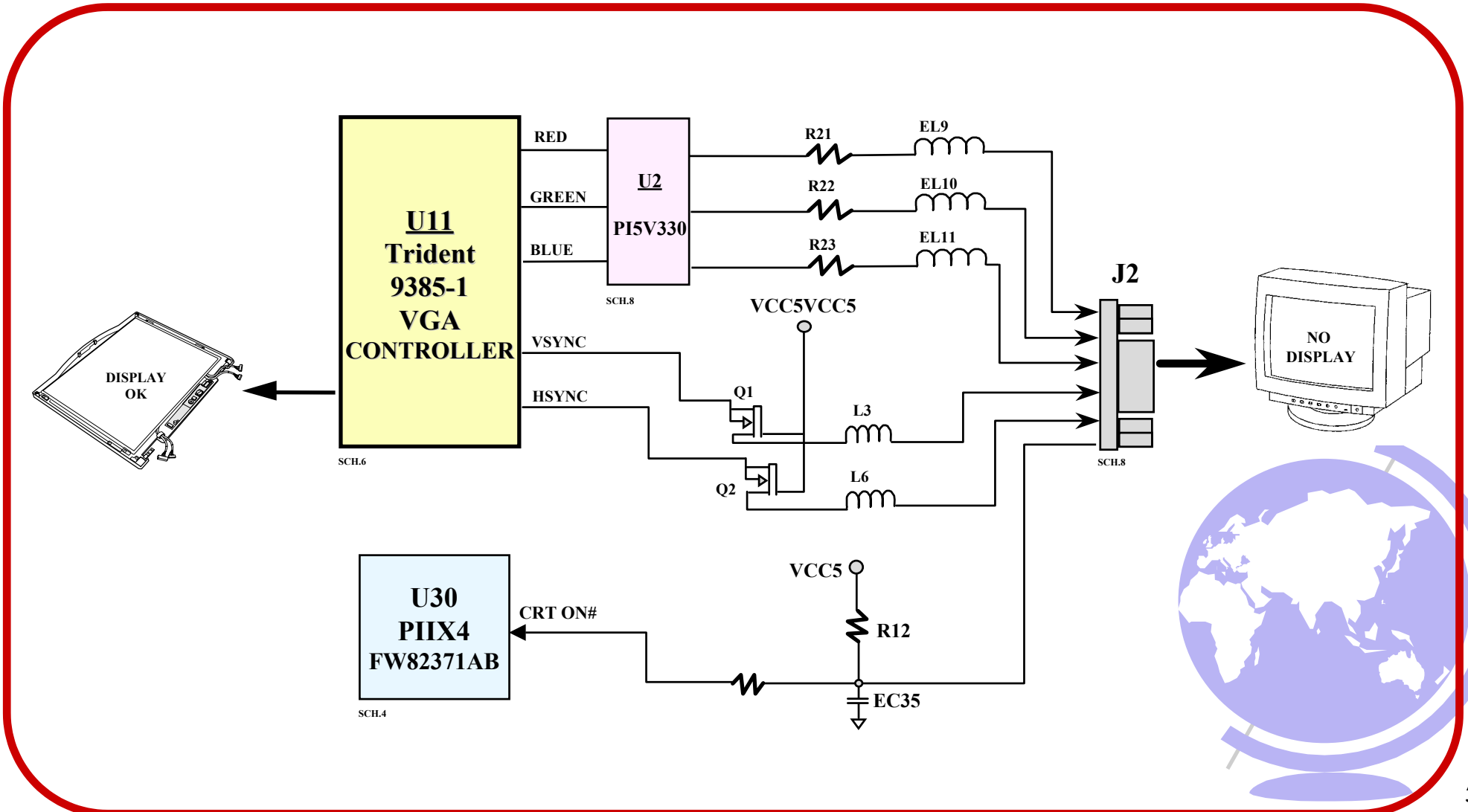
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

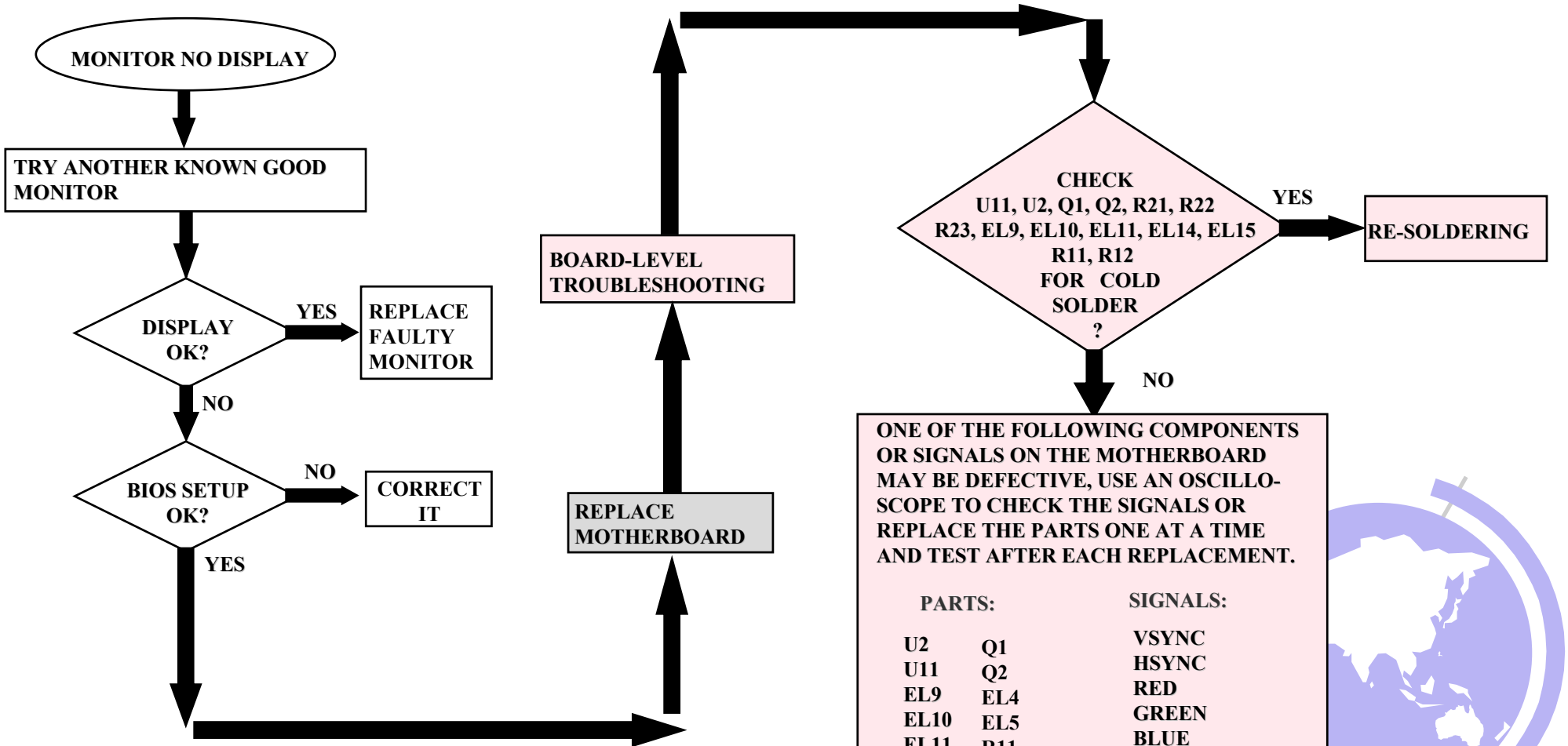
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

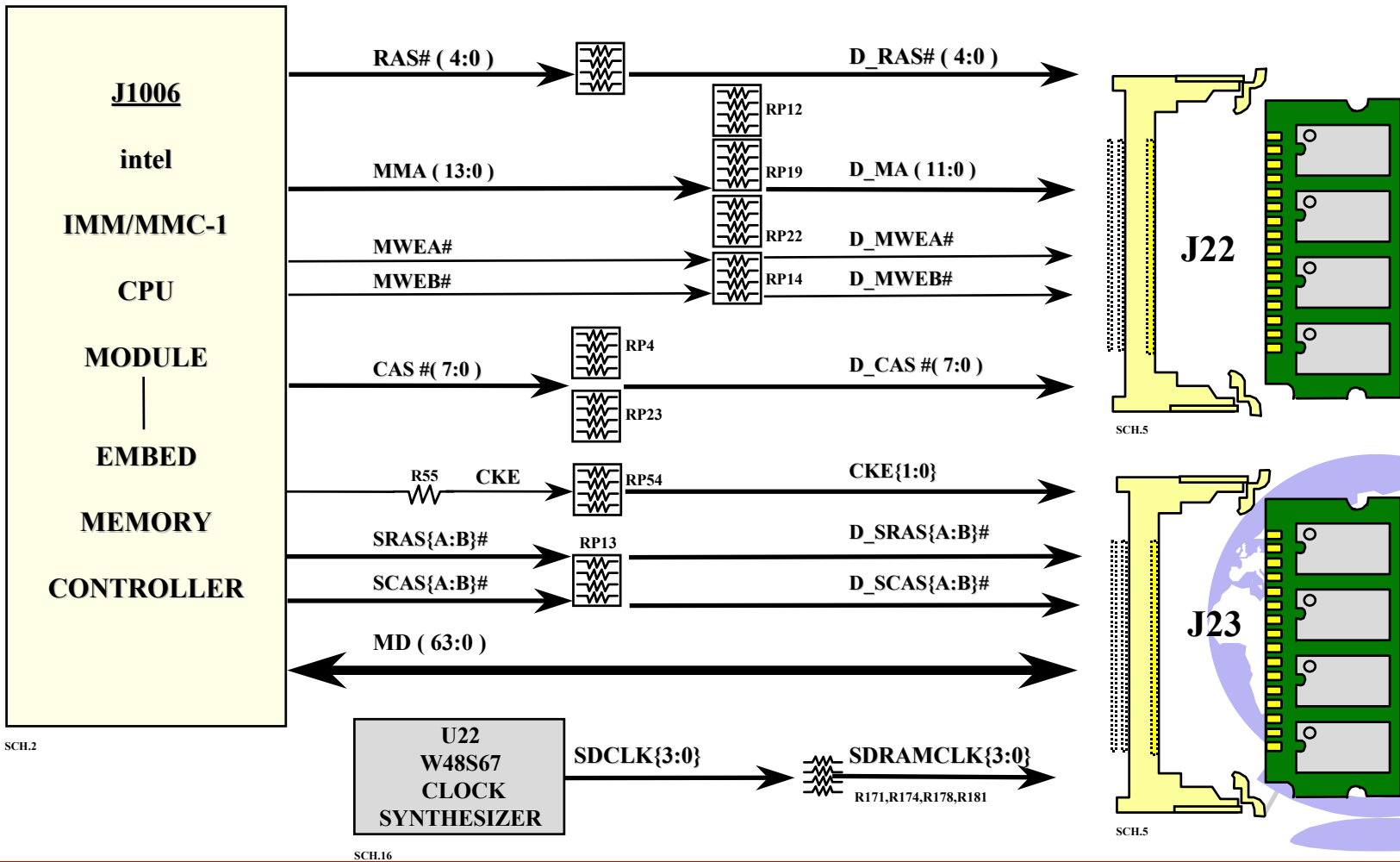
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



9.6 MEMORY TEST ERROR

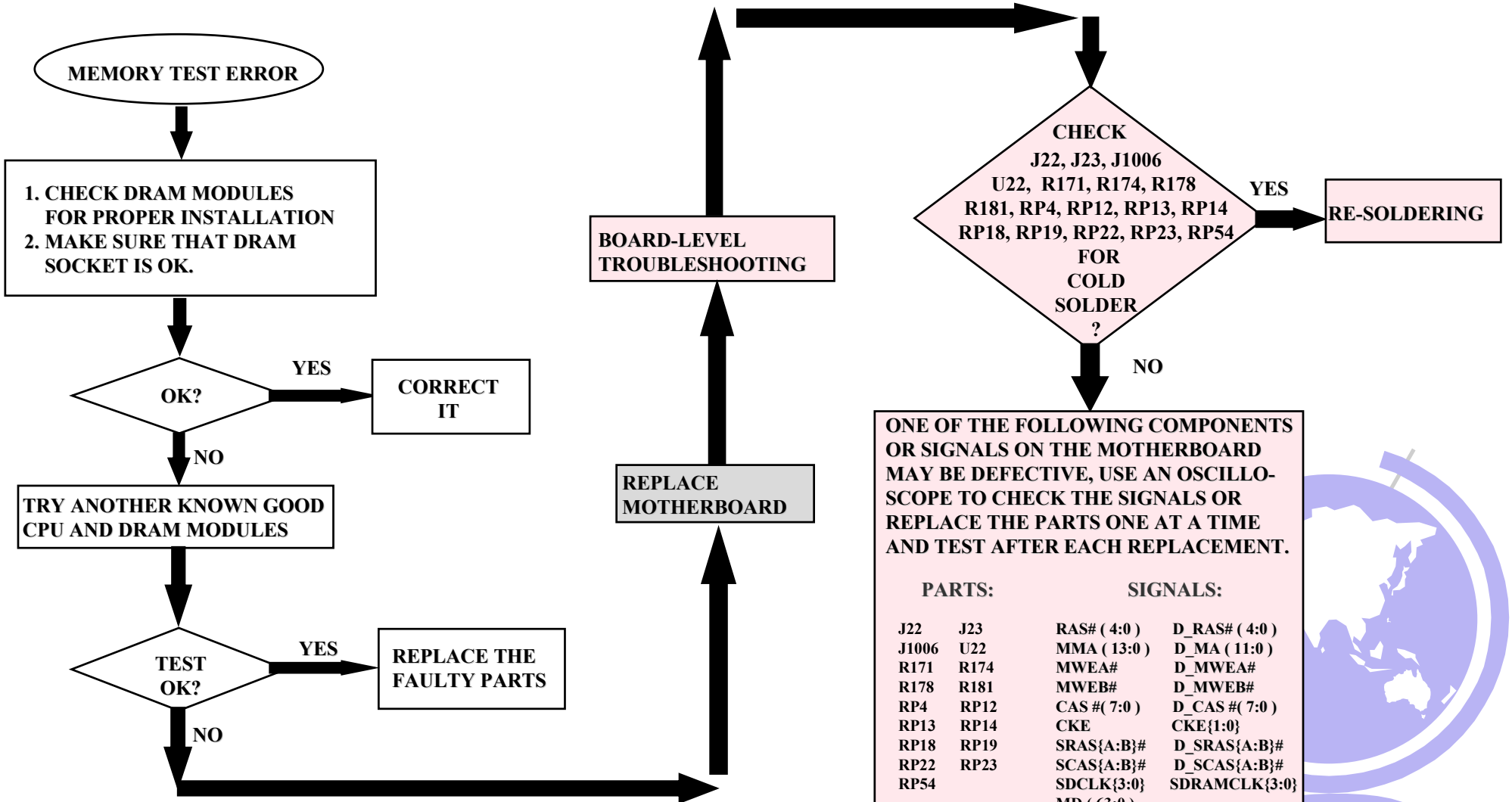
SYMPTOM:

PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



9.6 MEMORY TEST ERROR

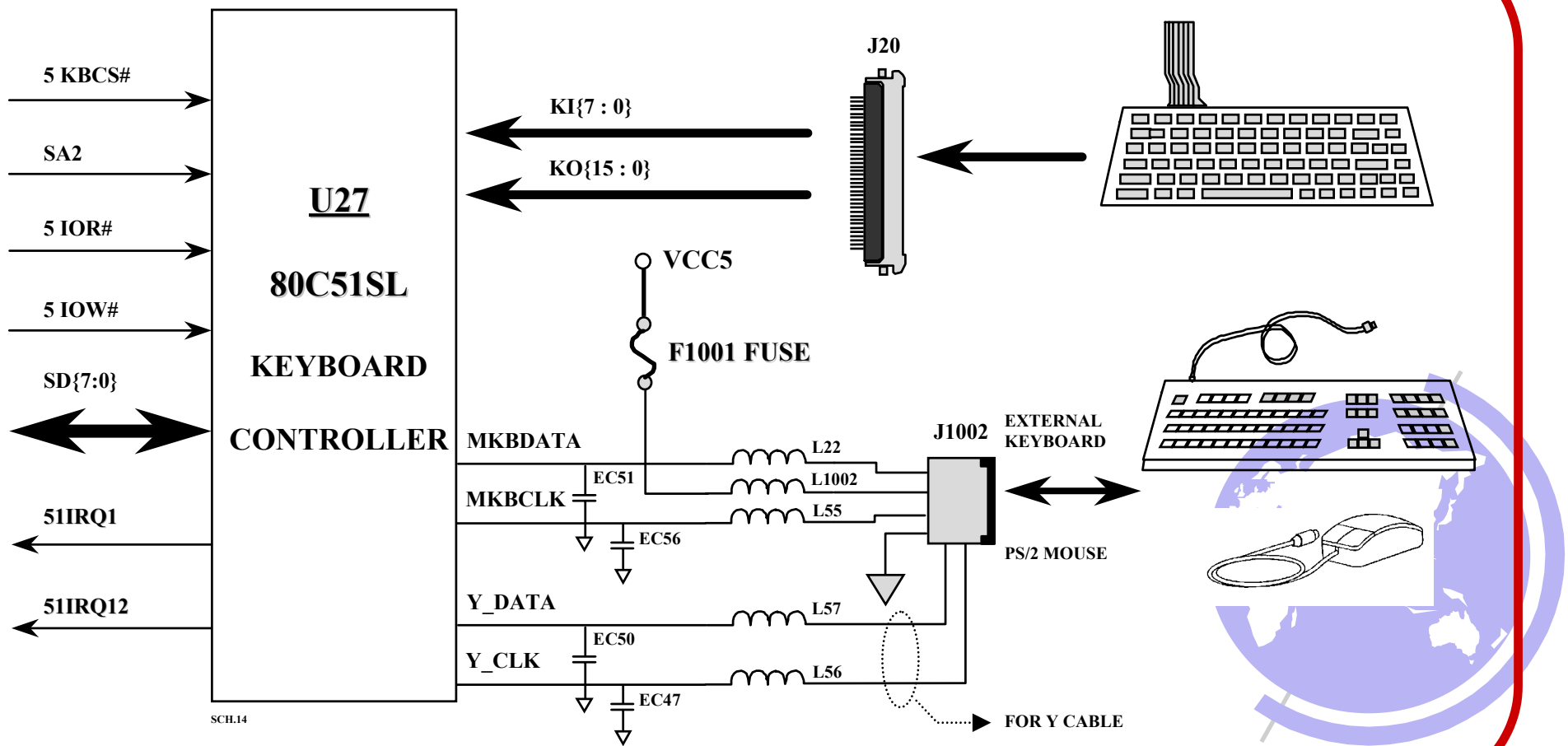
SYMPTOM:
PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



9.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

SYMPTOM:

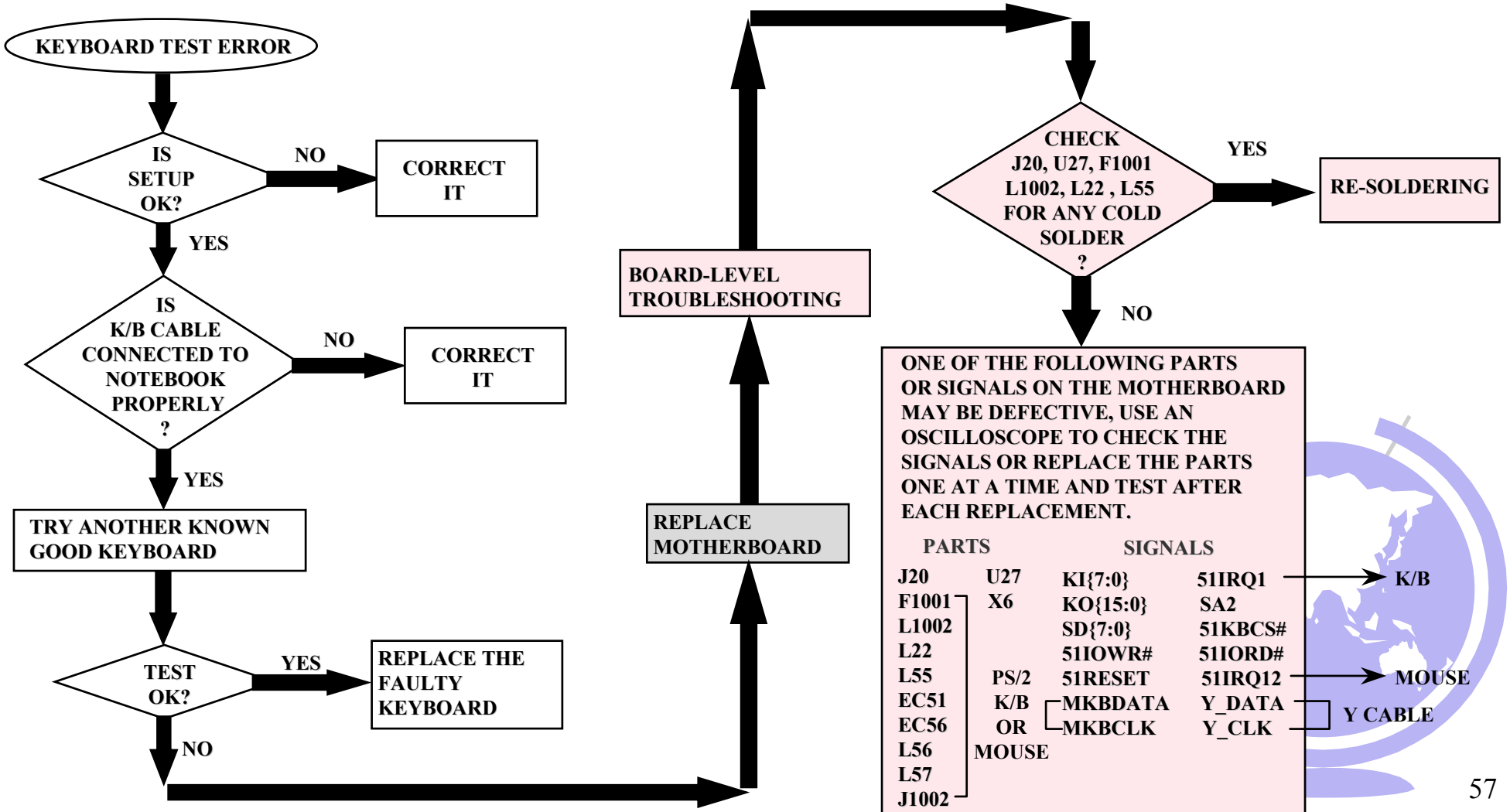
1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 21H.



9.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

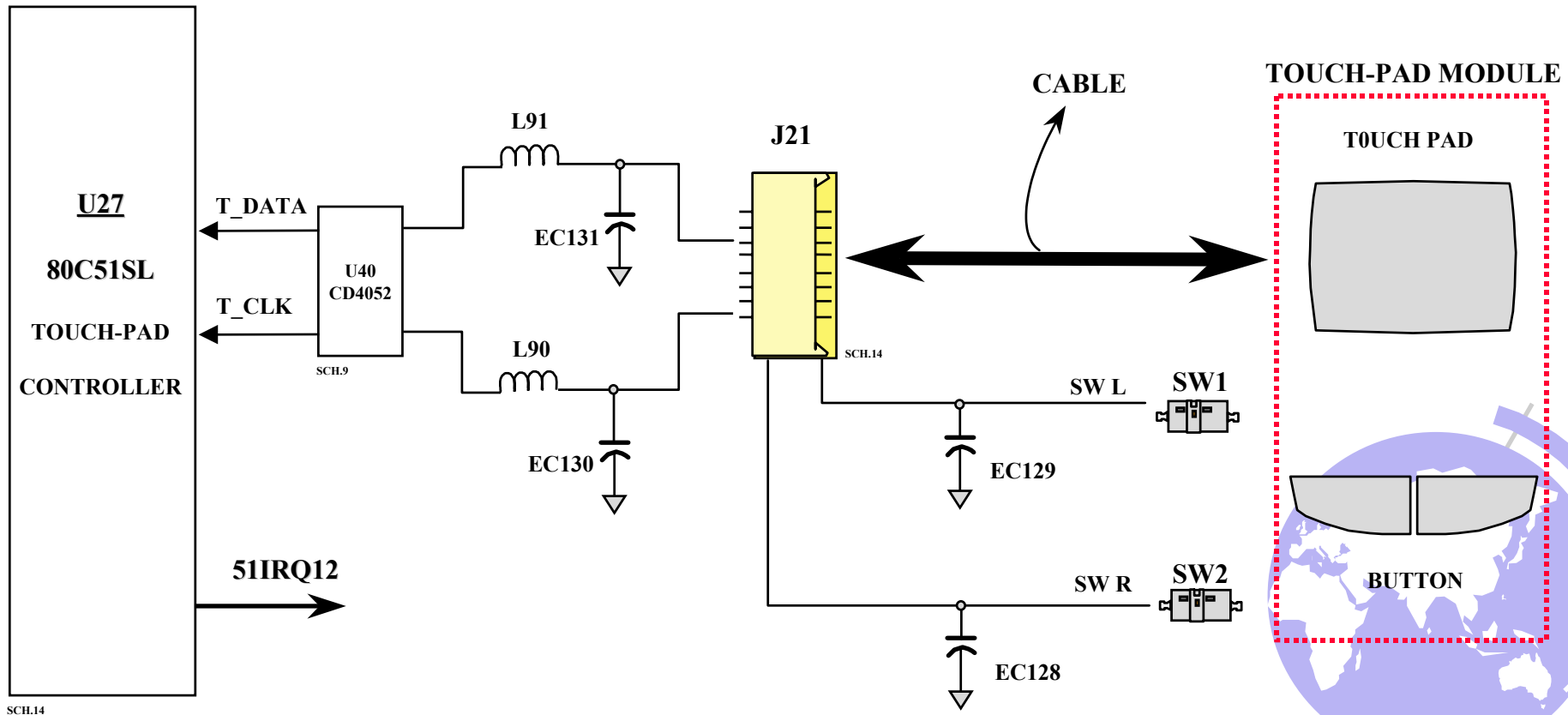
SYMPTOM:

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 21H.



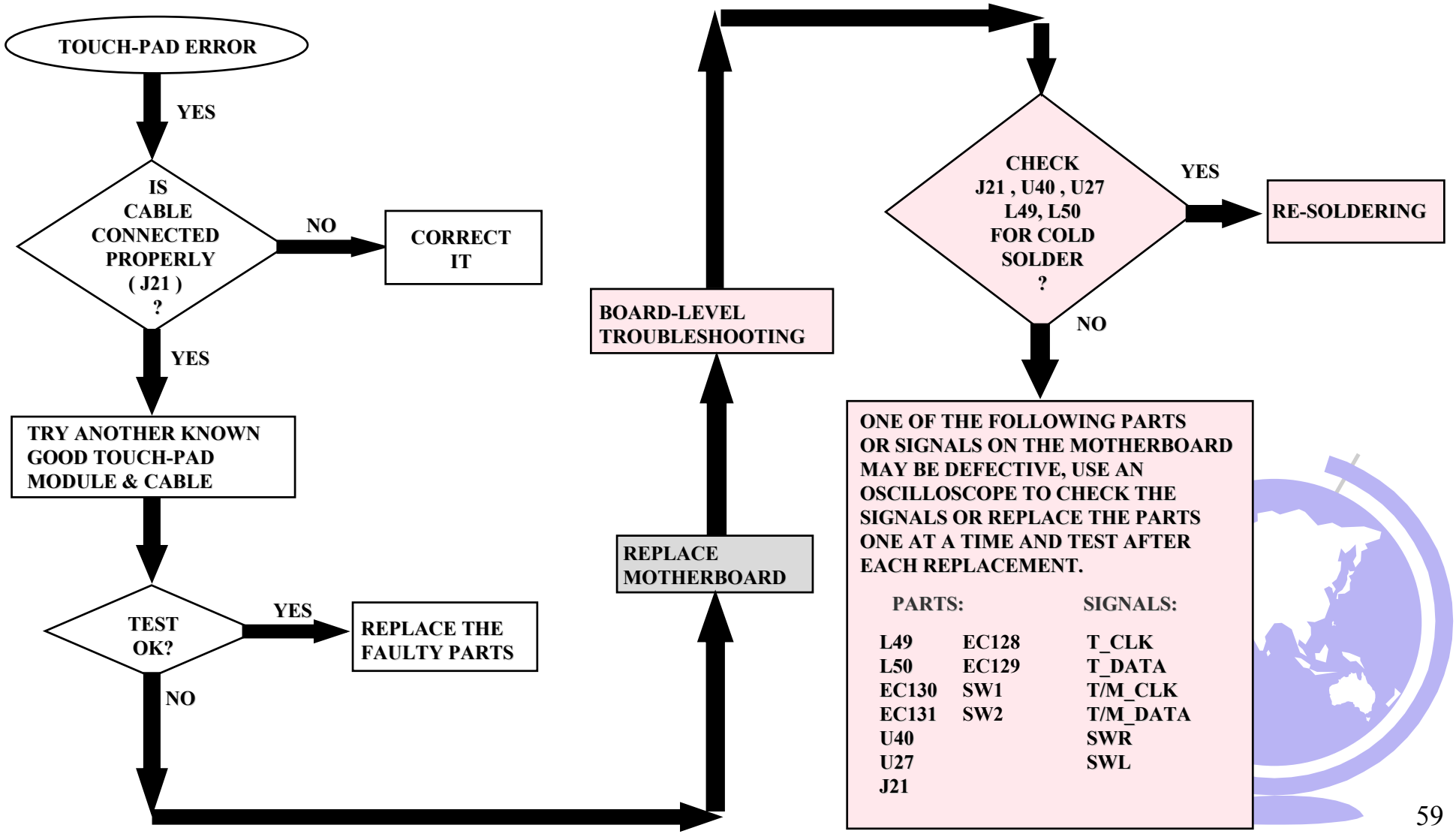
9.8 TOUCH-PAD TEST ERROR

SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



9.8 TOUCH-PAD TEST ERROR

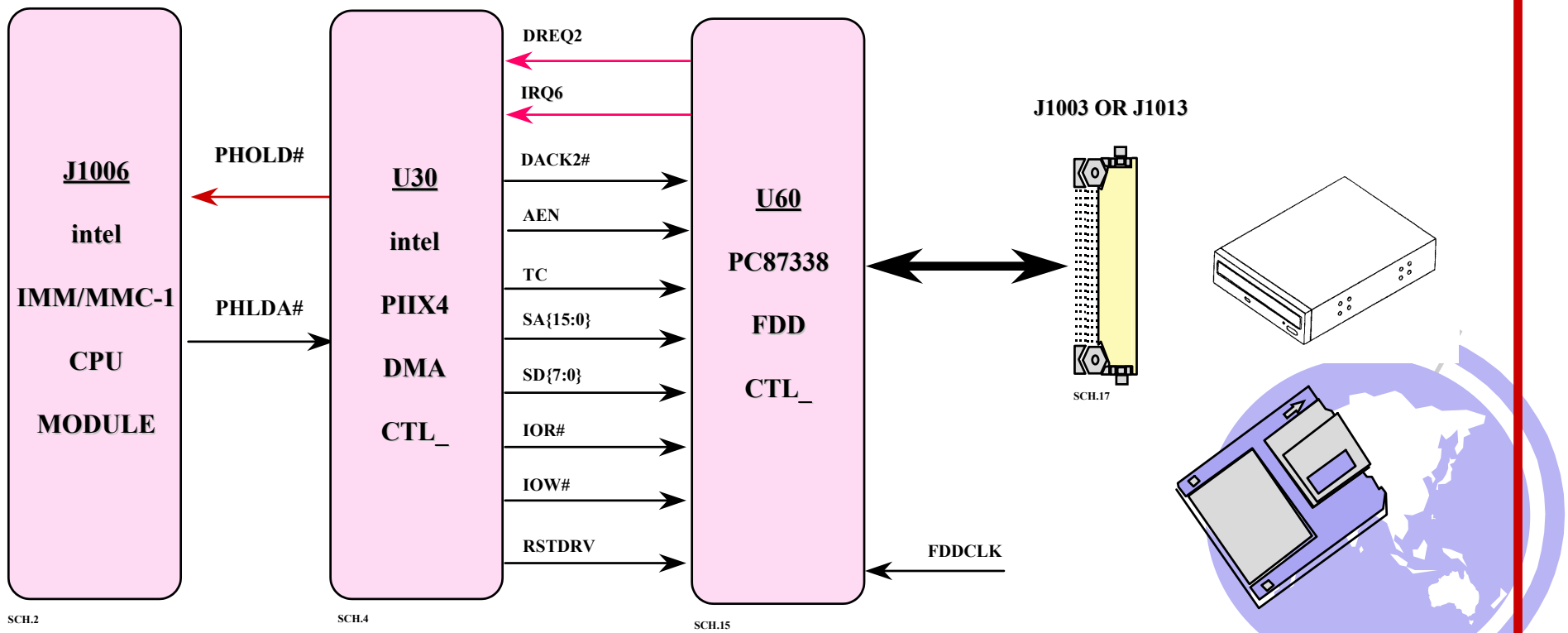
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



9.9 DISKETTE DRIVE TEST ERROR

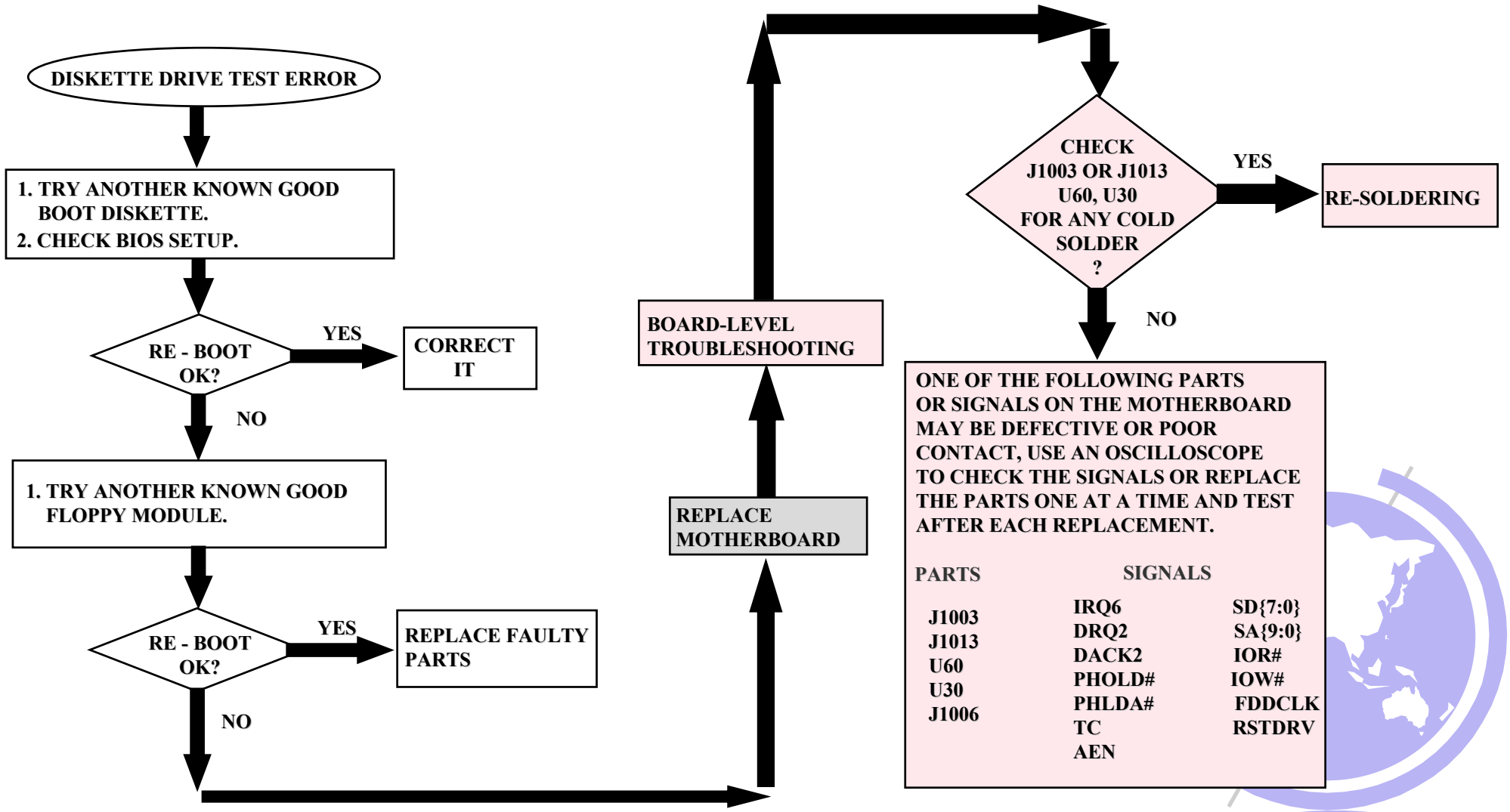
SYMPTOM:

AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



9.9 DISKETTE DRIVE TEST ERROR

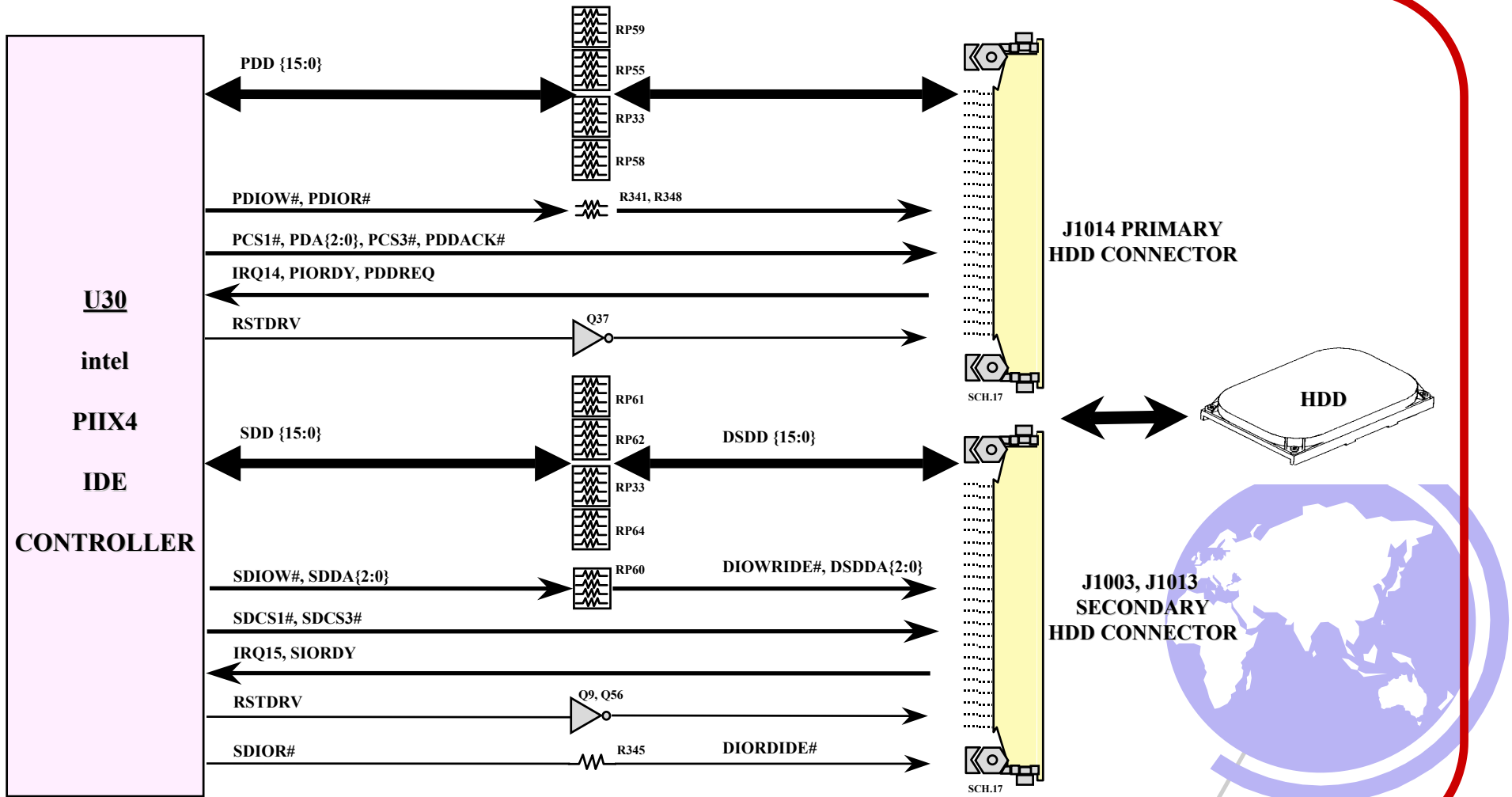
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



9.10 HARD DRIVE TEST ERROR

SYMPTOM:

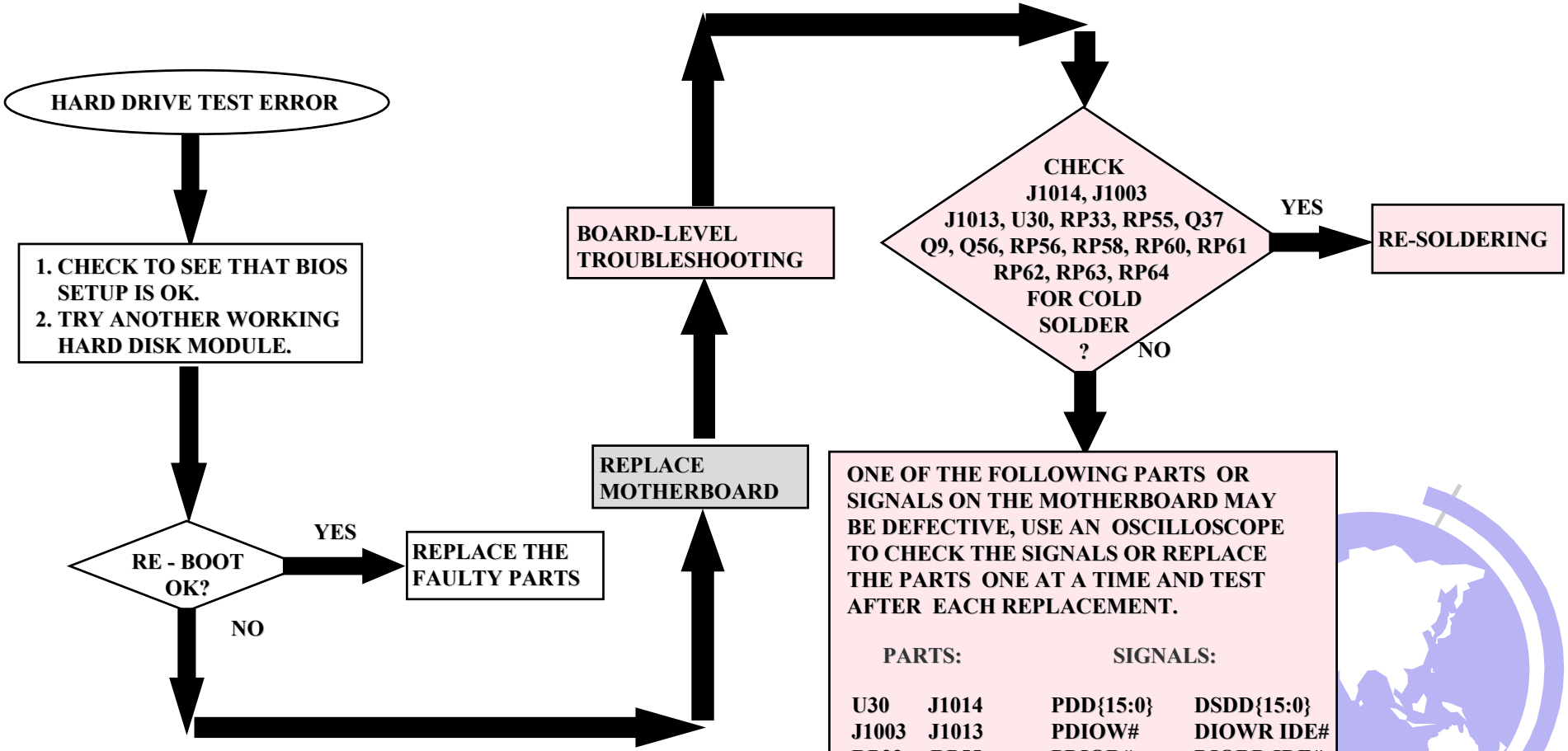
EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



9.10 HARD DRIVE TEST ERROR

SYMPTOM:

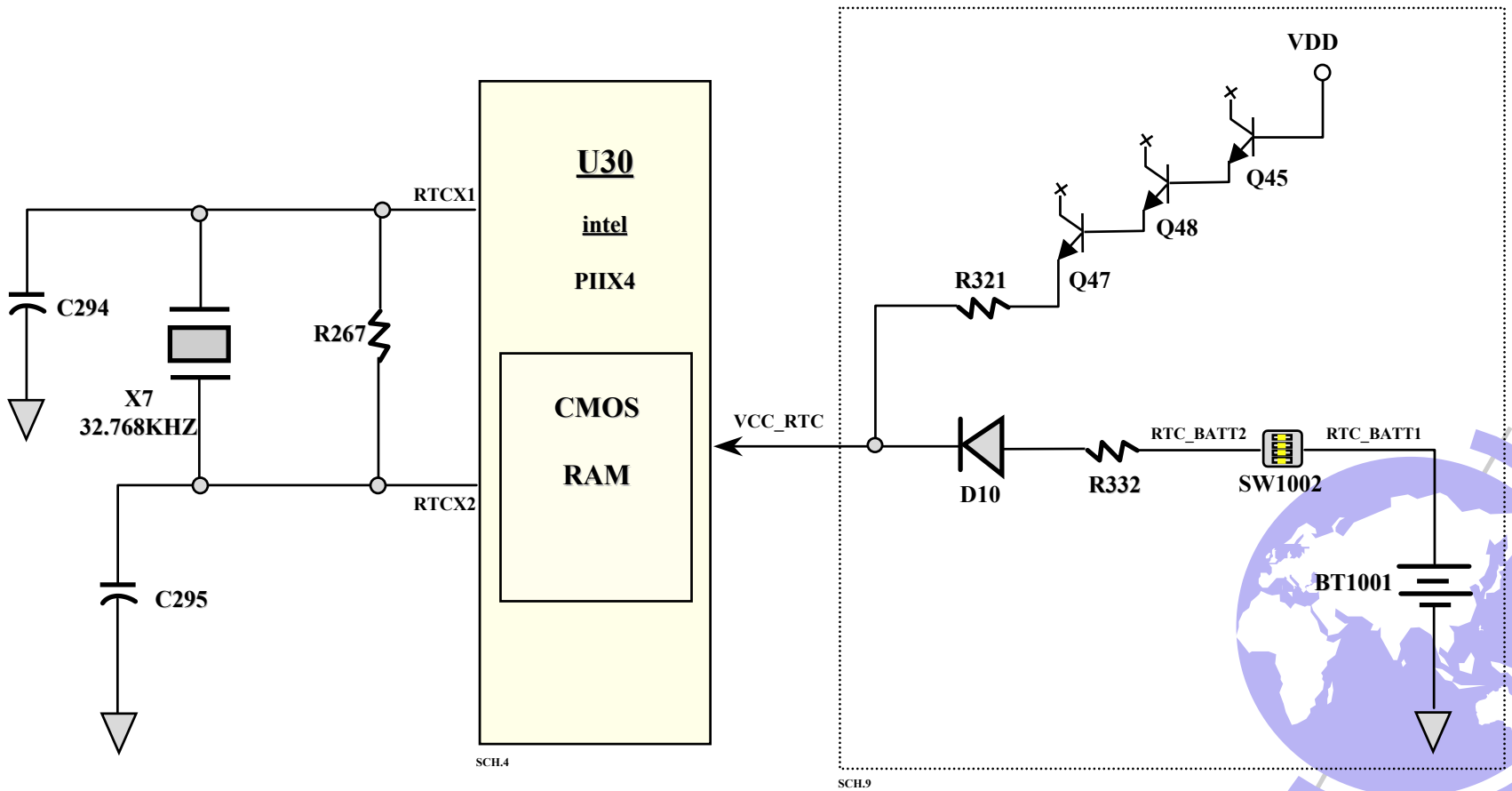
EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



9.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.

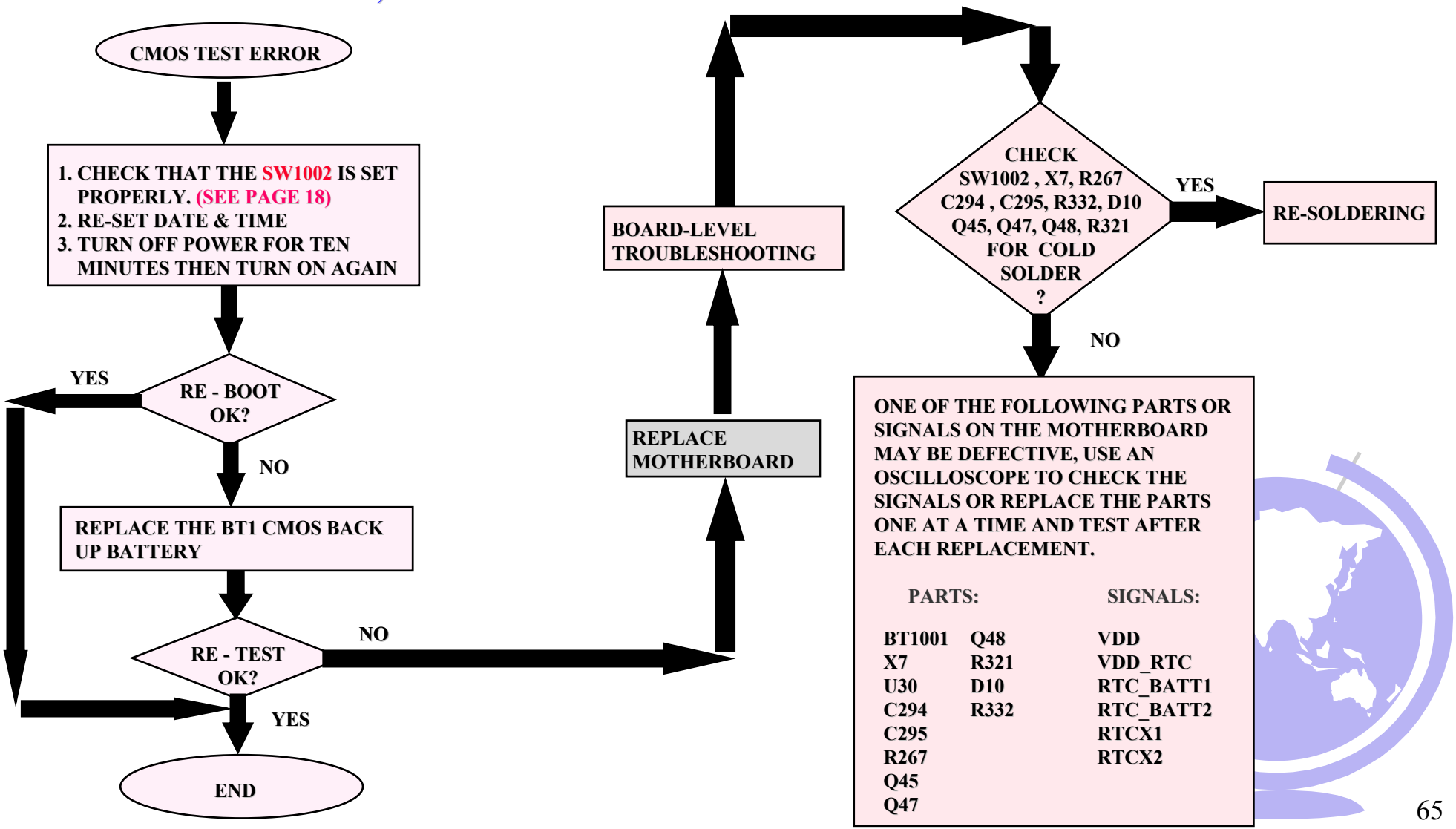


9.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.

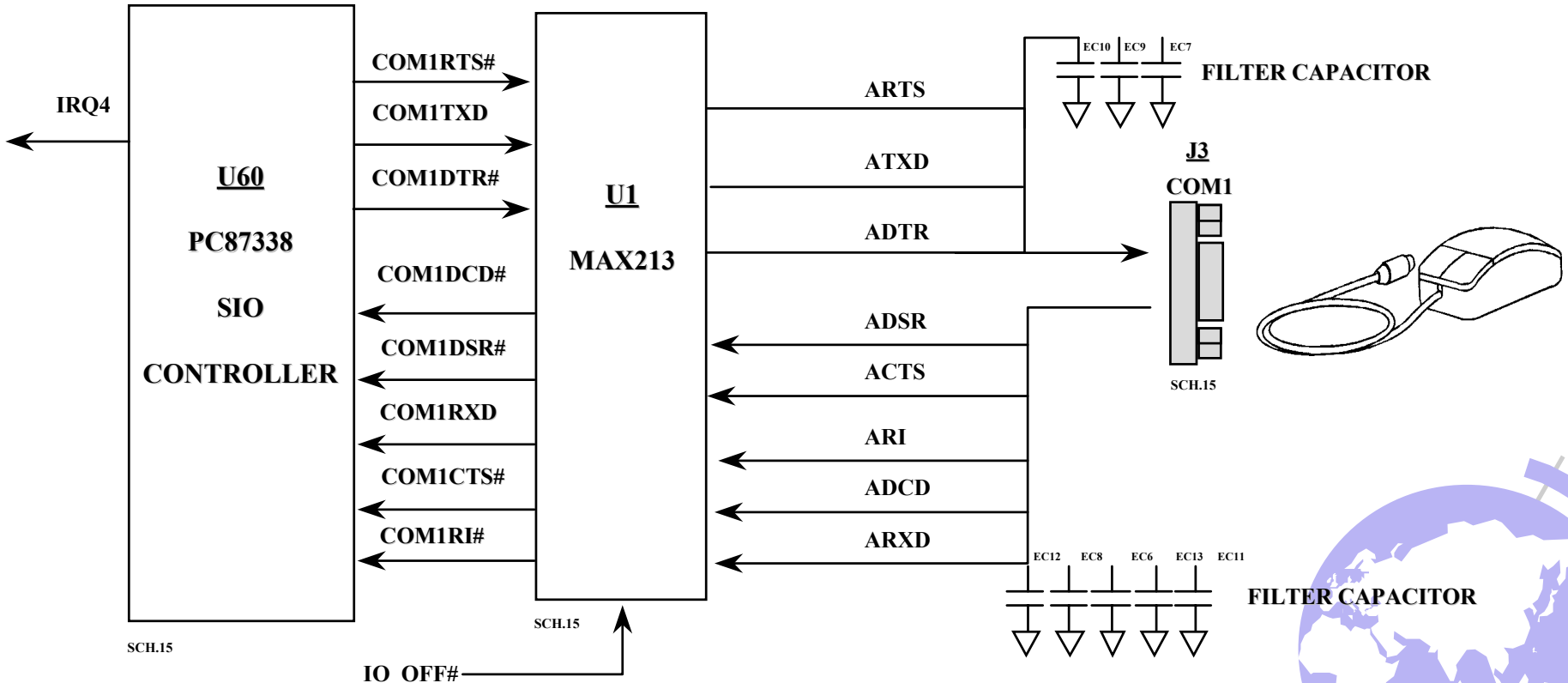
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.



9.12 SIO PORT TEST ERROR

SYMPTON:

ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

PIN 1	DCD	DATA CARRIER DETECT	PIN 6	DSR	DATA SET READY
PIN 2	RD	RECEIVE DATA	PIN 7	RTS	REQUEST TO SEND
PIN 3	TD	TRANSMIT DATA	PIN 8	CTS	CLEAR TO SEND
PIN 4	DTR	DATA TERMINAL READY	PIN 9	RI	RING INDICATOR
PIN 5	SG	SIGNAL GROUND			

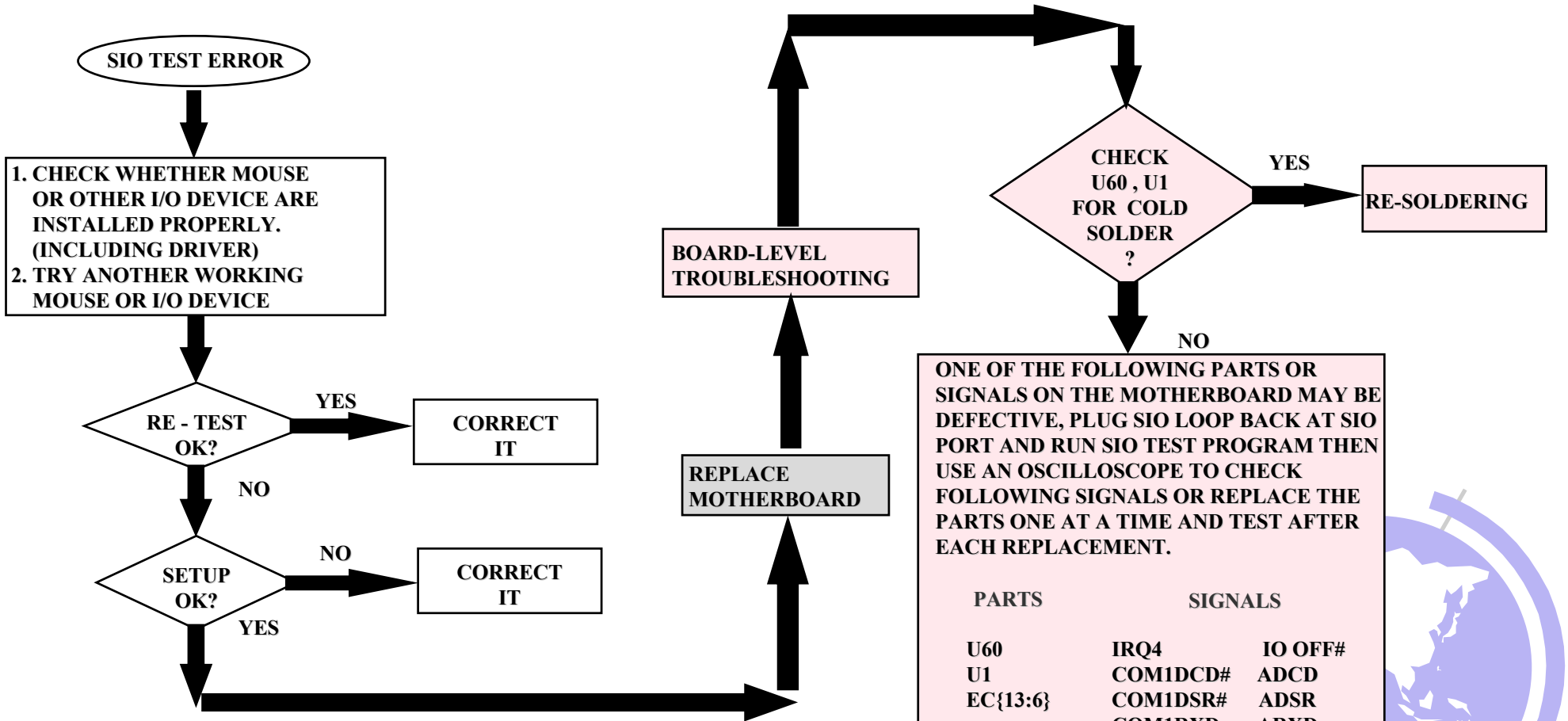
LOOPBACK CONNECTOR FOR SIO TEST:

PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

9.12 SIO PORT TEST ERROR

SYMPTON:

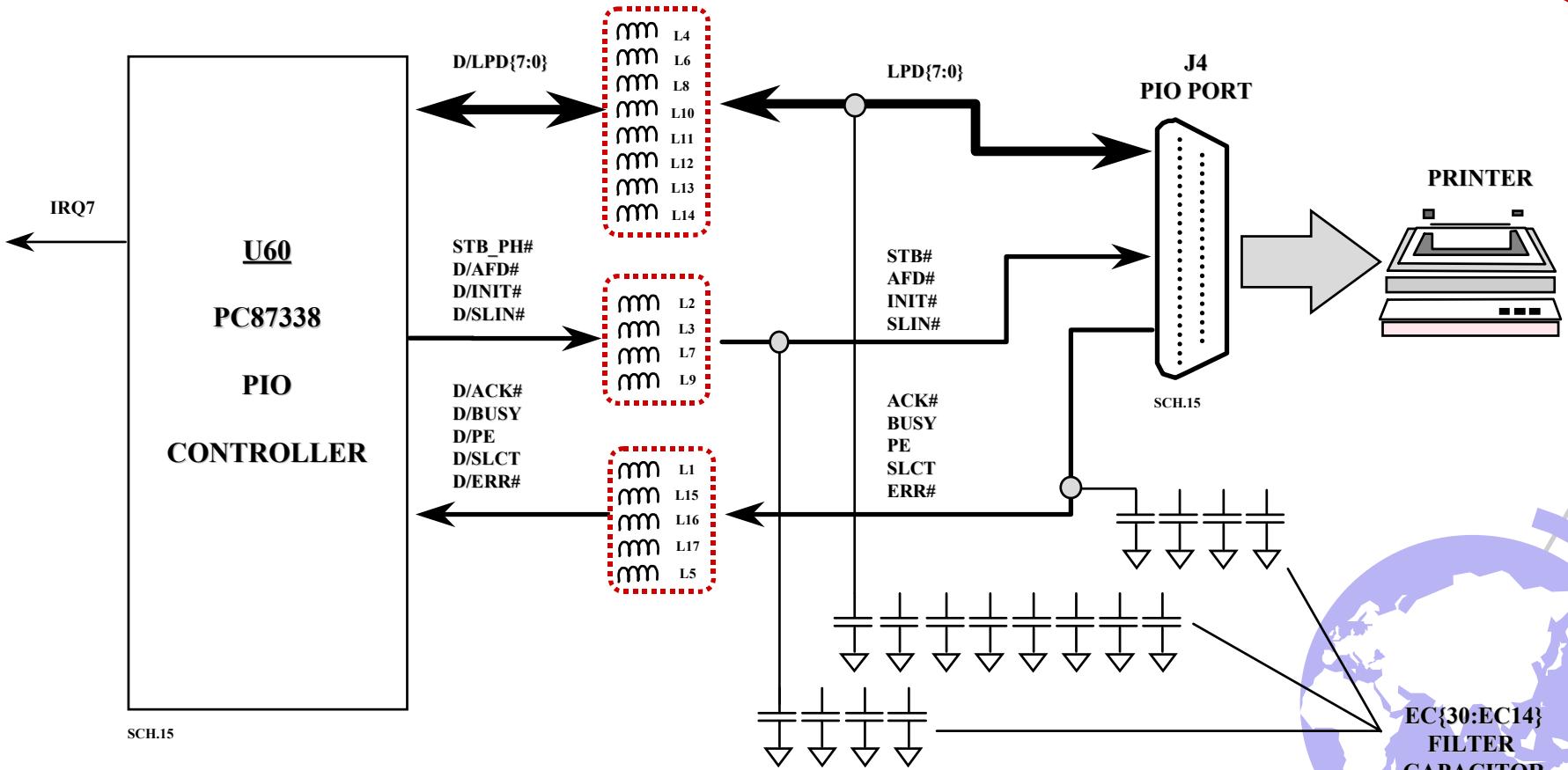
ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



9.13 PIO PORT TEST ERROR

SYMPTON:

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

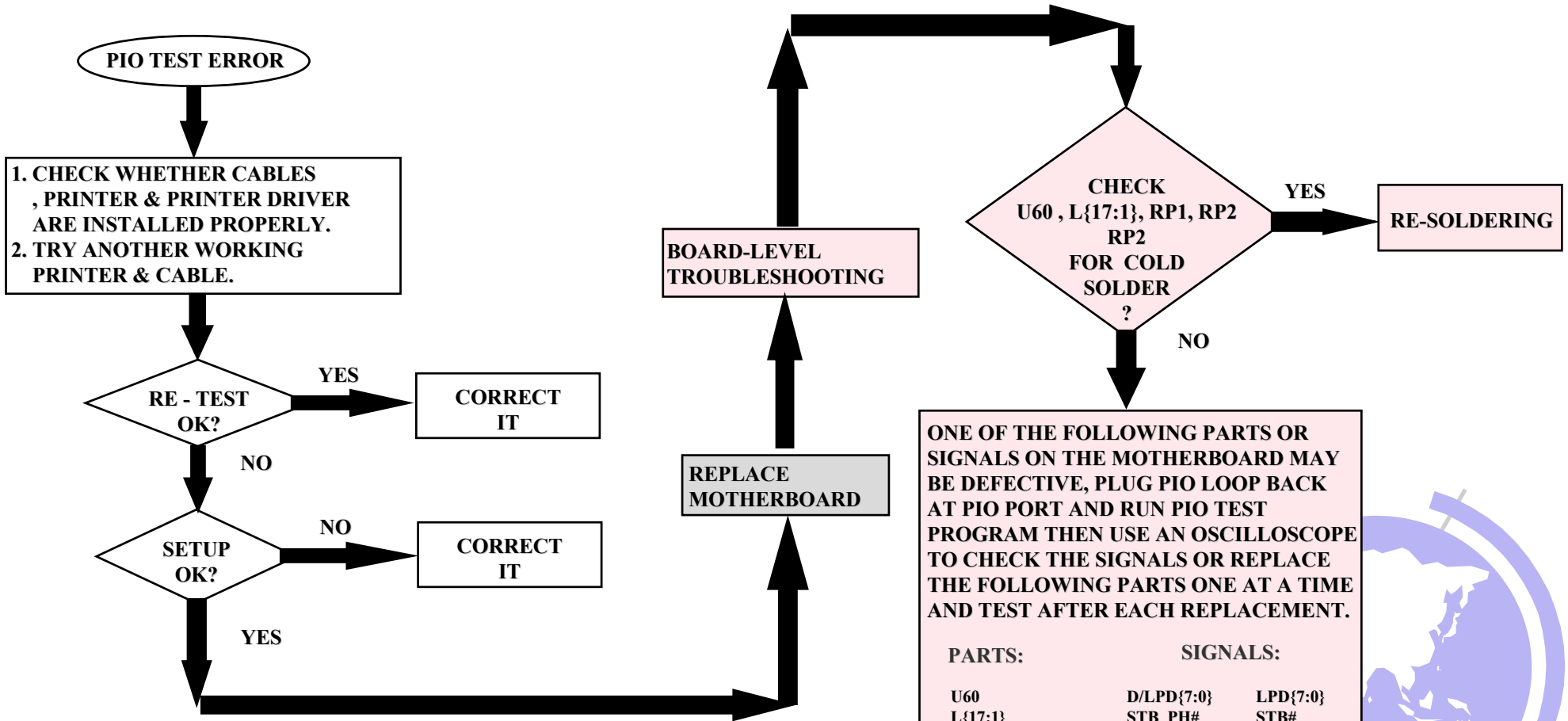
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

9.13 PIO PORT TEST ERROR

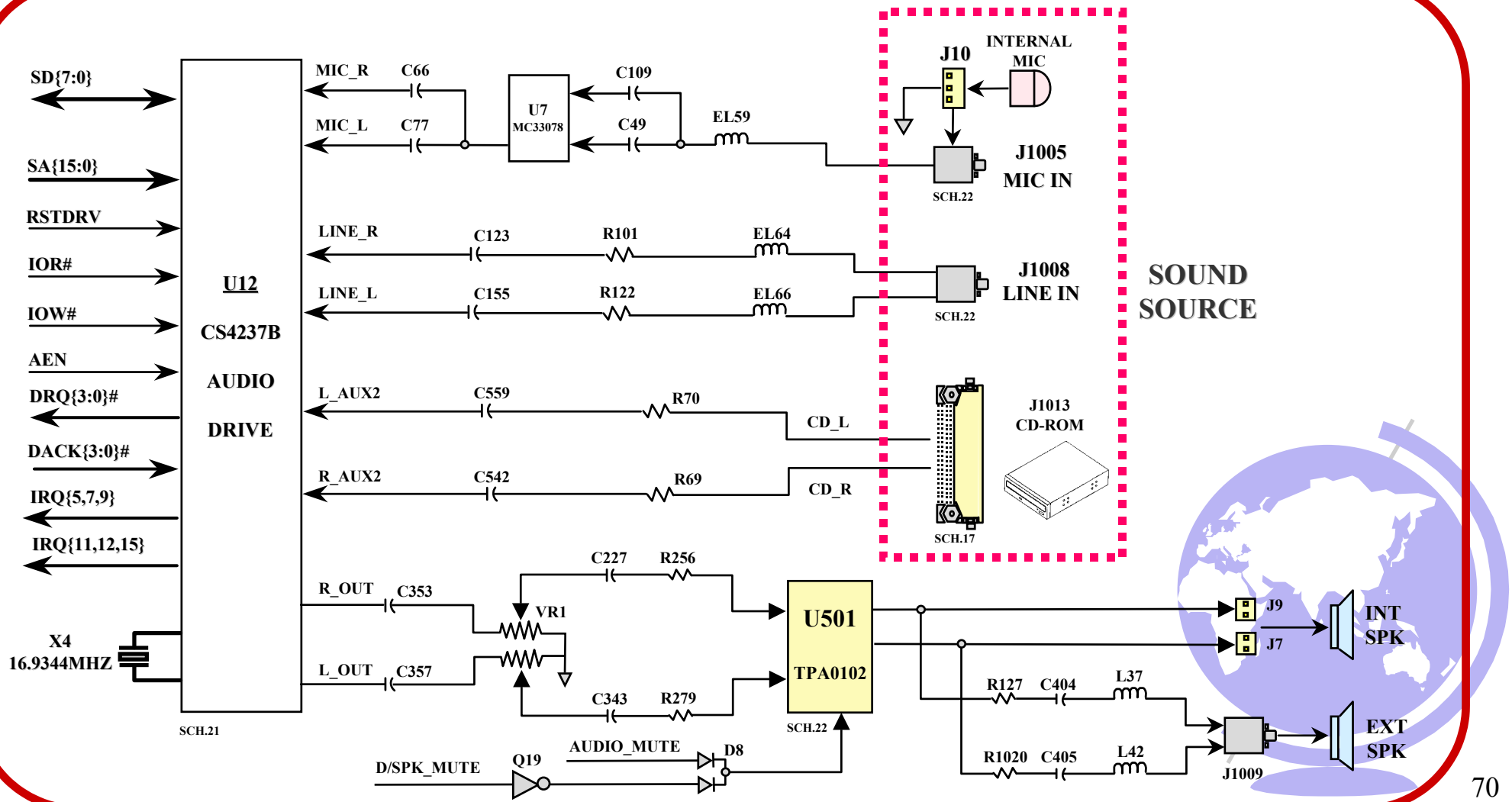
SYMPTON:
WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



9.14 AUDIO DRIVE FAILURE

SYMPTON:

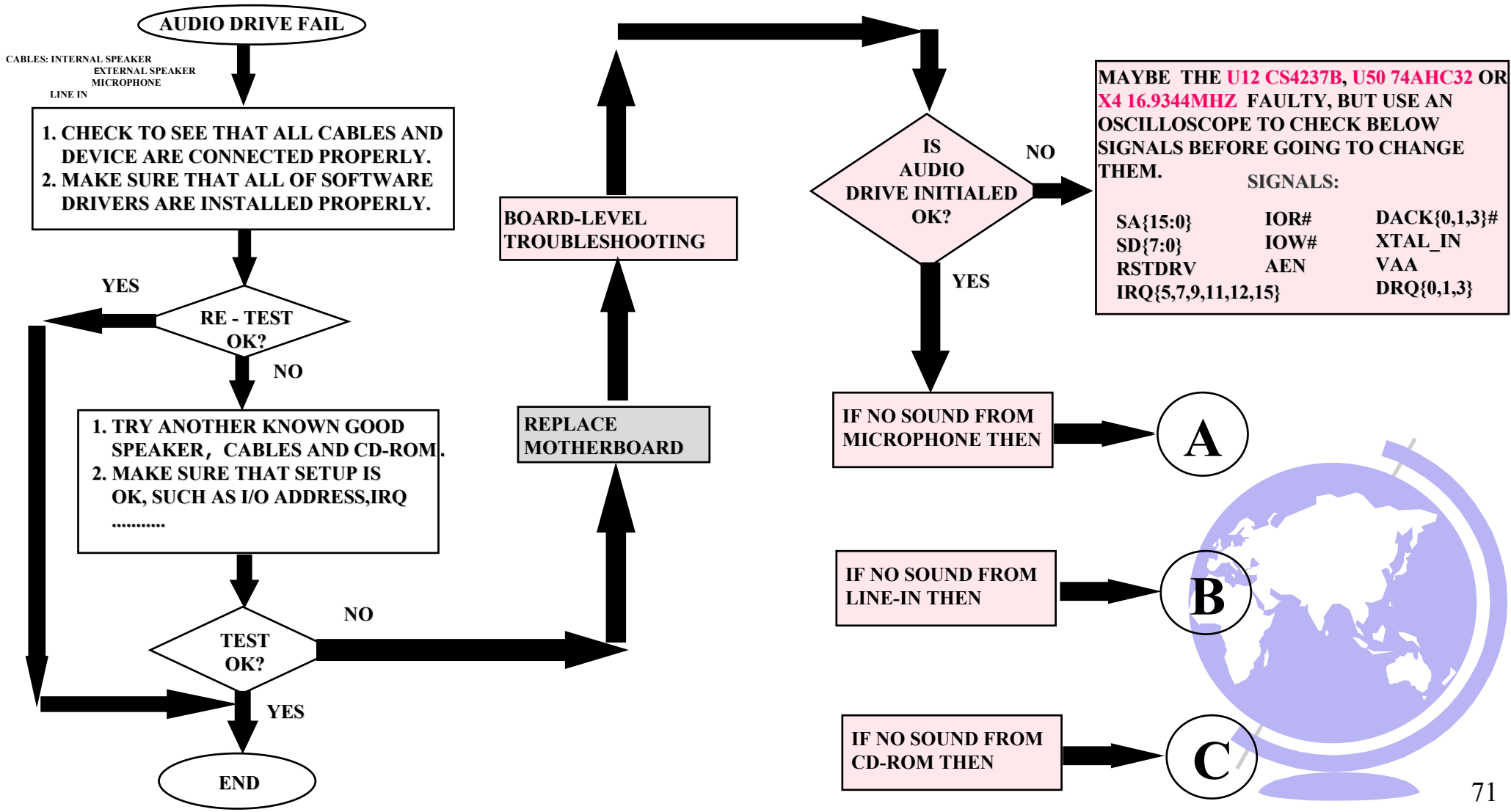
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND LINE IN.



9.14 AUDIO DRIVE FAILURE

SYMPTON:

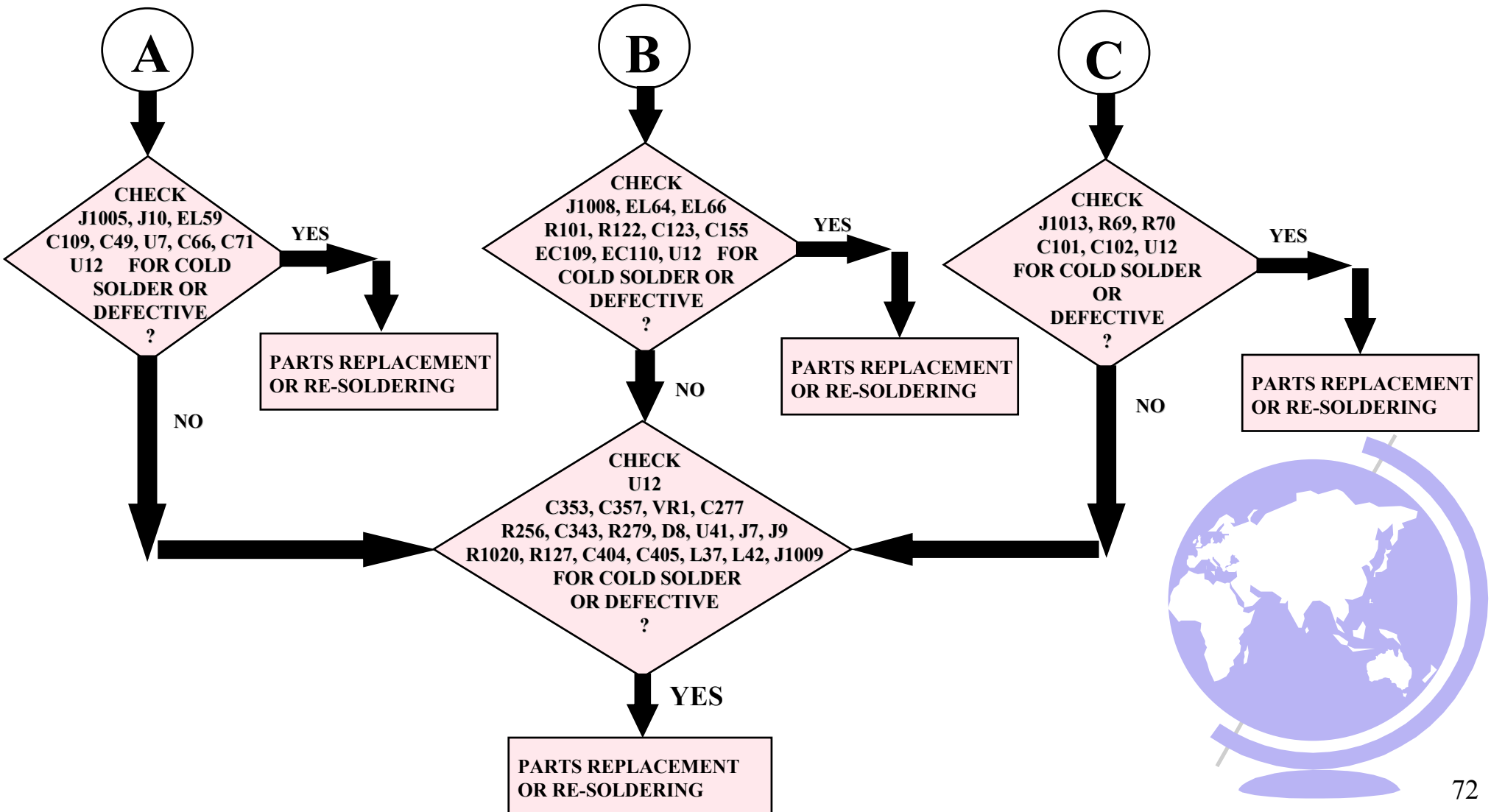
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND LINE IN.



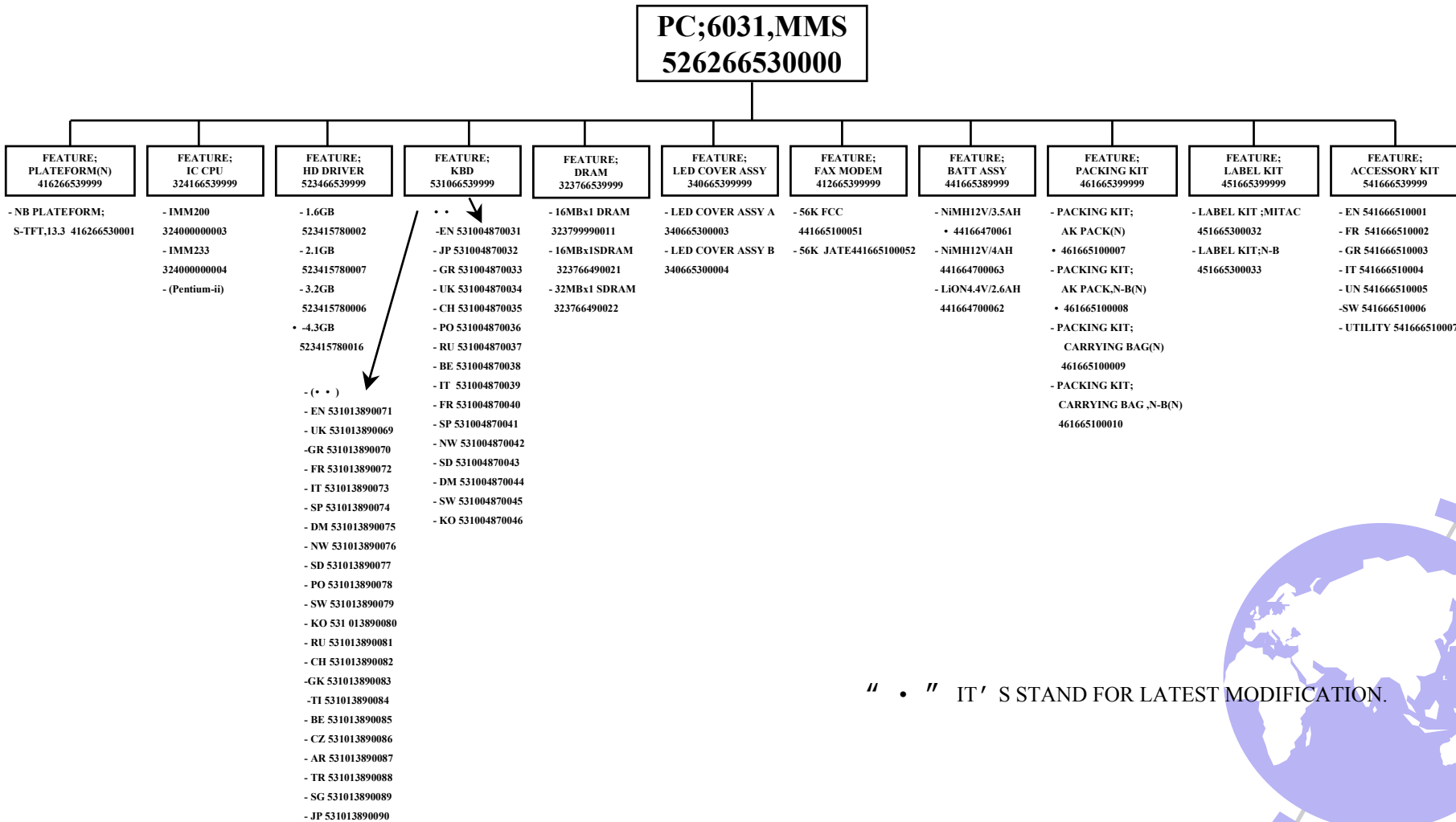
9.14 AUDIO DRIVE FAILURE

SYMPTON:

NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND LINE IN.



10. BOM TREE STRUCTURE(1)

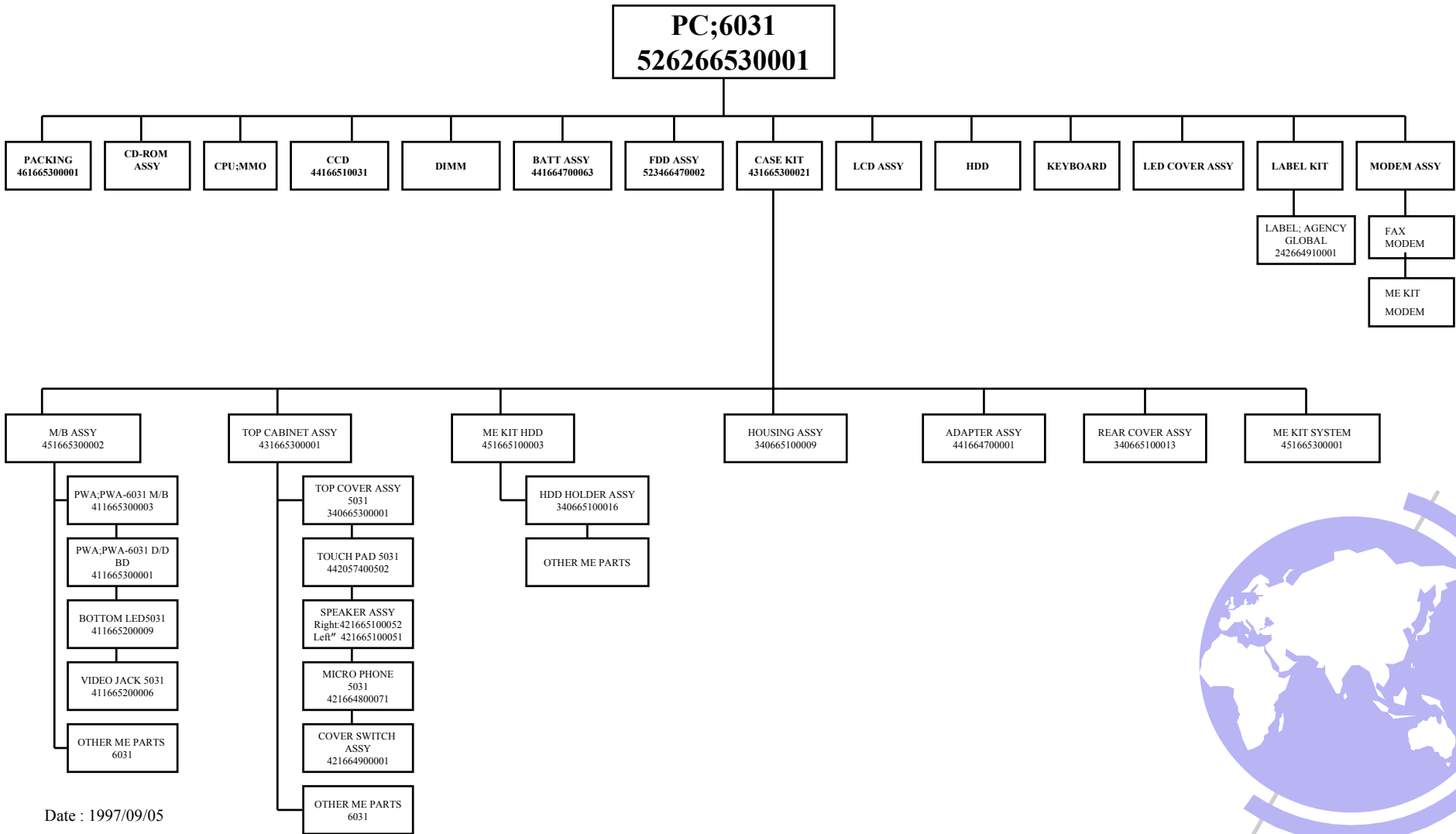


" • " IT' S STAND FOR LATEST MODIFICATION.

Date : 1998/03/19

FileName : 6031.MMS / TREE

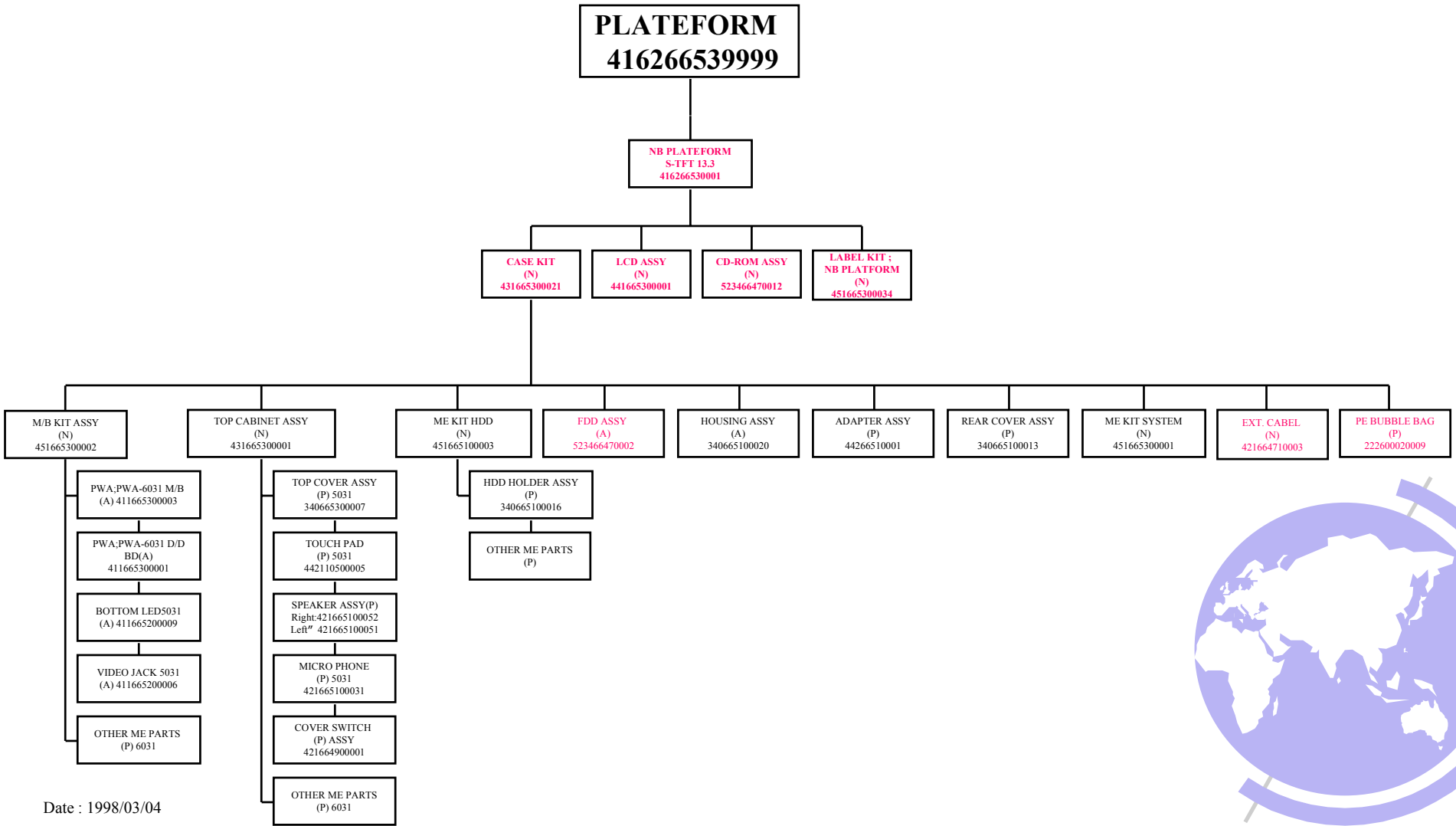
10. BOM TREE STRUCTURE(2)



Date : 1997/09/05

FileName : 6031 / TREE

10. BOM TREE STRUCTURE(3)



Date : 1998/03/04

FileName : 6031 / TREE

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

11. EXPLODED VIEWS

12. SPARE PARTS LIST(1)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
242665300001	LABEL;AGENCY-GLOBAL,ADP-MBC,6031	
461665300001	PACKING KIT;6031	
541566470014	FRU;CD ROM MODULE,20X,5026	
523466470013	CD ROM DRIVE ASSY;20X,SR200S,502	
222663920001	PE BAG;150*50,FRU,LP486	
222664820007	PE BAG;90*130,PITCHING	
340664710002	BEZEL ASSY;CD ROM(MITSU),5026	
342665100009	BRKT;CD ROM (MIT),5031	
340664710018	FRAME COMP;CD-ROM(MAT),1,5026	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
370102010701	SPC-SCREW;M2L7,NIW,K-HD	
377102010001	STANDOFF;M2 DP5 H4*13*L1.5	
421665200041	FPC ASSY;CD-ROM,PITCHING3	
523411442506	CD ROM DRIVE;8-20X,SR200S	
346665100009	PLATE;CD-ROM MODULE HOLE PLATE,5	
227664700004	END CAP-1;CD ROM,5026	
227664700005	END CAP-2;CD ROM,5026	
227664800008	END CAP-1;CD ROM,PITCHING	
221664740002	BOX;CD ROM,5026	
222664820003	PE BAG;CD ROM,PITCHING	
242600000088	LABEL;BAR CODE,125*65,COMMON	
565166470001	S/W;1.44M,UTILITY DRIVE,5026	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
561566470019	MANUAL;EN/GR,14X/20X CD ROM,5026	
441664700063	BATT ASSY;12V/4AH,NIMH,SANYO,502	
242664700021	LABEL;BATT ASSY,12V/4.0AH,SNY,50	
310131103002	CFM-BAT;NTCR,10K,ISUZU,103AT-2	
316664700011	PCB;PWA-5026/BATT CONN BD	R00
331030010006	CON;HDR,FM,10P*1,2.0MM,ST,GLD	
335152000020	CFM-BAT;THERMAL BREAKER,ISUZU,IP	
335152000021	CFM-BAT;FUSE,THERMAL,ELMWOOD,D09	

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
335512000001	POLYSWITCH;3.5A,SRP350	
338712010011	BATTERY;NIMH,1.2V/4AH,D18,SANYO	
340664710044	HOUSING ASSY;BATT 4000mA,1,5026	
344664710058	PANEL;BATTERY,1,5026	
344664710100	COVER;BATT,10*18D,1,5026	
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C1,2,3,4
288100062001	DIODE;RLZ6.2B,ZENER,SMT,LL34	D1
294011200004	LED;YE/GR,H1.1,L2,W1.25,CL170YG,	D2,3,4,5,6
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D501,502
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q1
271002104101	RES;100K ,1/10W,1% ,0805,SMT	R2
271002104301	RES;100K ,1/10W,5% ,0805,SMT	R1,3,501
271002909311	RES;909K ,1/10W,1% ,0805,SMT	R4
271002204301	RES;200K ,1/10W,5% ,0805,SMT	R7,8,11,511
271045507101	RES;.05 ,1W ,1% ,2512,SMT	R9,10
271002471301	RES;470 ,1/10W,5% ,0805,SMT	R504,505,506,507,508
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R509
297040105002	SW;PUSH BUTTON,SPST,12V/50MA,4P,	SW1
286002014001	IC;BQ2014,GAS GAUGE,SO,16P	U1
316664700052	PCB;PWA-5026/BATT VIEW 4AH BD	R00B
340665100008	COVER ASSY B;LED,5031	
344665100022	LENS;LED LENS,5031	
344665100028	COVER;LED COVER B,5031	
345665100007	PAD;MICROPHONE PAD,5031	
523466470002	FDD ASSY;1.44M,3.5",D-5026	
242664710020	LABEL;FDD,PC T=0.2,1,5026	
340664710008	HOUSING COMP;FDD,1,5026	
344664710036	COVER;FDD,1,5026	
421664700053	FPC ASSY;REM. FDD CON.,FPC,5026	
242664710019	LABEL;CAUTION,FDD,1,5026	
342664800006	HEATSINK;FDD,PITCHING	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
531013890071	KBD;87,US,K960618A-US,6031	

12. SPARE PARTS LIST(2)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
323766490021	SDRAM MODULE;16M,ATP,5027	
431665300021	CASE KIT;6031	
451665300002	ME KIT;MAIN BD,6031	
340665200008	PAD ASSY;MB,PITCHING3	
341664700013	SHIELDING;PS/2,M/B,5026	
341665100003	BRKT;PORT BRACKET,5031	
342664800009	STANDOFF;DOCKING,PITCHING	
346665100002	INSULATOR;PCMCIA,5031	
346665200010	INSULATOR;LED M/B,PITCHING3	
346665200012	INSULATOR;D/D PIN,PITCHING3	
346665200013	INSULATOR;DOCKING,PITCHING3	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
375120262008	NUT-HEX;M2.6,NIW	
377102610001	STANDOFF;M2,6DP3.5H5L5,NYLOK	
411665200006	PWA;PWA-PITCHING3 VIDEO JACK BD	
411665200007	PWA;PWA-PITCHING3 SMT VIDEO JACK	
316665200004	PCB;PWA-PITCHING3/VIDEO JACK BD	R00C
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C501,502
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L501
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L502
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	L503,504
331030006011	CON;HDR,MA,3P*2,2.0MM,ST,GLD	J1
331850002006	CON;RCA PIN JACK,2PYEL,JPJ254501	J502
331850002007	CON;RCA PIN JACK,2PBLK,RJ1091011	J501
411665200009	PWA;PWA-PITCHING3 BOTTOM LED BD	
316665200006	PCB;PWA-PITCHING3/LED BD	R0A
331030016005	CON;HDR,MA,8P*2,2.0MM,ST,GLD,SUY	J501
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C501-509
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D1-3,6-8
288100202002	DIODE;DAP202K,80V,SWITCH,DUAL,SO	D501,503
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D502
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q501-505,508
288200144001	TRANS;DTC144WK,NPN,SMT	Q506,507

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q509,510
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	PR501,503
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP502
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R501,502,504,508,
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R503
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R505-507
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U501
411665300001	PWA;PWA-6031 D/D BD	
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	C4
312271006151	EC;100U,6.3V,M,RA,8*5,-55+105,OS	C6
312271506154	EC;150U ,6.3V,M,RA,D10*5,OS-CON	C5
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	C11,C10,C12
411665300002	PWA;PWA-6031 D/D BD,SMT	
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C14
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C3,7,8,9,508,502,
272075103501	CAP;.01U ,50V ,20%,0603,SMT	C15,514,516
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C507,511
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	C2
272022106501	CAP;10U ,16V,20%,1210,Y5U,SMT	C1,503,504,512
272075102501	CAP;1000P,CR,50V ,20%,0603,SMT	C13
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D503
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D5,502,506
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D501,504,505
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D1,2,4
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	F1,2,3
291000015007	CON;HDR,SHROUD,MA,25P*2,1.27,ST,	J1
273000250005	FERRITE CHIP;160OHM/100MHZ,6A,45	L1,2
288200144001	TRANS;DTC144WK,NPN,SMT	Q512
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q501,507,509,510,518
286300431004	IC;AIC431,.5%,ADJ SHUNT REG,SOT-	Q516
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q502,503,504,505,
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	Q5,6,7,8
271071124311	RES;124K ,1/16W,1% ,0603,SMT	R507

12. SPARE PARTS LIST(3)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R503,504,511,536,556
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R512,513,520,529,539
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R519,527,537,560
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R525,506
271045107101	RES;.01 ,1W ,1% ,2512,SMT	R2
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R4,528,541,546,563
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R1,502,505,510,514,
271071000002	RES;0 ,1/16W,0603,SMT	R5
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R501,509,532,557
271071976211	RES;97.6K,1/16W,1% ,0603,SMT	R550,555
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R540,530
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R533
271071133311	RES;133K ,1/16W,1% ,0603,SMT	R515,542
271071169311	RES;169K ,1/16W,1% ,0603,SMT	R517,545
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R534
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R543,522
271071681111	RES;6.81K,1/16W,1% ,0603,SMT	R544,521
271071226311	RES;226K ,1/16W,1% ,0603,SMT	R524
271071237311	RES;237K ,1/16W,1% ,0603,SMT	R508,553
271045257101	RES;.025 ,1W ,1% ,2512,SMT	R3
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R551,559
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	U1
286303050001	IC;SB3050,PWM CTRL,SSOP,28P	U2
286100339002	IC;LP339,ULTRA-LOW PWR COMP.,SO,	U502,501
316665300004	PCB;PWA-6031/DD BD	R02B
273000500008	CHOKE COIL;16UH,15.5T,55040,SMT	T2
273001050012	XSFORMER;15UH-18UH,ER14.5,SMT	T1
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	Q1,2,3,4
271071562311	RES;562K ,1/16W,1% ,0603,SMT	R561,548
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R549,552
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R547
328306004001	DIODE;EA60QC04,RECT,6A,40V,TO-25	D3
342665100004	BRKT;D/D BD,5031	

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
411665300003	PWA;PWA-6031 MOTHER BD	
338530010009	BATTERY;LI,3V/195mAH,BR2032	BT1001
344600000215	IC CARD CON PART;160P,55150-1605	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
371102011201	SCREW;M2 L12,FLT(+),NIW	
371102510402	SCREW;M2.5L4,FLT(+),NIW	M/B TO PCMCIA SOCKET
411665300004	PWA;PWA-6031 M/B T/U BD	
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	C1003,C1004
313000510003	FILTER;4LINE,360OHM/100MHZ,8P	L1001
331040010002	CON;HDR,MA,10P,2MM,R/A,SUYIN	J1010,J1012
331210020401	CON;EDGE,204P,1.0MM,R/A,AMP	J6
331720009004	CON;D,MA,9P,2.775,R/A	J3
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J2
331720025005	CON;D,FM,25P,2.775,R/A	J4
331840005002	CON;STEREO JACK,5P,R/A,D3.6,2 SW	J1005,J1008,J1009
331872706019	CON;DIN,SKT,6P,MINI,R/A,PCB MT	J1002
331910003003	CON;POWER JACK,3P,16VDC/3A	J1
331910003006	CON;POWER JACK,3P,6.3VDC/2A	J1004
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW1001
338000000005	BATTERY HOLDER;FOR BR2032,BH-800	BT1001
411665300005	PWA;PWA-6031 M/B SMT	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	EL2,EL3
271012000301	RES;0 ,1/8W,5% ,1206,SMT	EL12,
271012202301	RES;2K ,1/8W,5% ,1206,SMT	R361
271012561301	RES;560 ,1/8W,5% ,1206,SMT	R358
271013100301	RES;10 ,1/4W,5% ,1206,SMT	R346,R349,R363
271071000002	RES;0 ,1/16W,0603,SMT	R24,R44,R45,R55,R62
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R26,R163,
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R210,R276,R321
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R13,R35,R118,R158,
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R124,R266,R277,R289
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,R14,R63,R65
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R6,R7,R10,R12,R37

12. SPARE PARTS LIST(4)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R47,R50,R73,R112
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R59
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R198,R207,R224,R225
271071169311	RES;169K ,1/16W,1% ,0603,SMT	R288
271071249311	RES;249K ,1/16W,1% ,0603,SMT	R130
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R51,406,407
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R15,R32,R69,R70,R84
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R139
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R18,R19,R20,R21,R22
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R28,R29,R100
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R125
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R286,131,116
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R315
271071242301	RES;2.4K ,1/16W,5% ,0603,SMT	R153,R155
271071244301	RES;240K ,1/16W,5% ,0603,SMT	R313
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R217,R220
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R169,R265
271071303301	RES;30K ,1/16W,5% ,0603,SMT	R48,R56
271071330302	RES;33 ,1/16W,5% ,0603,SMT	L1,L3,L4,L5,L6
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	R68
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R89,R90,R196,R214
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R162,R172,R240,R263
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R195
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R11,R64,R96,R119,
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R58,R72,R102,R103
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R304,120
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R243,R245
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R193,R218
271071563302	RES;56K ,1/16W,5% ,0603,SMT	R154,R152
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R8,R342
271071680301	RES;68 ,1/16W,5% ,0603,SMT	R1009,R1010,R1011
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R75,76,54,88,376
271071683301	RES;68K ,1/16W,5% ,0603,SMT	R211

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R3,R4,R5,R1015
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP54
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP34
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP8,RP15,RP16,RP25
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP39,RP46
271611203301	RP;20K*4 ,8P ,1/16W,5% ,0612,SMT	RP67,RP66
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP4,23,32
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP5,RP6,RP7,RP9,RP10
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP3,RP2
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT	RP45,RP1
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP33,RP35,RP37,RP38
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP28,RP36,RP42,RP44
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C89,C192,C311,C92,
272003224701	CAP;.22U ,CR,25V ,+80-20%,0805,Y	C179,C181,C256,C272
272005473401	CAP;.047U,CR,50V,10%,0805,X7R	C277,C343,C409
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C34,C55,C105,C135,
272012335701	CAP;3.3U ,CR,16V ,-20+80%,1206,S	C189
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C82,C142,C337,C353,
272015474501	CAP;.47U ,CR,50V,20%,1206,Z5U	C383,C391
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C7,C11,C19,C21,C22
272072221301	CAP;220P ,16V,5% ,-30+85'C,0603,	EC52,C67,C83
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C4,C8,C9,C14,C23,C26
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C5,C207,C219,
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	C59,C60,EC113,EC114
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C2,C3,EC6,C6,EC7,EC8
272075102501	CAP;1000P,CR,50V ,20%,0603,SMT	EC34,EC35,C42,EC53
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C10,C44,EC46,C51
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,S	EC4,EC31
272075181301	CAP;180P ,50V ,5% ,0603,SMT	EC14,EC15,EC16,EC17
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C138,C136,C412
272075222401	CAP;2200P,50V ,10%,0603,SMT	C377
272075331501	CAP;330P ,50V ,20%,0603,COG,SMT	C1035
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	EC1,EC2,EC3,EC5,EC33

12. SPARE PARTS LIST(5)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
272075471401	CAP;470P ,50V,10%,0603,SMT	C299,C304,C332,C333
272075561701	CAP;560P ,CR,50V ,+80-20%,0603,S	C91,C97
272075681401	CAP;680P ,50V ,10%,0603,X7R,SMT	C176,C177
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C1009,C1059
272602227502	EC;220U ,16V,M,6.3*7.7,-15+105',	C1018,C1019,C1038
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	L1002,L58,L59,L23
273000053228	INDUCTOR;2.2UH,5%,3225,SMT	L29
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	EL4,EL5,L18,L19,L22
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L37,L42,EL49,EL59
273000130012	FERRITE CHIP;70OHM/100MHZ,1608,S	EL22,EL23,EL24,EL25,
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	EL21,L28,L30,L31,
274011431404	XTAL;14.318MHZ,30PPM,32PF,SMT	X1,X5
274011600405	XTAL;16MHZ,30PPM,16PF,SMT	X6
274011693401	XTAL;16.9344MHZ,50PPM,20PF,SMT	X4
274012863401	XTAL;28.63636M,30PPM,30PF,SMT,FU	X2
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X7
274013546401	XTAL;35.46895MHZ,30PPM,30PF,SMT,	X3
282104052001	IC;CD4052BM,MULTIPLEXER,SO,16P	U39,U40,U52
282153238401	IC;PI5C32X384C,BUS SWITCH,QVSOP,	U13,U14,U20
282574000005	IC;74AHC00,QUAD 2I/P NAND,TSSOP,	U6
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U55,U62
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U50
282574074003	IC;74VHC74,D F/F,SSOP,14P	U56
282574123003	IC;74VHC123,RETRI. M/RESET,SSOP,	U48
282574244005	IC;74AHC244,OCT,BUF/DRIVE,TSSOP,	U38,U42,U43,U44,U45
282574373003	IC;74VHC373,OCT D-TRAN,SSOP,20P	U15
282574374003	IC;74AHC374,OCT 3ST D F/F,TSSOP,	U16,U21
283723003004	IC;DRAM,256K*16-60,EDO,SOJ-40,S-	U23,U24,U25,U26,U31
284100430002	IC;FW82371AB,PIIX4,PCI/ISA,BGA,3	U30
284500724001	IC;AD724,RGB TO NTSC/PAL,SO,16P	U1003
284500827001	IC;BT827,VIDEO DECODER,PQFP,100P	U5
284504237001	IC;CS4237B,AUDIO 3D SOUND,TQFP,1	U12
284504331001	IC;CS4331,STEREO D/A CONVERTER,S	U19

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
284504867001	IC;W48S67-02,SYSTEM CLOCK,SSOP,4	U22
284505330001	IC;PI5V330,WIDEBAND/VIDEO,QSOP,1	U2
284506701001	IC;CL-PD6701,PC CARD COMPANION,S	U28
284506832004	IC;OZ6832TC2,PCI/CARDBUS,TQFP,20	U36
284509385002	IC;CYBER9385-1X,VGA,CTRL,BGA,256	U11
284580051001	IC;80C51SL-BG,KBD CTLR,PQFP,100P	U27
284587338002	IC;PC87338VJG,SUPER I/O,TQFP,100	U60
284590363001	IC;DS90C363,LVDS,18BIT,SSOP,48P	U3,U4
286100102001	IC;TPA0102,AUDIO AMP,1.5W,TSSOP,	U41
286100358012	IC;LM358,DUAL OP/AMP,SO 8P	U10
286133078001	IC;MC33078D,LOW NOISE OP AMP.,SO	U7,U29,U35
286200213001	IC;MAX213,RS-232,SSOP,28P	U1
286300708002	IC;MAX708R,3V VOLT MONITORING,SO	U53
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U37
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U8
286305200001	IC;MIC5200-5BS,VOL REG,SOT-223	U51
288001100001	FIR;HSDL-1100,TRANSCEIVER,X07,SM	U61
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D8
288100202002	DIODE;DAP202K,80V,SWITCH,DUAL,SO	D13,D12
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D1,D2,D3,D4,D6
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D7
288200144001	TRANS;DTC144WK,NPN,SMT	Q3,Q4,Q6,Q9,Q10
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q25,Q59
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q45,Q47,48,64
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q46
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q5
288209430001	TR;NDS9430,P-FET,.06OHM,SO,8P	Q7,Q21,Q22
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q1,Q2,Q23,Q8,Q34
291000010604	CON;HDR,FM,6P*1,1.25MM,ST,SMT	J11,J13
291000010605	CON;HDR,FM,3P*2,2.0MM,ST,SMT	J1007
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J8
291000011601	CON;HDR,MA,80P*2,.635MM,ST,SMT	J24
291000011602	CON;HDR,FM,8P*2,2.0MM,ST,SMT	J14

12. SPARE PARTS LIST(6)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
291000012001	CON;HDR,MA,10P*2,1.25MM,ST,SMT	J15
291000015004	CON;HDR,FM,25P*2,1.27,ST,PITCHIN	J25
291000020402	CON;HDR,SHROUD,MA,4P*1,2.0,R/A,U	J5
291000025202	CON;HDR,MA,26P*2,.635MM,H11,R/A,	J1003,J1013,J1014
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J21
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J20
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J7,J9,J12,J1001
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J10,26
291000516005	CON;RBN,MA,30P*2,ST,H9.6,SMT,800	J1011
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U17,U18
291000621443	DIMM SOCKET;144P,.8MM,H=4MM,SMT	J22,J23
291000622801	DIMM SOCKET;280P,.6MM,GOLD,SMT	J1006
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,F2,F1001,F4
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	F3
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW2,SW1
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW1002
316665300001	PCB;PWA-6031/MOTHER BD	R04
273000500005	CHOKE COIL;7UH,T6*3*3,D.3,SMT	T1001
286501410001	IC;MK1410,NTSC/PAL CLOCK,SO,8P,S	U1004
274011431405	XTAL;14.318MHZ,20PPM,18PF,SMT	X1003
288209958001	TRANS;NDS9958,DUAL N&P MOSFET,SO	Q65
288209956001	TRANS;NDS9956A,DUAL N-MOSFET,SO,	U66,67
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	R34,L34,61
273000110006	FERRITE CHIP;105OHM/100MHZ,3216,	L21,L1008
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	R16
288200351001	TRANS;NDS351,N-MOSFET,.25HM,SOT-	Q1001
271911103901	VR;10K ,.05W,20%,XV0102GPH1N-93	VR1
342665200013	CONTACTOR;AUDIO,PITCHING3	
481665300001	F/W ASSY;SYS/VGA,6031	
242600000145	LABEL;10*10,BLANK,COMMON	
283420402003	IC;FLASH,256K*8-120,5V,PLCC32,BT	U18
481665300002	F/W ASSY;KBD CTRL,6031	
242600000145	LABEL;10*10,BLANK,COMMON	

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
283305402001	IC;EPROM,32K*8,120NS,CMOS,PLCC,3	U17
346665100002	INSULATOR;PCMCIA,5031	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
346665200024	INSULATOR;DIMM,PITCHING3	
346665200032	INSULATOR;CPU SCREW HOLE,PITCHIN	
345665200017	CONDTIVE SPONG;AUDIO,PITCHING3	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
377102010450	STANDOFF;M2DP1.6H4L5,NIW	
377102610009	STANDOFF;M2.6DP5.5H8L4	
343665300002	HEATSINK;THERMAL,6031	
375102010002	NUT-HEX;M2X1.5,NIW	
342665300001	BRKT;MMO,AL PLATE,6031	
345665300002	SPONGE;MMO AL,DOWN 63*10,6031	
346665300003	THERMAL PAD;CPU,DN,10*10*1.75T,6	
345665100017	PAD;T/P BUTTON CUSHION PAD,5031	
346665300009	INSULATOR;M/B,6031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
371102010302	SCREW;M2L3,PAN(+),NIW,NY	
371102010504	SCREW;M2L5,PAN(+),NIB	
431665300001	TOP CABINET ASSY;6031	
340665300007	COVER ASSY;TOP CASE#1,PAC12124,6	
342665200031	FINGER;H/S,COVER,PITCHING3	
343665300001	SUPPORT;K/B SUPPORT,6031	
344665100017	LENS;IR LENS,5031	
344665300003	COVER;TOP CASE,TAC12124,6031	
345665100010	CONDTIVE SPONGE;I/O SLOT,5031	
345665100011	CONDTIVE SPONGE;KEYBOARD,5031	
345665200017	CONDTIVE SPONG;AUDIO,PITCHING3	
345665200019	CONDTIVE SPONG;HINGE,PITCHING3	
371102610303	SCREW;M2.6L3,K-HEAD(+),NIW	
342665300005	HEATSINK;VGA,M/B,6031	
344665100014	HOLDER;T/P HOLDER,5031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	

12. SPARE PARTS LIST(7)

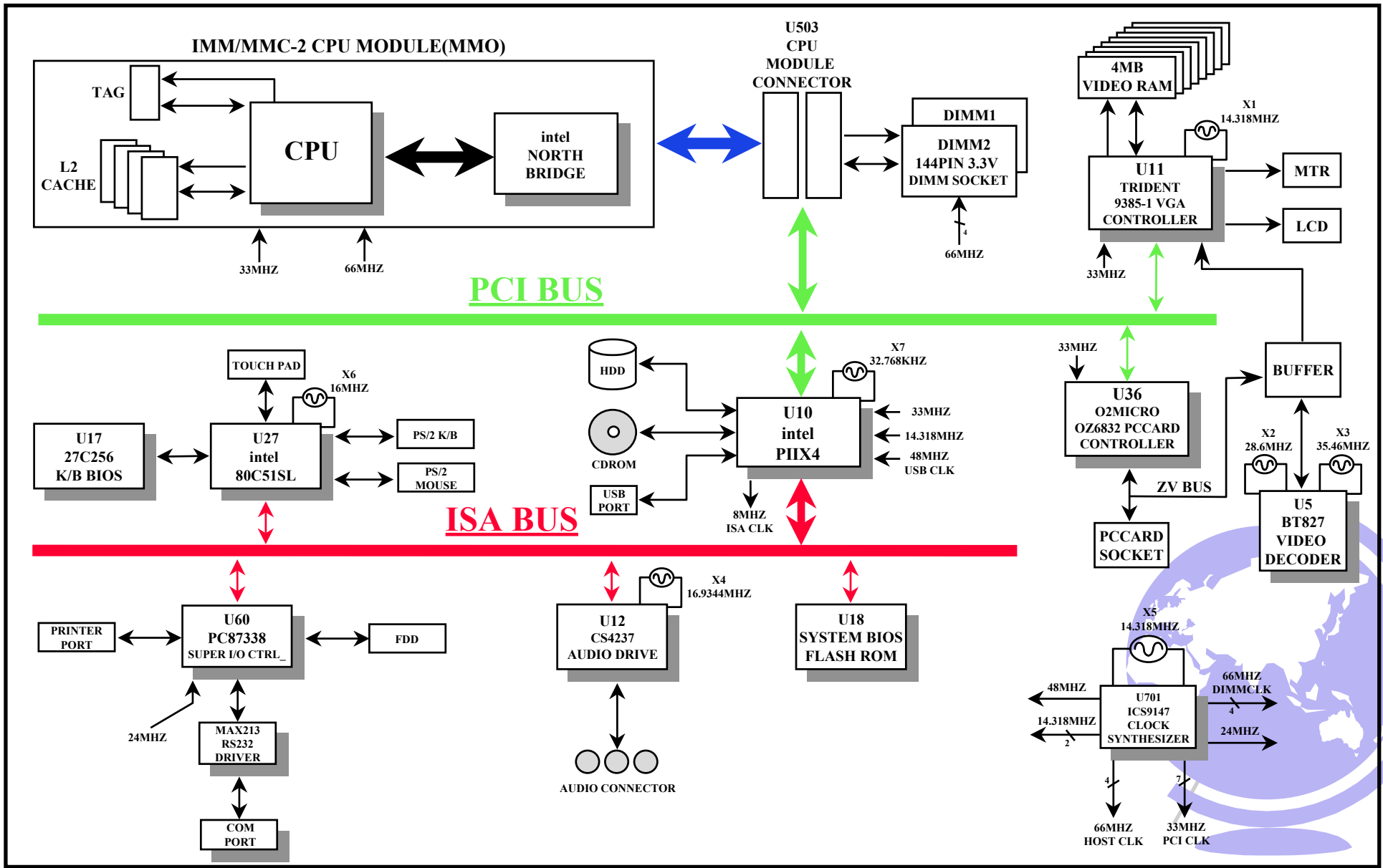
SPARE PARTS LIST FOR N/B 6031				SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION		PART_NO	DESCRIPTION	LOCATION
421664700071	FFC ASSY;TOUCH PAD,UPPER CASE,50			342664700024	SCREW;M3,FOOT,BTM CASE,5026	
421665100031	MICROPHONE ASSY;5031			343665100003	BRKT;FAN SUPPORT,5031	
421664900001	WIRE ASSY;COVER SWITCH,5027			344664700047	FOOT;R,BTM CASE,5026	
421665100051	SPEAKER ASSY;LEFT,5031			344664700048	FOOT;L,BTM CASE,5026	
339111100004	SPEAKER ASSY;LEFT,5031			344664710068	DOOR;CHANGE,B-CASE,1,5026	
342665100001	BRKT;SPEAKER BRACKET(L),5031			344664800021	HOOK;SLIDE,HOUSING,PITCHING	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	SPK/BKT		344665100002	HOUSING;BOTTOM CASE,5031	
421665100052	SPEAKER ASSY;RIGHT,5031			344665100005	BUTTON;MODULE LOCK BUTTON,5031	
339111100003	SPEAKER ASSY;RIGHT,5031			344665100010	BUTTON;POWER BUTTON,5031	
342665100002	BRKT;SPEAKER BRACKET(R),5031			344665100016	BUTTUN;LCD HOOK BUTTUN,5031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	SPK/BKT		345665100012	CONDTIVE SPONGE;I/O SLOT(L),5031	
442110500005	TOUCH PAD MODULE;904236-0000,502			345665100013	CONDTIVE SPONGE;I/O SLOT(R),5031	
345665100004	PAD;SPK WIRE PAD,5031			345665100014	CONDTIVE SPONGE;I/O BRKT,5031	
421664900062	CABLE ASSY;ESD TOUCH PAD,5027			345665200004	FOOT;PAD,PITCHING3	
345665100015	PAD;T/P BUTTON SUPPORT PAD,5031			345665100018	CONDTIVE SPONGE;VEDIO,5031	
451665100003	ME KIT;HDD,5031			346665100008	INSULATOR;FAN BRKT,5031	
340665100016	HDD HOLDER ASSY;5031			345665100016	PAD;FOOT PAD(REAR),5031	
342665100003	HOLDER;HDD HOLDER,5031			340665100013	COVER ASSY;REAR,5031	
344665100006	COVER;HDD COVER,5031			344665100023	COVER;DOCKING COVER,5031	C1
344665100007	COVER;PCMCIA COVER,5031			344665100027	COVER;REAR COVER,5031	J1
346664700002	INSULATOR;REM,HDD,5026			451665300001	ME KIT;SYSTEM,6031	J2
342665100005	BRKT;HDD,5031			342665300004	HEATSINK;W/FAN,6031	R03
346664700007	INSULATOR;HDD TOP,5026			344665100008	COVER;HINGE COVER(L),5031	R1,R2
370103010402	SPC-SCREW;M3L4,K-HEAD,NIW,T0.8			344665100009	COVER;HINGE COVER(R),5031	R3
371102010301	SCREW;M2L3,PAN(+),NIW			340665100017	COVER ASSY;CPU,5031	
412665200004	PCB ASSY;HDD CONN. BD,PITCHING3			344665100018	COVER;CPU COVER,5031	
340665100020	HOUSING ASSY;BOTTOM CASE,5031			346665100007	MESH;FAN MESH,5031	
341664700006	SPRING PLATE;FOOT,BTM CASE,5026			344665100019	COVER;MODEM COVER,5031	
341664700007	SPRING;SLIDE,BTM CASE,5026			344665100024	COVER;AUDIO COVER,5031	
341664700010	SPRING;CHANGE,BTM CASE,5026			370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
341664700021	SPRING-WASHER;BTM CASE,5026			370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,NYLOCK	
341664700023	SPRING PLATE;BASE,BTM,5026			342665200029	COVER;DRAM,PITCHING3	
341665100004	SPRING;LCD HOOK SPRING,5031			342665100008	BRKT;LCD CABLE(L),5031	

12. SPARE PARTS LIST(8)

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
344665100032	COVER;MODEM CON. COVER,5031	
346665100005	WASHER;MODEM COVER WASHER,5031	
342665100007	BRKT;LCD CABLE(R),5031	
371102612201	SCREW;M2.6L22,K HEAD	
222600020023	PE BAG;120*170MM,W/SEAL,COMMON	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
346665200015	FILM;LCD PROTECT,13.3",215*290,P	
346665300004	THERMAL PAD;FAN,DOWN,80*47,6031	
346665300005	THERMAL PAD;FAN,SIDE,25*15,6031	
371102010504	SCREW;M2L5,PAN(+),NIB	
442665100001	AC ADPT ASSY;5031	
523466470002	FDD ASSY;1.44M,3.5",D-5026	
242664710020	LABEL;FDD,PC T=0.2,1,5026	
340664710008	HOUSING COMP;FDD,1,5026	
344664710036	COVER;FDD,1,5026	
421664700053	FPC ASSY;REM. FDD CON.,FPC,5026	
242664710019	LABEL;CAUTION,FDD,1,5026	
342664800006	HEATSINK;FDD,PITCHING	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
421664710003	CABLE ASSY;EXT FDD,1,5026	
344664710065	COVER;FDD CON.,1,5026	
421664700002	CABLE ASSY;FDD,5026	
342664700021	GROUND;FDD CON.,5026	
411664700032	PWA;PWA-5026 FDD TRANS BD	
316664700029	PCB;PWA-5026/FDD TRAN BD	R01
331120020001	CON;HDR,SHROUD,MA,10P*2,2MM,ST	J2
331030052002	CON;HDR,MA,26P*2,1.27,ST,GOLD	J1
373203010601	T-SCREW;P,M3,L6,PAN(+),0,ZNC	
346665100002	INSULATOR;PCMCIA,5031	
222600020009	PE BUBBLE BAG;10"*8",COMMON	
441665100001	LCD ASSY;13.3(S),TFT,5031	
340665100005	HOUSING ASSY;13.3(S) LCD,5031	
344665100003	LENS;POWER LENS(B),5031	

SPARE PARTS LIST FOR N/B 6031		
PART_NO	DESCRIPTION	LOCATION
344665100011	HOUSING;13.3 LCD HOUSING,5031	
345665100001	PAD;LCD HOUSING(S),5031	
345665100003	PAD;LCD HOUSING SIDE PAD(S),5031	
345665100005	PAD;LCD HOUSING TOP PAD(S),5031	
345665100006	PAD;LCD HOUSING TOP PAD(H),5031	
340665100006	COVER ASSY;13.3(S) LCD,5031	
344665100004	LENS;POWER LENS(T),5031	
344665100012	COVER;13.3S LCD COVER,5031	
344665100030	PLUG;LCD HOOK,5031	
345665100009	CUSHION;TOP,LCD COVER,5031	
345665200006	CUSHION;DOWN,LCD,PITCHING3	
346665100003	INSULATOR;INVERTER,5031	
370102010301	SPC-SCREW;M2L3,NNIB,K-HD,727	
370102010601	SPC-SCREW;M2L6,K-HEAD(+),NIW	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
411665300006	PWA;PWA-6031 CCD TRANS BOTTOM BD	
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	
291000012004	CON;HDR,FM,10P*2,1.27MM,ST,SMT	
291000020803	CON;HDR,MA,8P*1,1.25,R/A,SMT,HIR	
316665300003	PCB;PWA-6031/CCD-TRAN BOTTON BD	
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	
412665200001	PCB ASSY;INVERTER BD,PITCHING3	
413000020093	LCD;LT133X1-104,TFT,13.3,XGA	
421665100001	WIRE ASSY;LCD(CCD)-M/B,5031	
421665100004	WIRE ASSY;D/A,5031	
421665200002	WIRE ASSY;LCD TO M/B,PITCHING3	
340665100001	TILT UNIT;13.3S(L),5031	
340665100003	TILT UNIT;13.3(R),5031	
341665100001	BRKT;13.3S(L) LCD BRACKET,5031	
341665100002	BRKT;13.3(R) LCD BRACKET,5031	
324180586054	IC;CPU,TILLAMOOK,200MHZ,1.8V	
523415780007	HD DRIVE;2.16G,2.5",MHA2021AT	

13. SYSTEM BLOCK DIAGRAM & SCHEMATICS



13. SYSTEM BLOCK DIAGRAM & SCHEMATICS

MOTHER-BOARD

DC /DC BOARD

52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74

75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96

97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113

114 115 116 117 118 119 120 121 122 123 124 125 125 127 128 129 130

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

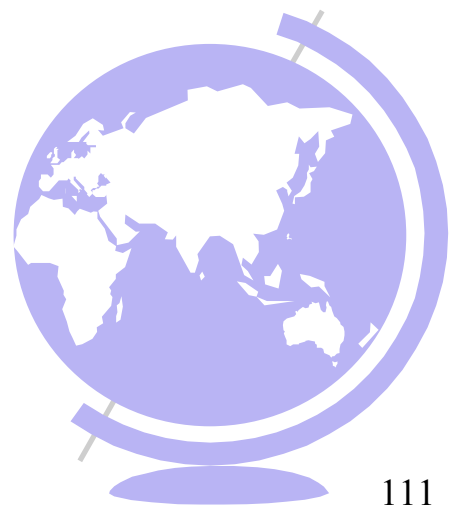
MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD



13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

13. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD