TROUBLE SHOOTING GUIDE FOR NOTEBOOK 5023

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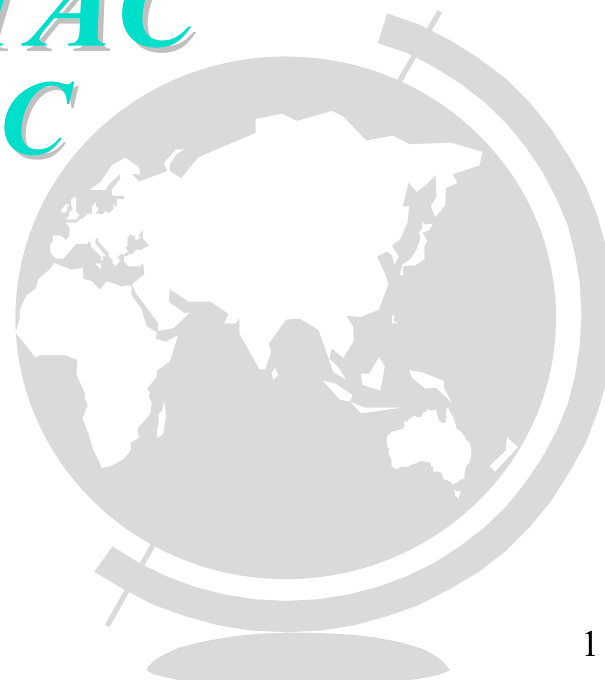

5023 N/B MAINTENANCE

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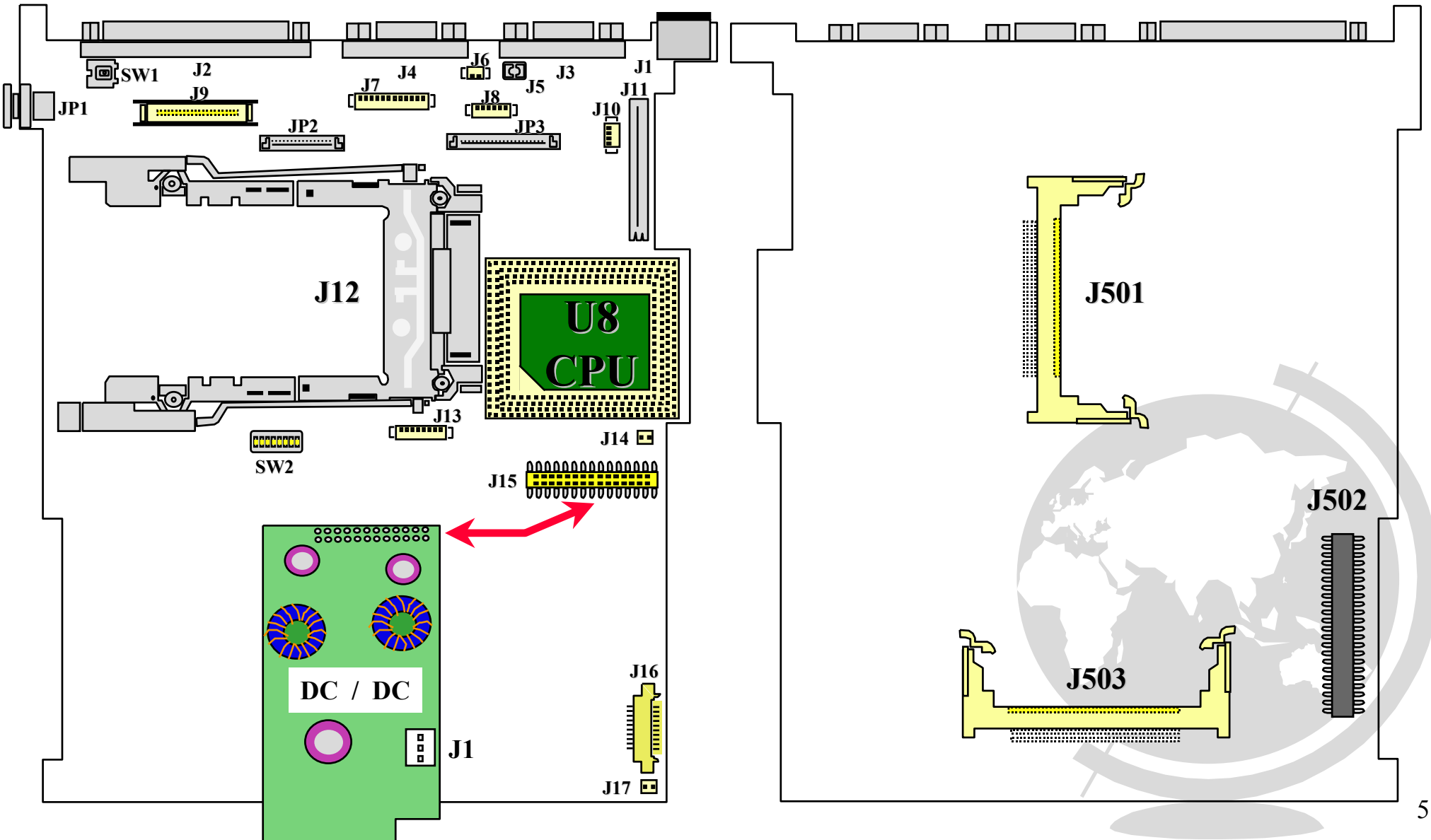
1. DEFINITION OF CONNECTORS & SWITCHES

- J1 : PS/2 KEYBOARD & MOUSE CONNECTOR
- J2 : PARALLEL PORT(PIO)
- J3 : SERIAL PORT (SIO)
- J4 : CRT VIDEO CONNECTOR
- J5 : SUSPEND / RESUME BUTTON
- J6 : COVER SWITCH
- J7 : ICON LCD MODULE CONNECTOR
- J8 : BACKLIGHT CONNECTOR
- J9 : LCD MODULE CONNECTOR
- J10 : SIR PORT
- J11 : FLOPPY DRIVE CONNECTOR
- J12 : PCMCIA IC CARD CONNECTOR
- J13 : TOUCHPAD CONNECTOR
- J14 : SPEAKER CONNECTOR
- J15 : DC/DC TO BOARD CONNECTOR
- J16 : AUDIO BOARD CONNECTOR
- J17 : MICROPHONE CONNECTOR
- J501, J503 : MEMORY MODULE CONNECTOR
- J502 : HARD DISK CONNECTOR
- JP1 : POWER JACK
- JP2, JP3 : INTERNAL KEYBOARD CONNECTOR
- SW1 : POWER BUTTON

DC /DC BOARD

- J1 : BATTERY CONNECTOR

2 . LOCATION OF CONNECTORS & SWITCHES

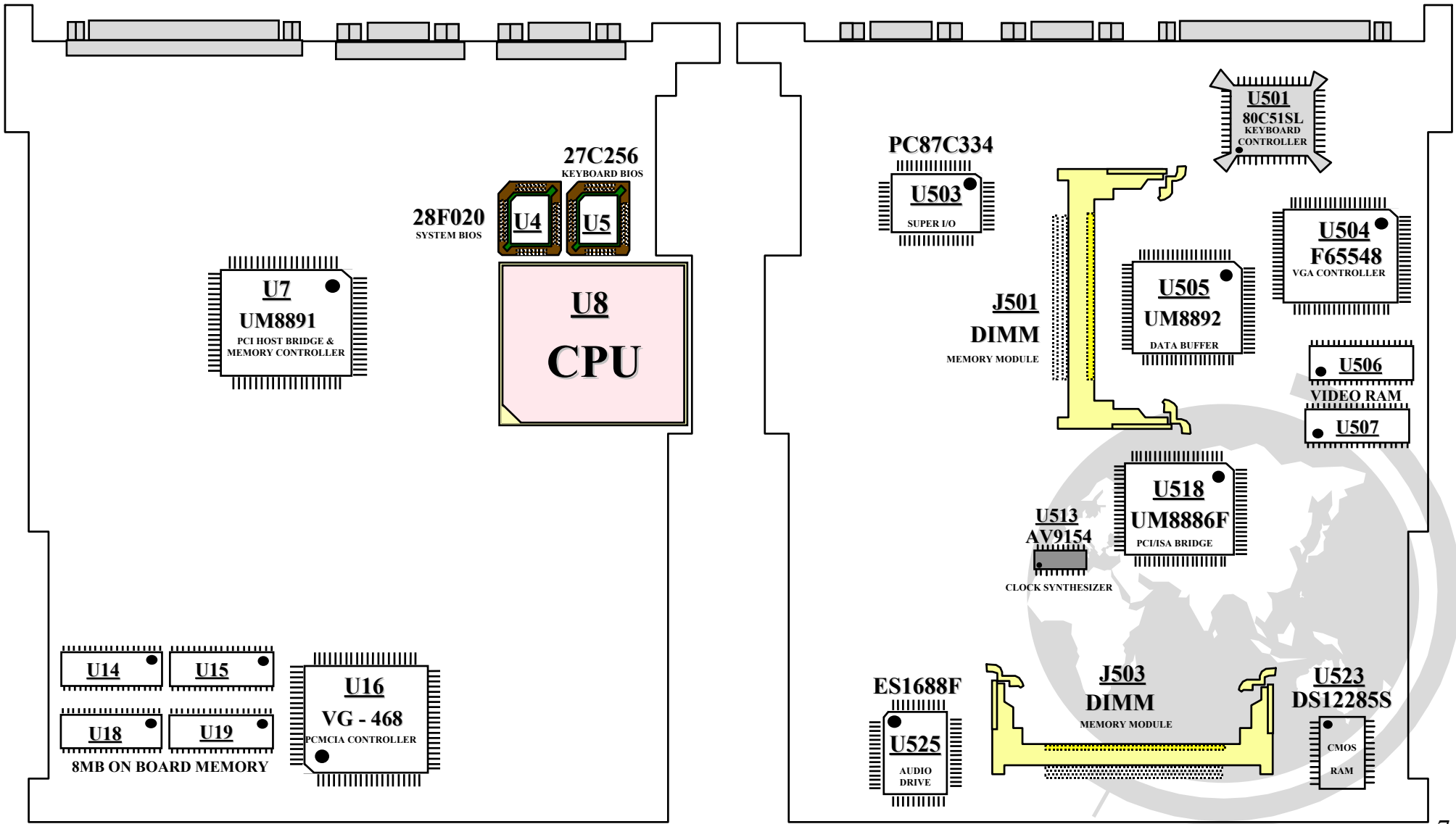


5023 N/B MAINTENANCE

3. MAJOR COMPONENTS

1. U8 PENTIUM PROCESSOR
2. U7 UM8891BE/CYS PCI BRIDGE & MEMORY/CACHE CONTROLLER
3. U509 UM8886BE/CYS PCI TO ISA BRIDGE
4. U505 UM8892BE/CYS DATA PATH CONTROLLER
5. U504 C&T 65548 VGA CONTROLLER
6. U503 NS PC87334 SUPER I/O CONTROLLER
7. U16 VADEM VG-468 PCMCIA CONTROLLER
8. U501 80C51 KEYBOARD CONTROLLER
9. J501, J503 OPTIONAL DIMM SOCKETS
10. U510 VG-468 PCMCIA CONTROLLER
11. U14, U15, U18, U19 8MB ON BOARD MEMORY
12. U4 SYSTEM BIOS
13. U5 KEYBOARD BIOS
14. U514 AV9154 CLOCK GENERATOR
15. U522 ESS1688 AUDIO CONTROLLER
16. U523 DS12885 RTC CONTROLLER

4. LOCATION OF MAJOR COMPONENTS



5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.1 PENTIUM MICROPROCESSOR (P54LM)

SYMBOL	TYPE	DESCRIPTION
A20M#	I	WHEN THE ADDRESS BIT 20 MASK PIN IS ACTIVE, THE 20 (A20) PENTIUNM MICORPROCESSOR MASKS PHYSICAL ADDRES BIT BEFORE PERFORMING A LOOKUP TO THE INTERNAL CACHE OR EMULATES THE ADDRESS WRAPAROUND AT THE AMB DRIVING A MEMORY BUS CYCLE ONTO THE BUSES. A20M# BOUNDARY THAT OCCUS ON THE 8086/8088.
A31-A5 A4-A3	I/O O	A31-A3 COMPRISE THR PENTIUME ,ICROPROCESSOR'S ADDRES BUS.
ADS#	I/O	WHEN ACTIVE ,THE ADDRESS STATUS OUTPUT INDICCATES THAT A VALID BUS CYCLE DEFINITION AND ADDRESS ARE AVAILABLE ON THE BUS CYCLE DEFINITION AND BUS LINES.
AHOLD	I	THE ADDRESS HOLD REQUEST INPUT ALLOWS ANOTHER BUS MASTER ACCESS TO PENTIUM MICROPROCESSOR'S ADDRESS BUS FOR A CACHE INVALIDATION, BACK INVALIDATION, OR INQUIRE CYCLE.
AP	I/O	THE PENTIUM PROCESS GENERATES ADDRESS PARITY DURING MEMORY WRITE OPERATIONS AND CHECK ADDRESS PARITY DURING CACHE INVALIDATION CYCLES(ADDRESS BUS SNOOPING).
APCHK#	O	THE PENTIUM PROCESS ASSERTS THE ADDRES PARITY CHECK OUTPUT WHEN AN ADDRES BUS PARITY ERROD IS DETECTED APCHK# IS ASSERTED 2 CLOCK CYCLES AFTER EADS# IS SAMPLE ACTIVE. APCHK$ REMAIN ACTIVE FOR ON CLOCK CYCLE.
[APICHEN] OR PICD1	I/O	APIC ENABLE.
BE0#	O	BYTE ENABLE,PATH0 (D7-D0).
BE1#	O	BYTE ENABLE,PATH1 (D15-D8).
BE2#	O	BYTE ENABLE, PATH 2 (D23-D16).
BE3#	O	BYTE ENABLE, PATH3 (D31-D24).
BE4#	O	BYTE ENABLE, PATH4 (D39-D32).
BE5#	O	BYTE ENABLE, PATH5 (D47-D40).
BE6#	O	BYTE ENABLE, PATH6 (D55-D48).
BE7#	O	BYTE ENABLE, PATH7 (D63-D56).

SYMBOL	TYPE	DESCRIPTION
BF	I	THE BUS FREQUENCY SIGNAL(BF) DETERMINES THE I/O BUS TO PROCESSOR CORE FREQUENCY RATIO.
BOFF#	I	ENSURE THAT THE PROCESSOR DOESN'T FETCH STALE DATA FROM MAIN MEMORY.
BP3-2	O	THE BREAK POINT OUTPUTS INDICATE THAT A BREAKPOINT MATCH HAS BEEN DETECTED THROUGH THE BRESKPOINT REGISTER.
BP/PM1-0	O	BREAKPOINT AND PERFORMANCE MONITORING PINS.
BRDY#	I	THE BURS READY INPUT INDICATES THAT THE CURRENTLY ADDRESSED DEVICE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT CURRENTLY ADDRESSED DEVICE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BRDCY#	I	THE BURS READY INPUT INDICATES THAT THE LEVEL 2 CACHE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT THE LEVEL 2 CACHE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BREQ#	O	THE INTERNAL CYCLE PENDING OUTPUT INDICATES THAT THE PENTIUM MICROCESSOR HAS A BUS CYCLE REQUEST PENDING.
BT3-BT0	NA	BRANCH TRACE LINES ARE DRIVEN DURING A BRANCH TRACE SPECIAL CYCLE.
BUSCHK#	I	THE BUS CHECK ALLOWS SYSTEM DESIGNERS TO NOTIFY THE CPU. IF A BUS CYCLE HAS NOT COMPLETED SUCCESSFULLY.
CACHE#	I/O	CACHE# SIGNAL IS ACTIVE WHEN INFORMATION IS BEGIN TRANSFREED BETWEEN EXTERNAL MEMORY AND AN INTERNAL CACHE.
CLK	I	CLOCK PROVIDES THE FUNDAMNTAL TIMING AND THE INTERNAL OPERATING FREQUENCY FOR THEE PENTIUM MICROPROCESSOR
CPUTYP	I	CPU TYPE PIN SAMPLED BY THE PROCESSOR AT THE TRAILING-EDGE OF RESET TO DETERMINE WHETHER IT IS PRIMARY OR THE DUAL PROCESSPR .

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.1 PENTIUM MICROPROCESSOR (P54LM)

SYMBOL	TYPE	DESCRIPTION
D7:D0	I/O	DATA PATH ZERO.
D51:D8	I/O	DATA PATH ONE.
D23:D16	I/O	DATA PATH TWO.
D31:D24	I/O	DATA PATH THREE.
D39:D32	I/O	DATA PATH FOUR.
D47:D40	I/O	DATA PATH FIVE.
D55:D48	I/O	DATA PATH SIX.
D63:D56	I/O	DATA PATH SEVEN.
D/C#	I/O	DATA OR CONTROL.AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF DATA WILL BE TRANSFERED DURING THE CURRENT BUS CYCLE,OTHERWISE SETS IT TO LOW .
D/P#	O	DUAL/PRIMARY .THIS IS AN OUTPUT OF PRIMARY PROCESSOR AND IS NOT USED BY THE DUAL PROCESSOR .IT ASSERTED(LOW)BY THE PRIMARY PROCESSOR WHEN IT HAS ACQUIRED PRIVATE BUS OWNERSHIP AND HAS INITIATED A BUS CYCLE
DP0	I/O	PARITY BIT FOR DATA PATH 0,D7:D0.
DP1	I/O	PARITY BIT FOR DATA PATH 1,D15:D8.
DP2	I/O	PARITY BIT FOR DATA PATH 2,D23:D16.
DP3	I/O	PARITY BIT FOR DATA PATH 3,D31:D24.
DP4	I/O	PARITY BIT FOR DATA PATH 4,D39:D32.
DP5	I/O	PARITY BIT FOR DATA PATH 5,D47:D40.
DP6	I/O	PARITY BIT FOR DATA PATH 6,D55:D48.
DP7	I/O	PARITY BIT FOR DATA PATH 7,D63:D56.
DPEN#	I/O	DUAL PROCESSOR ENABLE.
EADS#	I	THE EXTERNAL ADDRESS STROBE SIGNAL INDICATES THAT A VALID EXTERNAL ADDRESS HAS BEEN DRIVEN ONTO THE PENTIUM S A4:A31 ADDRESS LINES BY ANOTHER MASTER.
EWBE#	I	THE EXTERNAL WRITE BUFFER EMPTY IS USED TO ENSURE THAT MEMORY OPERATIONS OCCUR IN ORDER OF EXECUTION.
FLUSH#	I	THE CACHE FLUSH INPUT FORCES FORCES THE PENTIUM ROCESSOR TO FLUSH THE CONTENTS IN OF ITS INTERNAL CACHE.
FERR#	O	FLOATING0POINT ERROR OUTPUT PIN IS DRIVEN ACTIVE WHEN A FLOATING-POINT ERROR OCCURS.

SYMBOL	TYPE	DESCRIPTION
FRCMC#	I	THE FUNCTOIN REDUNDANCY CHECKING MASTER/CHECKER# PIN IS SAMPLED BY THE PENTIUM MICROPROCESSOR DURING RESET TO DETERMINE WHETHER THE MICROPROCESSOR SHOULD BE CONFIGED AS A FUNCTIONAL REDUNDANCY MASTER OR CHECKER.
HIT#	I/O	THE HIT# SIGNAL ACTIVE TO INDICATE A SNOOP HIT IN EITHER THE INTERNAL CODE OR DATA CACHE.
HITM#	I/O	THE PENTIUM MICOPROCESSOR DRIVES THE HIT MODIFIED SIGNAL ACTIVE TO INDICATE A SNOOP HIT TO A MODIFIED LINE IN THE DATA CACHE.
HLDA	I/O	BUS HOLD ACKNOW LEDGE.
HOLD	I	THE BUS HOLD REQUEST INPUT ALLOW S ANOTHER BUS MASTER TO GAIN COMPLETE CONTROL OF THE PENTIUM S LOCAL BUSES.
IBT	NA	THE INSTRUCTION BRANCH TAKEN SIGNAL IS DRIVEN ACTIVE FOR ONE CLOCK CYCLE WHEN PENTIUM MICROPROCESSOE EXECUTES AN INSTRUCTION RESULTING IN AN EXECUTION BRANCH.
IERR#	O	INTERNAL ERROR IS ASSERTED WHEN A PARITY ERROR IS ENCOUNTERED INSIDE THE PENTIUM MICROPROCESSOR.
IGNNE#	I	IGNORE NUMERIC ERROR INPUT IS ASSERTED BY EXTERNAL LOGIC THE PENTIUM MICROPROCESSOR WILL IGNORE A NUMERIC ERROR. AND CONTINUE EXECUTING NON-CONTROL FLOATING-POINT INSTRUCTIONS.
INIT	I	PENTIUM MICROCESSOR INIT INPUT HASTHE SAME EFFECT AS THE RESET SIGNAL EXCEPT THAT THE FOLLOWING RETAIN THE VALUES.
INTR	I	THIS IS MASKABLE INTERRUPT REQUEST INPUT.
INV	I	THE INVALIDATE INPUT TELLS THE PENTIUM MICROPROCESSOR WHETHER THE CACHE LINE STATE SHOULD BE MARKED INVALIDATED OR SHARED AS A RESULT OF SNOOP HIT.
IU	NA	THE IU SIGNAL DICATED THAT AN INSTRUCTION IN THE "u" PIPLINE HAS COMPLETED EXECUTION.
IV	NA	THE IU SIGNAL DICATED THAT AN INSTRUCTION IN THE "V" PIPLINE HAS COMPLETED EXECUTION.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.1 PENTIUM MICROPROCESSOR (P54LM)

SYMBOL	TYPE	DESCRIPTION
KEN#	I	THE CACHE ENABLE PIN IS SAMPLED TO DETERMINE IF THE CURRENT BUS CYCLE IS CACHEABLE.
LINT0 OR INTR	I	IF THE PROCESSOR'S LOCAL APIC IS ENABLE, THIS IS THE LINT0 INPUT TO THE APIC.
LOCK#	I/O	THE LOCK# SIGNAL IS ASSERTED WHEN THE PENTIUM MICROPROCESSOR WANTS TO RUN MULTIP BUS CYCLES WITHOUT HAVING THE BUSES TAKEN AWAY BY ANOTHER BUS MASTER.
M/IO#	I/O	MEMORY OR I/O. AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF ADDRESSING A MEMORY LOCATION AND LOW IF ADDRESSING AN I/O LOCATION.
NA#	I	THE NEXT ADDRESS INPUT INDICATES THAT THE MEMORY SUBSYSTEM IS CAPABLE FO TAKING ADVANTAGE OF THE PENTIUM MICROPROCESSOR'S ADDRESS PIPELINING.
NMI	I	NON-MASKABLE INTERRUPT REQUEST.
PBREQ#	I/O	PRIVATE BUS REQUEST. ONLY USED IN DUAL PROCESSOR SYSTEM.
PBGNT#	I/O	PRIVATE BUS GRANT. ONLY USED IN DUAL PROCESSOR SYSTEM.
PCHK#	O	SEE DP0.
PCD	O	PAGE CACHE DISABLE.
PEN#	I	PARITY ENABLE.
PHIT#	I/O	PARIVATE BUS HIT. PHIT# IS AN OUTPUT FROM THE LRM AND AN INPUT TO THE MRM. TIS USED IN A DUAL PROCESSOR SYTEM.
PHITM#	I/O	PRIVATE BUS HIT ON MODIFIED LINE.
PICCLK	I	PROGRAMMABLE INTERRUPT CONTROLLER CLOCK.
PICDO OR DEPN#	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE0.
PICD1 OR APICEN	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE1.
PRDY	O	PROBE READY ASSERTED BY THE PROCESSOR WHEN IT HAS STOPPED EXECUTION IN RESPONSE TO THE R/S# SIGNAL BEING ASSERTED LOW.
PWT	O	THE PAGE WRITE-THROUGHT PIN REFLECTS THE STATE OF THE PAGE ATTRIBUTE BIT.

SYMBOL	TYPE	DESCRIPTION
RESET	I	1.KEEPS THE MICROPROCESSOR FROM OPERATING UNTIL THE POWER SUPPLY VOLTAGES HAVE COME UP AND STSBILIZED. 2.FORCES KNOWN DEFAULT VALUES INTO THE PENTIUM PROCESSOR REGISTER.
R/S#	I	RUN/STOP. WHEN SET HIGH, THE PROCESSOR IS PERMITTED TO RUN NORMALLY WHEN SET LOW, THE PROCESSOR CEASES TO EXECUTE INSTRUCTIONS AND ENTERS PROBE MODE.
SCYC	I/O	SPLIT CYCLE IS VALID FOR LOCKED BUS CYCLES OLY. SCYC IS ASSERTED WHEN A LOCKED TRANSFER RESULTS IN A MISALIGNED MW MORY ACCESS.
SMI#	I	SYSTEM MANAGEMENT INTERRUPT INFORMS THE PROCESSOR THAT A SYSTEM MANAGEMENT INTERRUPT ROUTINE RESIDING IN SYSTEM MANAGEMENT ADDRESS SPACE NEEDS TO BE PERFORMED.
SMIACT#	O	SYSTEM MANAGEMENT INTERRUPT ACKNOWEDGW INFORMS EXTERNAL LOGIC THAT THE PROCESSOR IS IN SYSTEM MANAGEMENT MODE.
TCK	I	TEST CLOCK IJSED TO CLOCK STATE INFORMATION AND DATA INTO AND OUT OF DEVICE DURING BOUNDARY SCAN.
TDI	I	TEST INPUT IJSED TO SHIFT DATA AND INSTRUCTIONS INTO THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TDO	O	TEST OUTPUT IJSED TO SHIFT DATA OUT OF THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TMS	I	TEST MODE SELECT IJSED TO CONTROL THE STATE OF THE TEST ACCESS PORT CONTROLLER.
TRST#	I	TEST RESET IJSED TO FORCE THE TEST ACCESS PORT CONTROLLER INTO AN INITIALIZED STATE.
WB/WT#	I	THE WRITE-BACK OR WRITE THROUGH INPUT ALLOWS EXTERNAL LOGIC TO DETERMINE WHETHER A IS PLACED IN THE WRITE BACK OR WRITE THROUGH STATE.
W/R#	I/O	WRITE OR READ AT THE START OF A BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF THE CURRENT BUS CYCLE IS A WRITE BUS CYCLE W/R# IS SET LOW IF THE CURRENT BUS CYCLE IS A READ BUS CYCLE.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.2 UM8891-N PCI HOST BRIDGE AND MEMORY/CACHE CONTROLLER

SYMBOL	TYPE	DESCRIPTION
CA4A	O	CACHE RAM ADDRESS BIT. FOR ASYNCHRONOUS SECONDARY CACHE RAM APPLICATION. IT PROVIDES SYSTEM ADDRESS BIT 4 FOR BANK A.
CA4B	O	CACHE RAM ADDRESS BIT. FOR ASYNCHRONOUS SECONDARY CACHE RAM APPLICATION. IT PROVIDES SYSTEM ADDRESS BIT 4 FOR BANK B.
CA3	O	CACHE RAM ADDRESS BIT. FOR ASYNCHRONOUS SECONDARY CACHE RAM APPLICATION. IT PROVIDES SYSTEM ADDRESS BIT 3. FOR SYNCHRONOUS SECONDARY CACHE RAM APPLICATION.
CRCSA#/CE#	O	CACHE RAM CHIP SELECT FOR BANK A.
CRCSB#/ADSC#	O	CACHE RAM CHIP SELECT FOR BANK B.
CROEA#/OE#	O	CACHE RAM OUTPUT ENABLE FOR BANK A.
CROEB#/ADV#	O	CACHE RAM OUTPUT ENABLE FOR BANK A.
CRW[7:0]	O	CACHE RAM WRITE CONTROL. SECONDARY CACHE RAM WRITE CONTROL SIGNALS WITH RESPECT TO EACH BYTE.
TA[7:0]	I/O	ADDRESS TAG RAM DATA.
TRWR#	O	ADDRESS TAG RAM WRITE CONTROL SIGNAL.
PALTH	O	PROCESS ADDRESS LATCH CONTROL SIGNAL.
MDPERR#	I	MEMORY DATA PARITY ERROR. INPUT FROM UM8892N. INDICATES THERE IS A PARITY ERROR ON MD BUS.
ADPAR	I	PCI DATA PARITY. INPUT FROM UM8892N. FOR 32-BIT DATA BUS PARITY.
PDCTL[3:0]	O	PCI DATA BUS CONTROL. OUTPUT TO UM8892N. CONTROL PD BUS DIRECTION AND LATCH FUNCTIONS.
MDCTL[3:0]	O	MEMORY DATA BUS CONTROL. OUTPUT TO UM8892N. CONTROL THE MD BUS DIRECTION AND LATCH FUNCTION.
ADCTL[3:0]	O	PCI DATA BUS CONTROL. OUTPUT TO UM8892N. CONTROL AD BUS DIRECTION AND LATCH FUNCTION.
AD[31:0]	I/O	32-BIT PCI ADDRESS AND DATA BUS.
FRAME#	I/O	PCI BUS TRDY# SIGNAL. CYCLE FRAME. OUTPUT WHEN UM891N ACTS AS CURRENT PCI BUS INITIATOR; OTHERWISE, IT IS AN INPUT PIN. FRAME# IS DEASSERTED TO INDICATE THAT THE INITIATOR IS READY TO COMPLETE THE FINAL DATA PHASE.
PCICLK	I	PCI BUS CLOCK
CBE#[3:0]	I/O	PCI BUS COMMAND AND BYTE ENABLE SIGNALS
PAR	I/O	PCI BUS PARITY BIT
SERR#	O	PCI BUS SERR# SIGNAL
LOCK#	I/O	PCI BUS LOCK# SIGNAL. INDICATES A LOCK CYCLE.
STOP#	I/O	PCI BUS STOP# SIGNAL. OUTPUT WHEN UM8891 ACTS AS A TARGET OF PCI BUS CYCLE TO INDICATE THAT IT REQUESTS THE INITIATOR TO STOP THE TRANSACTION IN PROGRESS ON THE CURRENT DATA PHASE: OTHER IT IS AN OUTPUT PIN.
DEVSEL#	I/O	PCI BUS DEVSEL# SIGNAL. DEVICE SELECT. ASSERTED WHEN UM8891N DECODING LOGIC IS TRUE; OTHERWISE IT IS AN INPUT PIN.
TRDY#	I/O	PCI BUS TRDY# SIGNAL. TARGET READY. IT IS ASSERTED WHEN UM8891N IS READY TO COMPLETE THE CURRENT DATA PHASE.
IRDY#	I/O	PCI BUS IRDY# SIGNAL. INITIATOR READY. DURING A WRITE, IRDY# ASSERTED INDICATES THAT THE INITIATOR IS DRIVING VALID DATA ONTO THE DATA BUS. DURING A READ, IRDY# ASSERTED INDICATES THAT THE INITIATOR IS READY TO ACCEPT DATA FROM THE TARGET.
REQ#	O	PCI BUS REQUEST.
GNT#	I	PCI BUS GRANT.
MWE#	O	DRAM WRITE ENABLE
MA[11:0]	O	DRAM ADDRESS SIGNALS
CAS[7:0]	O	DRAM COLUMN SIGNAL STROBE

SYMBOL	TYPE	DESCRIPTION
RAS[5:0]	O	DRAM ROW SIGNAL STROBE
RAS[7:6]	O	DRAM ROW SIGNAL STROBE
PA[31:0]	I/O	PROCESSOR ADDRESS BUS.
PBE7#-PBE0#	I	BYTE ENABLE.
ADS#	I	ADDRESS STROBE. INDICATES THAT A NEW VALID BUS CYCLE IS CURRENTLY BEING DRIVEN BY THE CPU.
PMIO	I	MEMORY OR I/O ACCESS. DEFINES WHETHER THE CURRENT CPU CYCLE IS A MEMORY OR I/O ACCESS.
PWR	I	WRITE OR READ ACCESS. DEFINES WHETHER THE CURRENT CPU CYCLE IS A WRITE OR READ ACCESS.
PDC	I	DATA OR CODE ACCESS. DEFINES WHETHER THE CURRENT CPU CYCLE IS A DATA OR CODE ACCESS.
PLOCK#	I	BUS LOCK. INDICATES THAT CURRENT CPU BUS CYCLES SHOULD NOT BE INTERRUPTED. SUCH AS WHEN THE CPU IS RUNNING A READ-MODIFY-WRITE CYCLE OR INTERRUPT ACKNOWLEDGE CYCLE.
CACHE#	I	CACHE-ABILITY. INDICATES CPU INTERNAL CACHE-ABILITY FOR THE CURRENT CYCLE.
HITM#	I	HIT MISS TO A MODIFIED LINE. INDICATES THE CURRENT INQUIRE CYCLE HIT A MODIFIED LINE IN CPU DATA CACHE AND CPU WILL SCHEDULE A WRITE-BACK CYCLE TO THE BUS.
PHOLD	O	CPU HOLD.
PHLDA	I	CPU BUS HOLD ACKNOWLEDGE.
BOFF#	O	BACK-OFF. THIS SIGNAL IS USED TO FORCE CPU OFF THE BUS IN THE NEXT CLOCK.
KEN#	O	CACHE ENABLE.
BRDY#	O	BURST-OFF. THIS SIGNAL INDICATES TO THE CPU THAT THE VALID DATA IS ON THE DATA BUS IN RESPONSE TO A READ CYCLE, OR THE DATA PROVIDED BY CPU HAS BEEN ACCEPTED IN RESPONSE TO A WRITE CYCLE.
WBWT#	O	RESERVED
NA#	O	NEXT ADDRESS. THIS SIGNAL INDICATES TO THE CPU THAT UM8891 IS READY TO ACCEPT A NEW BUS CYCLE.
INVOT4	O	INVALIDATION REQUEST. THIS SIGNAL INDICATES TO THE CPU TO DETERMINE THE FINAL STATE OF A CACHE LINE AS A RESULT OF AN INQUIRE HIT.
EADS#	O	EXTERNAL ADDRESS STROBE.
SMIACT#	I	SYSTEM MANAGEMENT INTERRUPT ACTIVE. INDICATES THAT THE CPU IS OPERATING IN SMM.
SUSPA	I	SUSPENT ACKNOWLEDGE FOR CYRIX CPU
REFRESH#	I	REFREAH REQUEST INPUT
RESET	I	RESET. THIS IS A SIGNAL OF 8891N
CLK	I	CPU CLOCK INPUT
CLKDC	I	INPUT FROM UM8886N TO NOTIFY UM8891N
CLKRUN#	O	RESERVED
SCLKCTL	O	SSYNCHRONOUS SRAM CLOCK CONTROL.
CPUPD	I	NOTIFY UM8891N THAT CPU IS POWER-DOWN OR CLOCK DC..
891BUSY#	O	RESERVED
TESTI	I	TEST INPUT MUST BE LOW
TESTO	O	TEST OUTPUTVCC5
VCC5		5V POWER FOR PCI INTERFACE LOGIC
VCC3		3.3V POWER FOR CPU INTERFACE
VCCD		POWER FOR DRAM INTERFACE
VCCS		POWER FOR CACHE SRAM INTTERFACE PINS
GND		GROUNDING.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.3 UM8892-N DATA PATH CONTROLLER

SYMBOL	TYPE	DESCRIPTION
PD[63:0]	I/O	CPU DATA BUS DATA BUS DIRECTION AND INTERNAL LATCH ARE CONTROLLED BY PDCTL 3-0. FOUR BUFFERS STORE PD TO MD DATA.AND FOUR BUFFERS STORE PD TO AD DATA.
MD[63:0]	I/O	MEMORY DATA BUS DATA BUS DIRECTION AND INTERNAL LATCH ARE CONTROLLED BY MDCTL2-0 ONE BUFFER STORES MD TO AD DATA.
AD[31:0]	I/O	PCIAD BUS DATA BUS DIRECTION AND INTERNAL LATCH ARE CONTROLLED BY ADCTL3-0. TWO 32-BIT BUFFERS STORE AD TO PD DATA,AND TWO 32-BIT BUFFERS STORE AD TO MD DATA
MDCTL[3:0]	I	MEMORY DATA BUS CONTROL. INPUT FROM UM8891N,CONTROL MD(MEMORY DATA)BUS DIRECTION AND LATCH FUNCTION.
PDCTL[3:0]	I	CPU DATA BUS CONTROL. INPUT FROM UM8891N,CONTROL PD(CPU DATA_BUS DIRECTION AND LATCH FUNCTION.
ADCTL[3:0]	I	PCIDATA BUS CONTROL. INPUT FROM UM8891N,CONTROL AD(CPU DATA_BUS DIRECTION AND LATCH FUNCTION.
MDPERR#	O	MEMORY DATE PARITY ERROR.OUTPUT TO UM8891N, INDICATING A PARITY ERROR OCCURRED ON MD BUS.(64-BIT MD PARITY CHECK)
CLK	I	CPU CLOCK
PCICLK	I	PCIBUS CLOCK
ADPAR	O	PCIDATA PARITY.OUTPUT TO UM8891N, FOR 32-BIT PCIDATA PARITY(EVEN PARITY)
DP[7:0]	I/O	PARITY FO MD BUS.
VCCD		POWER FOR DRAM INTERFACE.FOR 5V OR 3.3V DRAM APPLICATIONS.CONNECT THESE POWER PINTS TO 5V OR 3.3V
VCC5		POWER PINS FOR 5V
VCC3		POWER FOR 3.3V
GND		GROUNG

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.4 UMC UM8886-N PCI TO ISA BRIDGE

SYMBOL	TYPE	DESCRPTION
AD{31:0}	I/O	32 BIT PCI ADDRESS AND DATA BUS
C/BE{3:0}	I/O	PCI BUS COMMAND AND BYTE ENABLE SIGNALS
DEVSEL#	I/O	PCI BUS DEVESEL SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
TRDY#	I/O	PCI BUS TRDY SIGNAL. THIS ACTS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
IRDY#	I/O	PCI BUS IRDY SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC ISSUES A CYCLE TO PCI BUS: OTHERWISE. IT IS AN INPUT PIN.
FRAME#	I/O	PCI BUS FRAME SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC ISSUES A CYCLE TO PCI BUS: OTHERWISE. IT IS AN INPUT PIN.
IDSEL	I	PCI BUS IDSEL INPUT SIGNAL. IDSEL IS USED AS CHIP SELECT DURING CONFIGURATION READ AND WRITE TRANSACTION.
PAR	O	PCI BUS PARITY BIT.
SERR#	I	SYSTEM ERROR. UPON SAMPLING THIS PIN ACTIVE. THE IBC GENERATES AN NMI TO THE CPU.
LOCK#	I	PCI BUS LOCK SIGNAL TO INDICATE LOCK CYCLE.
STOP#	I/O	PCI BUS STOP SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
INT{D:A}	I	PCI BUS INTERRUPT REQUEST A. B. C. D.
BCLK	O	ISA BUS CLOCK OUTPUT.
BALE	O	BUS ADDRESS LATCH ENABLE.
SA{19:0}	O	SYSTEM ADDRESS BUS SA{19:0}. SA{19:0} ARE OUTPUT. EXCEPT DURING ISA MASTER CYCLES.
LA{23:}	O	LATCH-ABLE ADDRESS BUS LA{23:17}. LA{23:17} ARE OUTPUT. EXCEPT DURING ISA MASTER CYCLES.
SBHE#	O	SYSTEM BUS HIGH ENABLE INDICATES THE HIGH BYTE ON THE ISA DATA BUS SD{15:8} IS VALID.
SD{15:0}	I/O	16 BIT ISA SYSTEM DATA BUS.
IOR#	O	ISA I/O READ COMMAND.
IOW #	O	ISA I/O WRITE COMMAND.
MEMR#	O	ISA MEMORY READ COMMAND.
MEMW #	O	ISA MEMORY WRITE COMMAND.

SYMBOL	TYPE	DESCRPTION
SMEMR#	O	ISA SYSTEM MEMORY READ COMMAND.
SMEMW #	O	ISA SYSTEM MEMORY WRITE COMMAND.
IOCS16#	I	16-BIT I/O. THIS SIGNAL INDICATES THAT BUS SIZE OF CURRENT ISA I/O SLAVE IS 16 BITS.
MEMCS16#	I/O	16-BIT MEMORY. THIS PIN INDICATES THAT THE BUS SIZE OF CURRENT ISA MEMORY SLAVE IS 16 BIT.
0WS#/ACIN	I	NO WAIT STATES. THIS SIGNAL IS ASSERTED BY ISA SLAVE IN ORDER TO SHORTEN THE CYCLE.
IOCHRDY	I/O	CHANNEL READY. IOCHRDY IS USED BY ISA SLAVES TO INSERT WAIT STATES.
MASTER#	I	16-BIT MASTER. INDICATES THAT A 16-BIT ISA MASTER HAS CONTROL OF THE ISA BUS.
AEN	O	ISA BUS AEN SIGNAL. WHEN HIGH. INDICATES THAT DMA OR REFRESH CONTROLS THE ISA BUS.
IOCHCK#/ CLKRUN#	I	I/O CHANNEL CHECK. IBC WILL GENERATE NMI TO CPU UPON SAMPLING THIS PIN ACTIVE; CLKRUN IS RESERVED FOR FUTURE USE.
REFRESH#	I/O	I/O SYSTEM REFRESH CONTROL. OUTPUT TO ISA BUS WHEN CONVERTING SYSTEM TIMER TICKS INTO REFRESH CYCLE.
CPUREQ REQ0#/	I	CPU REQUEST. CPU INITIATOR REQUESTS THE PCI BUS.
COVERSW #	I	PCI MASTER REQUEST 0. FOR REEQUESTS INITIATED FROM PCI BUS MASTER. COVERSW FROM EXTERNAL LCD COVER SWITCH TO INFORM THE PMU THAT THE LCD COVER HAD BEEN CLOSED SO THAT PMU CAN FORCE SYSTEM TO ENTER SUSPEND MODE.
REQ1#	I	PCI MASTER REQUEST 1.
REQ2#/ 891BUSY#	I	PCI MASTER REQUEST 2. THE 891BUSY IS RESERVED FOR FUTURE USE.
REQ3#/ COVERSW #	I	PCI MASTER REQUEST 3. THIS PIN ALSO ACTS AS "COVERSW " FROM EXTERNAL LCD COVER SWITCH TO INFORM THE PMU THAT LCD COVER HAD BEEN CLOSED SO THAT PMU CAN FORCE SYSTEM ENTER SUSPEND MODE.
GNT0#/ NCLKDC#	O	PCI MASTER GRANT 0. ARBITER HAS GRANTED PCI BUS MASTER OR AS NCLKDC# UM8886N WILL FORCE NCLKDC# LOW TO INFORM UM8891 THAT CPU CLOCK WILL BE D.C.
GNT1#	O	PCI MASTER GRANT 0.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.4 UMC UM8886-N PCI TO ISA BRIDGE

SYMBOL	TYPE	DESCRIPTION
GNT2#/ SUSP#	O	PCI MASTER GRANT 2. THIS PIN ALSO ACTS AS SUSP# OUTPUT WHICH WILL BE FORCED LOW AFTER ENTERING SUSPEND MODE AND THE CLOCK TO CPU HAD BEEN STOPED.
GNT3#/ NCLKDC#	O	PCI MASTER GRANT 3. OR NCLKDC# UM 8886N WILL FORCE NCLKDC# TO LOW TO INFORM UM 8891 THAT CPU CLOCK WILL BE D.C.
X32K	I	32K CLOCK INPUT.
DREQ{3:0} DREQ{7:5}	I	DMA REQUEST. THESE SIGNALS ARE USED TO REQUEST DMA SERVICE.
DACK#{7:0}	I/O	DMA ACKNOWLEDGE. THE IBC ASSERTS THESE OUTPUT LINES TO INDICATE THAT THE DMA DEVICE HAS BEEN GRANTED SERVICE.
EOP	I/O	END OF PROCESS. IN INPUT MODE. THIS PIN IS USED BY THE DMA DEVICES TO STOP CURRENT DMA TRANSFER. IN OUTPUT MODE. DMA CONTROLLER ASSERTS EOP TO INDICATE TO THE ACTIVE DMA DEVICE THAT THE TRANSFER HAS REACHED THE TERMINAL COUNT.
IRQ1	I	ISA BUS INTERRUPT REQUEST 1.
IRQ{7:3}	I	ISA BUS INTERRUPT REQUEST {7:3}
IRQ8	I	RTC INTERRUPT REQUEST.
IRQ{12:9}	I	ISA BUS INTERRUPT REQUEST {12:9}
IRQ{15:14}	I	ISA BUS INTERRUPT REQUEST {15:14}
INTR	O	MASKABLE INTERRUPT TO CPU.
NMI	O	NONMASKABLE INTERRUPT TO CPU.
SMI#	I/O	SYSTEM MANAGEMENT INTERRUPT. OUTPUT TO CPU TO REQUEST SMM SERVICE. INPUT FROM CPU INDICATES THAT CPU HAS ENTERED SMM MODE.
STPCLK#	O	CPU SLOW DOWN /STOP CLOCK CONTROL.
PWRLCH2	O	LATCH SIGNAL TO LATCH PMC OUTPUT PINS FROM SD{7:0} TO GENERATE PMC0-5. PMC8 AND CKGENPD.
PWRLCH1	O	LATCH SIGNAL TO LATCH PMC OUTPUT PINS FROM SD{7:0} TO GENERATE PMC6. PMC7/SUSP. PMC8. PMC9 AND CLKSEL{2:0}.
EXTSMI#	I	EXTERNAL SMI1.
SMIACT#	I	SYSTEM MANAGEMENT INTERRUPT ACKNOWLEDGE FROM INTEL SL ENHANCED CPU.
PCICLKI	I	PCIBUS CLOCK INPUT TO THE IBC.
CLKIN	I	OSCILLATOR CLOCK INPUT TO GENERATE CPU AND PCICLOCKS.
OSC	I	TIME BASE 14.318 MHZ CLOCK INPUT.
HCLK	O	CLOCK OUTPUT TO CPU HOST.
PCICLK0	O	CLOCK OUTPUT TO PCIBUS.

SYMBOL	TYPE	DESCRPTION
RSTIN	I	RESET INPUT: RSTIN IS USED TO INITALIZE THE ENTIRE SYSTEM.
CPURST	O	CPU RESET. THIS PIN IS USED TO INITALIZE CPU.
RSTDRV	O	RSTDRV. THIS PIN IS USED TO RESET ENTIRE SYSTEM, EXCEPT THE CPU.
KBCLK	I/O	KEYBOARD CONTROLLER CLOCK. CLOCK OUTPUT TO THE 8742.
RC/PGP0	I/O	RESETS INPUT FROM 8042, OR ACTS AS PROGRAMMABLE INPUT, OR OUTPUT PIN 0.
GA20/PGP1/ LDEV#	I/O	ADDRESS A20 GATE FROM 8042. OR ACTS AS PROGRAMMABLE INPUT/OUTPUT PIN 1. OR ACTS AS LOCAL DEVICE INPUT FROM VL BUS.
ROMCS#/ KBCS#	O	ROM CS AND KBCS. DUAL FUNCTION PIN. FOR I/O CYCLES, THIS PIN IS KBCS: FOR MEMORY CYCLES, IT IS ROMCS.
SPKR	O	SPEAKER DRIVE OUTPUT.
XDEN/PGP3 TCRAMWR	O	XD BUS DIRECTION CONTROL. OR ACTS AS PROGRAMMABLE OUTPUT PIN 3. OR AS TCRAMWR TO READ/WRITE EXTERNAL 4KB RTC.
RTCAS	O	RTC ADDRESS LATCH.
RTCWR	O	RTC WRITE COMMAND.
RTCRD	O	RTC READ COMMAND.
IDE1FX	O	IDE 1FX CHIP SELECT.
IDE3FX	O	IDE 3FX CHIP SELECT.
ONOFF#/ ACIN	I	"ON/OFF" SWITCH INPUT TO PMU. SWITCHES BETWEEN FULL-ON MODE AND SUSPEND MODE OR ACTS AS ACIN.
LB1/LB2	I	LOW BATTERY 1 OR LOW BATTERY 2 INPUT.
IDE17X/ PGP3	O	IDE 17X CHIP SELECT. OR ACTS AS PROGRAMMABLE OUTPUT PIN 3.
IDE37X/ PGP2	O	IDE 37X CHIP SELECT. OR ACTS AS PROGRAMMABLE OUTPUT PIN 2.
IDEHDEN	O	ENABLE IDE CYCLE.
A20M	O	MASK PROCESSOR ADDRESS 20: ACTIVE WHEN GA20 IS LOW OR I/O PORT 92H BIT 1 IS HIGH.
EXSMI2/LB2 /KBCLKI	I	EXTERNAL SMI INPUT 2 OR ACTS AS LOW BATTERY 2 INPUT OR KEY BOARD CLOCK INPUT.
FERR#	I	WHEN LOW INDICATES THAT A FLOATING POINT ERROR HAS OCCURRED.
IGNNE#	O	IGNNE IS ASSERTED LOW TO INSTRUCT THE CPU TO IGNORE A NUMERIC ERROR AND CONTINUE EXECUTING NON-CONTROL FLOATING POINT INSTRUCTIONS.
TEST	I	THIS PIN USED FOR TESTING ONLY. FOR NORMAL OPERATION. IT SHOULD BE PULLED HIGH.
VCC5		+5V VOLT POWER SUPPLY.
VCC3		3.3-VOLT POWER SUPPLY.

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.5 C&T F65548 VGA CONTROLLER

SYMBOL	TYPE	DESCRIPTION
RESET#	I	RESET.FOR VL-BUS INTERFACES CONNECT TO RESET#.FOR DIRECT CPU LOCAL BUS INTERFACES,CONNECT TO THE SYSTEM RESET GENERATED BY THE MOTHERBOARD SYSTEM LOGIC FOR ALL PERIPHERALS.
ADS#	I	ADDRESS STROBE.IN VL-BUS AND CPU LOCAL BUS INTERFACES INDICATES VALID ADDRESS AND CONTROL SINGAL INFORMATION IS PRESENT.
M/IO#	I	MEMORY I/O.IN VL-BUS AND APU LOCALBUS INTERFACES INDICATES MEMORY OR I/O CYCLE :1=MEMORY,0=I/O
W/R#	I	WRITE/READ.THIS CONTROL SINGAL INDICATES A WRITE (HIGH)OR READ (LOW)OPERATION.IT IS SAMPLED ON THE RISING EDGE OF THE(INTERNAL)1x CPU CLOCK WHEN ADS# IS ACTIVE.
RDYRTN#	I	READY RETURN.HANDSHAKING SINGAL IN VL-BUS INTER-
CRESET	I	FACES INDICATING SYNCHRONIZATION OF RDF# BY THE LOCAL BUS MASTER/CONTROL TO THE PROCESSOR.UPON RECEIPT OF THIS LCLK-SYNCHRONOUS SIGNAL THE CHIP WILL STOP DRIVING THE BUS (IF A READ CYCLE WAS ACTIVE)AND TERMINATE THE CURRENT CYCLE.
LRDY#	O	LOCAL READY . DRIVEN LOW DURING VL-BUS AND CPU LOCAL BUS CYCLES TO INDICATE THE CURRENT CYCLE SHOULD BE COMPLETED .THIS SIGNAL IS DRIVEN HIGH AT THE END OF THE CYCLE.THEN TRI-STATED.
LDEV#	O	LOCAL DEVICE .IN VL-BUS AND CPU LOCAL BUS INTERFACES,THIS PIN INDICATES THAT THE CHIP OWNS THE CURRENT CYCLE BASE ON THE MEMORY OR I/O ADDRESS WHICH HAS BEED BROADCAST.
LCLK	I	LOCAL CLOCK.IN VL-BUS THIS PIN IS CONNECTED TO THE CPU 1x CLOCK. IN CPU LOCAL BUS INTERFACES IT IS CONNECTED TO THE CPU 1x OR 2x CLOCK.IF THE INPUT IS A 2x CLOCK, THE PROCESSORRESET SIGNAL MUST BE CONNECTED TO CRESET (PIN23) FOR SYNCHRONIZATION OF THE CLOCK PHASE.

SYMBOL	TYPE	DESCRIPTION
BE0#	I	BYTE ENABLE 0.INDICATES DATA TRANSFER ON D7-D0 FOR THE CURRENT CYCLE.
BE1#	I	BYTE ENABLE 1.INDICATES DATA TRANSFER ON D15-D8 FOR THE CURRENT CYCLE.
BE2#	I	BYTE ENABLE 2. INDICATES DATA TRANSFER ON D23-D16 FOR THE CURRENT CYCLE.
BE3#	I	BYTE ENABLE 3. BE3# INDICATES THAT DATA IS TO BE TRANSFERRED OVER THE DATA BUS ON D31-24 DURING THE CURRENT ACCESS.
A(2-23)	I	SYSTEM ADDRES BUS. IN VL-BUS, AND DIRECT CPU
		INTERFACES, THE ADDRESS PINS ARE CONNECT DIRECTLY
A24	I/O	TO THE BUS.
A25	I/O	ADDRESS INPUTS THROUGH A23 ARE ALWAYS AVAILABLE
		A24-27 MAY BE OPTIONALLY USED FOR OTHER FUNCTION :
A26	I/O	IN INTERNAL CLOCK SYNTHESIZER TEST MODE (TS#=0 AT
A26	I/O	RESET),A24 BECOMES VCLK OUT AND A25 BECOMES MCLK OUT A26 AND A27 MAY BE ALTRNATELY BE USE AS GENERAL PURPOSE I/O PINS OR ACTIVITY INDICATOR AND ENABLE BACKLIGHT RESPECTIVELY (SEE PANEL INTERFACE PIN DESCRIPTIONS AND XR5C AND XR72 FOR MORE DETAILS) IF A26 AND A27 ARE USED AS GPIO PINS, THEY MAY BE PROGRAMMED AS 2-PIN CRT MONITOR DDC INTERFACE. EITHER A26 OR A27 MAY ALSO BE USED TO OUTPUT COMPOSITE SYNC. FOR SUPPORT OF AN EXTERNAL NTSC/PAL ENCODER CHIP
D(0-31)	I/O	SYSTEM DATA BUS IN 32-BIT CPU LOCAL BUS DESIGNS THESE DATA LINES CONNECT DIRECTLY TO THE PROCESSOR DATA LINES.ON THE VL-BUS THEY CINNECT TO THE CORRESPONDING BUFFERED OR UNBUFFERED DATA SIGNAL. THESE PINS ARE TRI-STATED DURING STANDBY MODE

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.5 C&T F65548 VGA CONTROLLER

SYMBOL	TYPE	DESCRIPTION
RESET#	I	RESET. THIS INPUT IS USED TO BRING SIGNALS AND IN THE CHIP TO A CONSISTENT STATE. ALL OUTPUT FROM THE CHIP ARE TRI-STATED OR DRIVEN TO AN INACTIVE STATE
CLK	I	BUS CLOCK. THIS INPUT PROVIDES THE TIMING REFERENCE FOR ALL BUS TRANSACTION.
PAR	I/O	PARITY. THIS SIGNAL IS USED TO MAINTAIN EVEN PARITY ACROSS AD0-31 AND C/BE0-3#. PAR IS STABLE AND VALID ONE CLOCK AFTER THE ADDRESS PHASE.
FRAME#	I	CYCLE FRAME. DRIVEN BY THE CURRENT MASTER TO INDICAYE THE BEGINAND DURATION OF AN ACCESS.
IRDY#	I	INITATOR READY. INDICATE THE TARGET ABILITY TO COMPLETE THE CURRENT DATA PHASE OF THE TRANS-ACTON.
TRDY#	S/TS	TARGET READY. INDICATES THE TARGET'S ABILITY TO COMPLETE THE CURRENT DATA PHASE OF THE TRAN-ACTION.
STOP#	S/ST	STOP. INDICATES THE CURRENT TARGET IS REQUESTING THE MASTER TO STOP THE CURRENT TRANSACTION
DEVSEL#	S/ST	DEVICE SELECT. INDICATES THE CURRENT TARGET HAS DECODES ITS ADDRESS AS THE TARGET OF THE CURRENT ACCESS.
PESS#	S/TS	PARITY ERROR. THIS SIGNAL IS FOR THE REPORTING OF DATA PARITY ERRORS (EXCEPT FOR SPECIAL CYCLE WHERE SERR# IS USED).
SERR#	O	SYSTEM ERROR. USED TO REPORT SYSTEM ERROR WHERE THE RESULT WILL BE CATASTROPHIC (ADDRESS PARITY ERROR, DATA PARITY ERROR FOR SPECIAL CYCLE COM-MAND, ETC.)
ROMA(0:17)	O	BIOS ROM ADDRESS OUTPUT. SEE MAD8-15 (PIN170-177) FOR BIOS ROM DATA INPUT
ROMOE#	O	BIOS ROM OUTPUT ENABLE.
AD(00:31)	I/O	PCIADDRESS /DATA BUS

SYMBOL	TYPE	DESCRIPTION
C/BE0#	I	BUS COMMAND /BYTE ENABLES. DURING THE ADDRESS PHASE OF A BUS TRANSACTION, THESE PINS DEFINE THE BUS COMMAND. (SEE LIST BELOW)
IDSEL	I	INITALIZATION DEVICE SELECT. USED AS A CHIP SELECT DURING CONFIGURATION READ AND WRITE TRANS-ACTION.
AA0 AA1 A22 AA3 AA4 AA5 AA6 AA7 AA8	I/O	ADDRESS BUS FOR DRAMS A AND B PLEASE SEE THE CONFIGURATION TABLE IN THE EXTENDED REGISTER DESCRIPTION SECTION FOR COMPLETE DETAILS ON THE CONFIGURATION OPTION FOR CFG0-8(XR01 AND XR6C).
CA(0:7) CA8	O	ADDRESS BUS FOR DRAM C CA8 MAY BECONFIGURED AS VAFC BLANK# OUT
RASA# RASB# RASC#	O	RAS FOR DRAM A RAS FOR DRAM B RAS FOR DRAM C OR COLOR KEY INPUT FROM EXTERNAL PC VIDEO SOURCE.
CASAL# CASAH# CASBL# CASBH#	O	CAS FOR THE DRAM A LOWER BYTE CAS FOR THE DRAM A UPPER BYTE CAS FOR THE DRAM B LOWER BYTE CAS FOR THE DRAM B UPPER BYTE
CASCL# CASCH#	I/O	DRAM C LOW BYTE. VIDEO IN RED-6 OR VAFC VP14 DRAM C HIGH BYTE. VIDEO IN RED-7 OR VAFC VP15
WEA# WEB# WEC#	O	WRITE ENABLE FOR DRAM A WRITE ENABLE FOR DRAM B WRITE ENABLE FOR DRAM C OR VIDEO IN PORT PCLK OUT
OEAB# OEC#	O	OUTPUT ENABLE FOR DRAMS A AND B OUTPUT ENABLE FOR DRAMS C OR VAFC"VIDEO INPUT CLOCK" IF DRAM C NOT USED

5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.5 C&T F65548 VGA CONTROLLER

SYMBOL	TYPE	DESCRIPTION
MAD(0:15)	I/O	MEMORY DATA BUS FOR DRAM A (LOWER 512K OF DISPLAY MEMORY)
MBD(0:15)	I/O	MEMORY DATA BUS FOR DRAM B(UPPER 512K)
MCD(0:15)	I/O	MEMORY DATA BUS FOR DRAM C(FRAME BUFFER)
P(0:15)	O	8,9,12 OR 16-BIT FLAT PANEL DATA OUTPUT. 18-BIT AND 24-BIT PANEL INTERFACES MAY ALSO BE SUPPORTED (SEE CA0-7 FOR P16-23).REFER TO THE TABLE BELOW FOR CONFIGURATIONS FOR VARIOUS PANEL TYPES.
SHFCLK	O	SHIFT CLOCK.PIXEL CLOCK FOR PANEL DATA.
FLM	O	FIRST LINE MARKER.FLAT PANEL EQUIVALENT OF VSYNC.
LP	O	LATCH PULSE.FLAT PANEL EQUIVALENT OF HSYNC.
M	O	M SIGNAL FOR PANEL AC DRIVE CONTROL (MAY ALSO BE CALLED ACDCLK). MAY ALSO BE CONFIGURED AS BLANK# OR AS DOSPLAY ENABLE (DE)FOR TFT PANEL.
ENAVDD ENAVEE	O	POWER SEQUENCING CONTROLA FOR PANEL DRIVER ELECTRONICS VOLTAGE VDD AND PANEL LCD BIAS VOLTAGE VEE.
ACTI ENBKL	I/O	AVTIVITY INDICATOR AND ENABLE BACKLIGHT OUTPUT. MAY BE CONFIGURED FOR OTHER FUNCTIONS.
HSYNC	O	CRT HOROZONTAL SYNC (POLARITY IS PROGRAMABLE) OR " COMPOSITE SYNC " FOR SUPPORT OF VARIOUS EXTERNAL NTSC /PAL ENCODER CHIP (SEE ALSO XR27)
VSYNC	O	CRT VERTICAL SYNC (POLARITY IS PROGRAMABLE)OR "VSYNC INTERVAL"FOR SUPPORT OF VARIOUS EXTERNAL NTSC /PAL ENCODER CHIP (SEE ALSO XR27)
RED GREEN BLUE	O	CRT ANALOG VIDEO OUTPUT FROM THE INTERMAL COLOR PALETTE DAC.
RSET	I	SET POINT RESISTOR FOR THE INTERNAL COLOR PALETTE DAC.
AVCC AVGND		ANALOG POWER AND GROUND PINS FOR NOISE ISOLATION FOR THE INTERNAL COLOR PALETTE DAC.
XTALI	I	CRYSTAL IN. THIS PINS SERVES AS THE INPUT FOR AN EXTERNAL REFERENCE OSCILLATOR (USUALLY 14.31818 MHZ)

SYMBOL	TYPE	DESCRIPTION
CVCC0 CGND0 CVCC1 CGND1		ANALOG POWER AND GROUND PINS FOR NOISE ISOLATION FOR THE INTERNAL COLOR SYNTHESIZER.MUST BE THE AS VCCFOR INTERNAL LOGIC.
32KHZ	I	CLOCK INPUT FOR REFRESH OF NON -SELF -REFRESH DRAMS AND PANEL POWER SEQUENCING.
STNDBY#	I	STANDBY CONTROL PIN.PULLING THIS PIN TO GROUND PLACES THE 65548 IN STANDBY MODE.
IVCC IGND IVCC IGND		POWER /GROUND (INTERNAL LOGIC).5V±10% OR 3.3V±0.3V .NOTE THAT THIS VOLTAGE MUST BE THE SAME SA CVCC (VOLTAGE FOR INTERNAL CLOCK SYNTHESIZER)
BVC BGND BGND BVC BGND BGND		POWER /GROUND (BUS INTERFACE).5V+10% OR 3.3V+0.3V
DVCC DGND DGND		POWER /GROUND (DISPLAY INTERFACE).5V±10% OR 3.3V +0.3V
MVCCA MGNDA MVCCA MGNDA MVCCA MGNDA		POWER /GROUND (MEMORY INTERFACE A). 5V±10% OR 3.3V±0.3V. POWER /GROUND (MEMORY INTERFACE B). 5V±10% OR 3.3V±0.3V. POWER /GROUND (MEMORY INTERFACE C). 5V±10% OR 3.3V±0.3V.

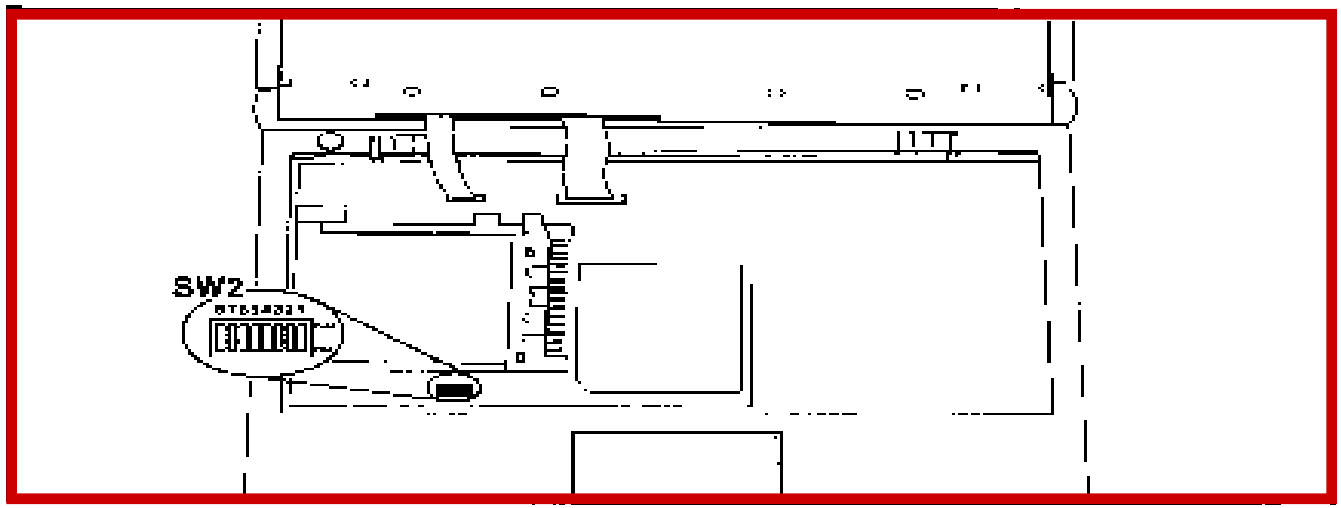
5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.6 PC87C334 SUPER I/O CONTROLLER.

SYMBOL	TYPE	DESCRIPTION
3F3RD	O	3F3 READ
ADRATE0,1	O	ADDITIONAL DATA RATE0,1
A10-A0	I	ADDRESS
ACK	I	ACKNOWLEDGE
AFD	I	AUTOMATIC FEED XT
AEN	I	ADDRESS ENABLE
ASTRB	O	ADDRESS STROBE
BARDR0,1	I	BASE ADDRESS
BOUT1,2	O	BAUD OUTPUT
BUSY	I	BUSY
CFG0-4	I	DEFAULT CONFIGURATION
CLK48	I	CLOCK 48.
CTS1,2	I	CLEAR TO SEND.
D7-D0	I/O	DATA.
DCD1,2	I	DATA CARRIER DATECT.
DENSEL	O	DENSITY SELECT.
DIR	O	DIRECTION
DR0,1	O	DRIVE SELECT 0,1
DRATE0,1	O	DATA RATE 0,1
DRID0,1	I	DRIVE ID
DRV2	I	DRIVE2
DR23	I	DRIVE 2 OR 3
DSKCHG	I	DISK CHANGE
DSR1,2	I	DATA SET READY.
DSTRB	O	DATA STROBE.
DTR1,2	O	DATA TERMINAL READY.
ERR	I	ERROR
FDACK	I	DMA ACKNOWLDGE
FDRQ	O	DMA REQUEST
HCS0	O	HARD DRIVE CHIP SELECT 0.
HCS1	O	HARD DRIVE CHIP SELECT 1.
HDSEL	O	HEAD SELECT.
IDEACK		IDE DMA ACKNOEW LEDGE.
IDED7	I/O	IDE BIT 7.
IDEHI	O	IDE HIGH BYTE.
IDELO	O	IDE LOW BYTE.
IDENT	I	IDENTITY.
IDLE	O	IDLE.
IOCHRDY	O	I/O CHANNEL READY.
INDEX	O	INDEX.
INIT	I/O	INITALIZE.
IOCS16	I	I/R CHIP SELECT 16-BIT

SYMBOL	TYPE	DESCRIPTION
IRQ3,4	O	INTERRUPT 3 AND 4.
IRQ5	I/O	INTERRUPT 5
IRQ6	O	INTERRUPT 6
IRQ7	I/O	INTERRUPT 7
IRRX	I	INFRARED RECEIVE.
IRTX	O	INFRARED TRANSMIT.
MR	I	MASTER RESET.
MFM	I/O	MFM.
MTR0,1	O	MOTOR SELECT 0,1.
MSEN0,1	I	MEDIA SENSE.
PD	O	POWER DOWN.
PD0-7	I/O	PARALLEL PORT DATA.
PDACK	I	PRINTER DMA REQEST.
PWDN	I	POWER DOWN.
PE	I	PAPER END.
PNF	I	PRINTER NOT FLOPPY.
RD	I	READ.
RDATA	I	READ DATA.
RI1,2	I	RING INDICATOR.
RTS1,2	O	REQUEST TO SENT.
SIN1,2	I	SERIAL INPUT.
SLCT	I	SELECT.
SLIN	I/O	SELECT INPUT.
SOUT1,2	O	SERIAL OUTPUT.
STB	I/O	DATA STROBE.
STEP	O	STEP.
TC	I	TERMINAL COUNT.
TRK0	I	TRACK 0.
VDDB,C		POWER SUPPLY.
VLD0,1	I	VALID DATA.
VSSB-E		GROUND.
WAIT	I	WAIT.
WR	I	WRITE.
WDATA	O	WRITE DATA.
WGATE	O	WRITE GATE.
WP	I	WRITE PROTECT.
WRITE	O	WRITE STROBE.
X1/OSC	I	CRYTAL1/CLOCK.
X2	O	CRYTAL2.
ZWS	O	ZERO WAIT STATE.

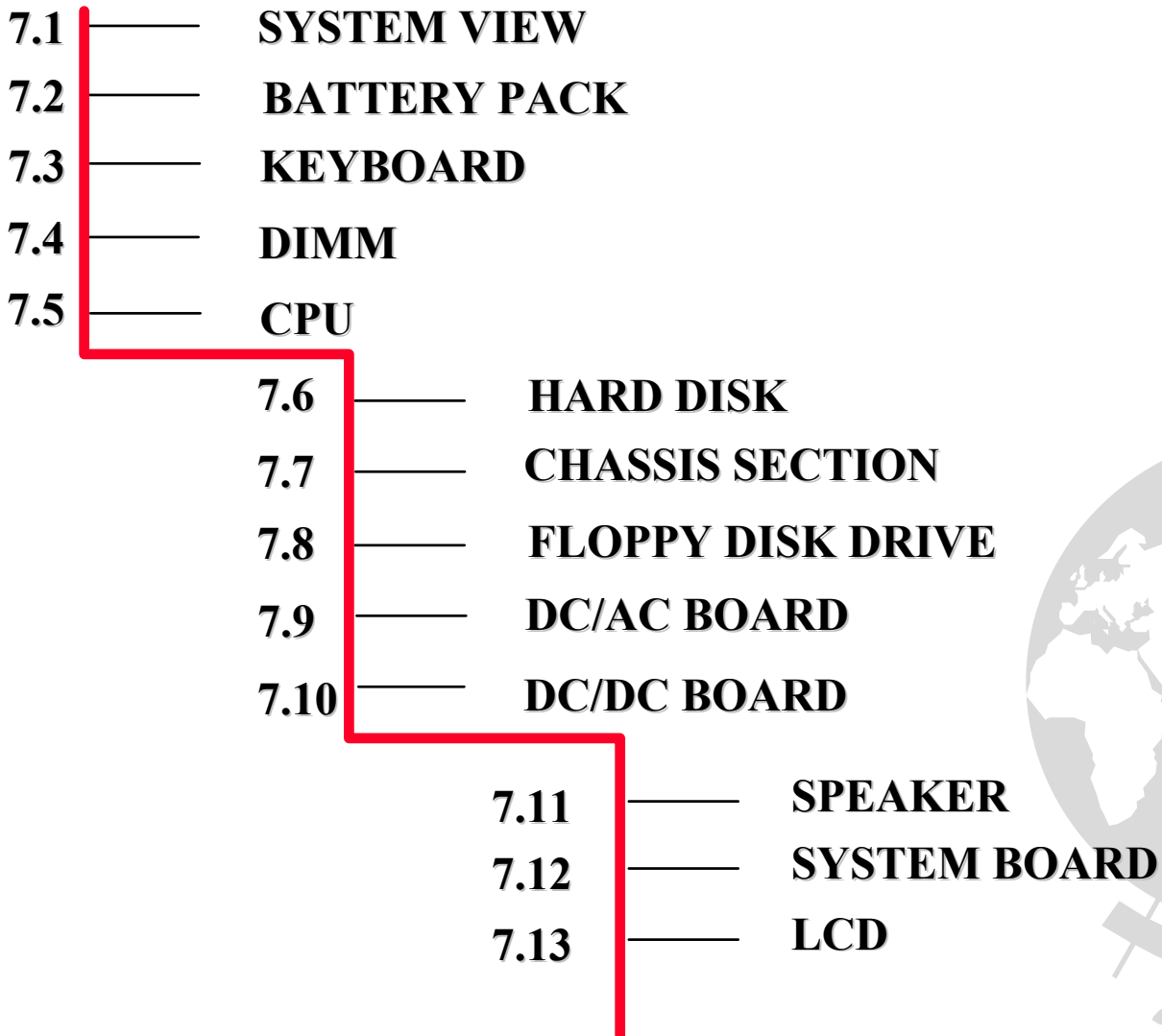
6. SWITCH SETTING



NOTE: TO ACCESS THE SWITCH, REMOVE THE KEYBOARD AND SHIELD PLATE.

CPU TYPE	SW 2							
	1	2	3	4	5	6	7	8
INTEL P54LM -75	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
INTEL P54LM 90	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
INTEL P54LM -100	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON

7. SYSTEM VIEW AND DISASSEMBLY



5023 N/B MAINTENANCE

7.1 SYSTEM VIEW

1. POWER CONNECTOR.
2. PC CARD SLOT.
3. BATTERY PACK.
4. TOP COVER LATCHES.

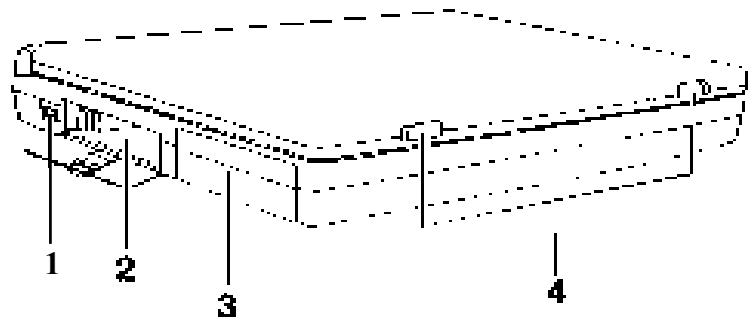


FIGURE 7-1. FRONT AND LEFT SIDE VIEWS

1. HARD DISK DRIVER COVER.
2. 3.5-INCH FLOPPY DISK DRIVE.
3. SIR PORT (COM2).
4. VOLUME CONTROL.
5. MIC IN CONNECTOR.
6. SPEAKER CONNECTOR.
7. LINE IN CONNECTOR.
8. AUXILIARY DEVICE PORT.
9. VIDEO PORT.
10. PARALLEL PORT.

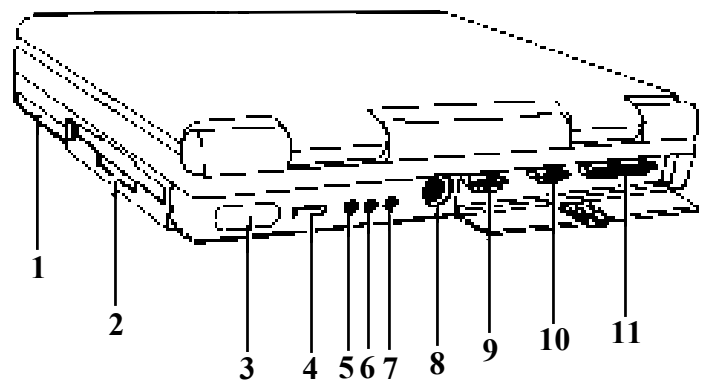


FIGURE 7-2. REAR AND RIGHT SIDE VIEWS

7.2 BATTERY PACK

DISASSEMBLY

1. PLACE THE COMPUTER UPSIDE DOWN.
2. RELEASE THE BATTERY PACK'S LATCH BY SLIDING IT AWAY FROM THE BATTERY PACK (FIGURE 7-3 ARROW A).
3. LIFT THE BATTERY PACK OUT OF ITS COMPARTMENT (FIGURE 7-3 ARROW B).

REASSEMBLY

1. REPLACE THE BATTERY PACK BACK INTO ITS COMPARTMENT.
2. SLIDE THE LATCH TOWARD THE BATTERY PACK TO LOCK IT INTO POSITION.

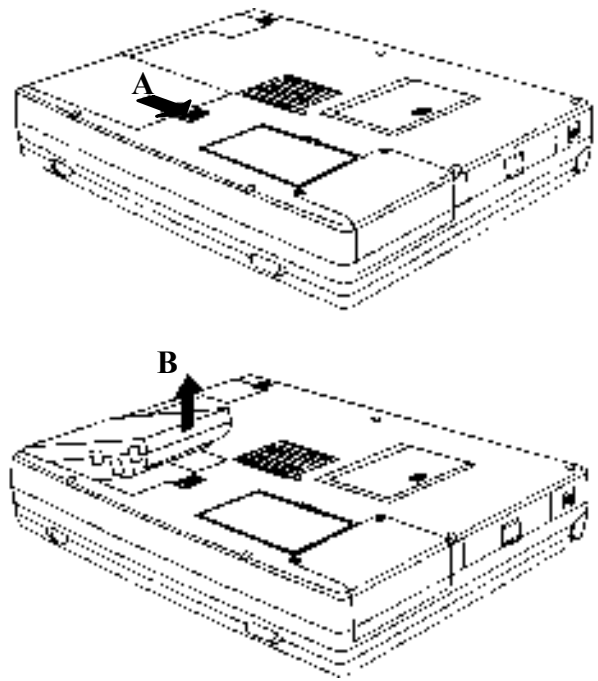


FIGURE 7-3. BATTERY PACK DISASSEMBLY/REASSEMBLY

7.3 KEYBOARD

DISASSEMBLY

1. OPEN THE TOP COVER OF THE NOTEBOOK.
2. SLIDE THE TWO KEYBOARD LATCHES INWARD (FIGURE 7-4 ARROW A).
3. LEVER UP THE SMALL TABS (FIGURE 7-4 ARROW B) AND DETACH THE KEYBOARD.
4. REMOVE ONE SCREW (FIGURE 7-4 #1) AND REMOVE THE SHIELD PLATE BY PUCHING THE THREE TABS (FIGURE 7-4 #2) DOWNWARD AND LIFTING UP.
5. UNPLUG THE TWO KEYBOARD CABLES (FIGURE 7-4 #3).

REASSEMBLY

1. RECONNECT THE TWO KEYBOARD CABLES (FIGURE 7-4 #1).
2. FIT THE SHIELD PLATE BACK INTO PLACE AND SECURE WITH ONE SCREW (FIGURE 7-4 #1).
3. INSERT THE THREE BOTTOM HOOKS (FIGURE 7-4 #3) TO THE NOTEBOOK CHASSIS AT AN ANGLE AND THEN LAY DOWN THE KEYBOARD.
4. SLIDE THE TWO KEYBOARD LATCHES OUTWARD TO LOCK THE KEYBOARD IN POSITION.

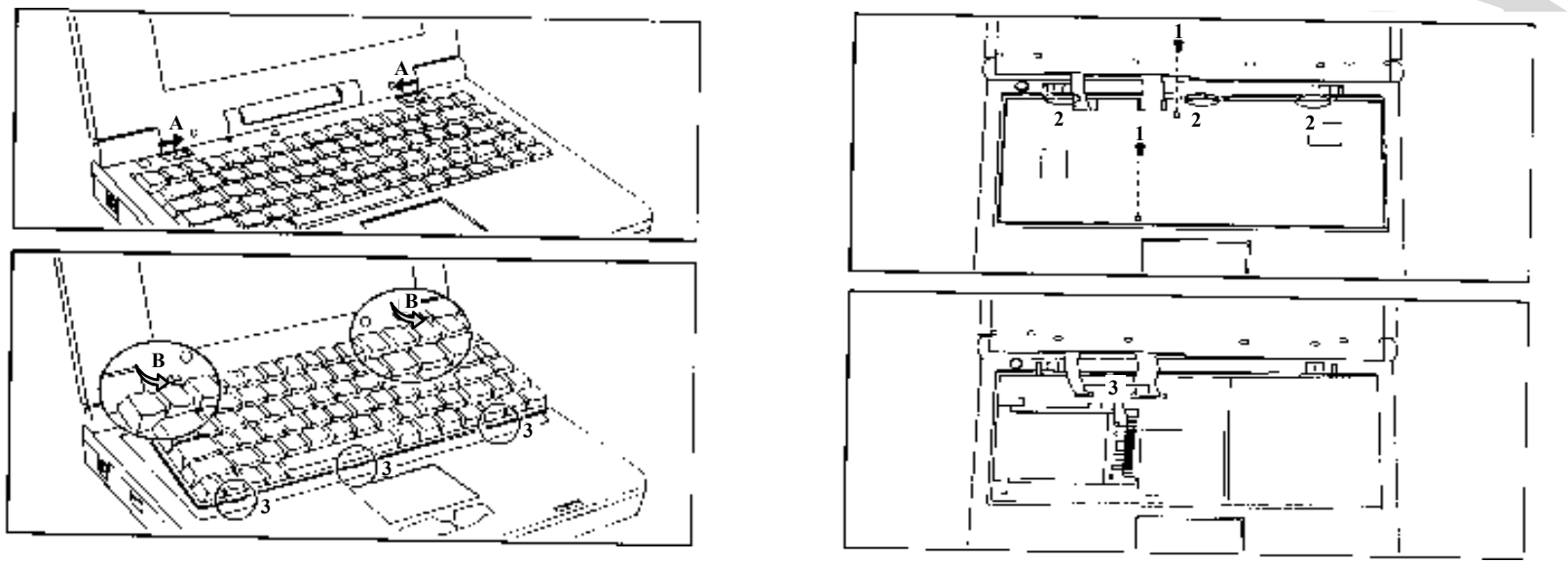


FIGURE 7-4. KEYBOARD DISASSEMBLY/REASSEMBLY

7.4 DIMM

DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. REMOVE THE ACCESS COVER FOR DIMM 0 AND DIMM 1.
3. TO REMOVE THE DIMM, FIRST FORCE THE TWO RETAINING CLIPS OUTWARD (FIGURE 7-5 ARROW A) SO THAT THE DIMM COMES LOOSE, THEN PULL OUT THE DIMM (FIGURE 7-5 ARROW B).

REASSMEBLY

1. TO INSTALL THE DIMM, ALIGN THE DIMM'S NOTCHED END WITH THE SOCKET'S CORRESPONDING END AND FIRMLY INSERT THE DIMM INTO THE SOCKET AT AN ANGLE. THEN PUSH DOWN UNTIL THE RETAINING CLIPS LOCK THE DIMM INTO POSITION.
2. REPLACE THE ACCESS COVER.

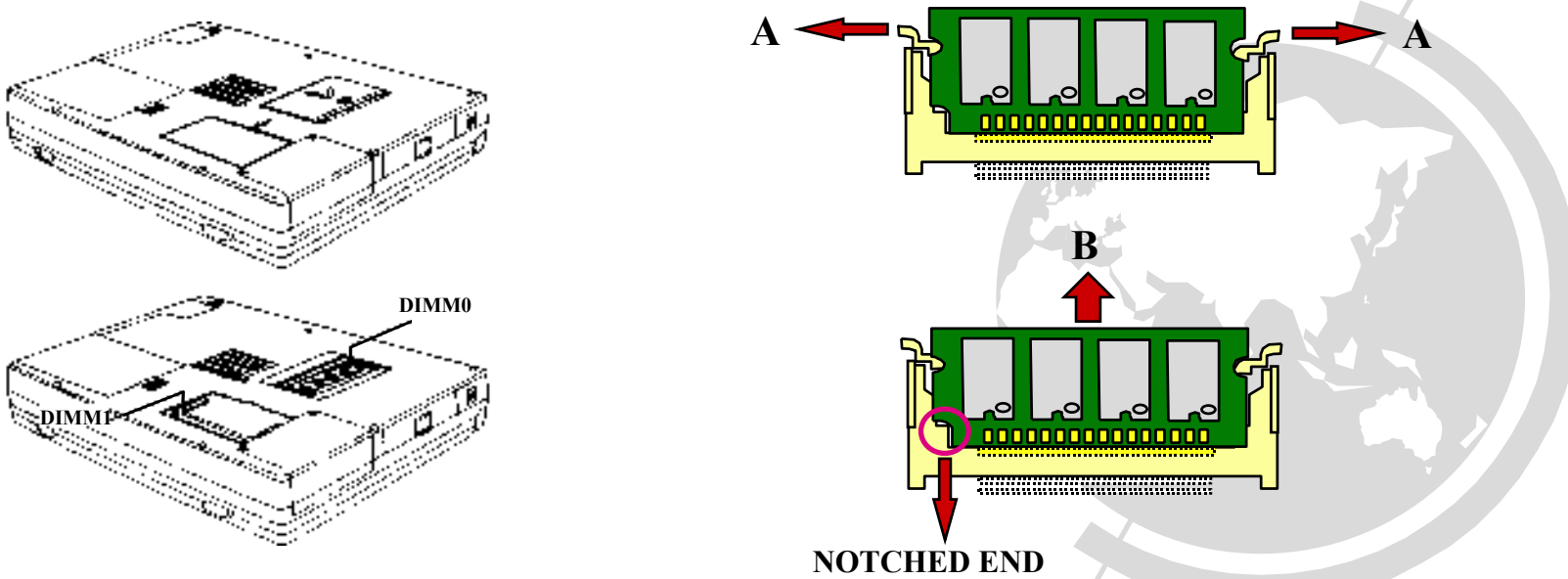


FIGURE 7-5. MEMORY MODULE DISASSEMBLY/REASSEMBLY

7.5 CPU

DISASSEMBLY

1. DETACH THE KEYBOARD WITHOUT UNPLUGGING THE KEYBOARD CABLES. (SEE SECTION 7.3 DISASSEMBLY STEPS 1 TO 4).
2. USE AN EXTRACTION TOOL TO REMOVE THE CPU.

REASSEMBLY

1. INSTALL THE CPU.
2. REPLACE THE KEYBOARD. (SEE SECTION 7-3 REASSEMBLY STEPS 2 TO 4).

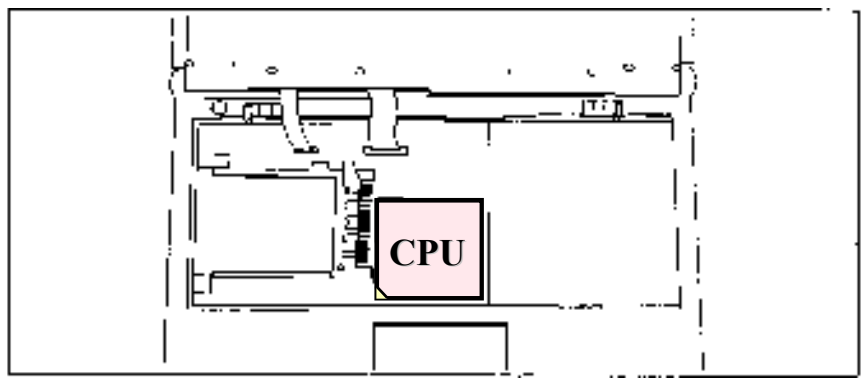


FIGURE 7-6. CPU DISASSEMBLY/REASSEMBLY

7.6 HARD DISK

DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. REMOVE THE TWO SCREWS (FIGURE 7-7 #1) FROM THE HARD DISK ACCESS COVER.
3. REMOVE THE ACCESS COVER BY PRESSING IN THE COVER SIDE (FIGURE 7-7 ARROW A).
4. UNPLUG THE HARD DISK CABLE.
5. SLIDE THE HARD DISK OUT OF THE COMPARTMENT.

REASSEMBLY

1. SLIDE THE HARD DISK INTO ITS COMPARTMENT.
2. RECONNECT THE HARD DISK CABLE.
3. REPLACE THE ACCESS COVER AND SECURE WITH TWO SCREWS (FIGURE 7-7 #1).

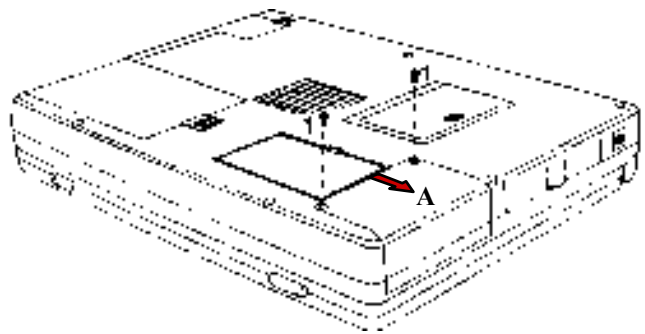


FIGURE 7-7. HARD DISK DISASSEMBLY/REASSEMBLY

7.7 CHASSIS SECTION

DISASSEMBLY

1. REMOVE THE BATTERY PACK. (SEE SECTION 7-2 DISASSEMBLY).
2. REMOVE THE KEYBOARD. (SEE SECTION 7-3 DISASSEMBLY).
3. PUT THE NOTEBOOK UPSIDE DOWN. REMOVE THE TWO SCREWS (FIGURE 7-8 #1) FROM THE BATTERY PACK COMPARTMENT.
4. REMOVE THE SEVEN BOTTOM SCREWS (FIGURE 7-8 #2).
5. UNPLUG THE CABLES BETWEEN THE NOTEBOOK BODY AND THE AHASSIS SECTION.
6. SEPARATE THE CHASSIS FROM THE NOTEBOOK BODY.

REASSEMBLY

1. PUT THE CHASSIS UPRIGHT. RECONNECT THE CONNECTORS FROM THE NOTEBOOK BODY TO THE CHASSIS SECTION.
2. ALIGN THE NOTEBOOK BODY WITH THE CHASSIS BY FIRST ALIGNING THE POWER BUTTON AND SUSPEND BUTTON WITH THE CORRESPONDING OPENING. THEN FIX THE NOTEBOOK BODY AND CHASSIS TOGETHER. BE CAREFUL NOT TO LEAVE ANY CABLES OUTSIDE.
3. CAREFULLY PLACE THE NOTEBOOK UPSIDE DOWN. REPLACE THE NINE SCREWS (FIGURE 7-8 #1).
4. REPLACE THE KEYBOARD. (SEE SECTION 7-3 REASSEMBLY).
5. REPLACE THE BATTERY PACK. (SEE SECTION 7-2 REASSEMBLY).

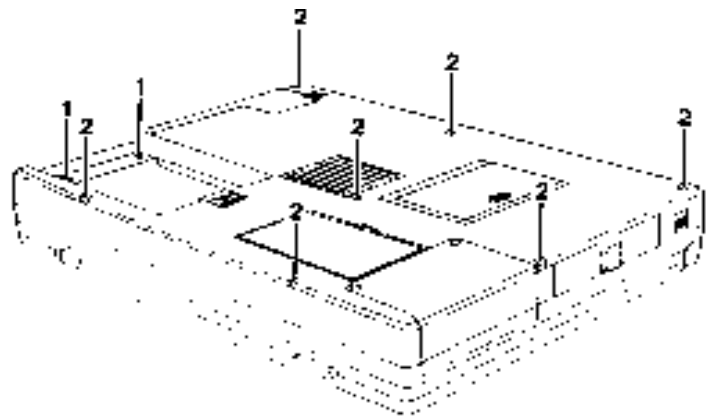


FIGURE 7-8. CHASSIS SECTION DISASSEMBLY/REASSEMBLY

7.8 FLOOPY DISK DRIVE

DISASSEMBLY

1. SEPARATE THE CHASSIA SECTION FROM THE NETEBOOK BODY. (SEE SECTION 7.7 DISASSEMBLY).
2. UNPLUG THE AUDIO CABLE (FIGURE 7-9 #1) AND MICROPHONE CABLE (FIGURE 7-9 #2).
3. REMOVE THE TAPES THAT ATTACH THE AUDIO AND MICROPHONE CABLE TO THE FLOPPY DISK DRIVE.
4. UNPLUG THE FLOPPY DISK DRIVE DATA CABLE (FIGURE 7-9 #3).
5. TO REMOVE THE FLOPPY DISK DRIVE, FIRST LIFT UP ITS END (FIGURE 7-9 ARROW A) TO UNLOCK AND THEN SLIDE IT OUT OF ITS COMPARTMENT (FIGURE 7-9 ARROW B).

REASSEMBLY

1. TO REPLACE THE FLOPPY DISK DRIVE, FIRST SLIDE IT ALL THE WAY INTO THE COMPARTMENT WITH ITS END LIFTED AND THEN PRESS DOWN THE END TO LOCK THE DISK DRIVE INTO PLACE.
2. RECONNECT THE DATA CALE (FIGURE 7-9 #3).
3. RECONNECT THE AUDIO CABLE (FIGURE 7-9 #1) AND THE MICROPHONE CABLE (FIGURE 7-9 #2). FIT THE CABLES TO THE CORRESPONDING NOTCHES (FIGURE 7-9 #4).
4. REPLACE THE TAPES.
5. REPLACE THE CHASSIS. (SEE SECTION 7.7 REASSEMBLY).

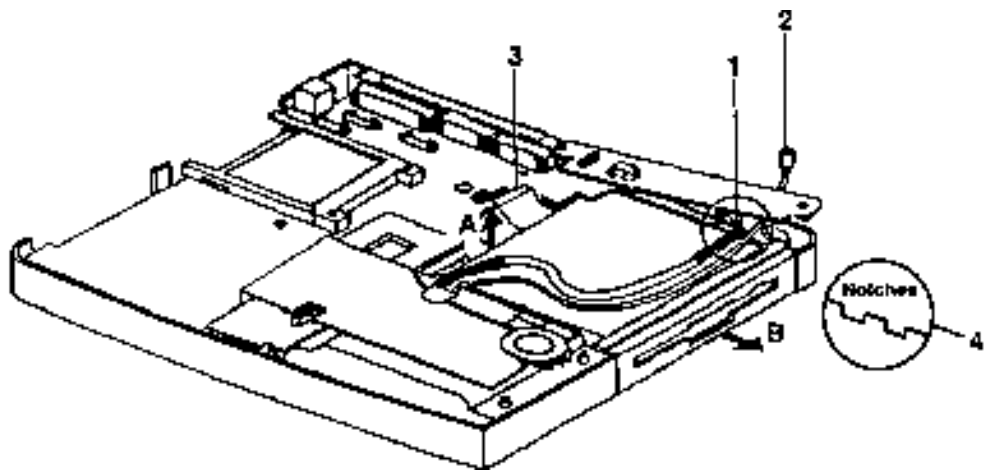


FIGURE 7-9. FLOPPY DISK DRIVE DISASSEMBLY/REASSEMBLY

7.9 DC/AC BOARD

DISASSEMBLY

1. SEPARATE THE CHASSIS SECTION FROM THE NOTEBOOK BODY. (SEE SECTION 7.7 DISASSEMBLY).
2. UNPLUG THE TWO CABLES FROM THE DC/AC BOARD.
3. REMOVE ONE SCREW (FIGURE 7-10 #1) AND LIFT THE DC/AC BOARD FREE.

REASSEMBLY

1. FIX THE DC/AC BOARD INTO PLACE AND REPLACE THE SCREW (FIGURE 7-10 #1).
2. RECONNECT THE TWO CABLES.
3. REPLACE THE CHASSIS. (SEE SECTION 7.7 REASSEMBLY).

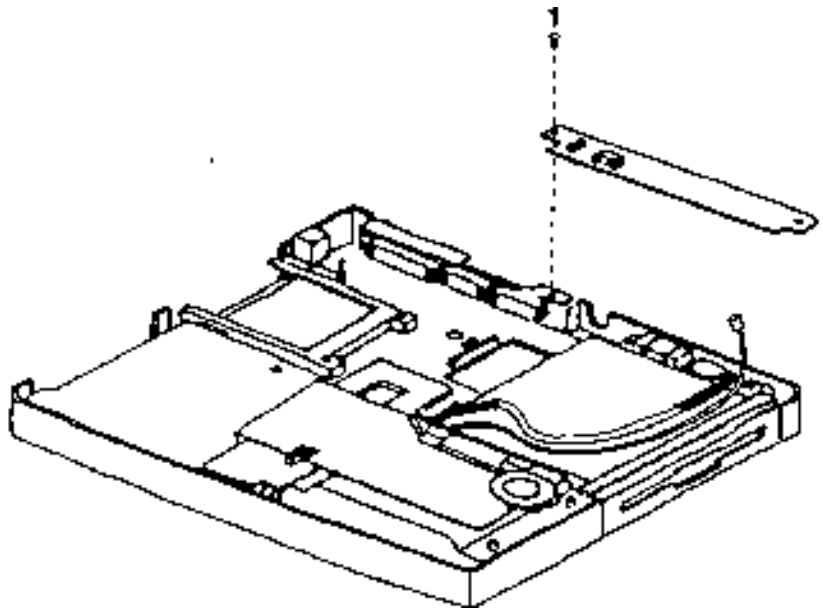


FIGURE 7-10. DC/AC BOARD DISASSEMBLY/REASSEMBLY

7.10 DC/DC BOARD

DISASSEMBLY

1. SEPARATE THE CHASSIS SECTION FROM THE NOTEBOOK BODY. (SEE SECTION 7.7 DISASSEMBLY).
2. LIFT ONE END OF THE SHIELD PLATE (FIGURE 7-11 ARROW).
3. UNPLUG THE CABLE (FIGURE 7-11 #1) FROM THE DC/DC BOARD.
4. REMOVE ONE SCREW (FIGURE 7-11 #2) AND LIFT THE DC/DC BOARD DREE.

REASSEMBLY

1. FIX THE DC/DC BOARD INTO PLACE AND REPLACE THE SCREW (FIGURE 7-11 #2).
2. RECONNECT THE CABLE (FIGURE 7-11 #1).
3. REPLACE THE SHIELD PLATE.
4. REPLACE THE CHASSIS. (SEE SECTION 7-7 REASSEMBLY).

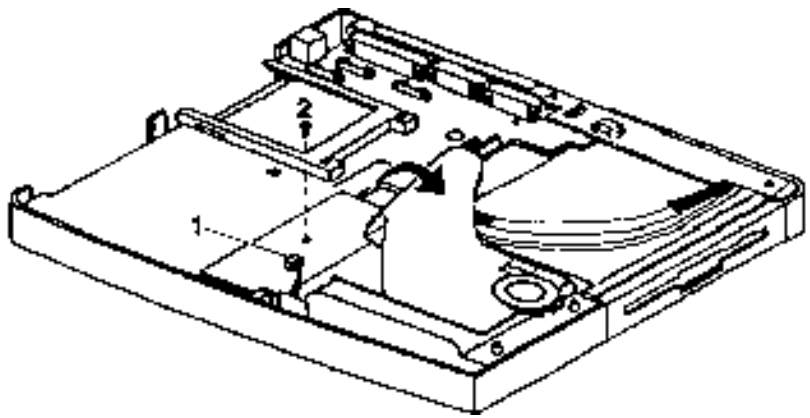


FIGURE 7-11. DC/DCBOARD DISASSEMBLY/REASSEMBLY

7.11 SPEAKER

DISASSEMBLY

1. SEPARATE THE CHASSIS SECTION FROM THE NOTEBOOK BODY. (SEE SECTION 7.7 DISASSEMBLY).
2. UNPLUG THE SPEAKER CABLE (FIGURE 7-12 #1).
3. REMOVE THE SPEAKER BY PULLING IT OFF THE CHASSIS.

REASSEMBLY

1. ALIGN THE SPEAKER WITH ITS SEAT IN THE WAY THAT THE METAL PARTS ON THE BOTTOM OF THE SPEAKER CONTAINING THE CABLE ENDS FACE THE RIGHT. THE PURPOSE IS TO AVOID THE METAL PARTS CONTACT WITH THE PLASTIC SURFACE OF THE CHASSIS. THEN, ATTACH THE SPEAKER TO ITS SEAT WITH THE TAPE PROVIDED.
2. FIX THE CABLE IN THE FOLDS (FIGURE 7-12 #2) AND RECONNECT THE CABLE (FIGURE 7-12 #1).
3. REPLACE THE CHASSIS. (SEE SECTION 7.7 REASSEMBLY).

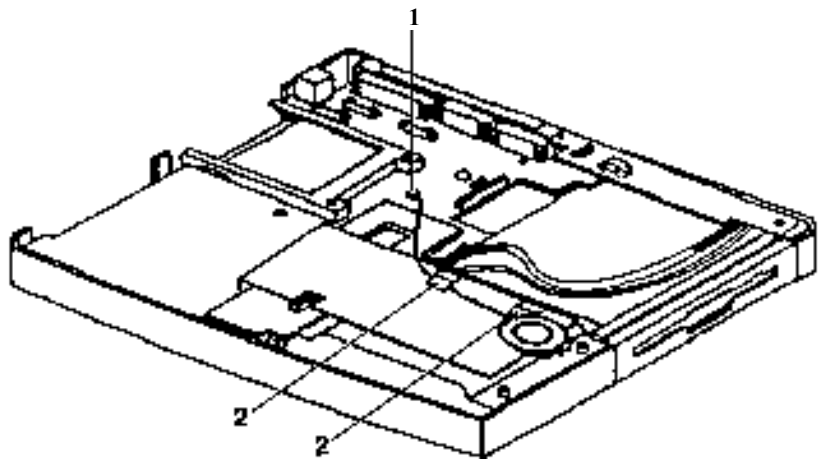


FIGURE 7-12. SPEAKER DISASSEMBLY/REASSEMBLY

7.12 SYSTEM BOARD

DISASSEMBLY

1.REMOVE THE HARD DISK DRIVE. (SEE SECTION 7.6 DISASSEMBLY).
2. SEPARATE THE CHASSIS SECTION FROM THE NOTEBOOK BODY. (SEE SECTION 7.7 DISASSEMBLY).
3. REMOVE THE DC/DC BOARD. (SEE SECTION 7.10 DISASSEMBLY).
4. REMOVE THE DC/AC BOARD. (SEE SECTION 7.9 DISASSEMBLY).
5. UNPLUG ALL CONNECTORS FROM THE SYSTEM BOARD.
6. REMOVE ONE SCREW (FIGURE 7-13 #1) FROM THE SYSTEM BOARD.
7. LIFT THE SYSTEM BOARD FREE.

REASSEMBLY

1. ALIGN THE SYSTEM BOARD WITH THE CHASSIS AND REPLACE THE SCREW (FIGURE 7-13 #1).
2. RECONNECT ALL CONNECTORS.
3. REPLACE THE DC/AC BOARD. (SEE SECTION 7.9 REASSEMBLY).
4. REPLACE THE DC/DC BOARD. (SEE SECTION 7.10 REASSEMBLY).
5. REPLACE THE CHASSIS. (SEE SECTION 7.7 REASSEMBLY).
6. REPLACE THE HARD DISK DRIVE. (SEE SECTION 7.6 REASSEMBLY).

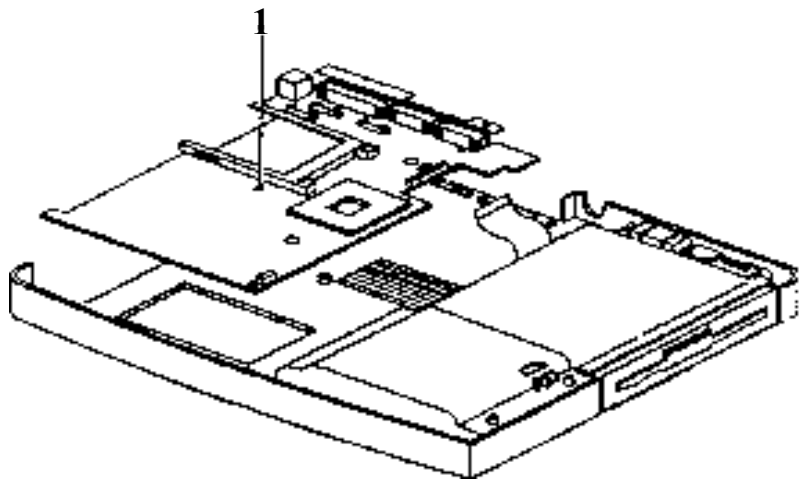


FIGURE 7-13. SYSTEM BOARD DISASSEMBLY/REASSEMBLY

5023 N/B MAINTENANCE

7.13 LCD

DISASSEMBLY

1. REMOVE THE HINGE COVERS BY INSERTING A FLAT SCREWDRIVER TO FORCE THEM OUT (FIGURE 7-14 ARROW).
2. OPEN THE LCD/COVER.
3. REMOVE THE FOUR SCREWS (FIGURE 7-14 #1) UNDER THE HINGE COVERS AND THE TWO SCREWS UNDER THE RUBBER CUSHIONS (FIGURE 7-14 #2).
4. CLOSE THE LCD/COVER AND SEPARATE THE LCD HOUSING FROM THE LCD.
5. UNPLUG ALL CONNECTORS FROM THE LCD.
6. REMOVE THE FOUR SCREWS (FIGURE 7-14 #3) SECURING THE LCD TO THE LCD PANEL AND LIFT THE LCD FREE.

REASSEMBLY

1. ALIGN THE LCD WITH THE LCD PANEL AND SECURE WITH FOUR SCREWS (FIGURE 7-14 #3).
2. RECONNECT ALL THE CABLES.
3. ALIGN AND FIX THE LCD HOUSING INTO PLACE.
4. REPLACE THE SIX SCREWS (FIGURE 7-14 #1 & #2).
5. CLOSE THE LCD/COVER.
6. REPLACE THE TWO HINGE COVERS.

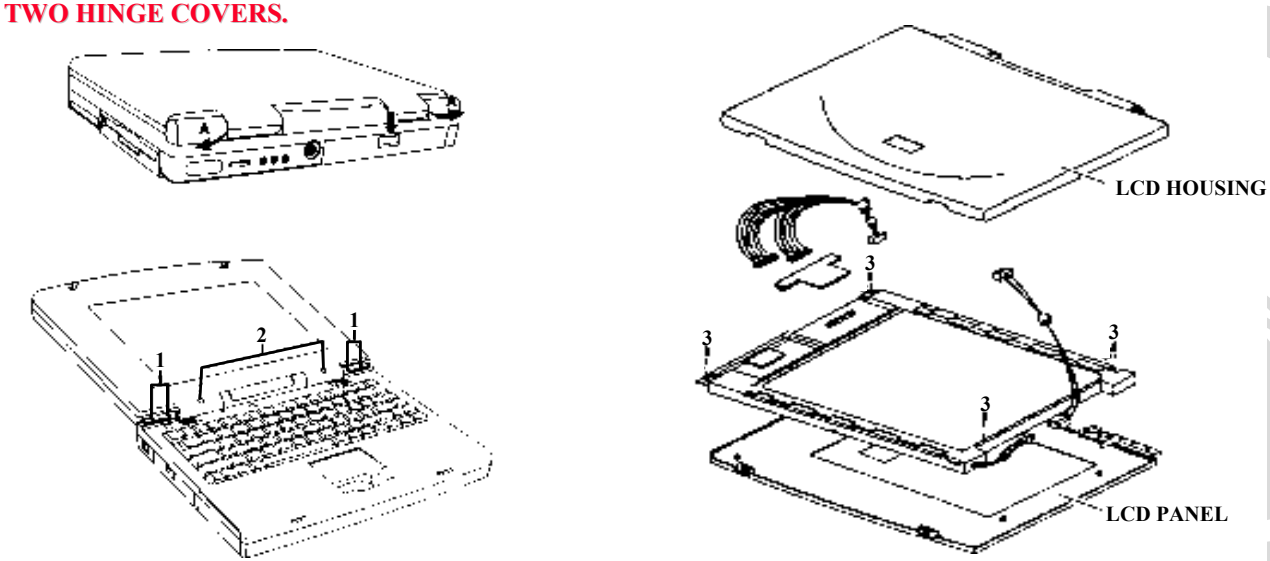


FIGURE 7-14. LCD DISASSEMBLY/REASSEMBLY

8. MAINTENANCE DIAGNOSTICS

8.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON, THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED,THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC PORT (378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE, IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO PORT 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

8. MAINTENANCE DIAGNOSTICS

8.2 ERROR CODES

FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

CODE	BEEP	DESCRIPTION
02		VERIFY REAL MODE
04		GET PCU TYPE
06		INITIALIZE SYSTEM HARDWARE
08		INITIALIZE CHIPSET REGISTERS WITH INITIAL POST VALUES
09		SET IN POST FLAG
0A		INITIALIZE CPU REGISTERS
0C		INITIALIZE CACHE TO INITIAL POST VALUES
0E		INITIALIZE I/O
0F		INITIALIZE THE LOCAL BUS IDE
10		INITIALIZE POWER MANAGEMENT
11		LOAD ALTERNATE REGISTERS WITH INITIAL POST VALUES
12		JUMP TO USERPATCH0
14		INITIALIZE KEYBOARD CONTROLLER
16	2-2-3	BIOS ROM CHECKSUM
18		8254 TIMER INITIALIZATION
1A		8237 DMA CONTROLLER INITIALIZATION
1C		RESET PROGRAMMABLE INTERRUPT CONTROLLER
20	3-1-1	TEST DRAM REFRESH
22	3-1-3	TEST 8742 KEYBOARD CONTROLLER
24		SET ES SEGMENT REGISTER TO 4GB
28		AUTOSIZE DRAM
2A		CLEAR 512K BASE RAM
2C	3-4-1	TEST 512K BASE ADDRESS LINES
2E	3-4-3	TEST 512K BASE MEMORY
32		TEST CPU BUS-CLOCK FREQUENCY
34		TEST CMOS RAM
35		INITIALIZE ALTERNATE CHIPSET REGISTERS.
37		REINITIALIZE THE CHIPSET(MB ONLY)
38		SHADOW SYSTEM BIOS ROM
39		REINITIALIZE THE CAHE(MB ONLY)

CODE	BEEP	DESCRIPTION
3A		AAUTOSIZE CACHE
3C		CONFIGURE ADVANCED CHIPSET REGISTERS
3D		LOAD ALTERNATE REGISTERS WITH CMOS VALUES
40		SET INITIAL CPU SPEED
42		INITIALIZE INTERRUPT VECTORS
44		INITIALIZE BIOS INTERRUPTS
46	2-1-2-3	CHECK ROM COYRIGHT NOTICE
47		INITIALIZE MANAGER FOR PCIOPTION ROMS
48		CHECK VIDEO CONFIGURATION AGAINST CMOS
49		INITIALIZE PCIBUS AND DEVICES
4A		INITIALIZE ALL VIDEO ADAPTER IN SYSTEM
4C		SHADOW VIDEO BIOS ROM
4E		DISPLAY COPYRIGHT NOTICE
50		DISPLAY CPU TYPE AND SPEED.
51		INITIALIZE EISA BOARD.
52		TEST KEYBOARD
54		SET KEY CLICK IF ENABLED.
56		ENABLED KEYBOARD.
58	2-2-3-1	TEST FOR UNEXPECTED INTERRUPTD
5A		DISPLAY PROMPT "PRESS F2 TO ENTER SETUP"
5C		TEST RAM BETWEEN 512 AND 640KB
60		TEST EXTENDED MEMORY.
62		TEST EXTENDED MEMORY ADDRES LINES
64		JUMP TO USERPATCH1
66		CONFIGURE ADVANCED CACHER REGISTERS
68		ENABLE EXTERNAL AN CPU CACHES
6A		DISPLAY EXTERNAL CACHE SIZE
6C		DISPLAY SHADOW MESSAGE
6E		DISPLAY NON-DISPOSABLE SEGMENTS
70		DISPLAY ERROR MESSAGES

(TO BE CONTINUED)

8. MAINTENANCE DIAGNOSTICS

CODE	BEEP	DESCRIPTION
72		CHECK FOR CONFIGURATION ERRORS
74		TEST REAL-TIME CLOCK
76		CHECK FOR KEYBOARD ERRORS
7C		SET UP HARDWARE INTERRUP VECTORS
7E		TEST COPROCESSOR IF PRESENT
80		DISABLE ONBOARD I/O PORTS
82		DETECT AN INSTALL EXTERNAL RS232 PROTS
84		DETECT AN INSTALL EXTERNAL PARALLEL PROTS
86		RE-INITIALIZE ONBOARD I/O PORTS
88		INITALIZE BIOS DATA AREA
8A		INITALIZE EXTENDED BIOS DATA AREA
8C		INITALIZE FLOPPY CONTROLLER
90		INITALIZE HARD-DISK CONTROLLER
91		INITALIZE LOCAL-BUS HARD-DISK CONTROLLER
92		JUMP TO USERPATCH2
93		BUILD MPTABL FOR MULIT-PROCESSOR BOARDS
94		DISABLE A20 ADDRESS LINE
96		CLEAR HUGE ES SEGMENT REGISTER
98		SEARCH FOT OPTION ROMS
9A		SHADOW OPTION ROMS
9C		SET UP POWER MANAGEMENT
9E		ENABLE HARDWARE INTERRUPTS
A0		SET TIME OF DAY
A2		CHECK KEY CLOCK
A4		INITALIZETYPEMATIC RATE
A8		ERASE F2 PROMPT
AA		SCAN FOR F2 KEY STROKE
AC		ENTER SETUP
AE		CLEAR IN-POST FLAG
B0		CHECK FOR ERRORS

CODE	BEEP	DESCRIPTION
B2		POST DONE-PREPARE TO BOOT OPERATING SYSTEM
B4		ONE BEEP
B6		CHECK PASSWORD(OPTIONAL)
B8		CLEAR GLOBAL DESCRIPTOR TABLE
BC		CLEAR PARITY CHECKERS
BE		CLEAR SCREEN(OPTION)
BF		CECK VIRUS AND BACKUP REMMINDERS
C0		TRY TO BOOT WITH INT19
D0		INTERRUPT HANDLER ERROR
D2		UNKNNOW INTERRUPT ERROR
D4		PENDING INTERRUPT ERROR
D6		INITALIZE OPTION ERROR
D8		SHUTDOWN ERROR
DA		EXTENDED BLOCK MOVE
DC		SHUTDOWN 10 ERROR
		THE FOLLOWING ARE FOR BOOT BLOCK IN FLASH ROM
E2		INITALIZE THE CHIPSET
E3		INITALIZE REFRESH COUNTER
E4		CHECK FOR FORCED FLASH
E5		CHECK HW STATUS OF ROM
E6		BIOS ROM IS OK
E7		DO A COMPLETE RAM TEST
E8		DO OEM INITALIZATION
E9		INITALIZE INTERRUPT CONTROLLERREAD IN THE BOOTSTRAP CODE
EA		READ IN THE BOOTSTRAP CODE
EB		INITALIZE ALL VECTORS
EC		BOOT THE FLASH PROGRAM
ED		INITALIZE TH BOOT DEVICE
EE		BOOT CODE WAS READ OK

8. MAINTENANCE DIAGNOSTICS

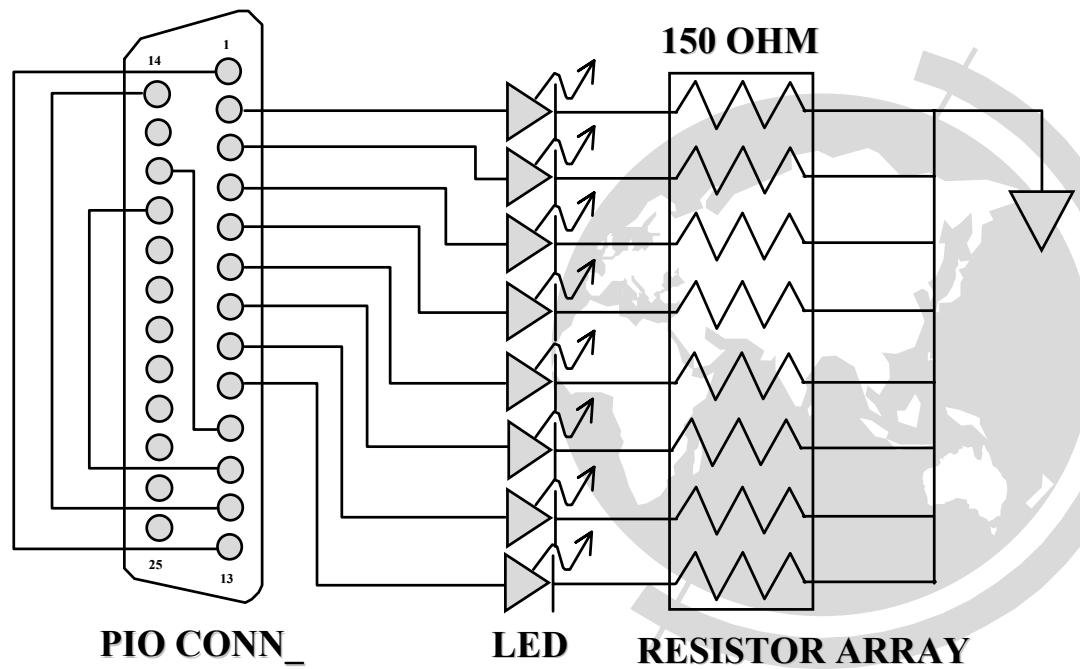
8.3 PIO PORT (378H) DIAGNOSTIC TOOLS

A. PARTS USED:

- LED * 8
- RESISTOR ARRAY, 10PIN, 150 OHM * 1
- PIO CONNECTOR * 1

B. CIRCUIT:

PIN1 : STROBE ⟷ PIN 13 : SLCT
PIN10: ACK# ⟷ PIN 16 : INT#
PIN11: BUSY ⟷ PIN 17 : SELIN#
PIN12: PTERR ⟷ PIN 14 : AUTOFD#
PIN{9:2}: PD{7:0}

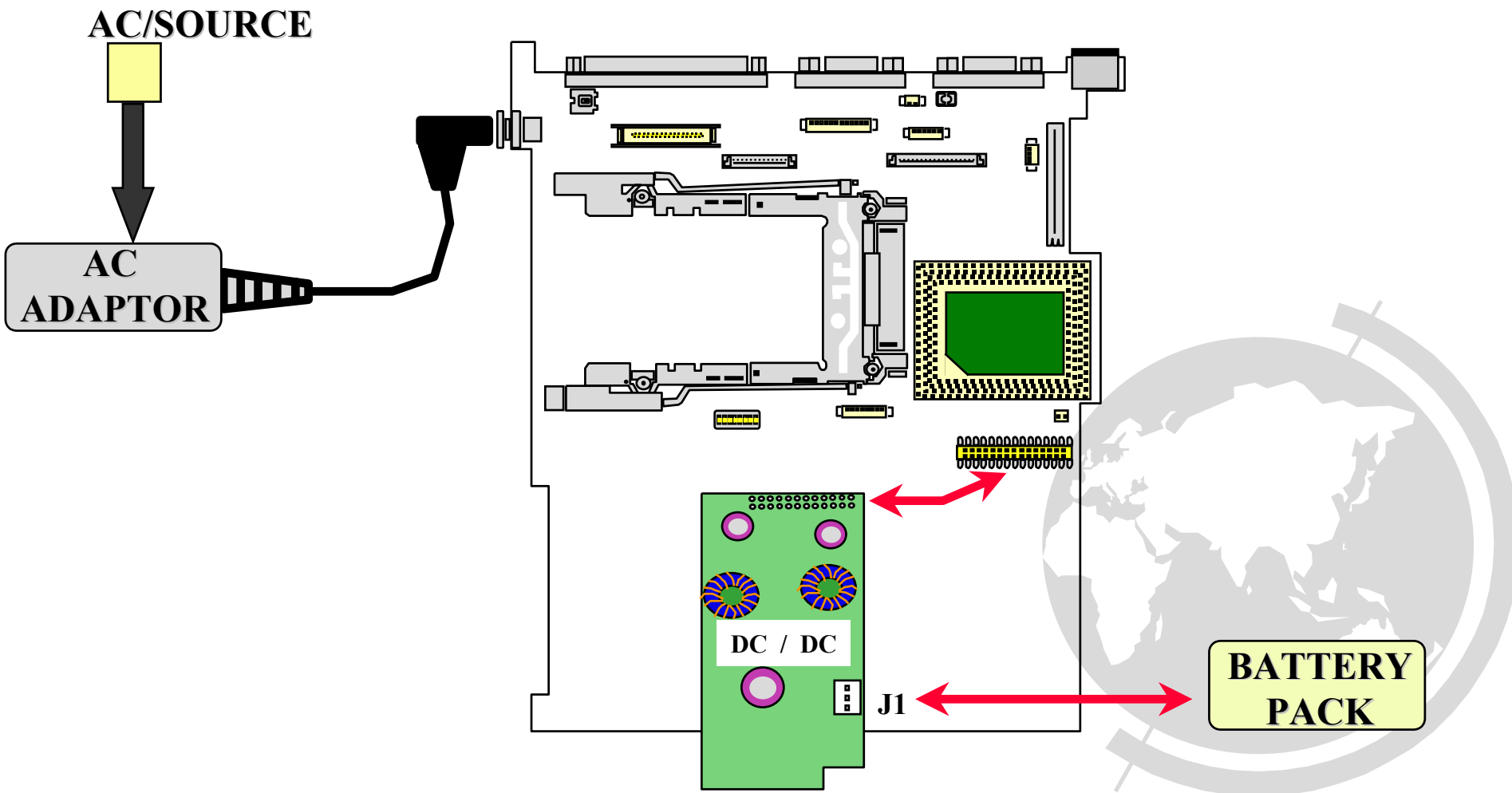


9. TROUBLE SHOOTING

9.1 NO POWER

SYMPTOM:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.

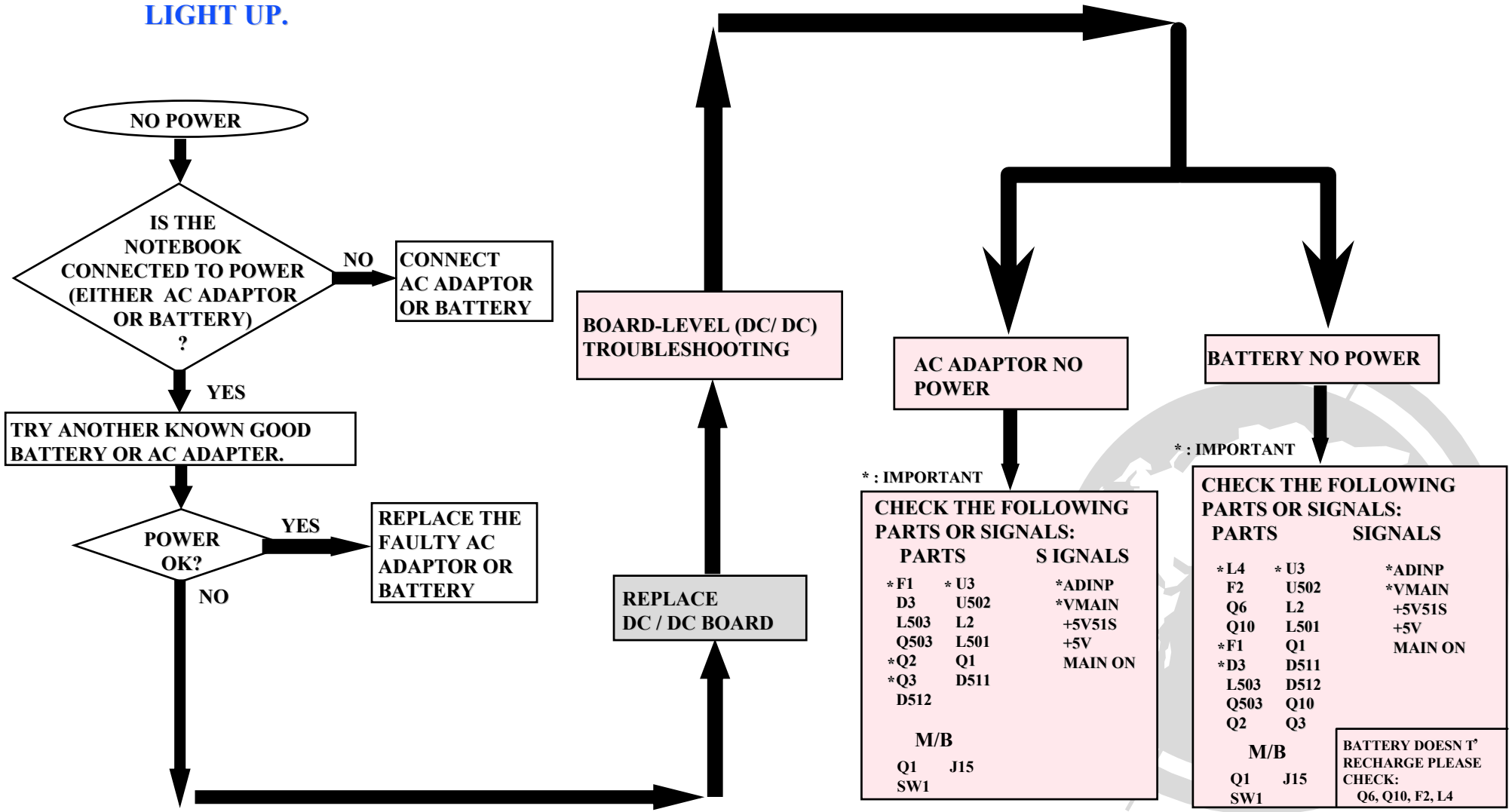


5023 N/B MAINTENANCE

9.1 NO POWER

SYMPTOM:

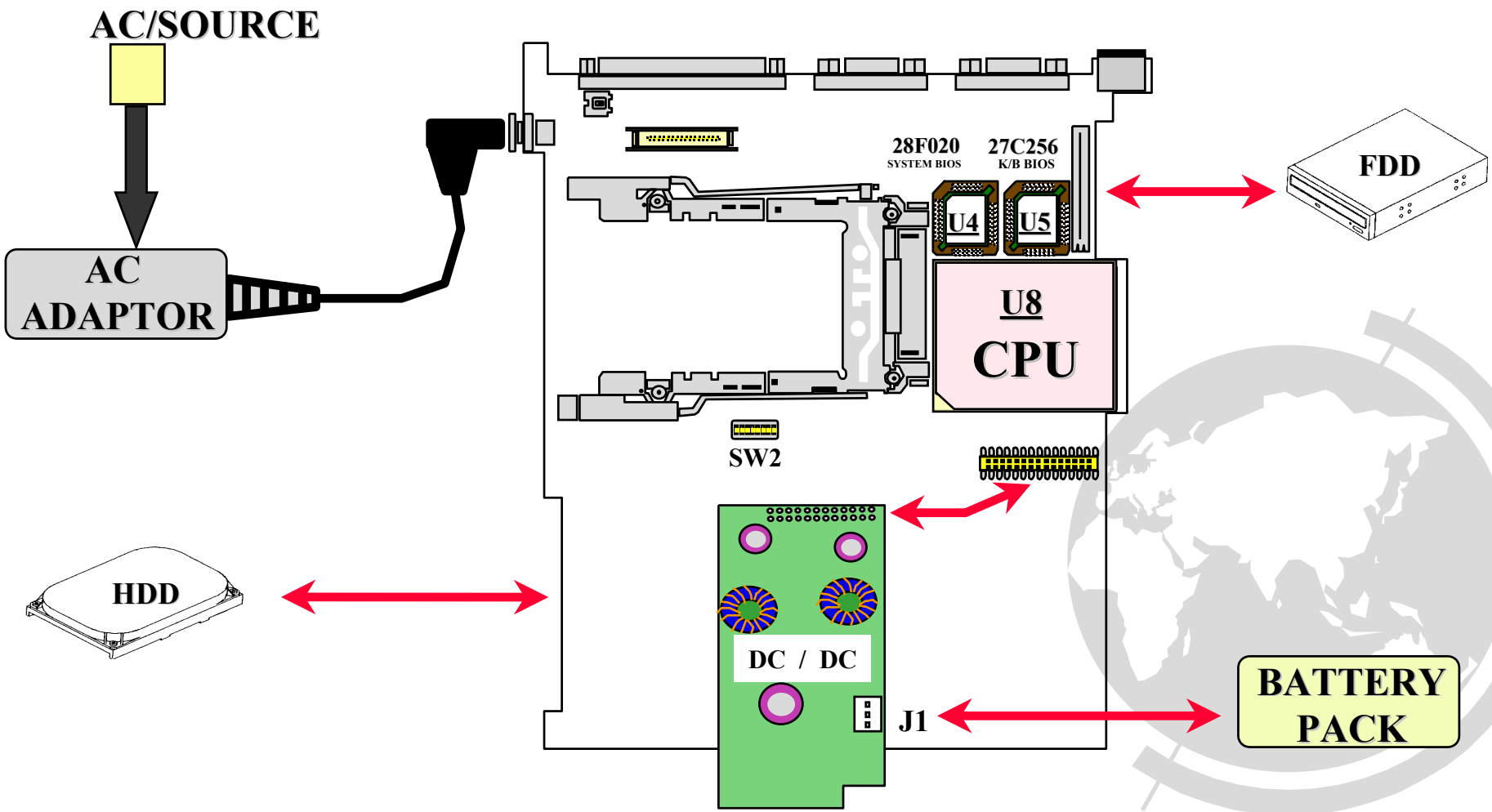
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



9.2 NO DISPLAY (SYSTEM FAILURE)

SYMPTOM:

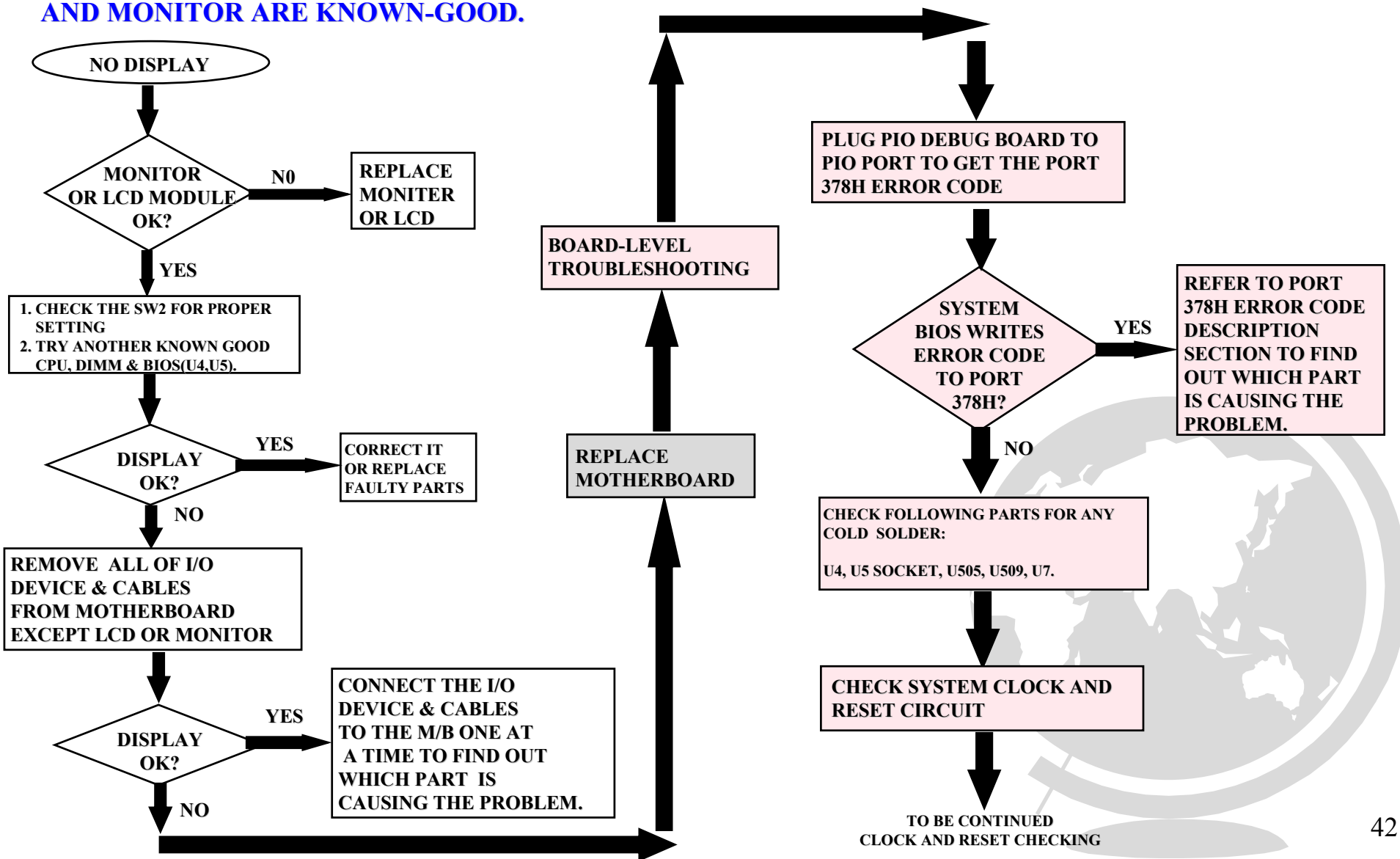
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



9.2 NO DISPLAY (SYSTEM FAILURE)

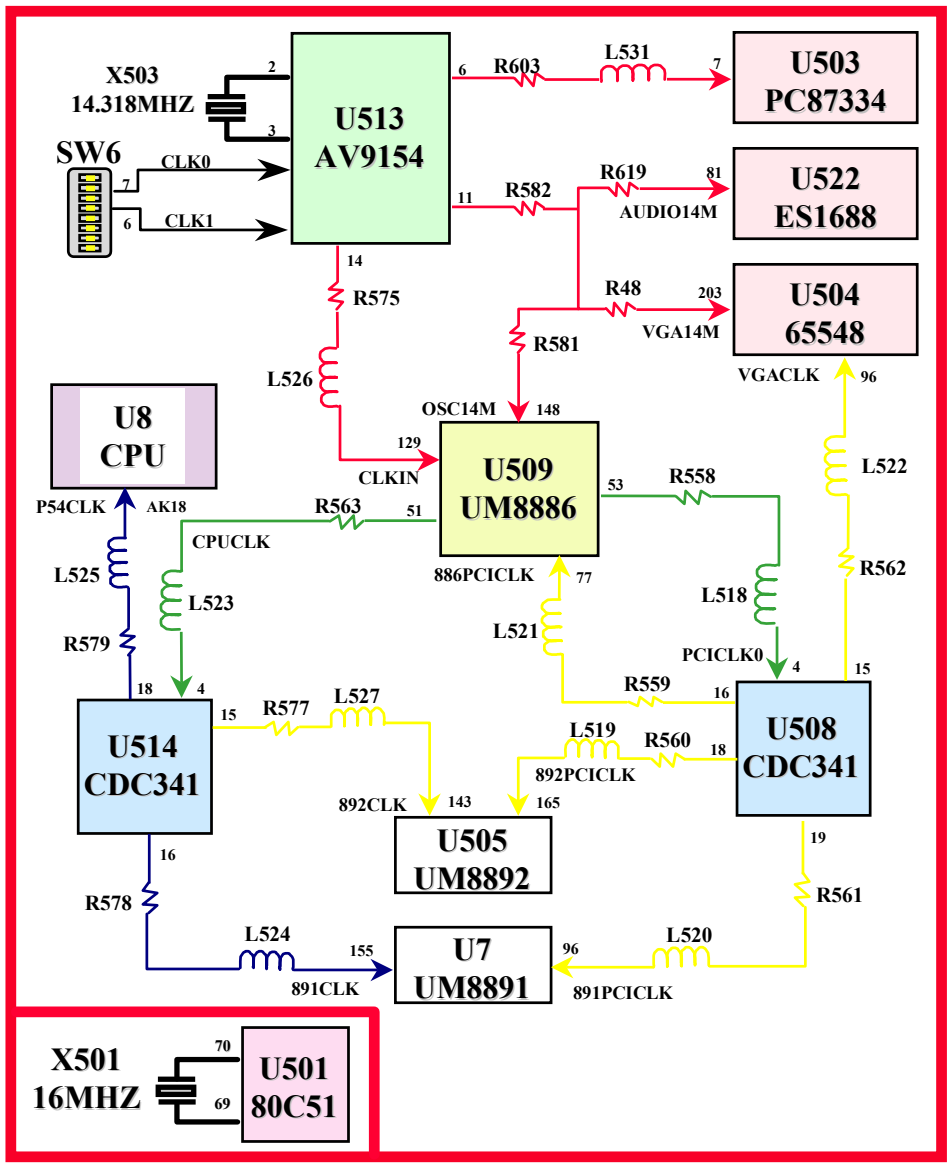
SYMPTOM:

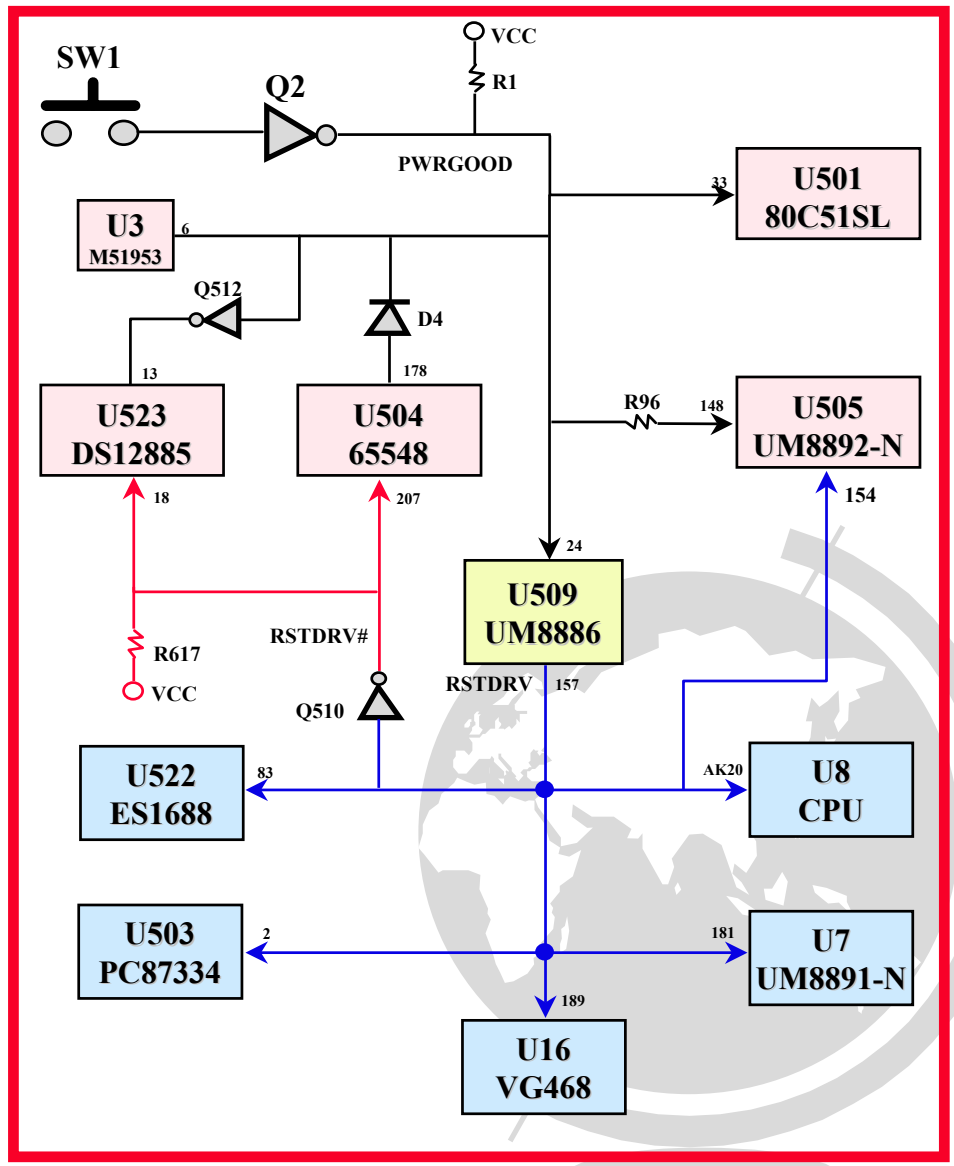
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



9.2 NO DISPLAY (SYSTEM FAILURE)

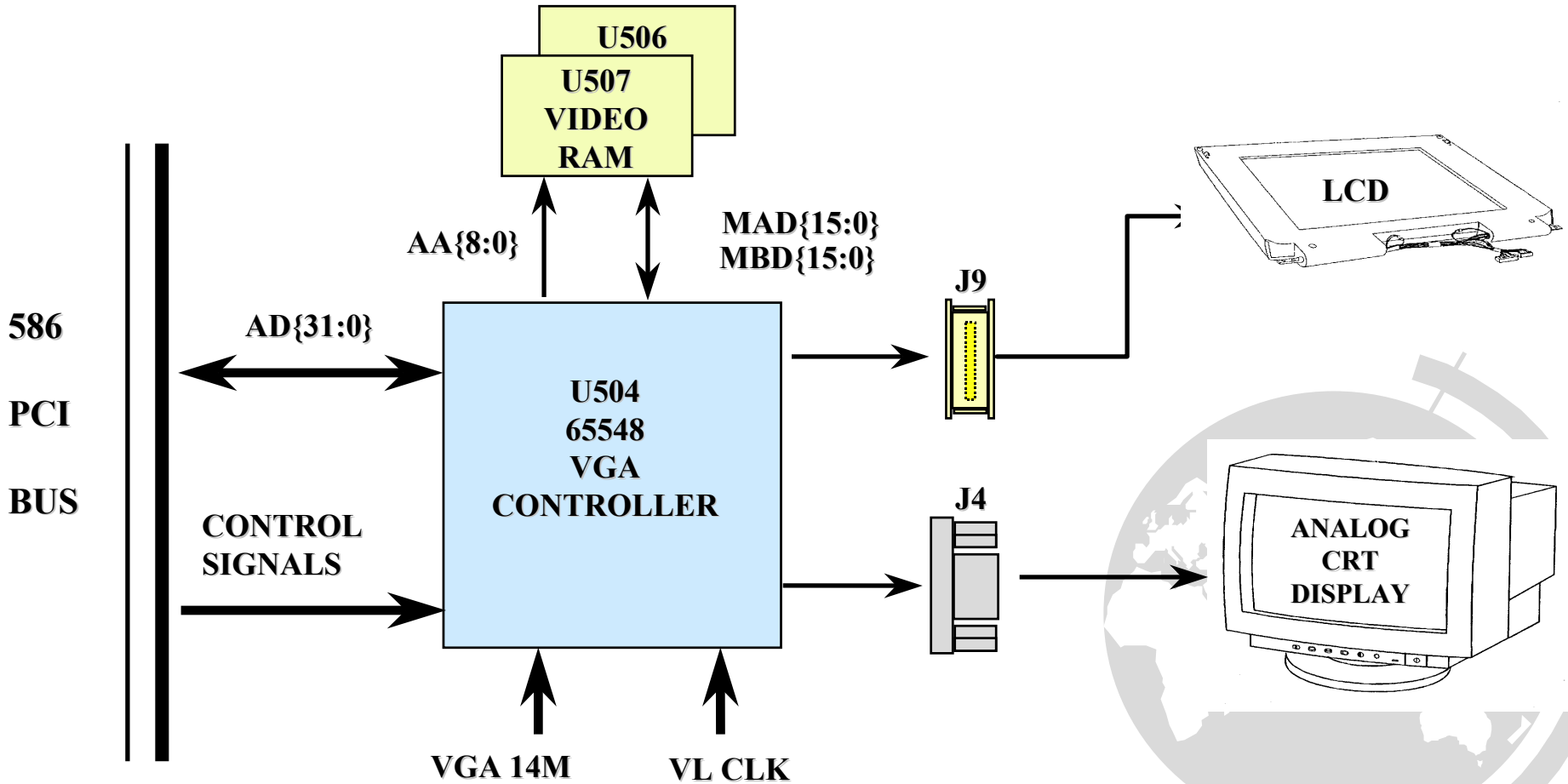
*******CLOCK AND RESET CIRCUIT CHECKING*******





9.3 VGA CONTROLLER FAILURE

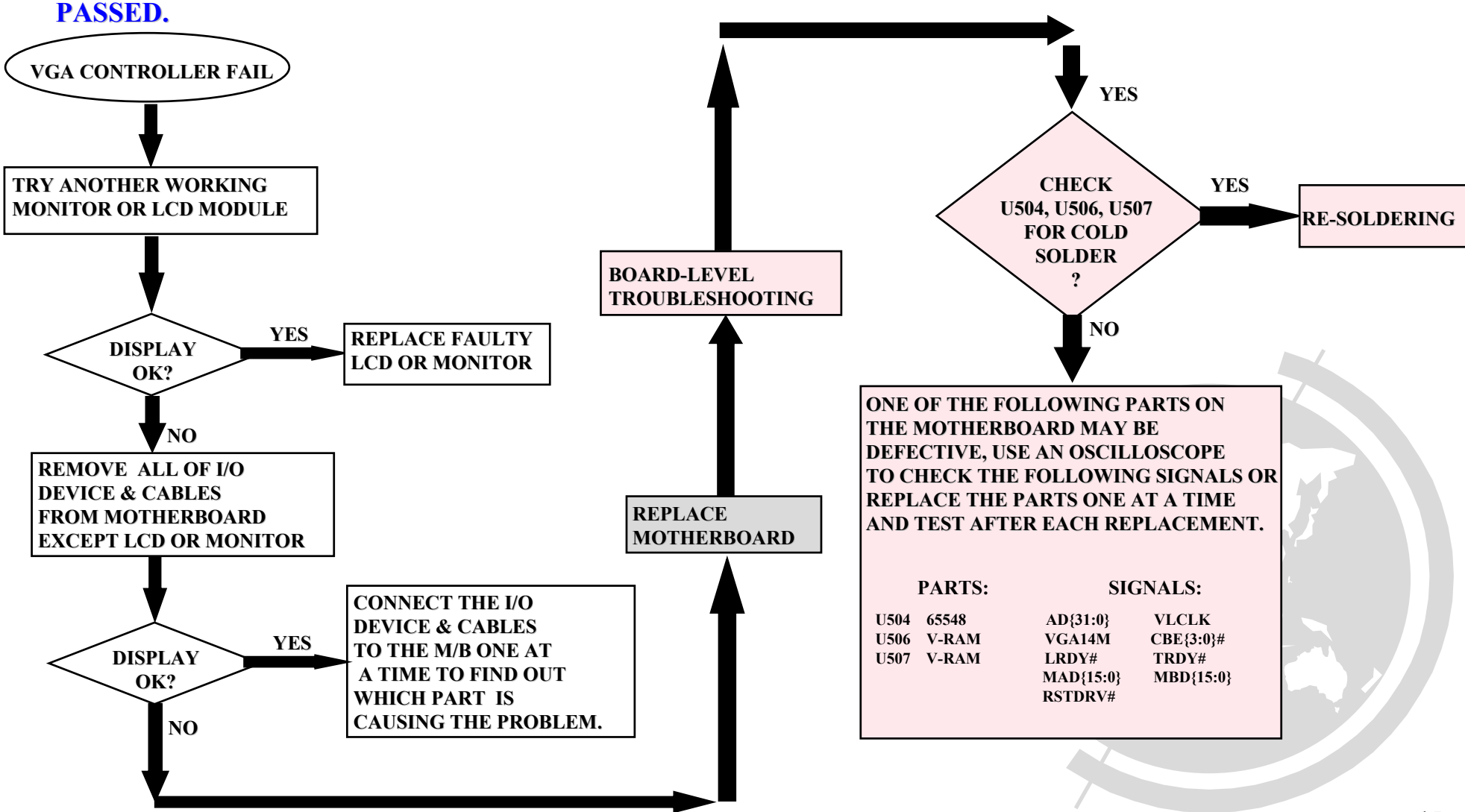
SYMPTOM:
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



9.3 VGA CONTROLLER FAILURE

SYMPTOM:

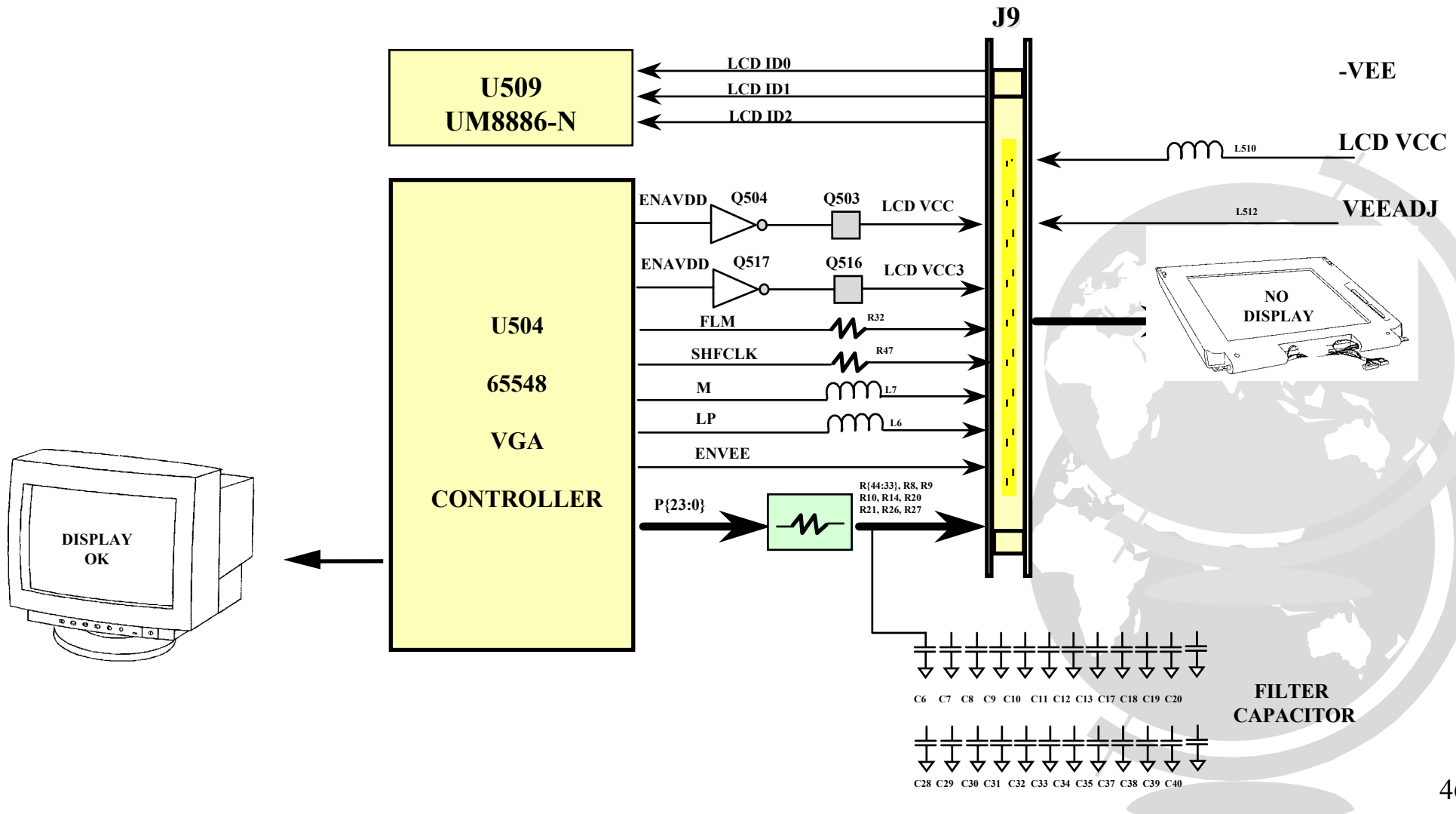
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

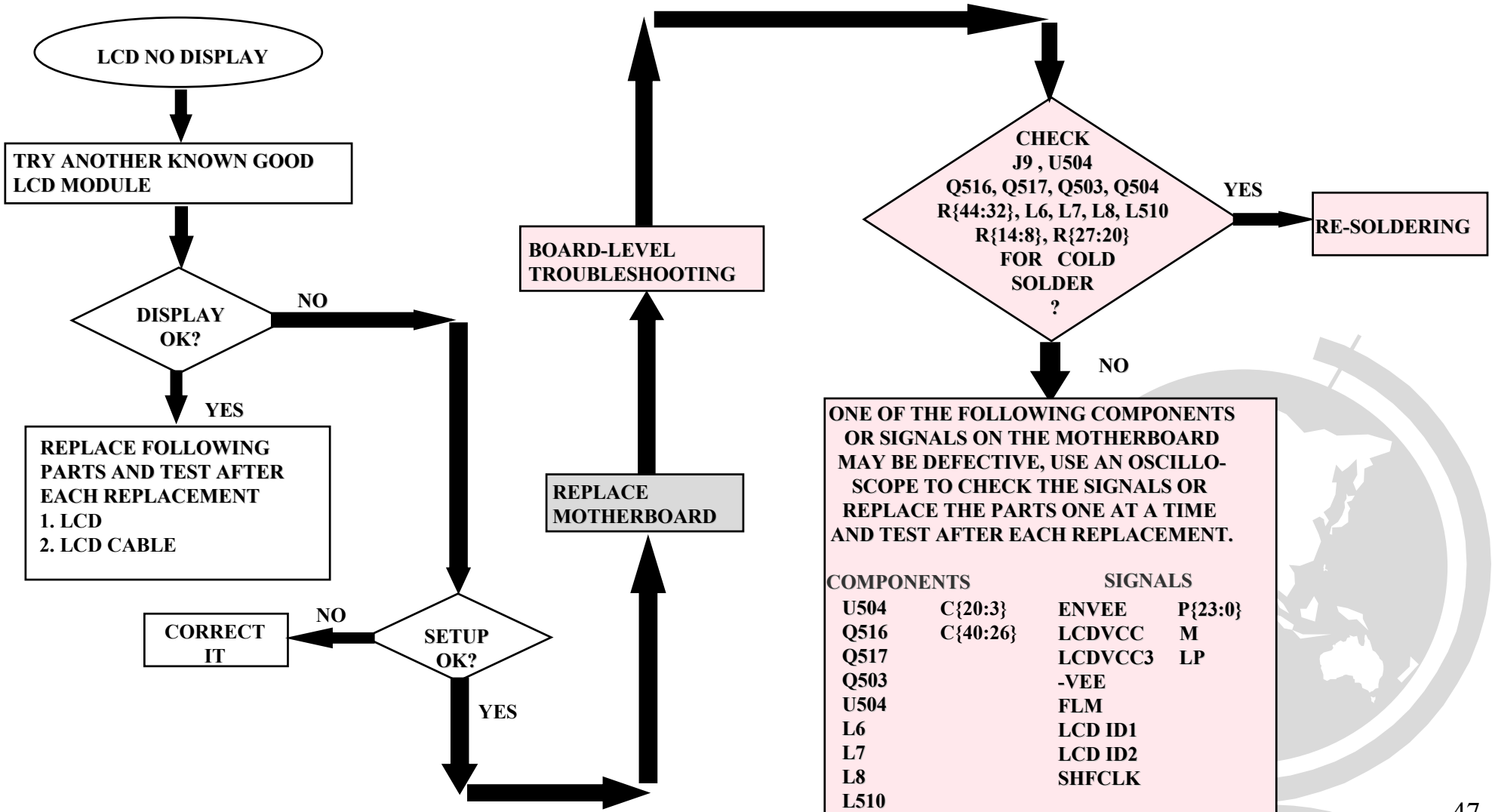
SYMPTOM:

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT THE DISPLY ON EXTERNAL MONITOR IS OK.



9.4 LCD NO DISPLAY OR PICTURE ABNORMAL

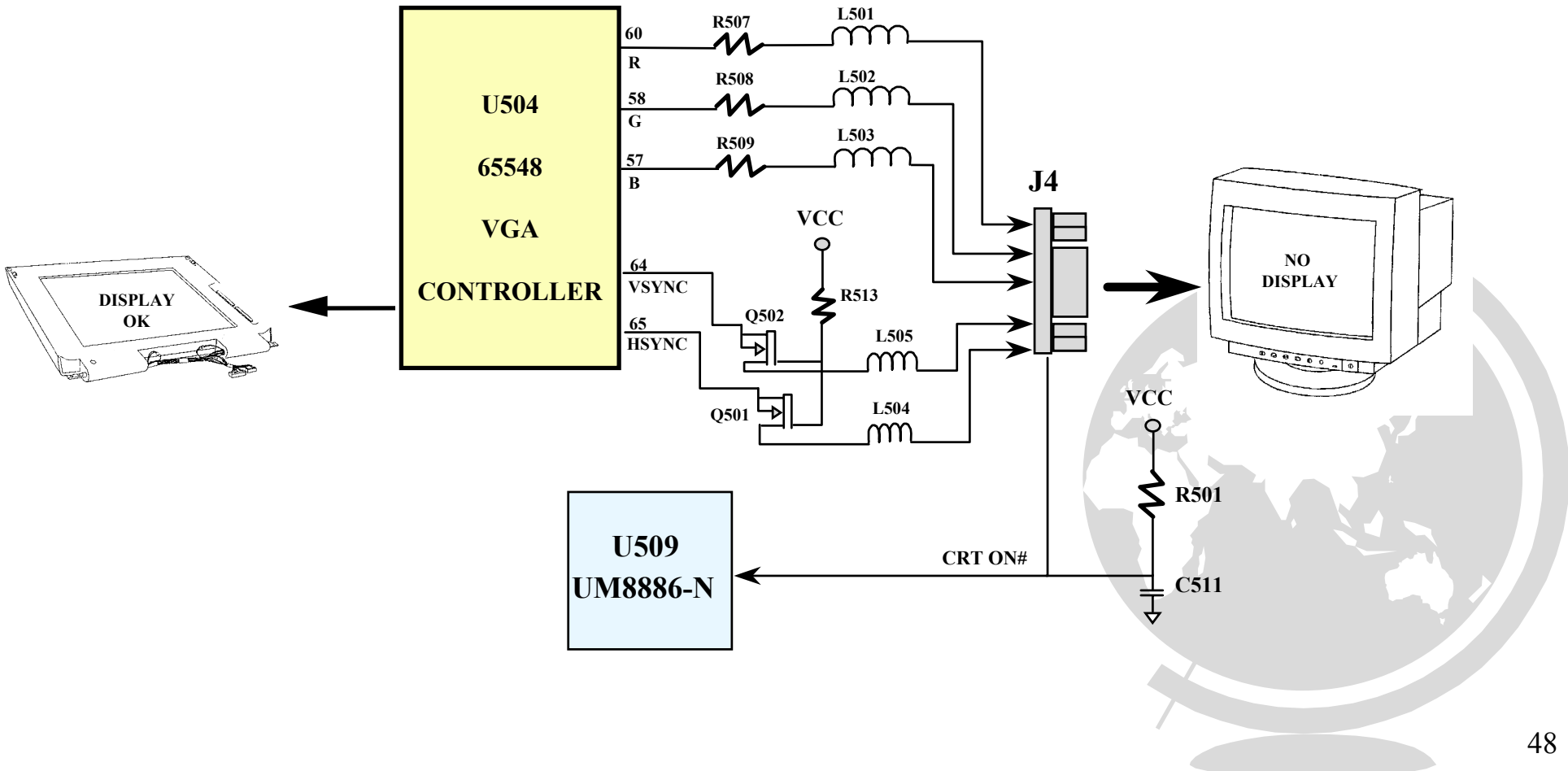
SYMPTOM:
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT THE DISPLY ON EXTERNAL MONITOR IS OK.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

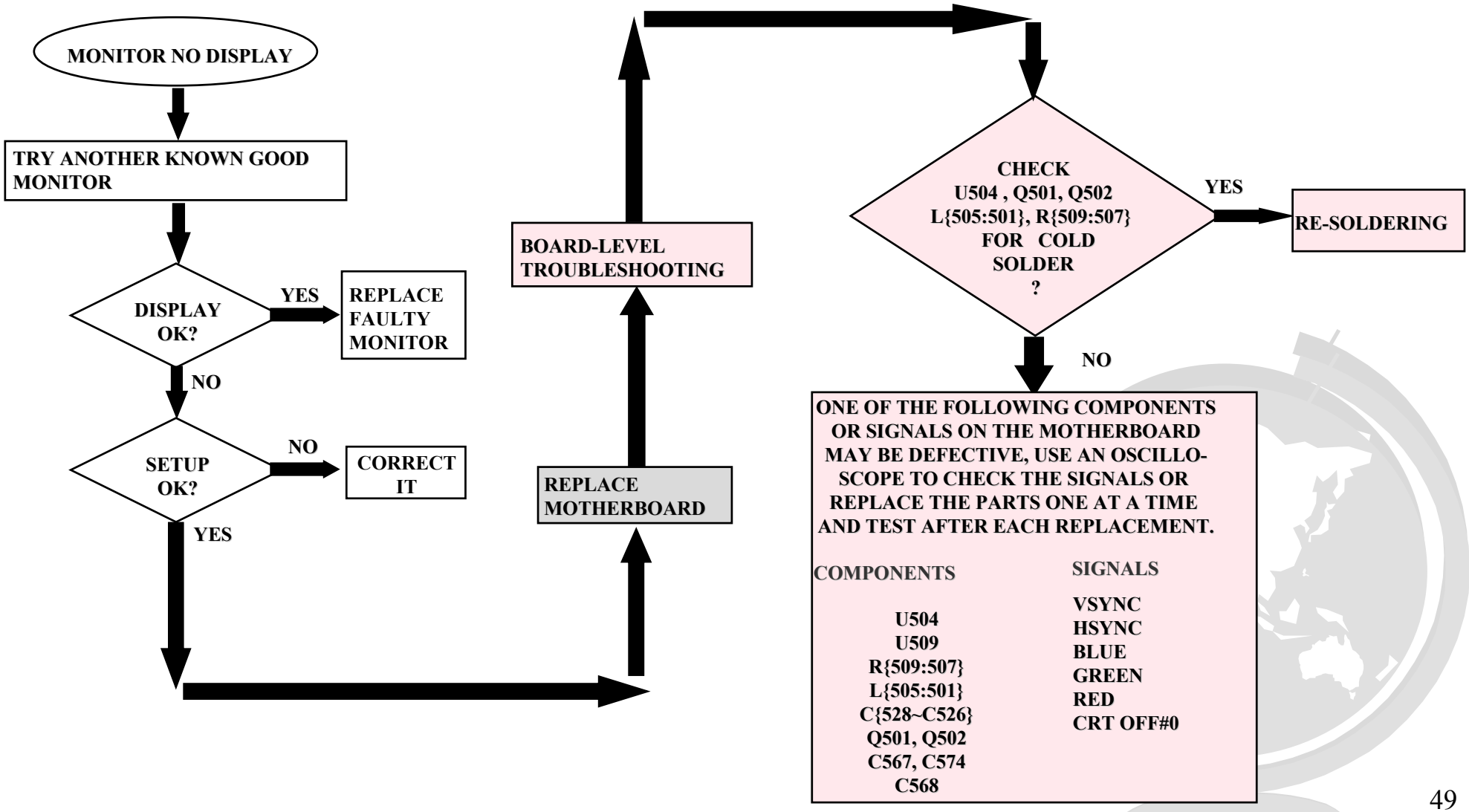
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT THE DISPLAY ON LCD IS OK.



9.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

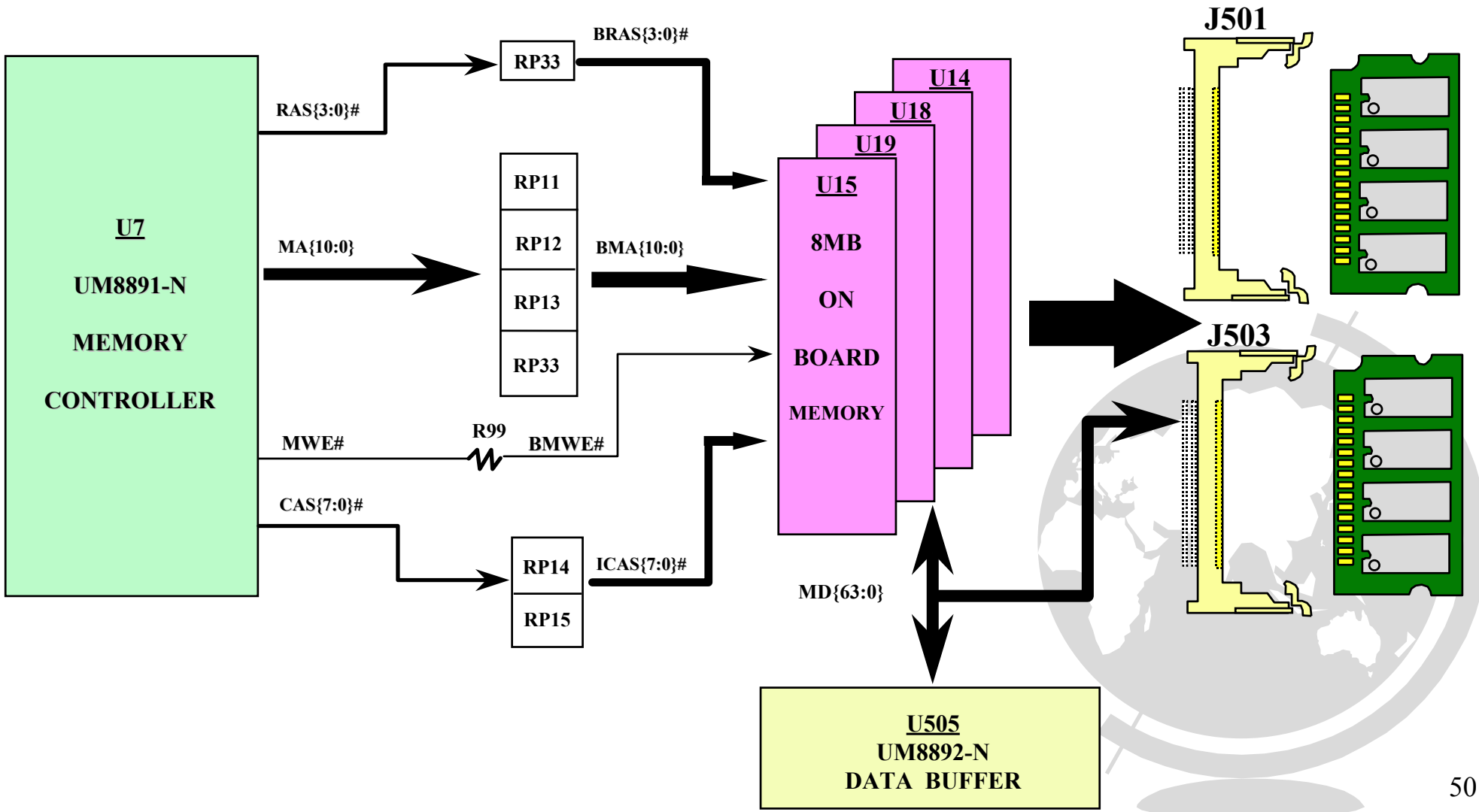
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT THE DISPLAY ON LCD IS OK.



9.6 MEMORY TEST ERROR

SYMPTOM:

PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 20H, 2CH ,2EH OR MEMORY EXTENSION FAILURE.



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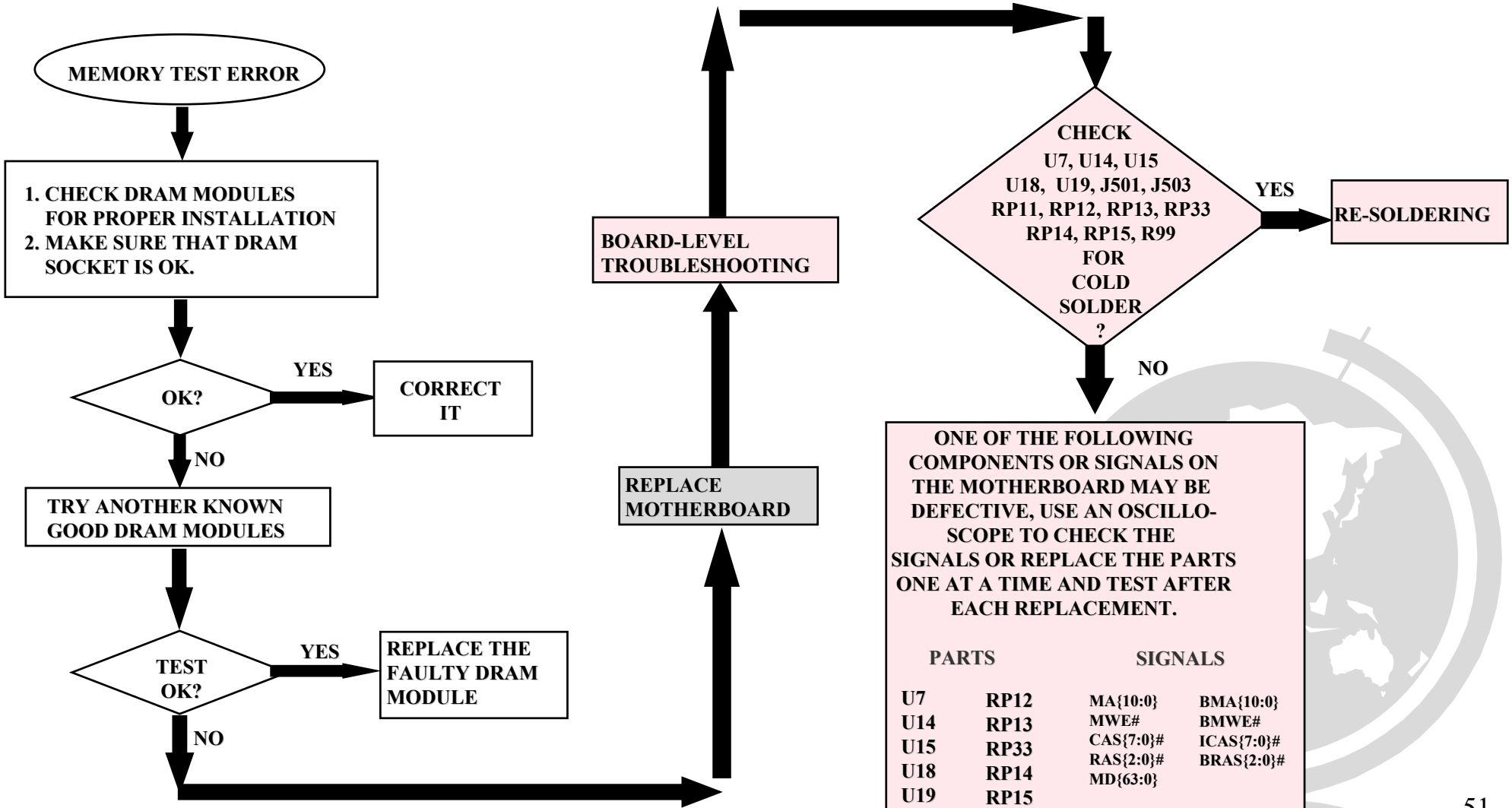

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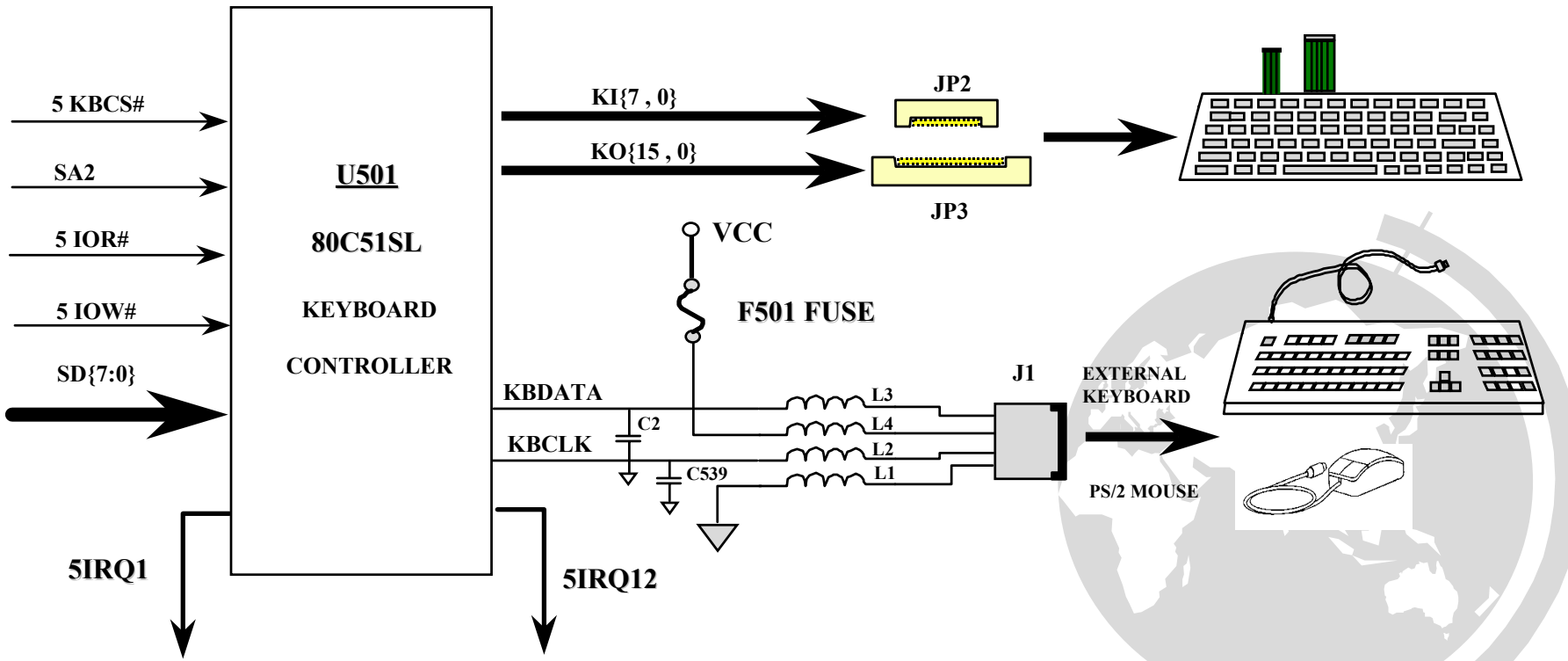
9.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

SYMPTOM:

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 22H



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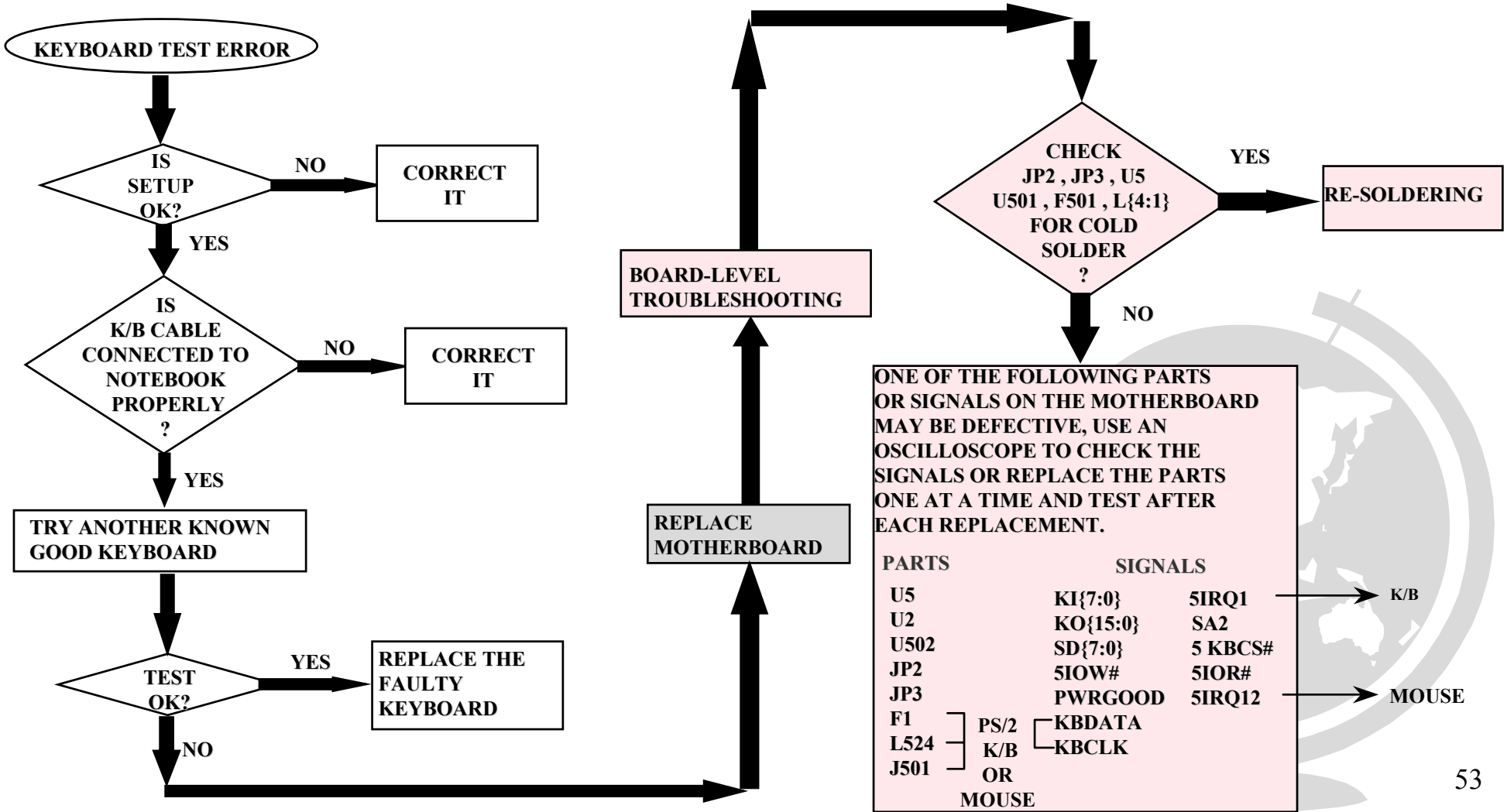
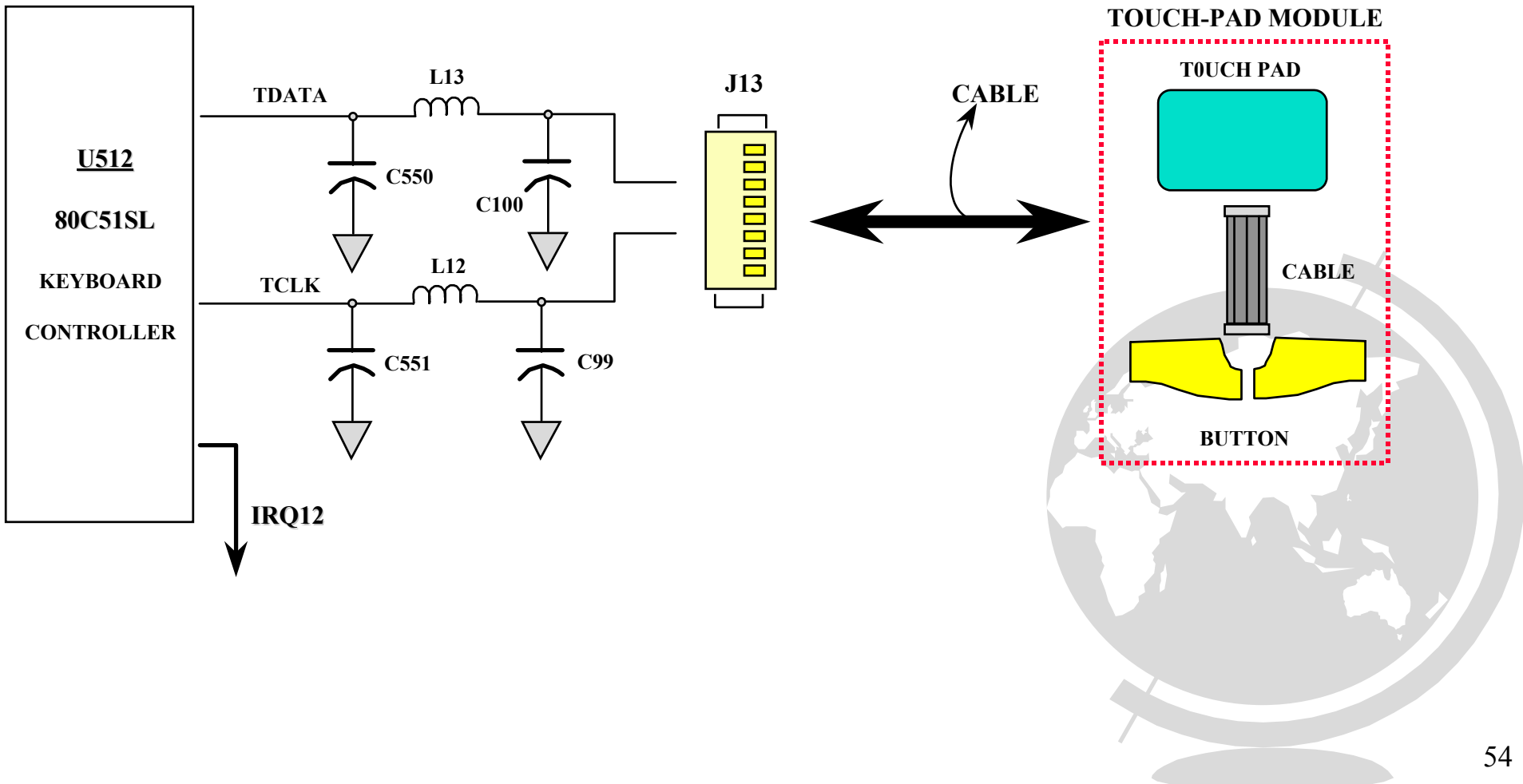


9.8 TOUCH-PAD TEST ERROR

SYMPTOM:
FAILURE OCCURS WHEN THE TOUCH-PAD IS ENABLED.



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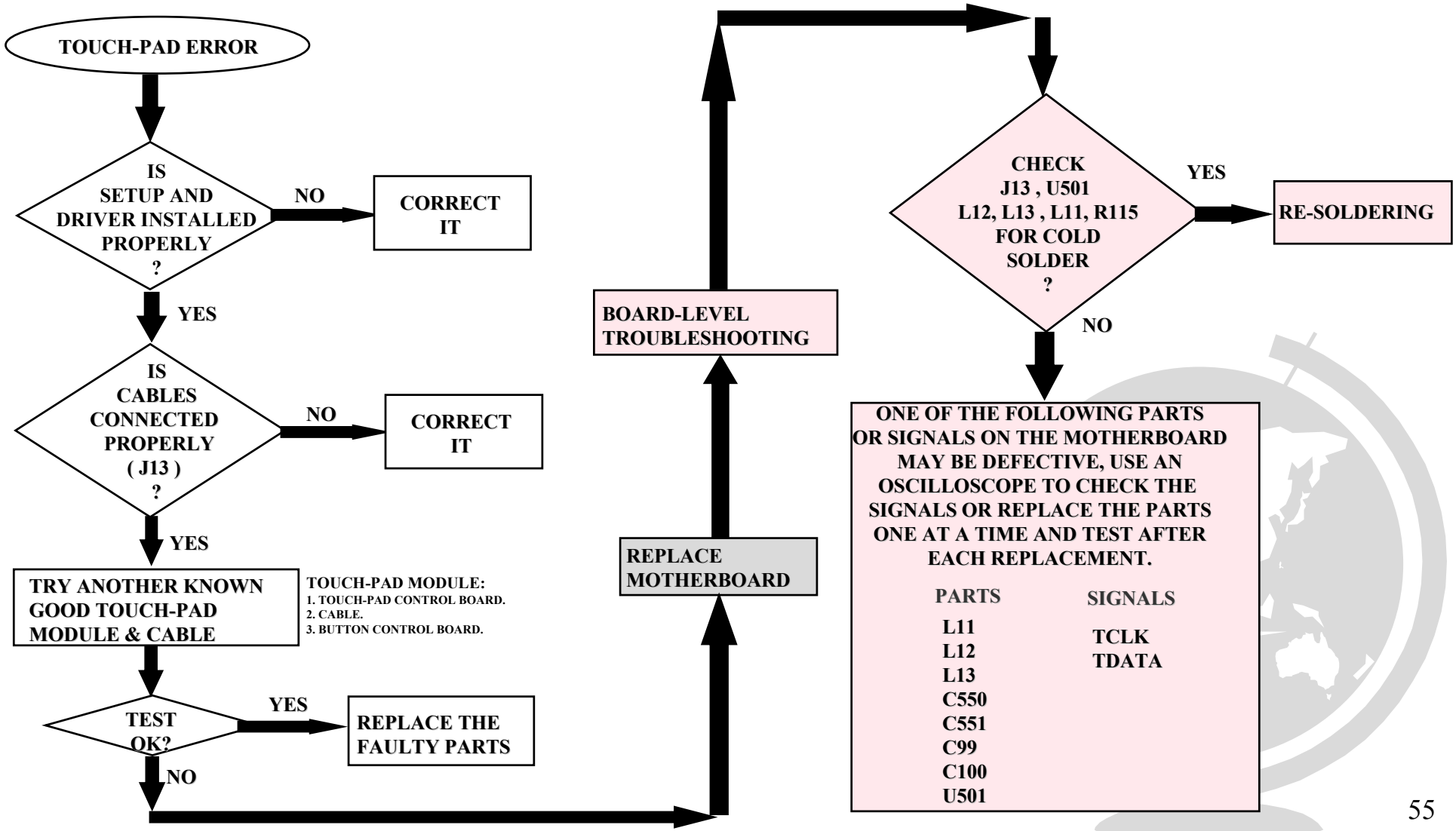
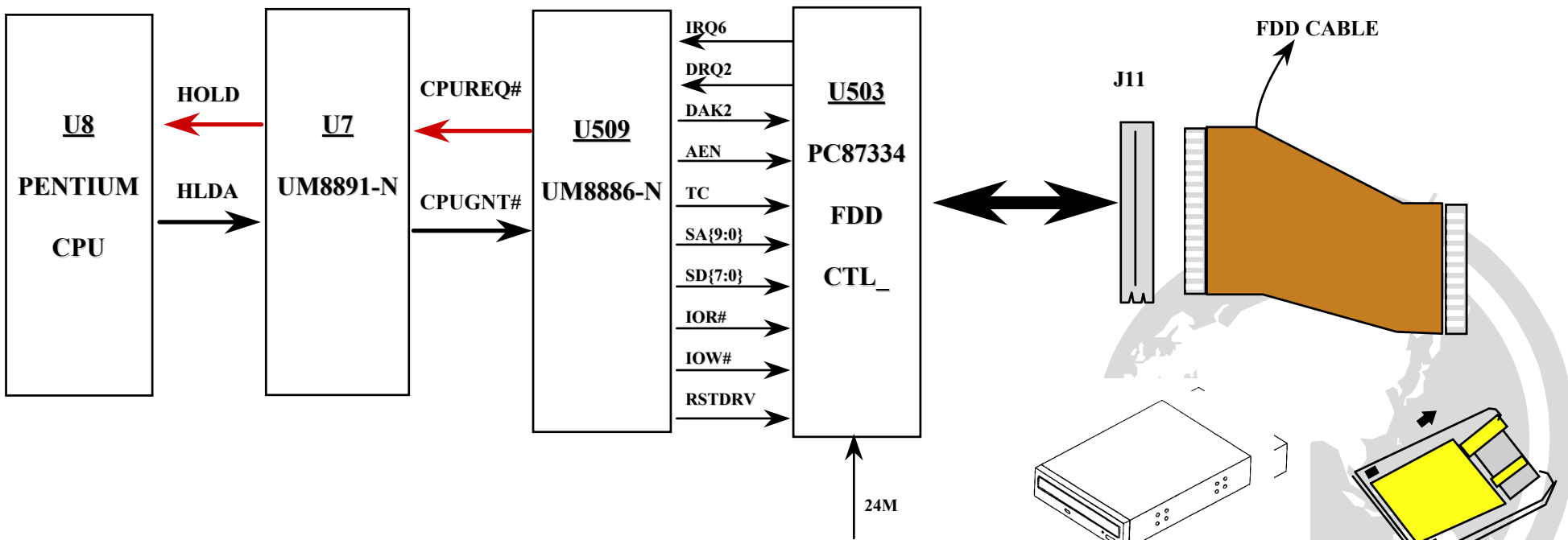


9.9 DISKETTE DRIVE TEST ERROR

SYMPTOM:

FAILURE OCCURS WHILE LOADING DATA FROM DISK TO SYSTEM.



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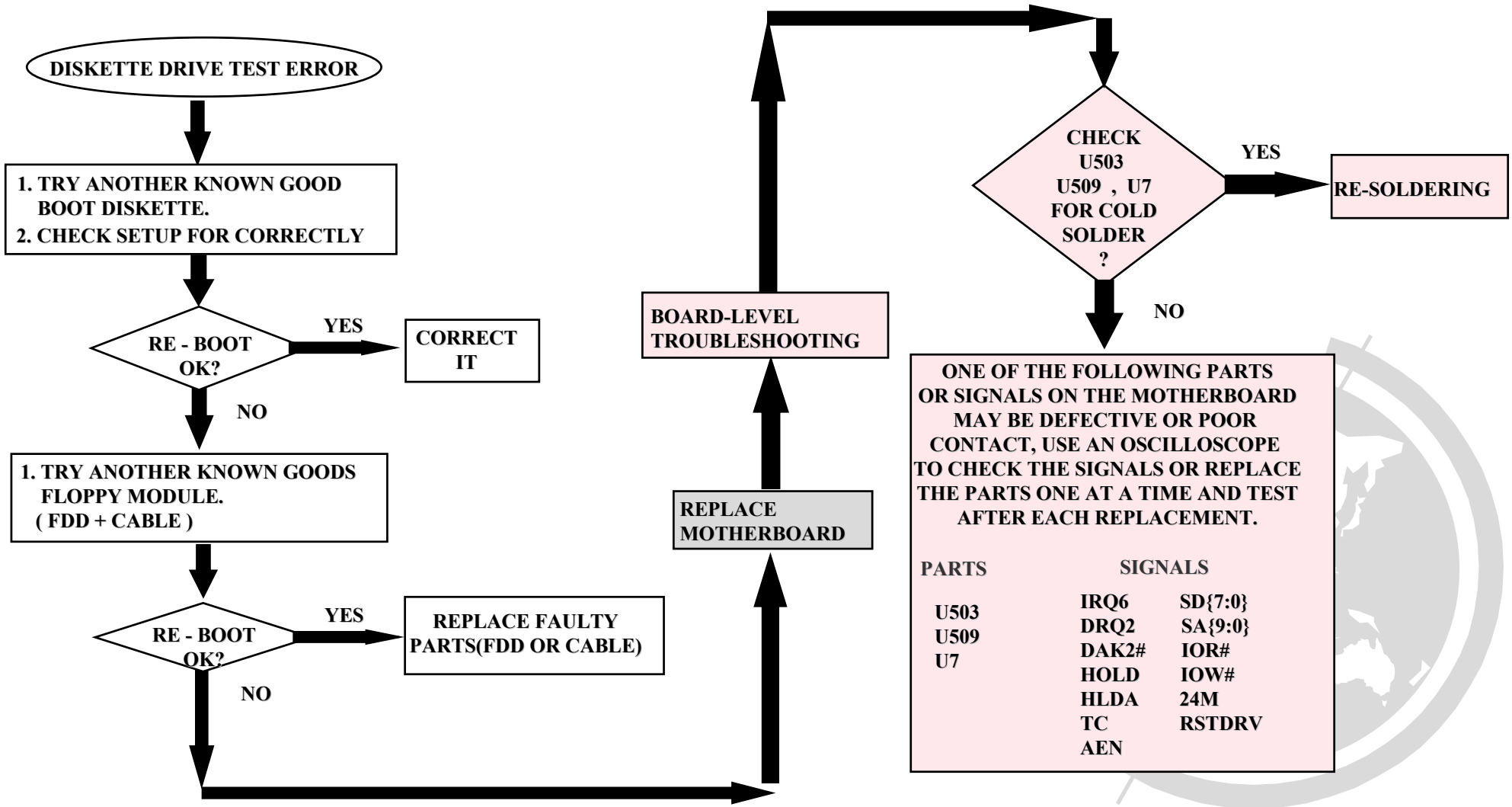
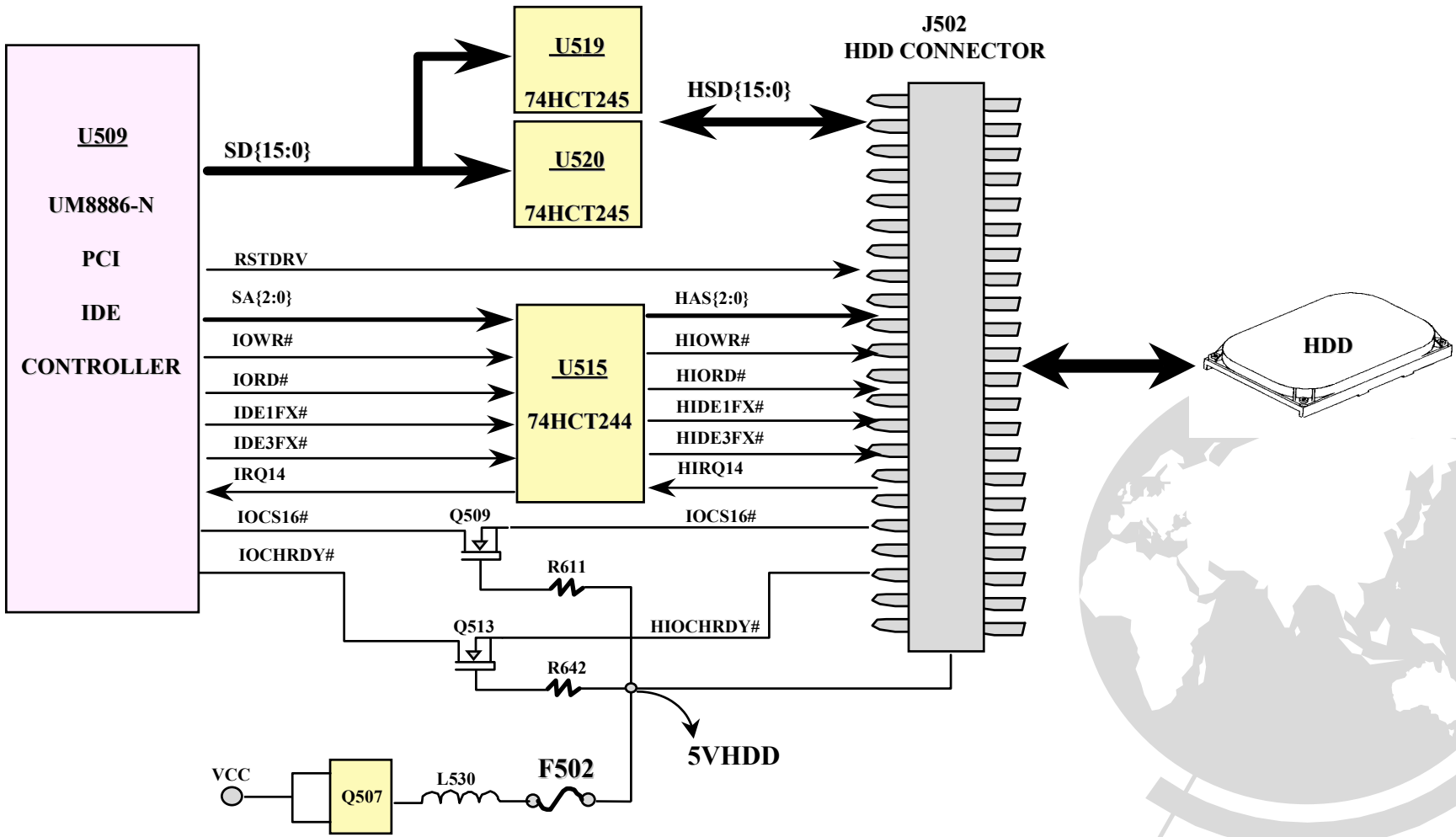


9.10 HARD DRIVE TEST ERROR

SYMPTOM:

EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



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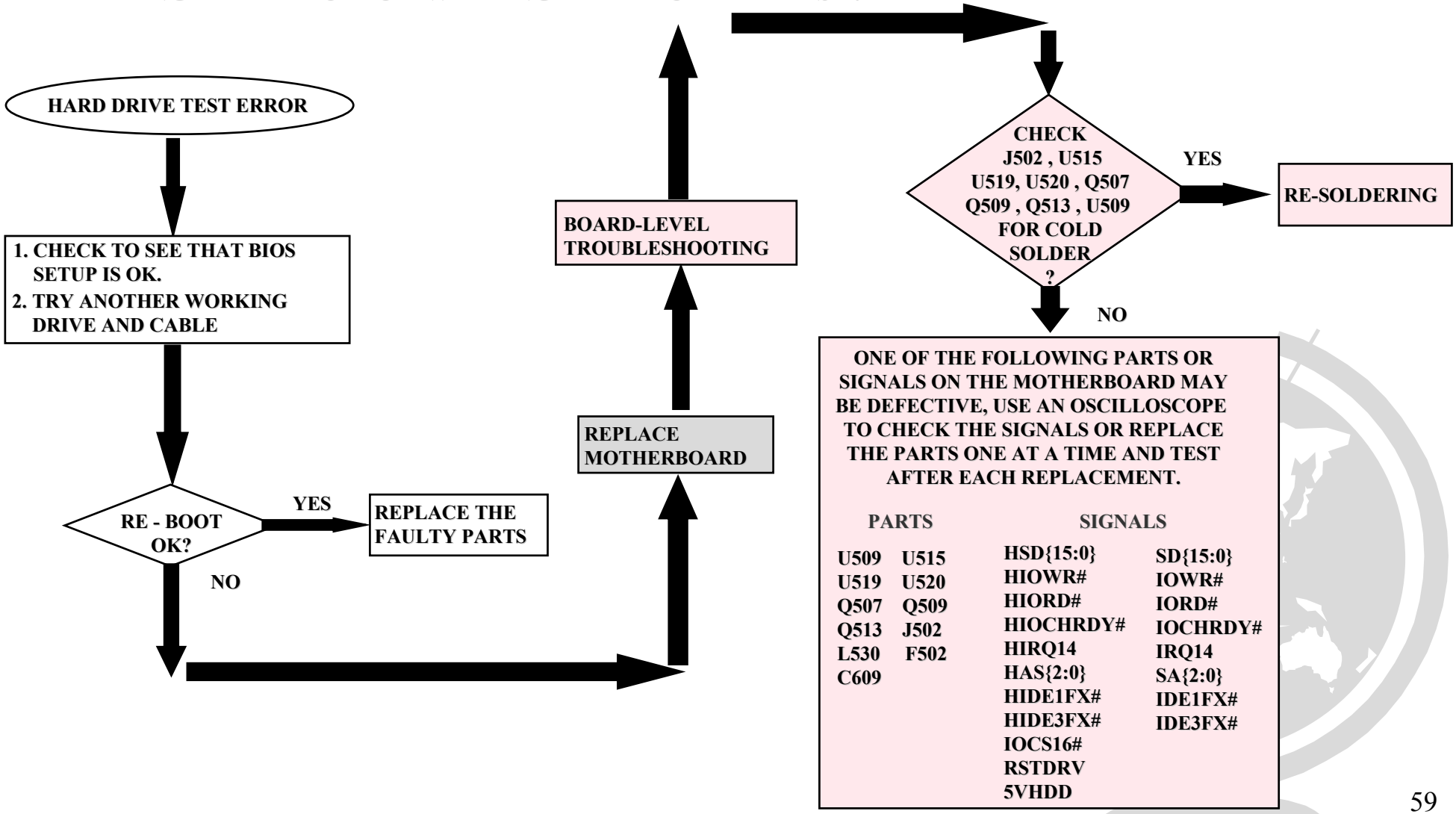
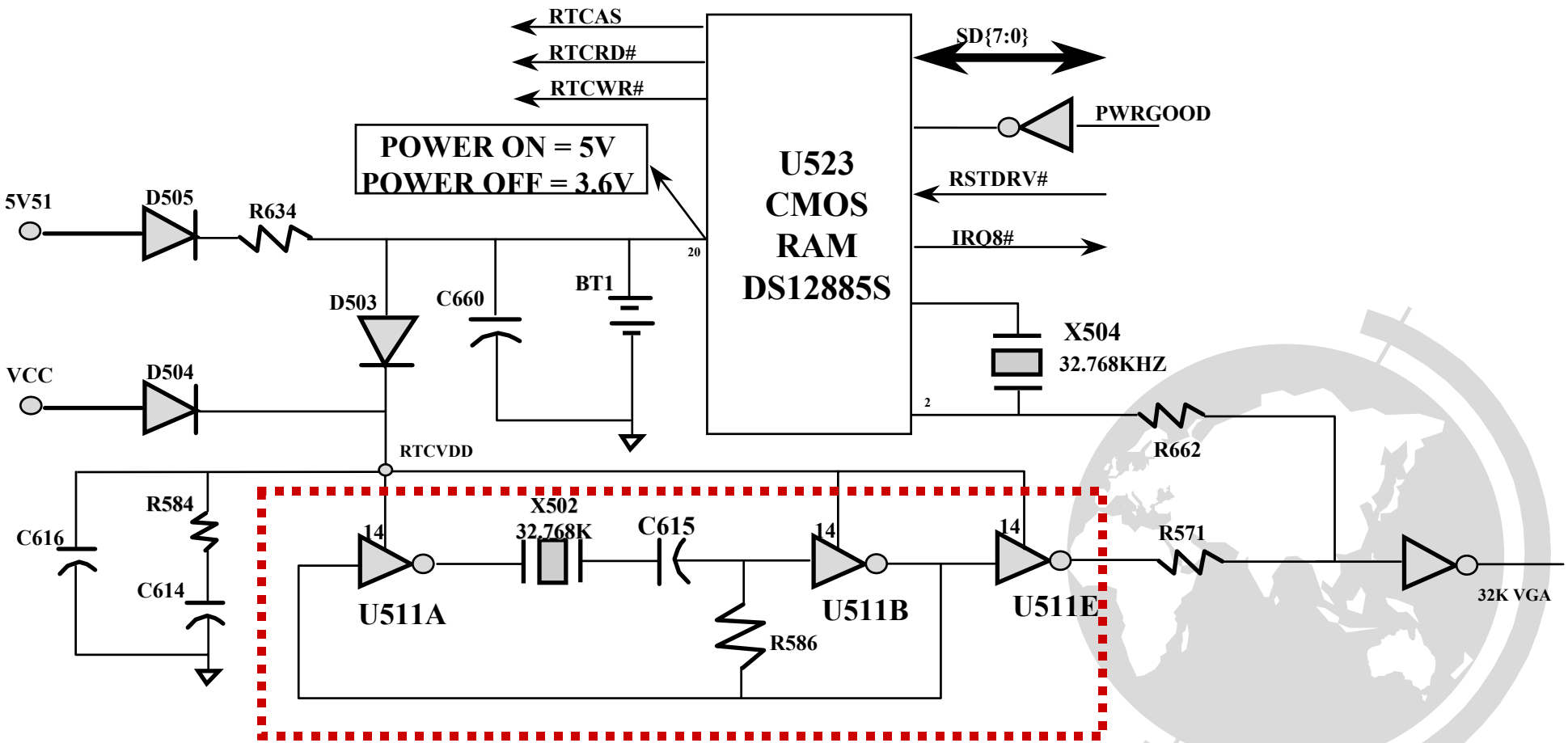


9.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 34H.
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.



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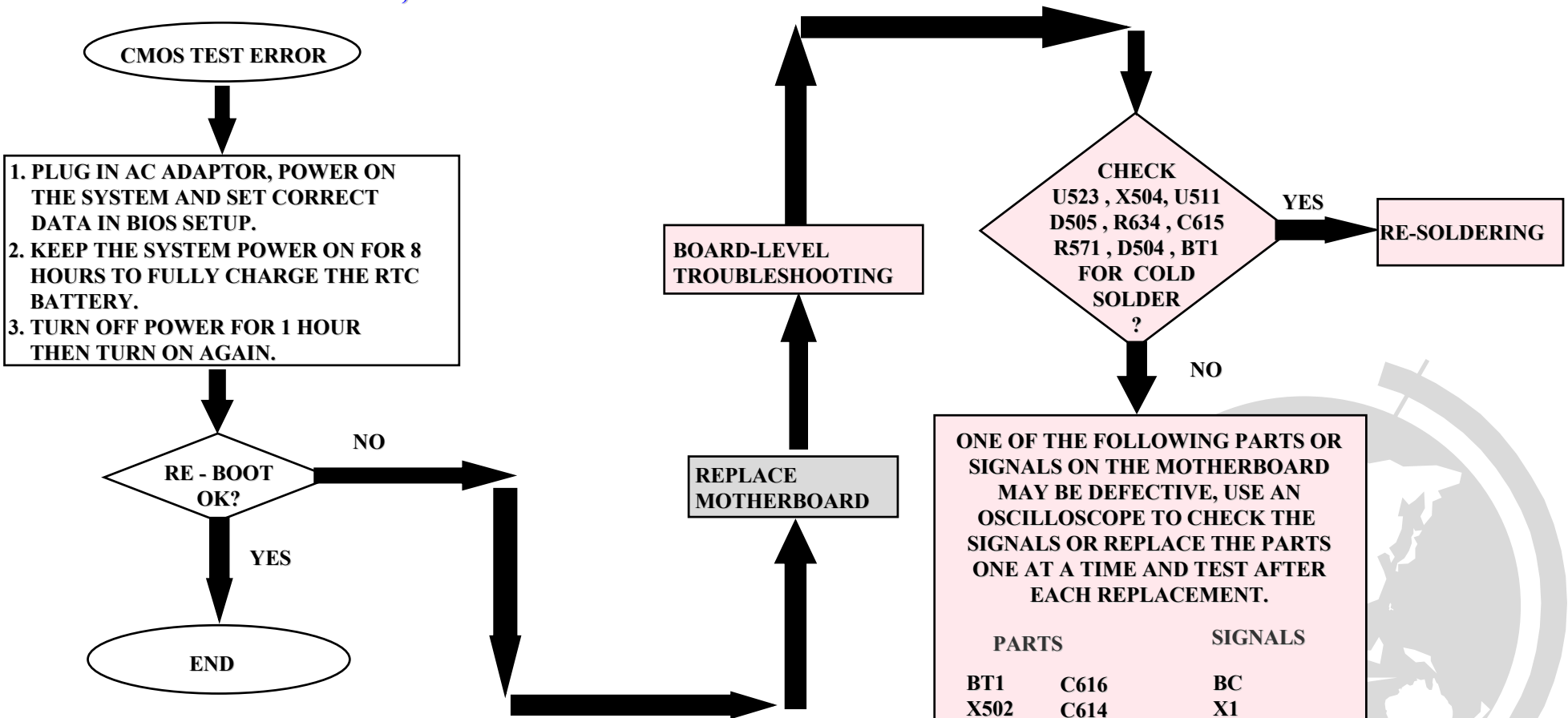
SYMPTOM:

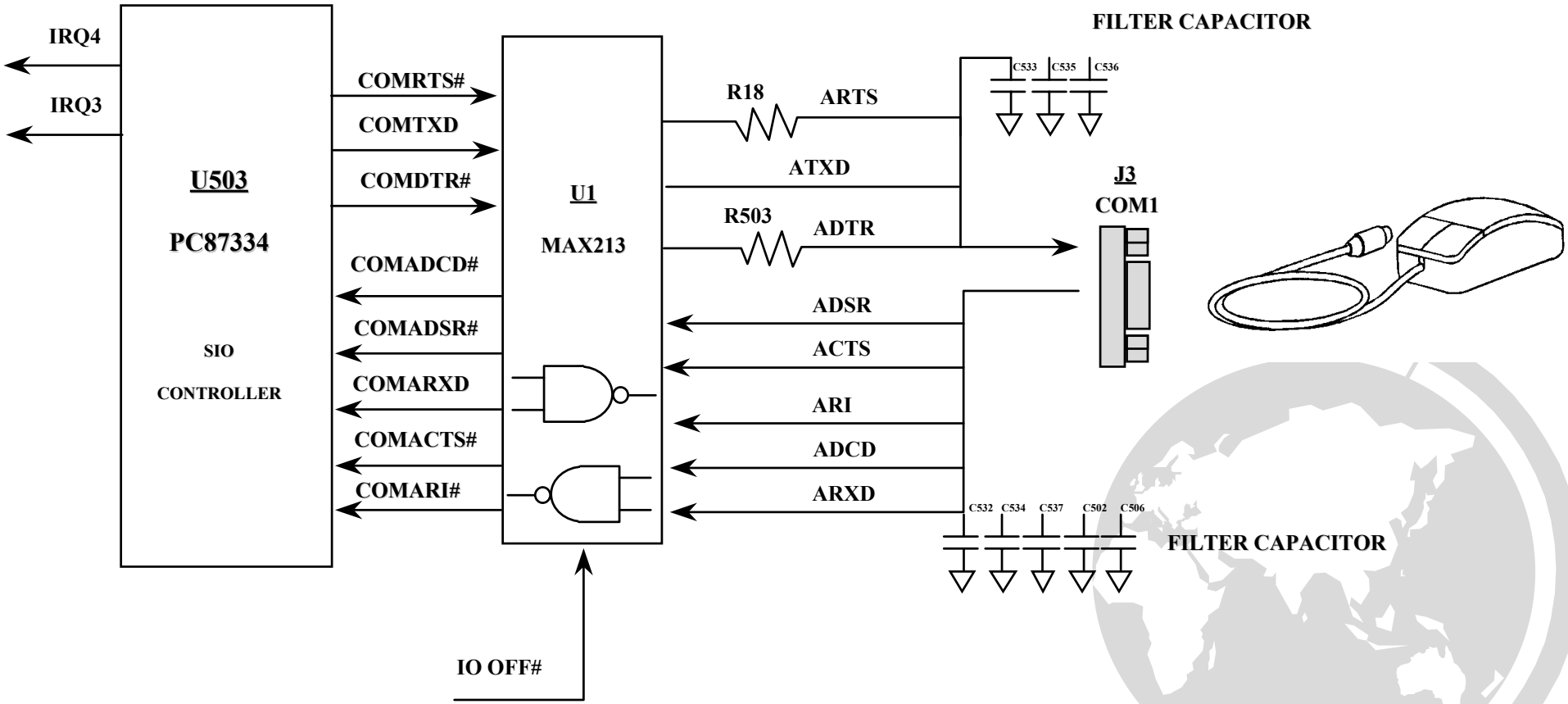
1. ERROR CODE IS STOPEED AT 34H.
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.



9.12 SIO PORT TEST ERROR

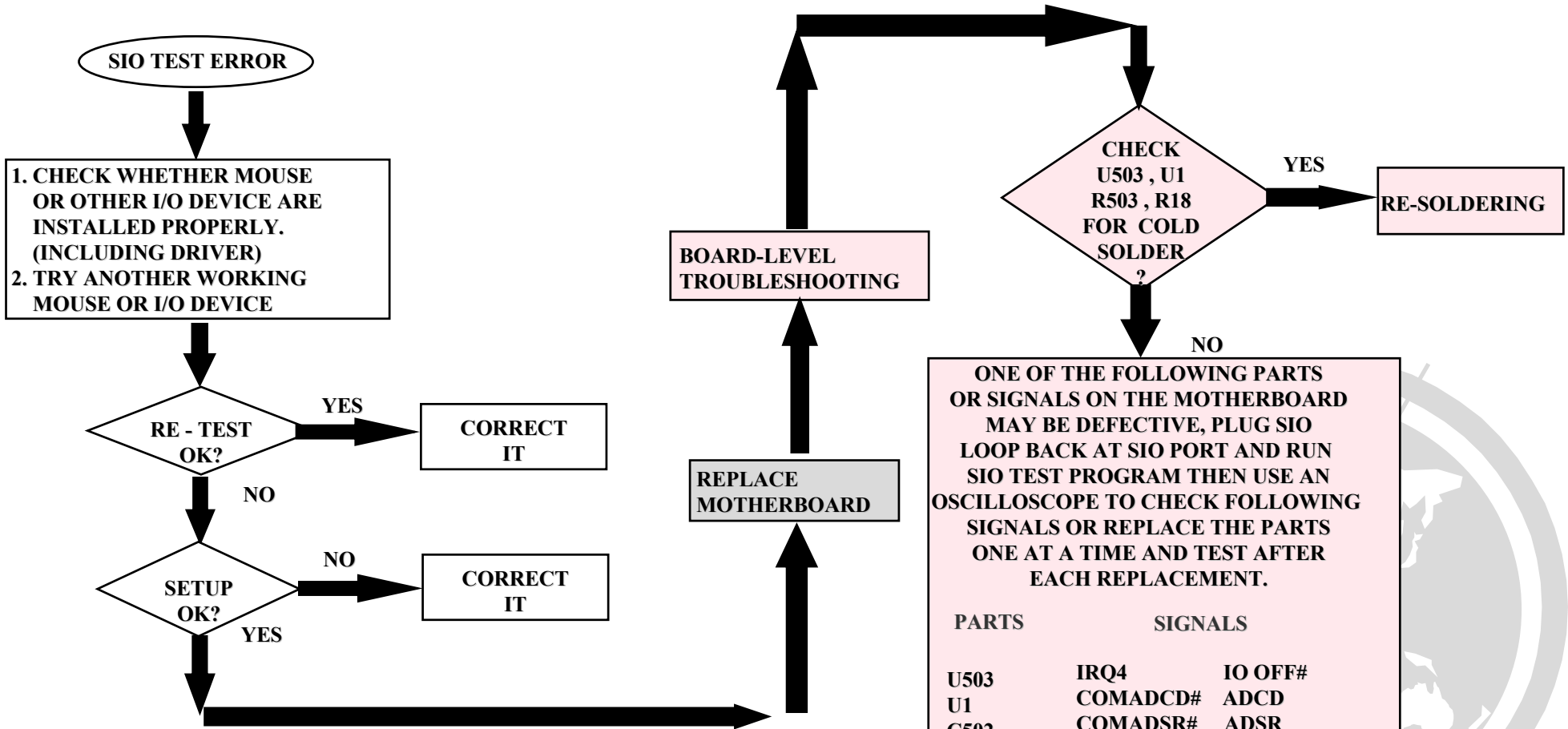
SYMPTON:

FAILURE OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



9.12 SIO PORT TEST ERROR

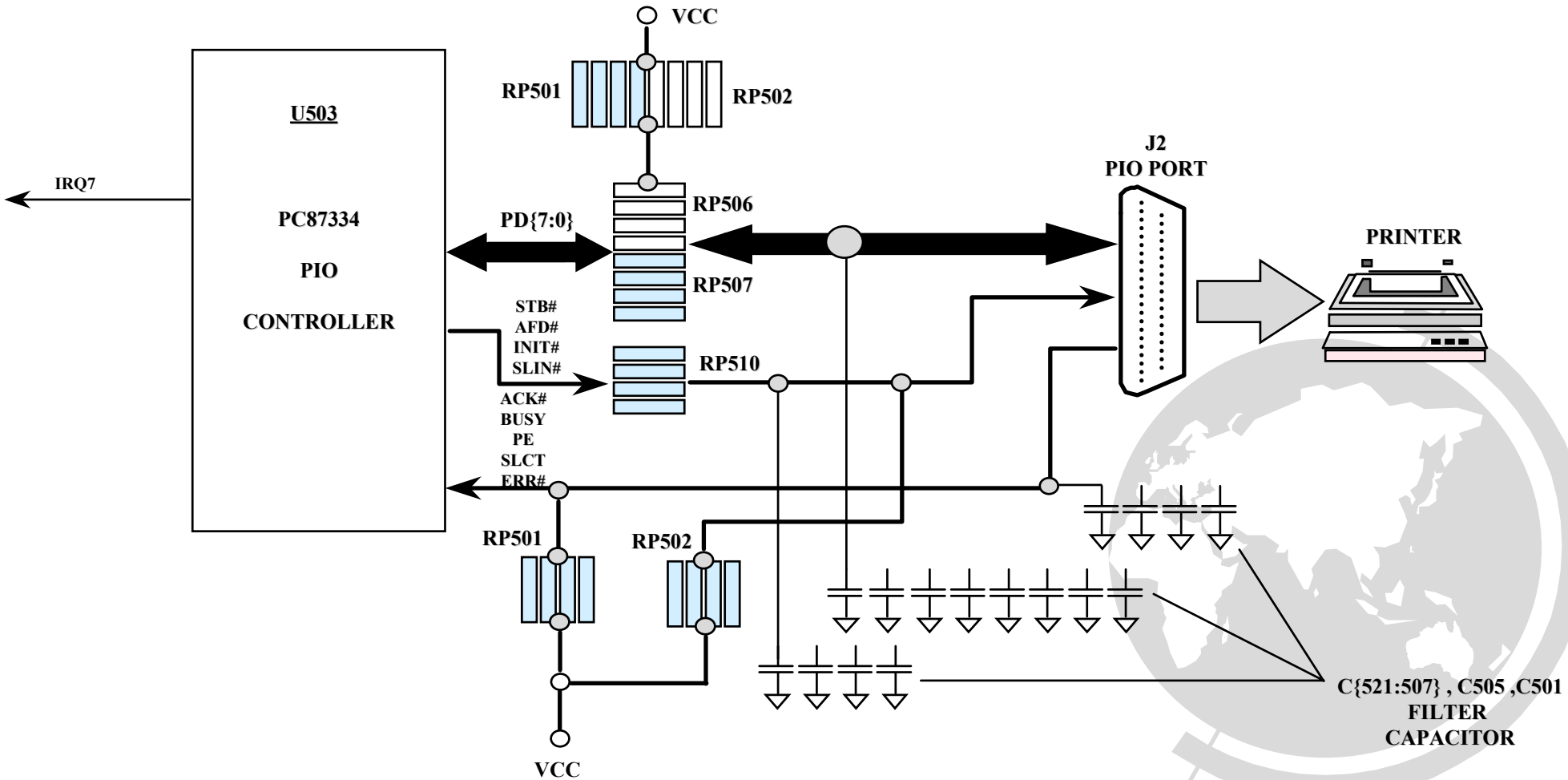
SYMPTON:
FAILURE OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



9.13 PIO PORT TEST ERROR

SYMPTON:

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



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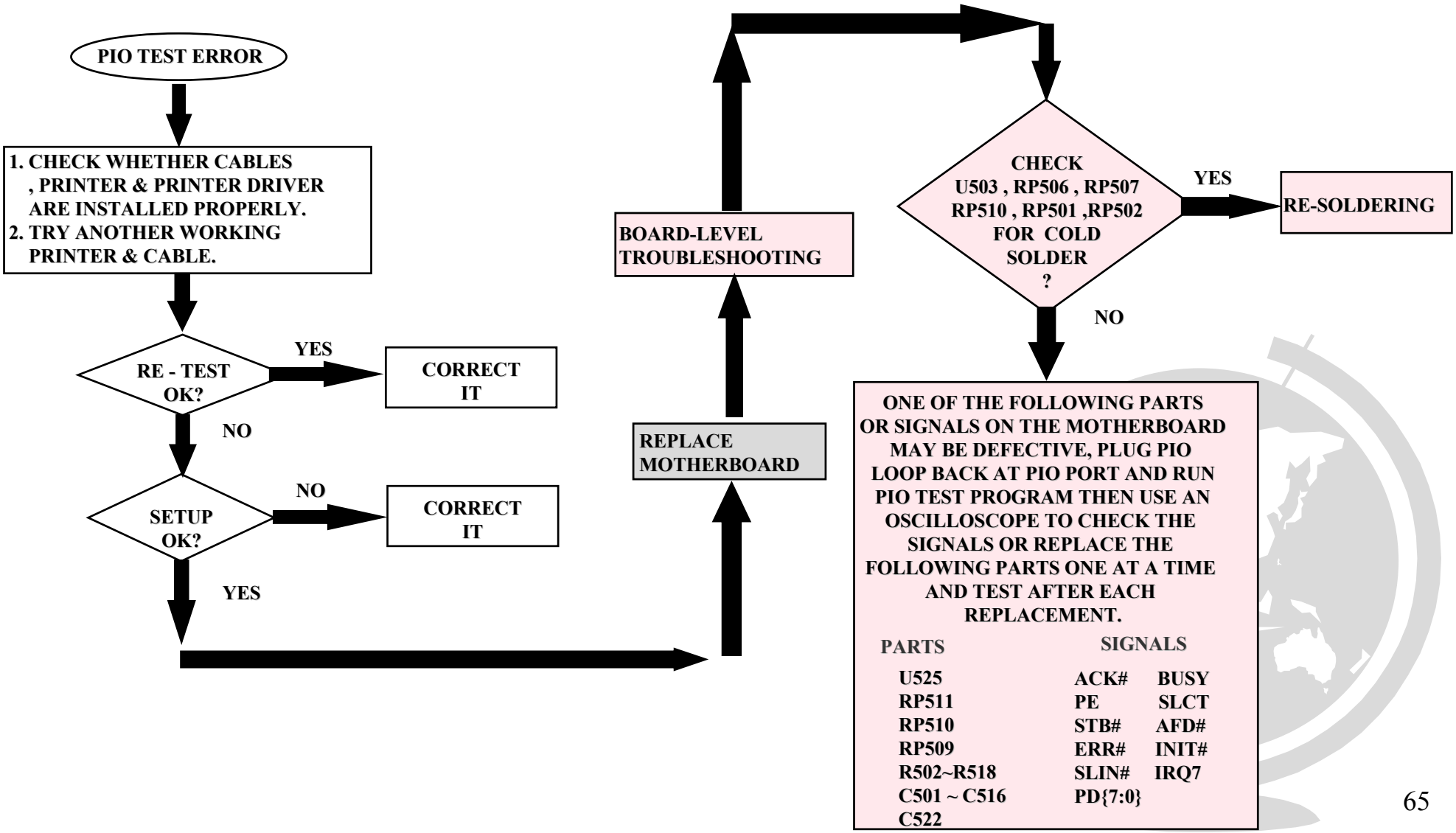
SYMPTON:

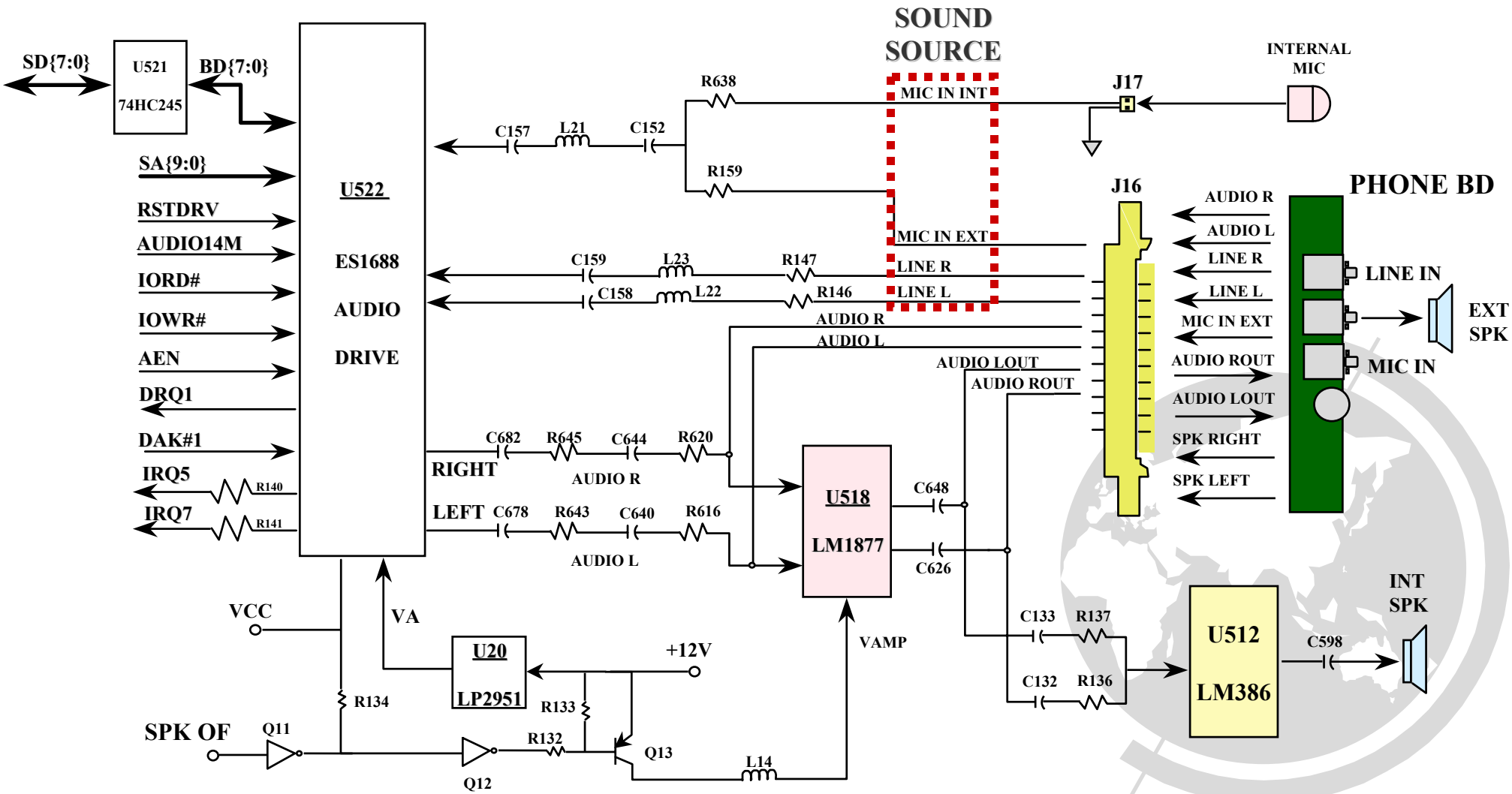
WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



9.14 AUDIO DRIVE FAILURE

SYMPTON:

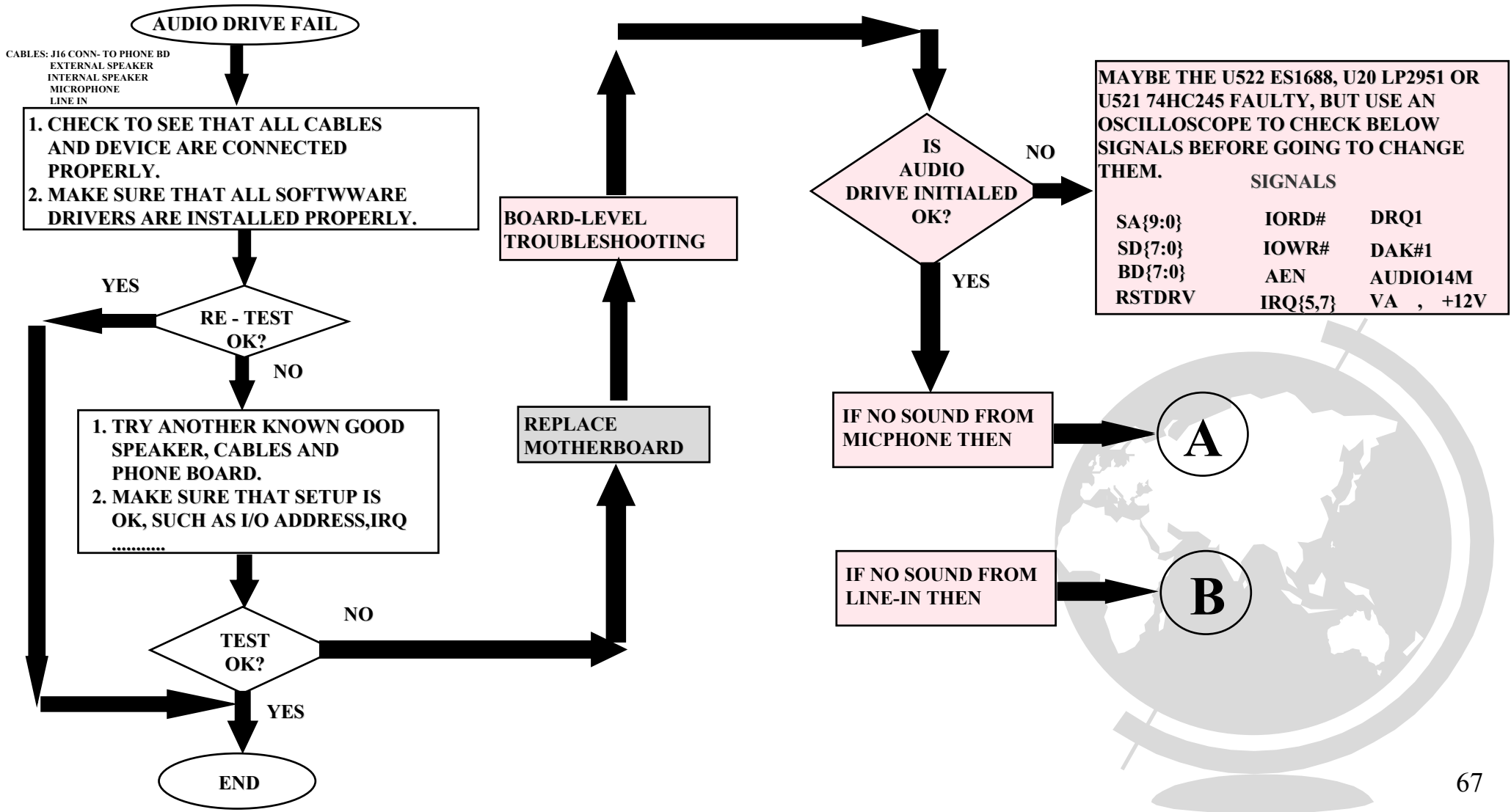
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED.



9.14 AUDIO DRIVE FAILURE

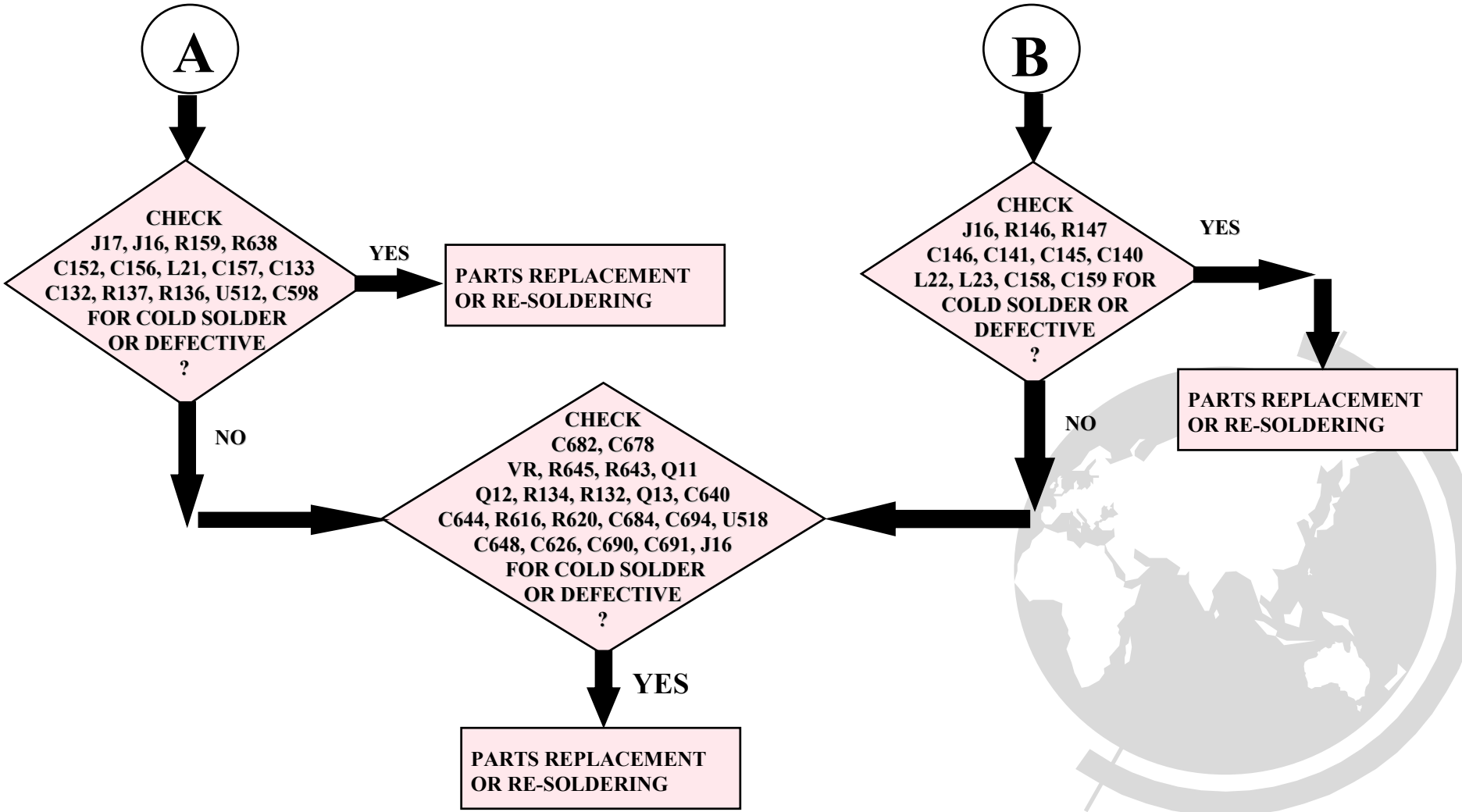
SYMPTON:

NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND LINE IN.

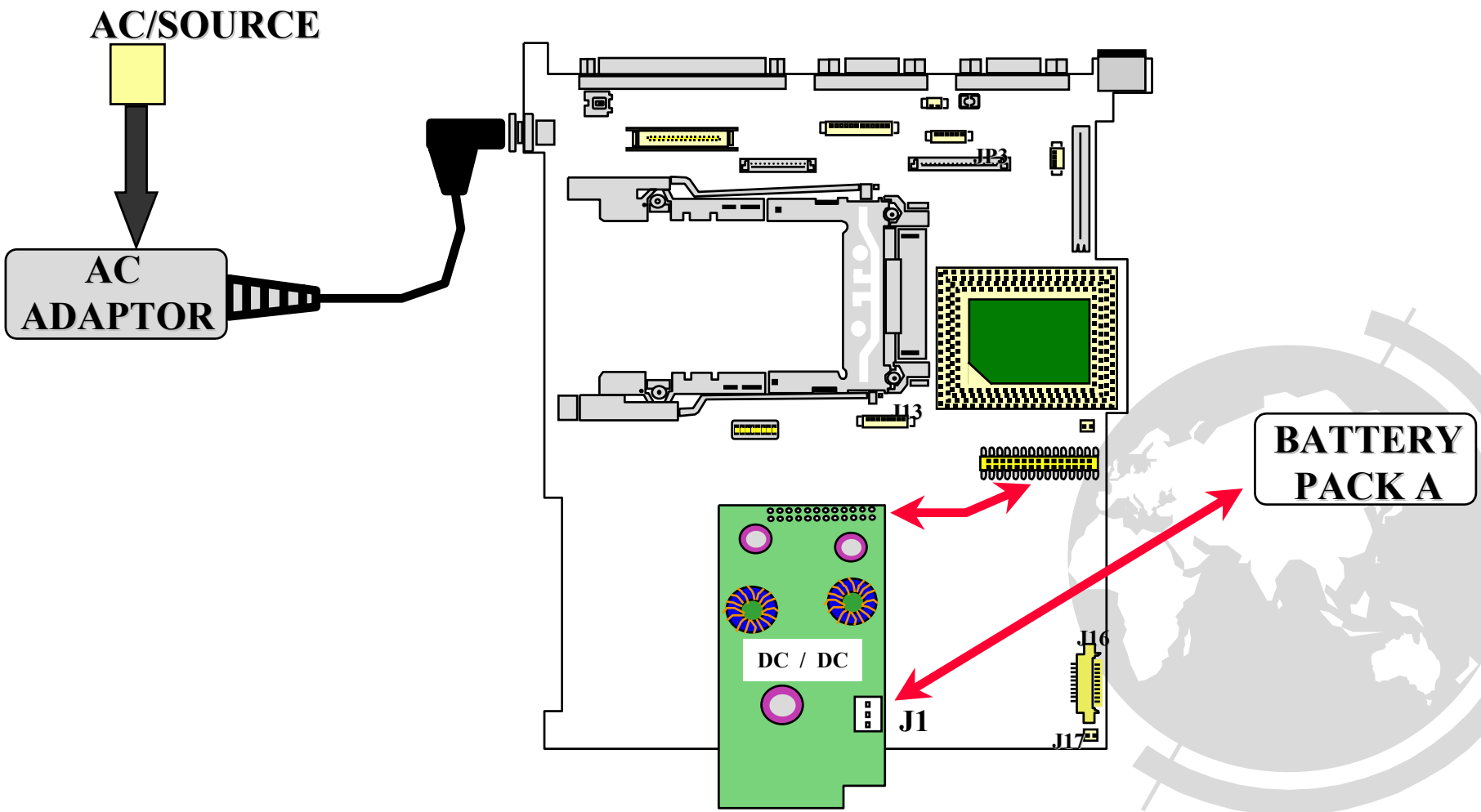


9.15 AUDIO DRIVE FAILURE

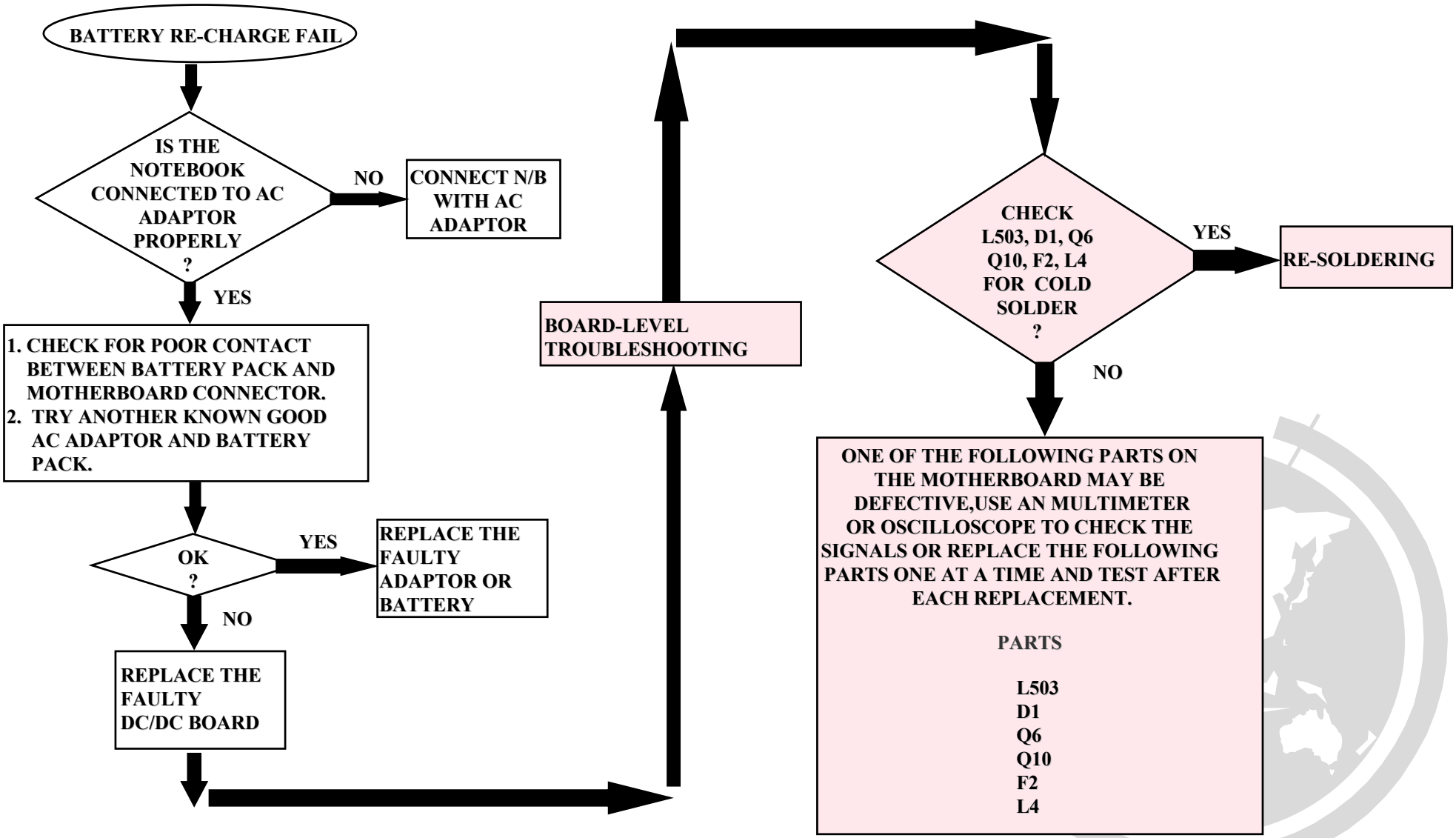
SYMPTON:
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND LINE IN.



9.15 BATTERY RE-CHARGE FAILURE



9.15 BATTERY RE-CHARGE FAILURE



10. SYSTEM BLOCK DIAGRAM & SCHEMATISS

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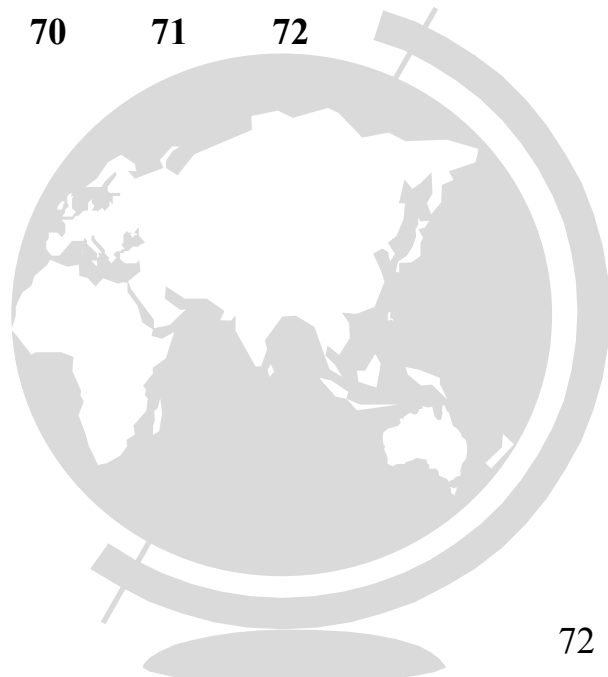
86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

101 102 103 104 105 106 107 108 109 110 111 112 113

114 115 116 117 118 119 120 121 122 123

124 125 61 62 63 64 65 66 67 68 69 70 71 72

73 74 75 76 77 78 79 80 81 82 83 84



10. SYSTEM BLOCK DIAGRAM & SCHEMATISS

MOTHER-BOATD

DC /DC BOARD

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10. SYSTEM BLOCK DIAGRAM & SCHEMATISS