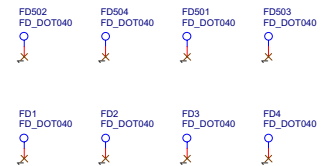
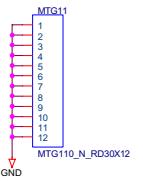
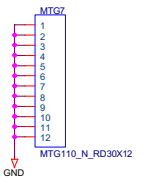
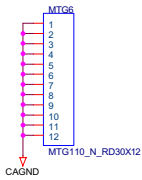
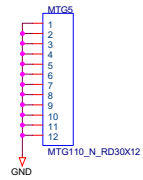
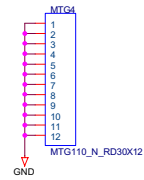
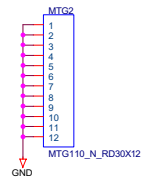
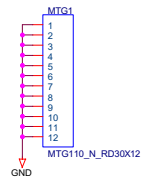
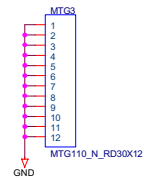


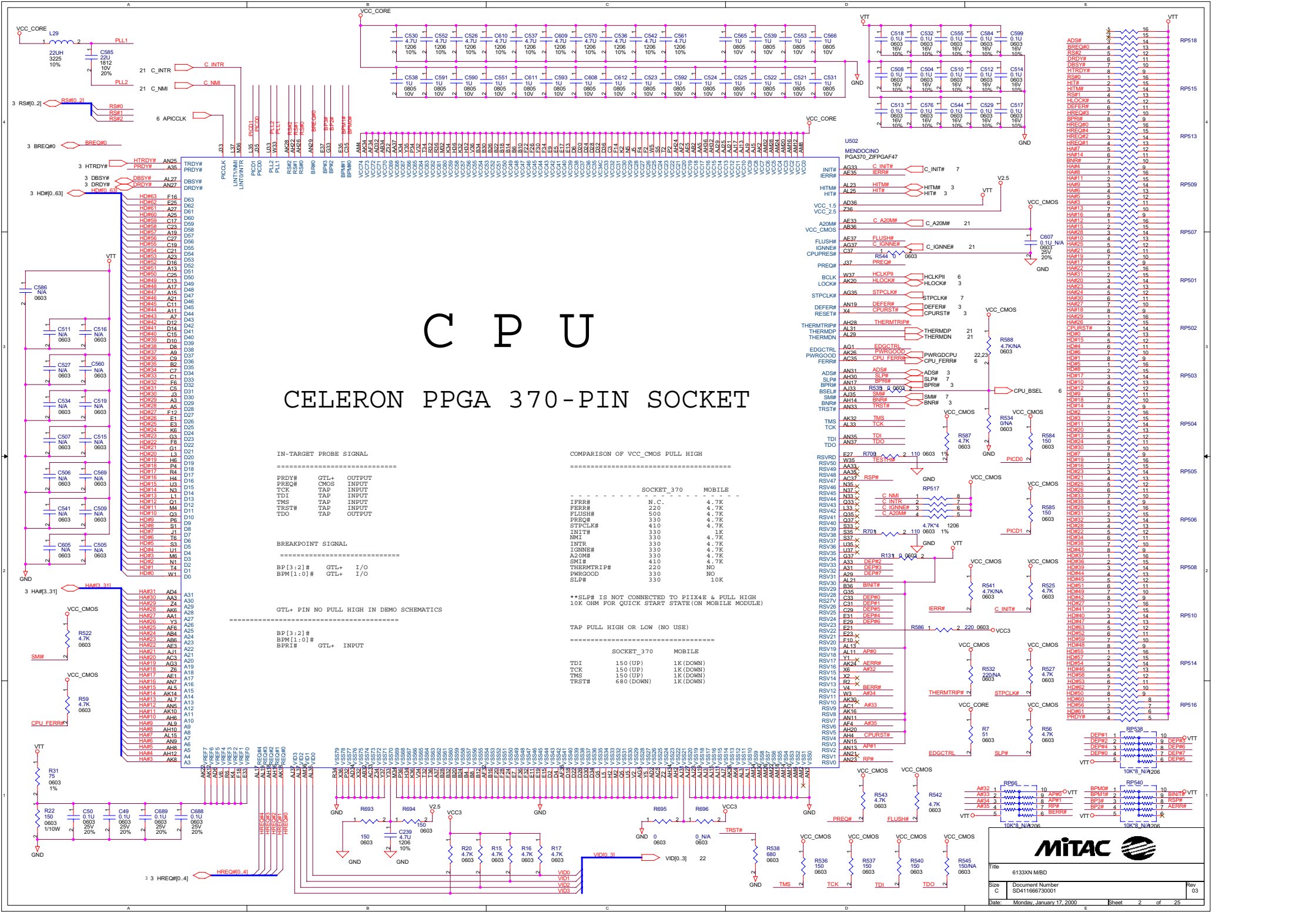
REV	DESCRIPTION OF CHANGE	ECO	DATE	APPROVAL
R00	Relayout base on 6133SX M/B R01 1. Replaced embeded controller from Hitachi H8 to NS PC87570. 2. Add Socket 370 FPGA CPU support. 3. Shared system BIOS memory. 4. Replace USB connector. 5. Remove 7408. 6. Remove 3384. 7. Remove 74164.		8/30/'99	
R01	1. Add VDD5N to do power reset. 2. Change T_DATA and T_CLK from port 1 to port 3. 3. Add cmos between core logic and EC to prevent current leakage. 4. Add 3384.		9/15/'99	
R02	1. Reserve FC-PGA solution. 2. Phase in EMI solution.		11/05/'99	
R03	1. Relayout to phase in Sanyo HPA LM-JK63-22NTR panel.		01/13/'00	

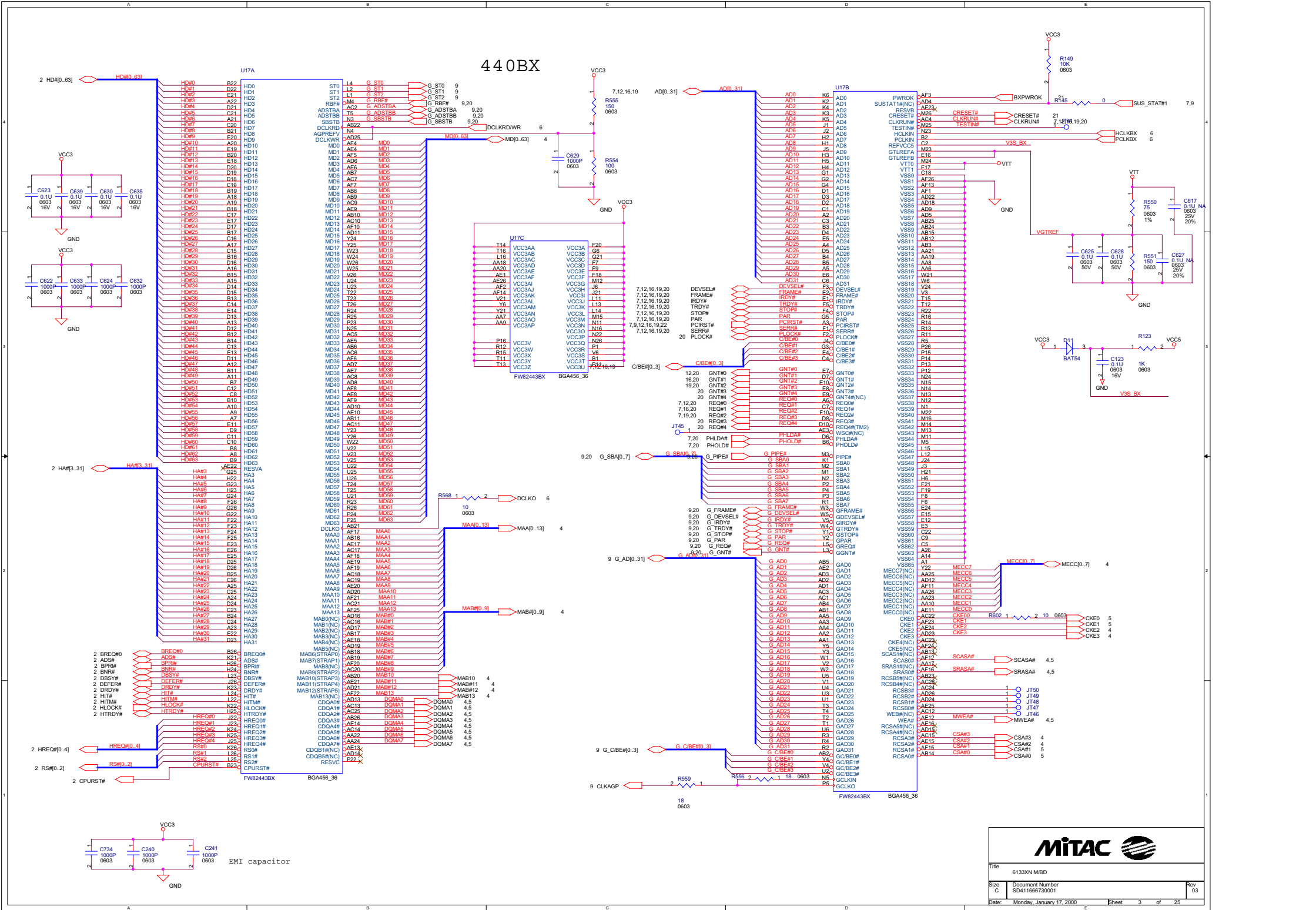


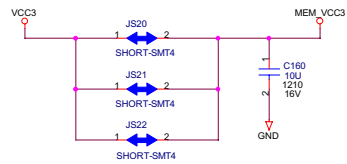
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				Title	6133XN M/B
				Size	Document Number
				C	SD41667120003
				Date	Monday, January 17, 2000
				Sheet	1 of 25
				Rev	03

C P U

CELERON PPGA 370-PIN SOCKET

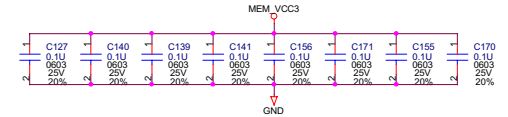




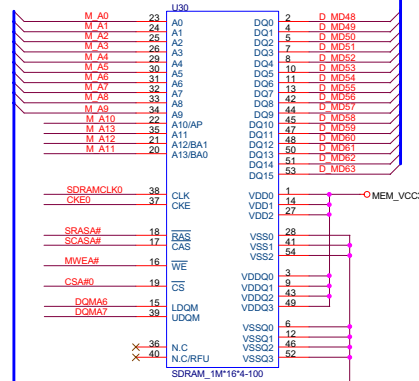
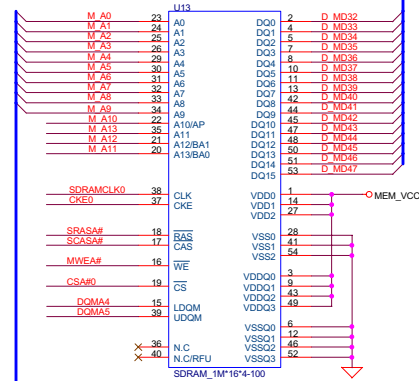
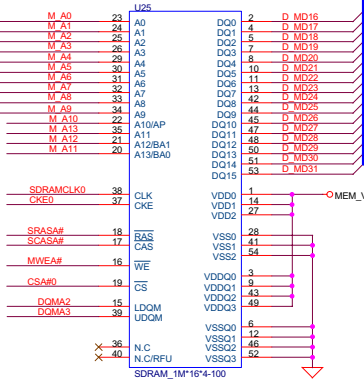
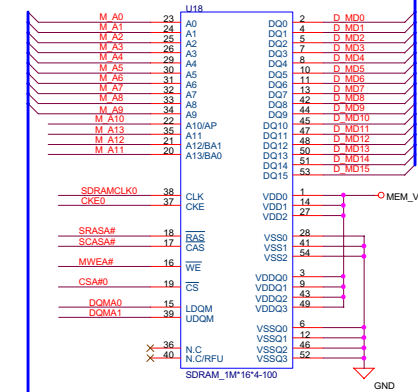


ON BOARD SDRAM 0 (32 MB)

100MB SDRAM 4BANK*1M*16bit*4CHIPS



4 D_MD0[0..63]

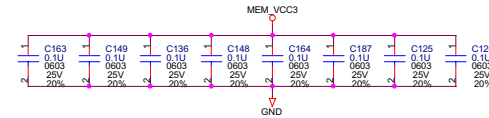


4 M_A[0..9]

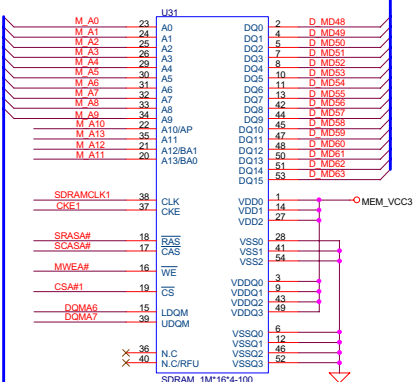
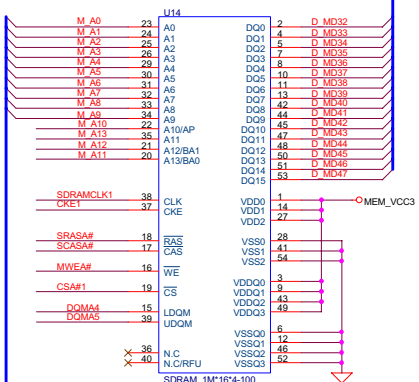
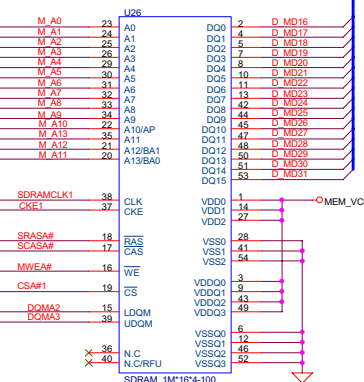
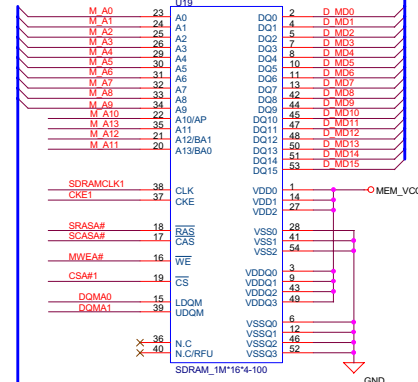


ON BOARD SDRAM 1 (32 MB), RESERVED ONLY

100MB SDRAM 4BANK*1M*16bit*4CHIPS

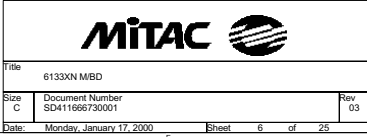


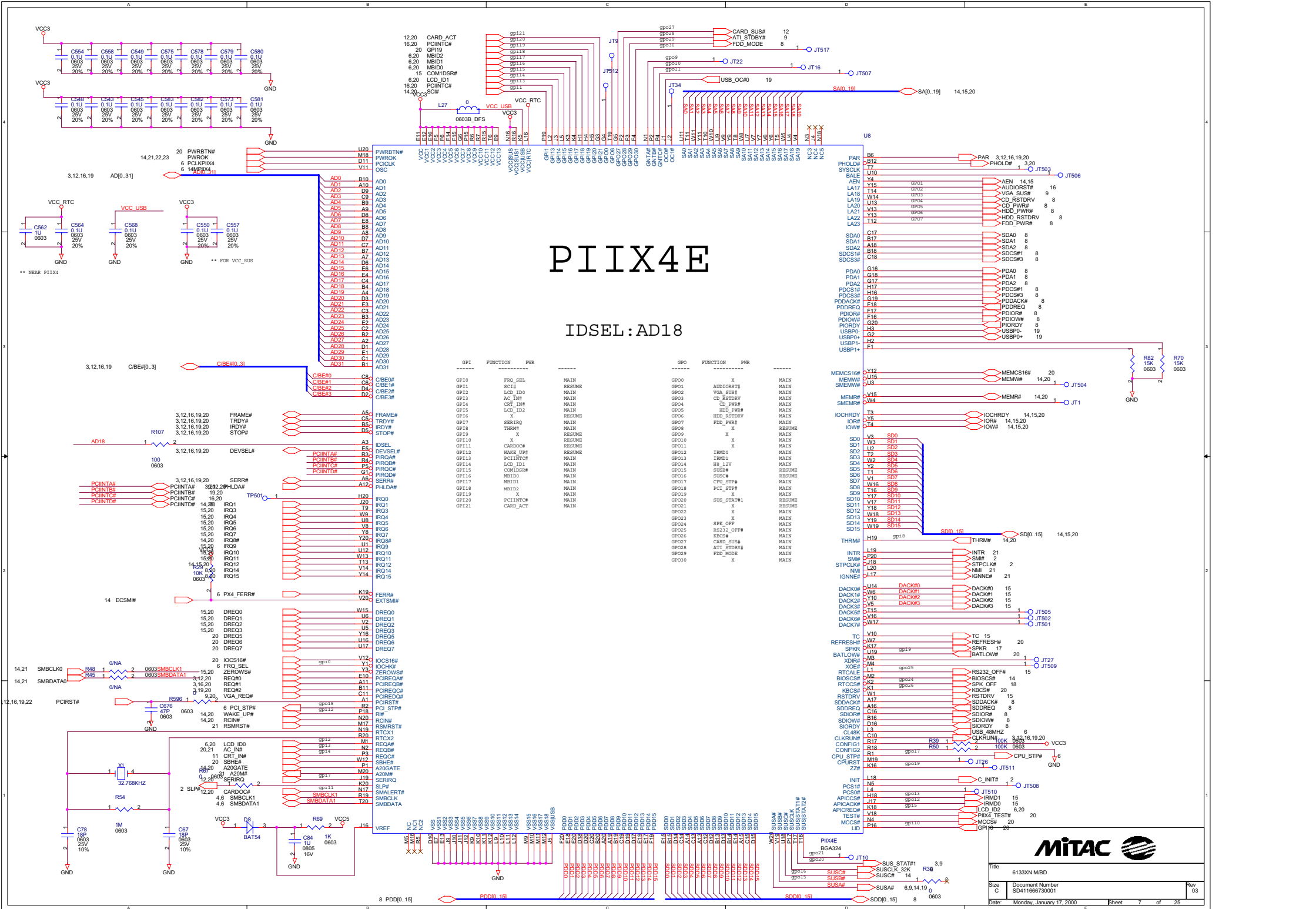
4 D_MD0[0..63]



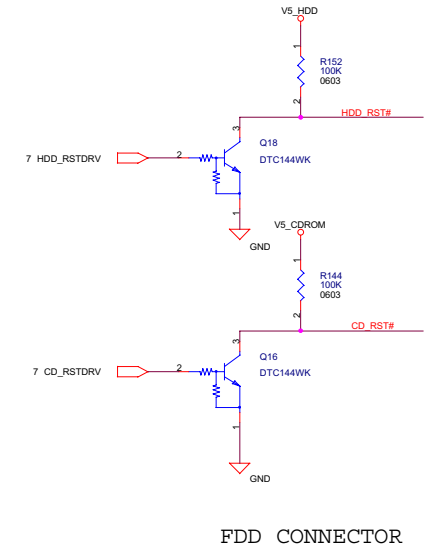
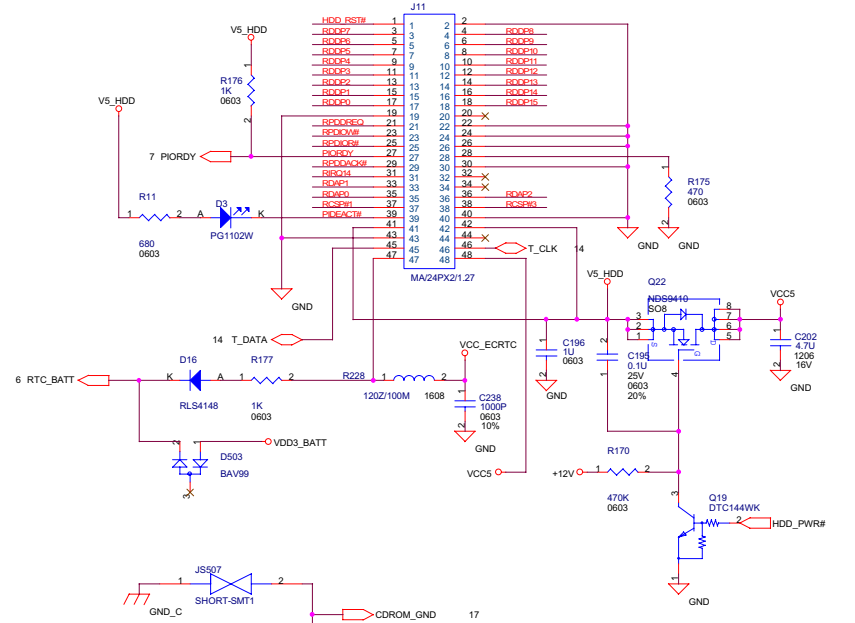
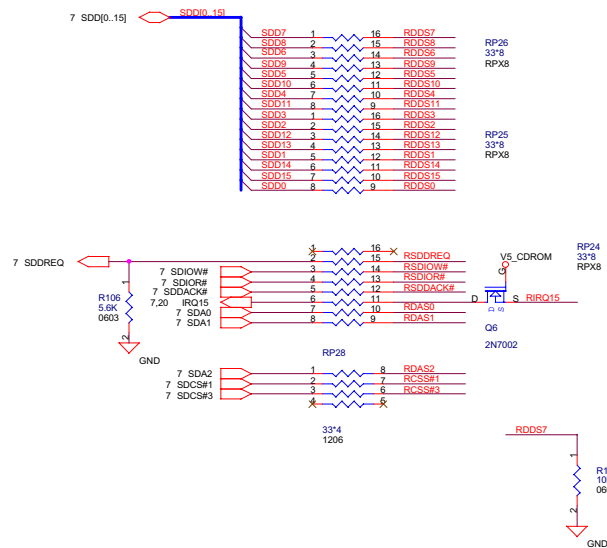
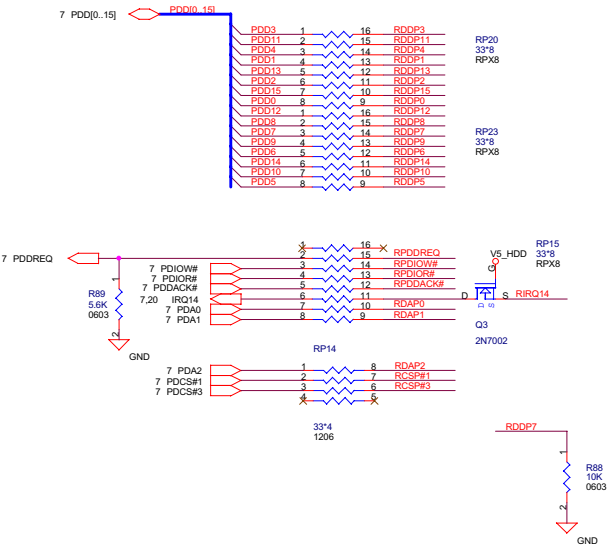
4 M_A[0..9]



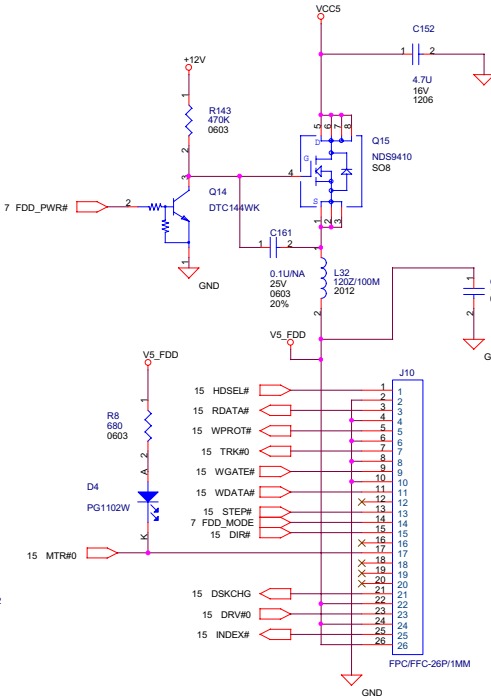
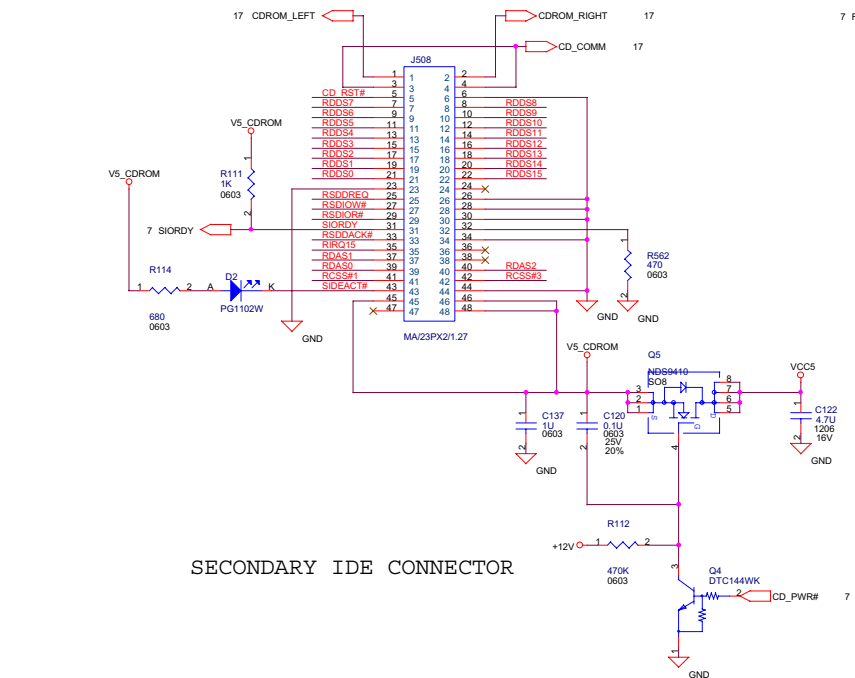


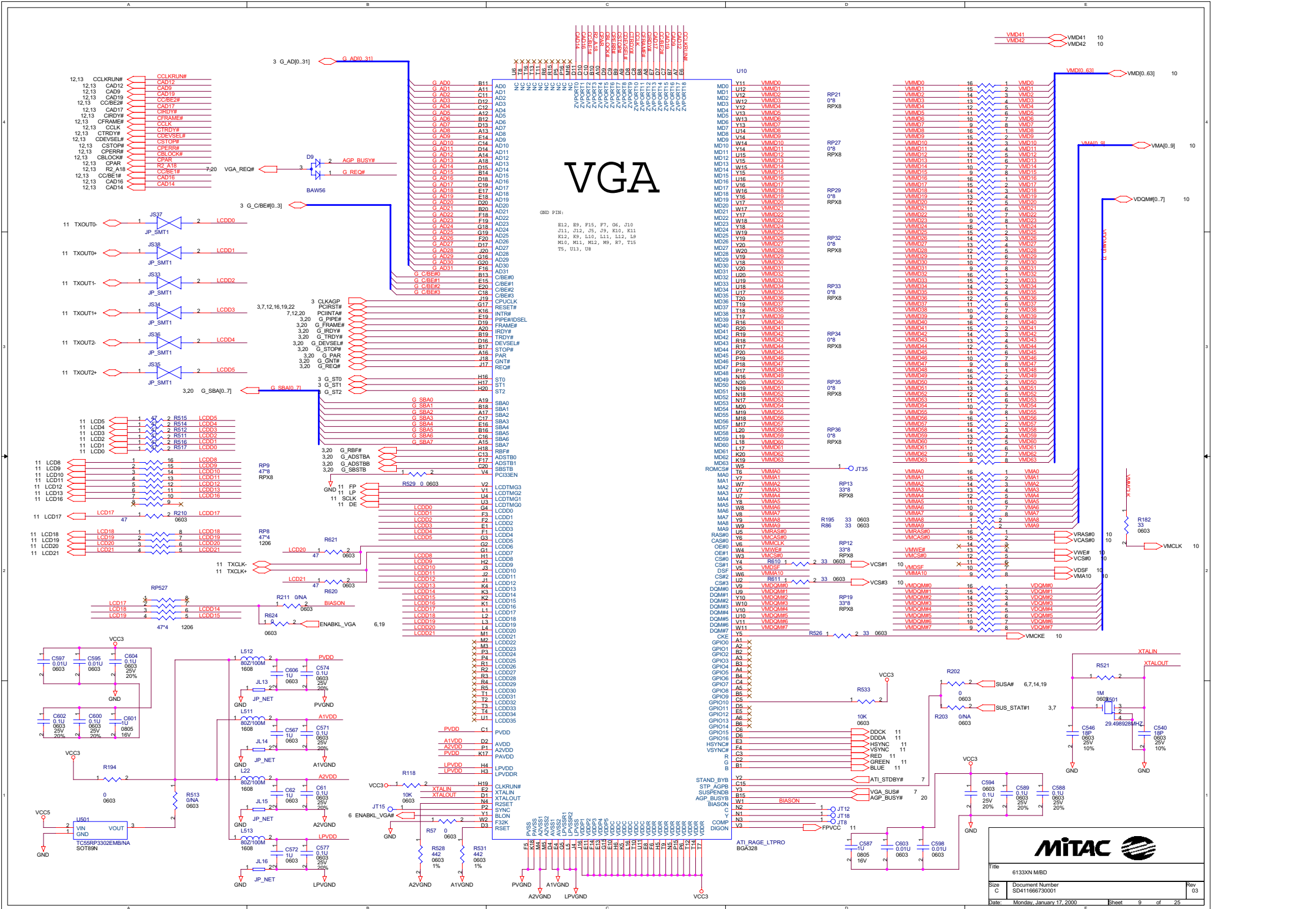


PRIMARY IDE & GLIDE PAD CONNECTOR



SECONDARY IDE CONNECTOR





FOR SAMSUNG

9 VCS#1 VCS#1

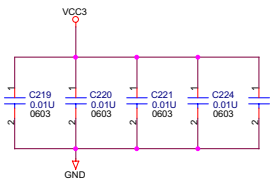
9 VCS#3 VCS#3

FOR HYUNDAI, ELITE

9 VMD[0..63] VMD[0..63]

9 VMA[0..9] VMA[0..9]

9 VMA10 VMA10



9 VMCKE

9 VCS#0

9 VRAS#0

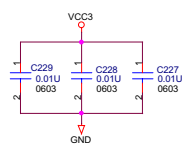
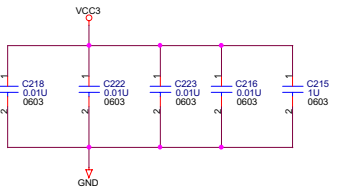
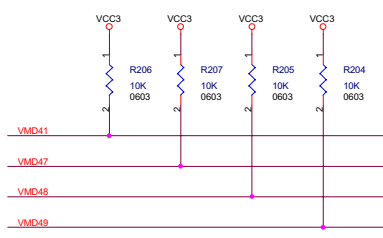
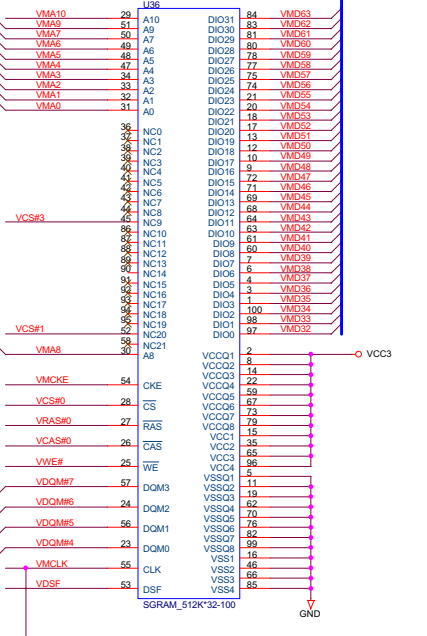
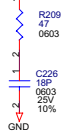
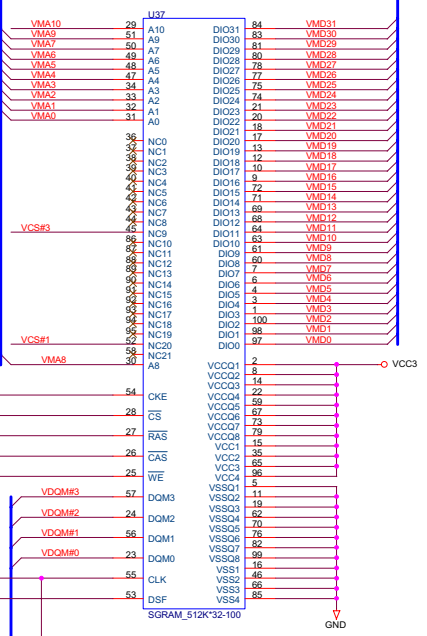
9 VCAS#0

9 VWE#

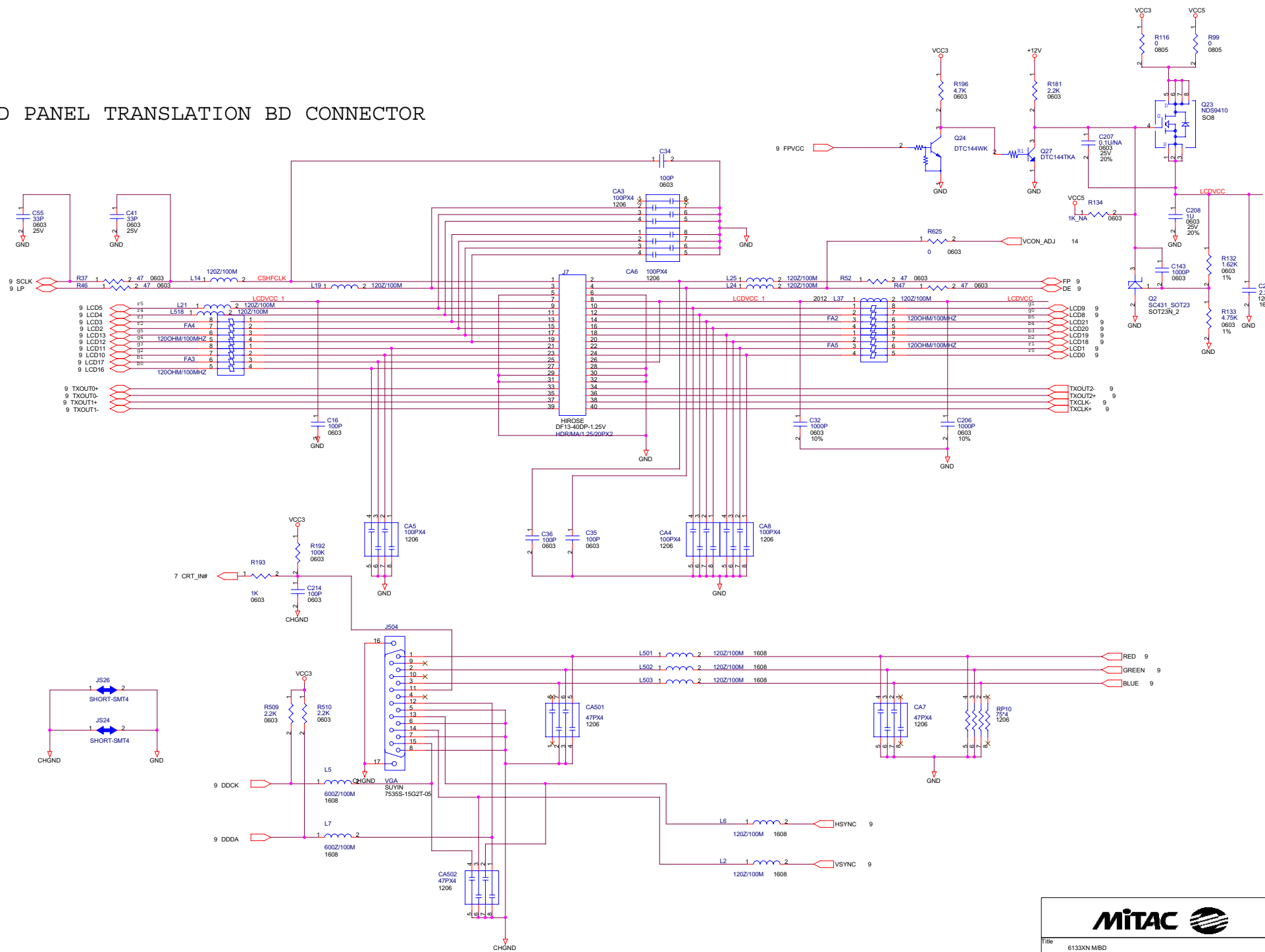
9 VMCLK

9 VDSF

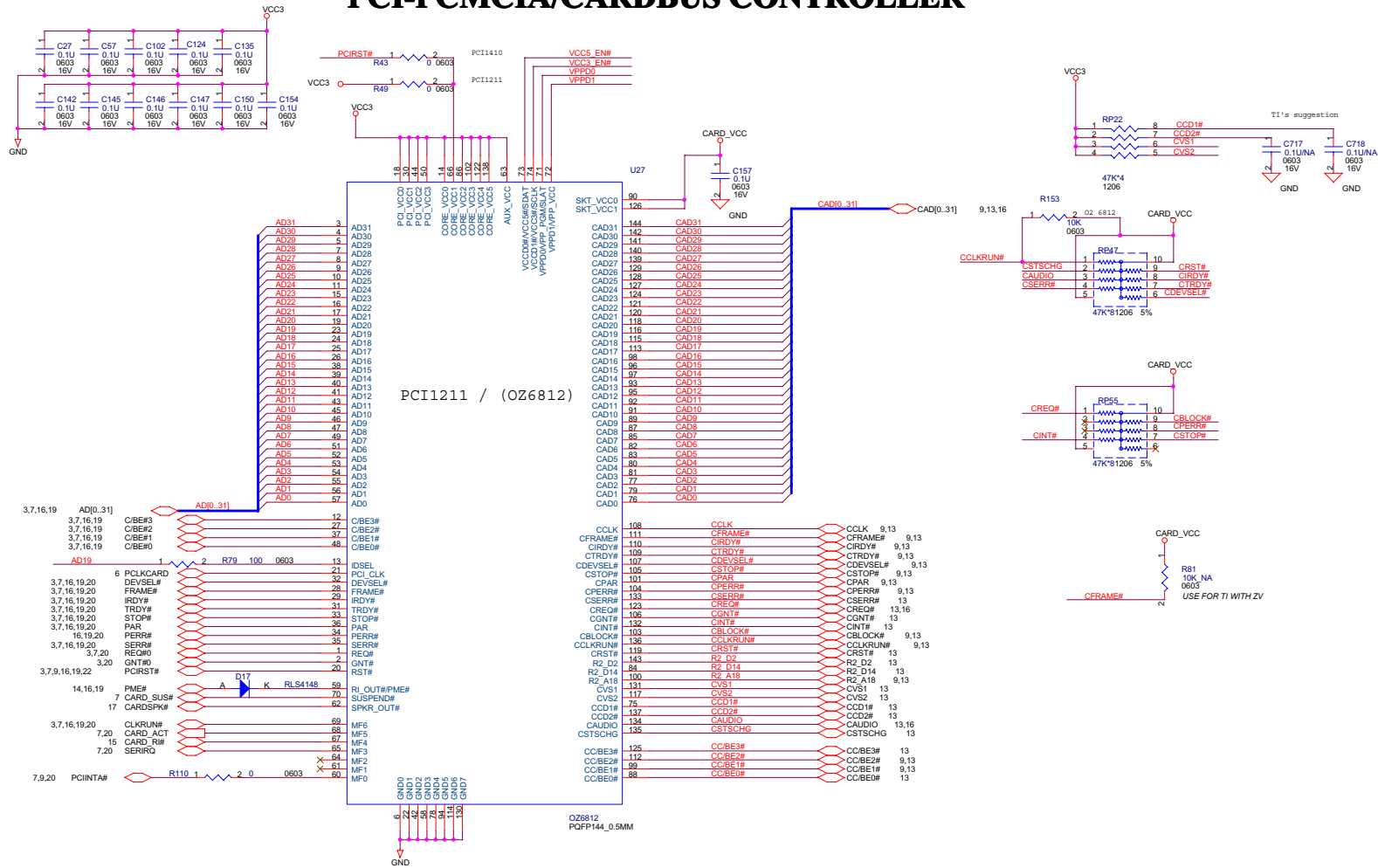
9 VDQM[0..7]



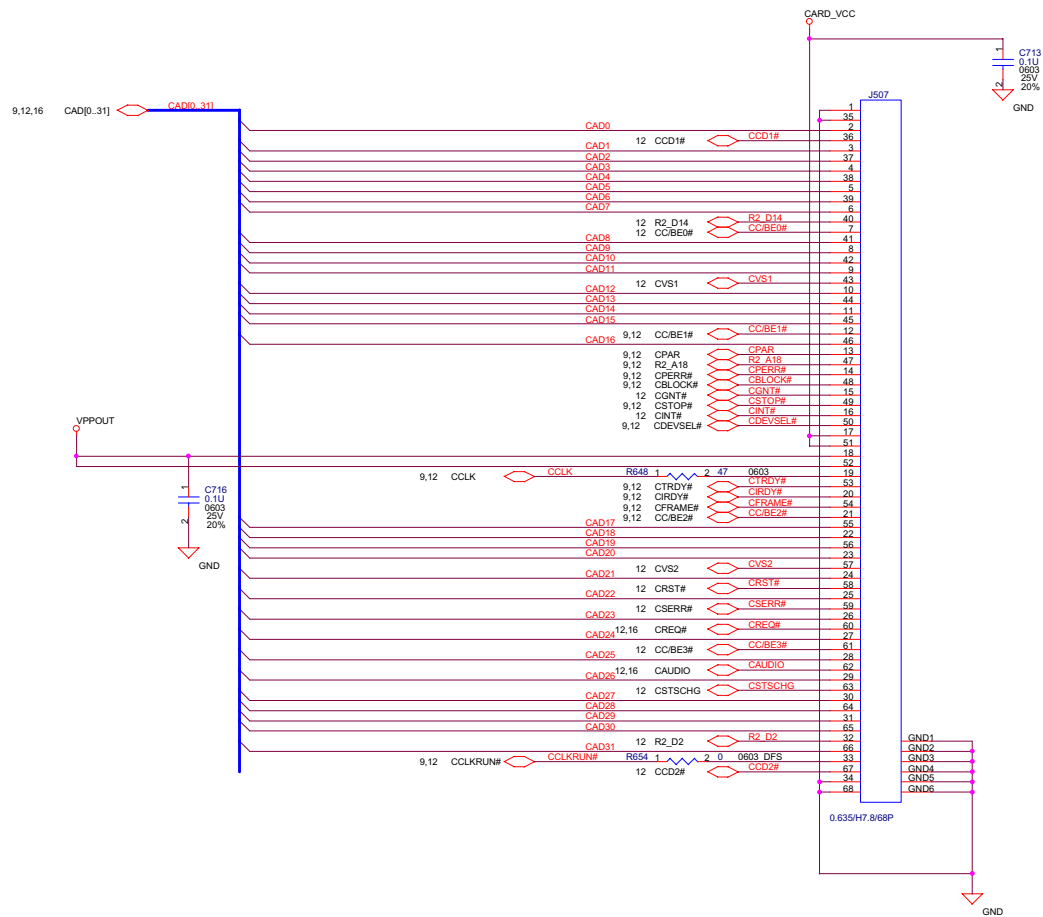
LCD PANEL TRANSLATION BD CONNECTOR

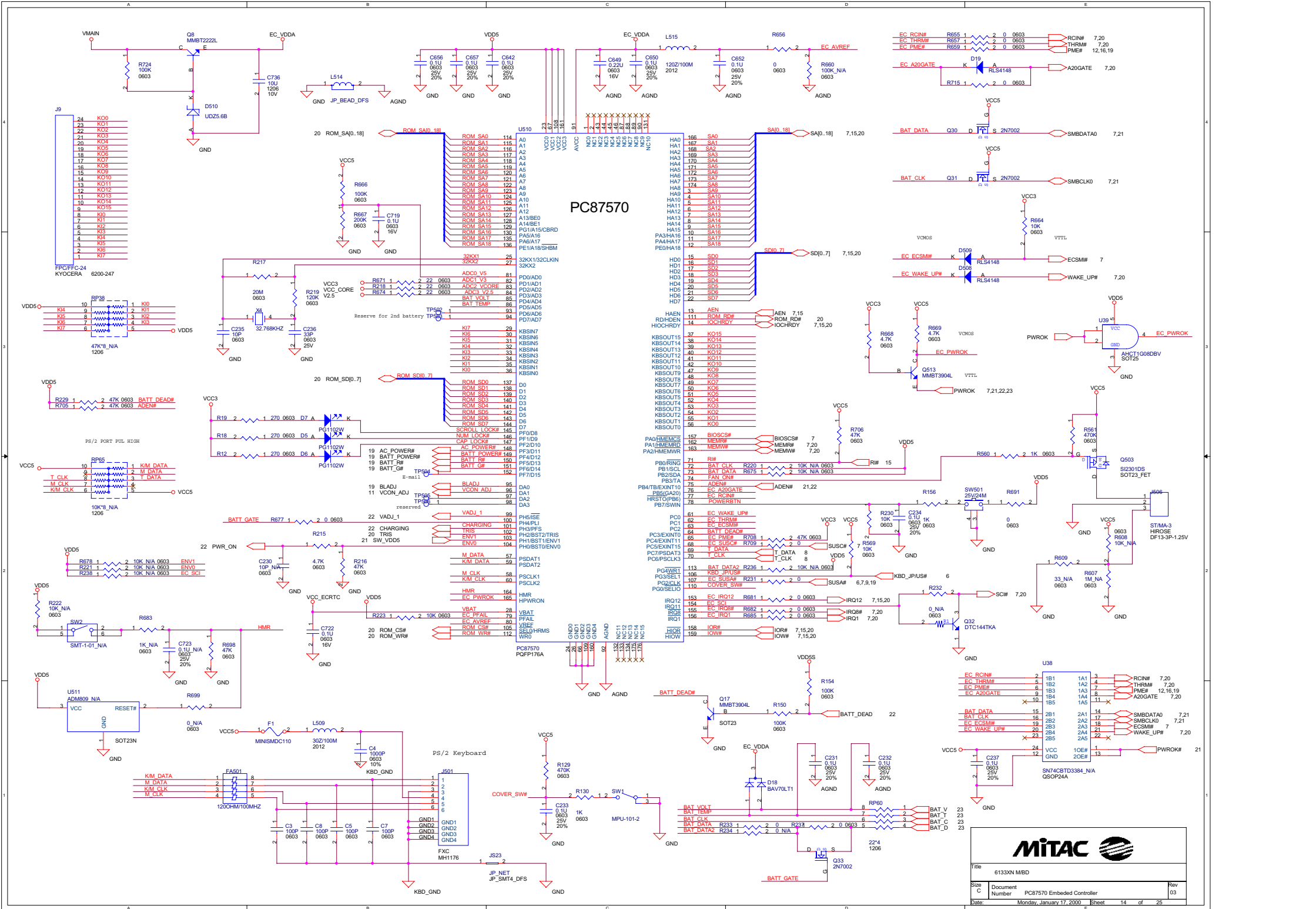


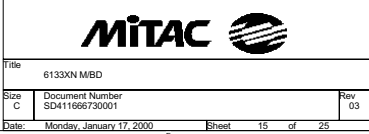
PCI-PCMCIA/CARDBUS CONTROLLER

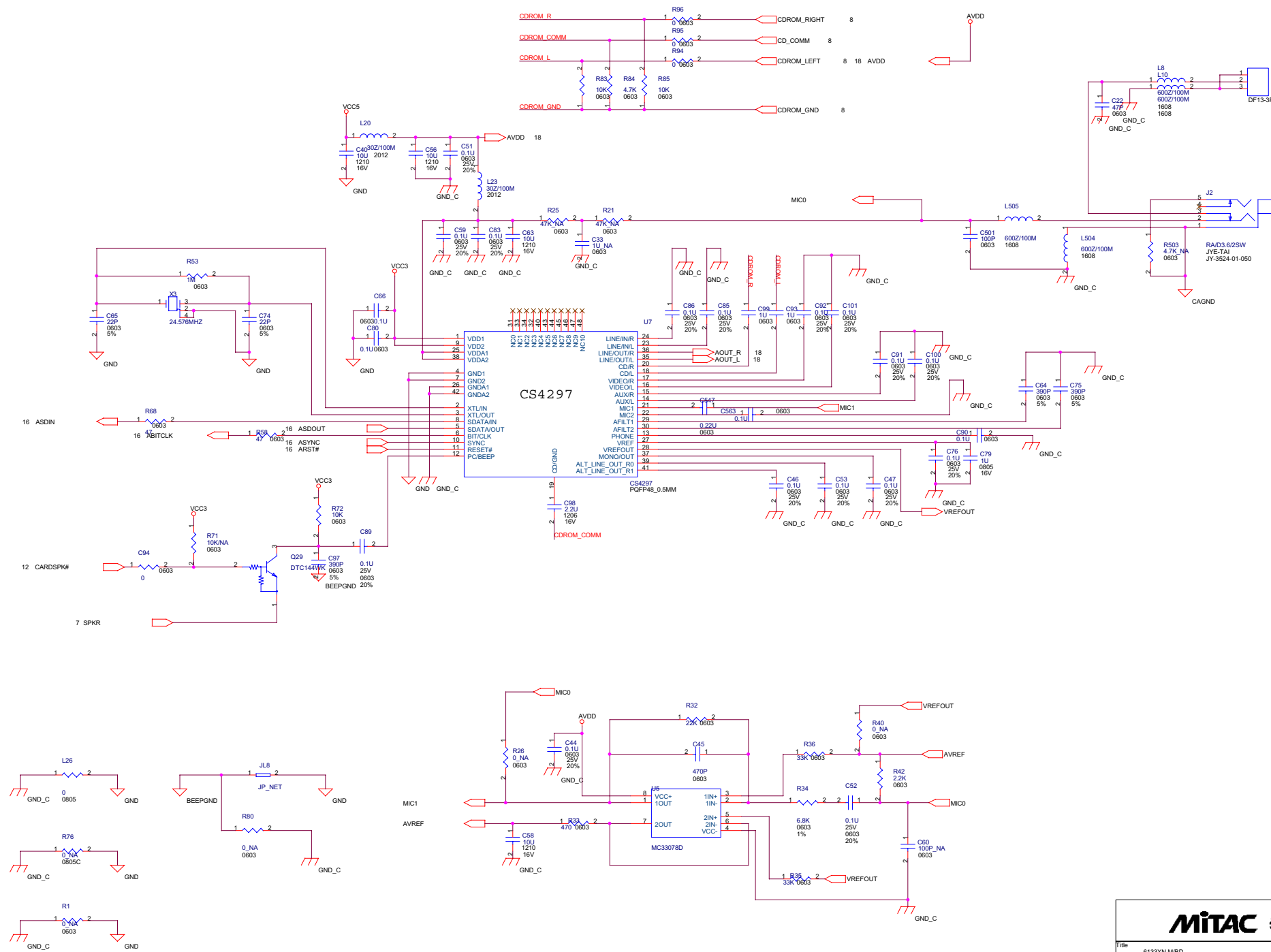


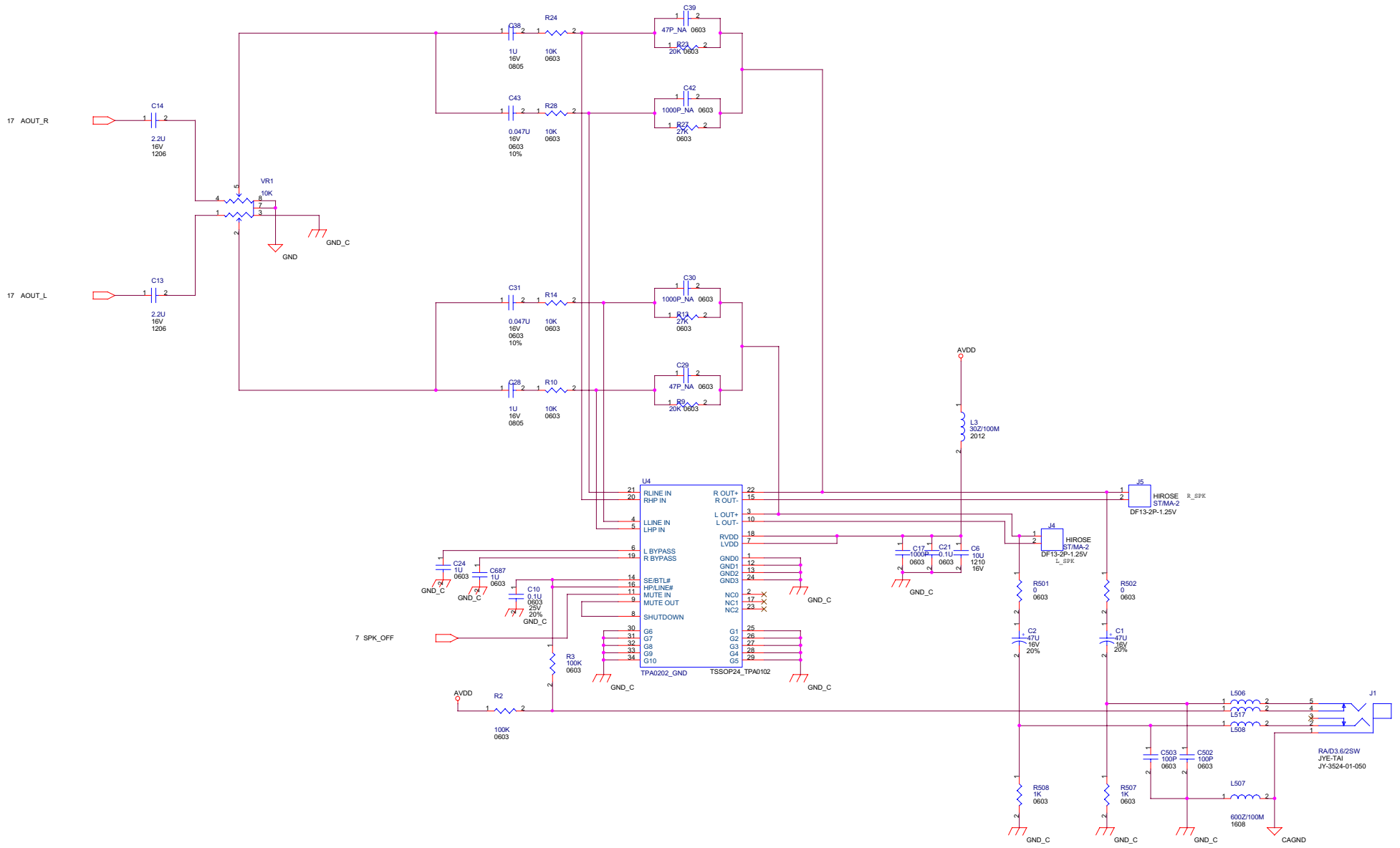
PCMCIA/ CARDBUS SLOT





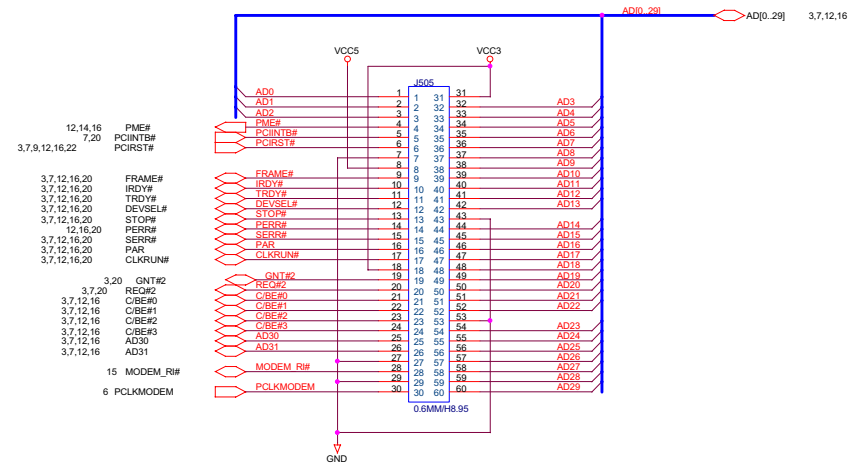






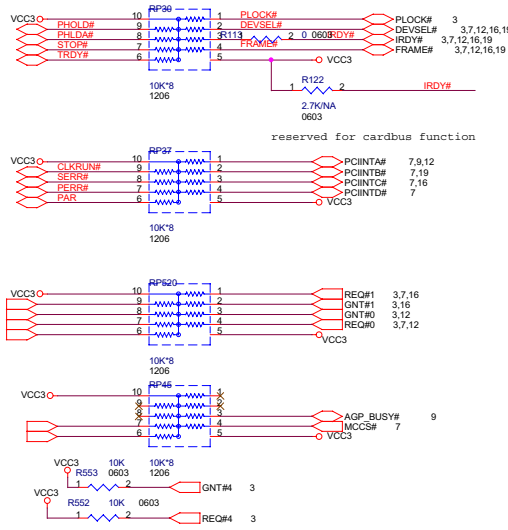
The schematic illustrates the electrical connections between various components on the PCB. Key elements include:

- Power Management:** A voltage regulator section featuring U22C, U22A, and U22B (74AHC14_V TSSOP14) configured as inverters/buffers. It includes decoupling capacitors C9, C23, C153, and C28.
- Signal Processing:** A buffer stage with Q12 (DTC144TKA_N/A) and Q13 (DTC144TKA_N/A) transistors, along with associated resistors R235 and R142.
- Connectivity:** Multiple connectors are shown, including J3 (HDI4PX1USB), J505 (JP_NET), J506 (JP_SMT4_DFS), J8 (HIROSE ST/MA-10 DF13-10P-1.25V), and J17 (L17 600Z/100M).
- Passive Components:** Numerous resistors (R5, R6, R74, R75, R77, R78, R140, R142, R235) and capacitors (C9, C23, C153, C25, C28, C37) are distributed throughout the circuit for timing, filtering, and impedance matching.
- Grounding:** Multiple ground symbols (GND) indicate the reference plane for the circuit.

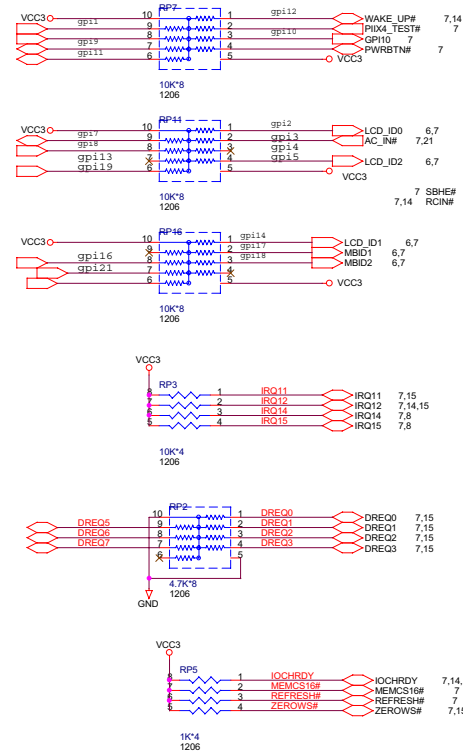


MITAC

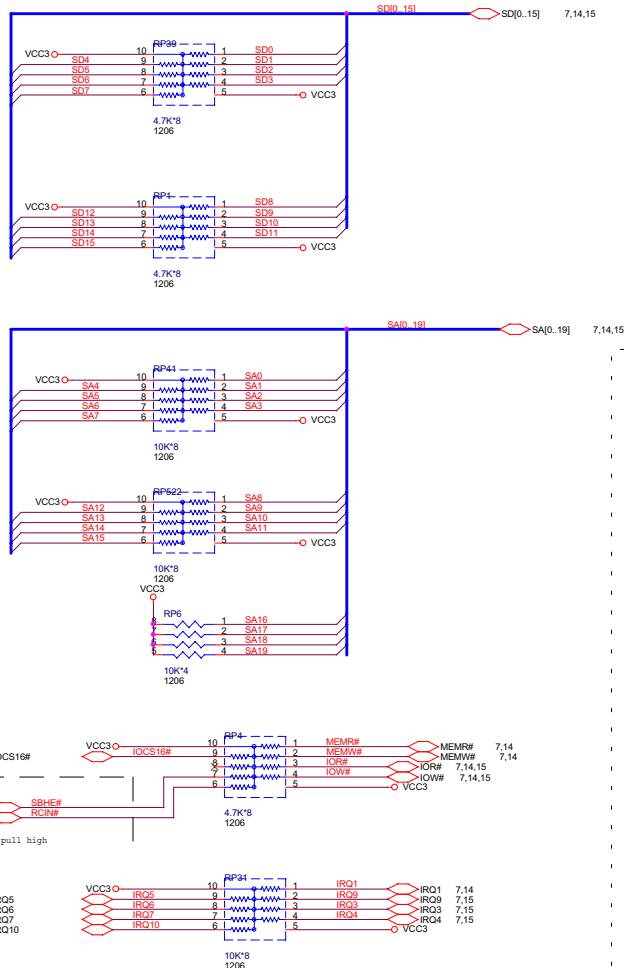
PCI PULL HIGH



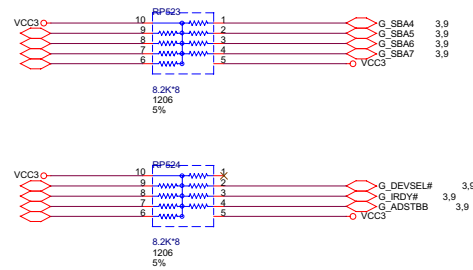
GPIN PULL HIGH



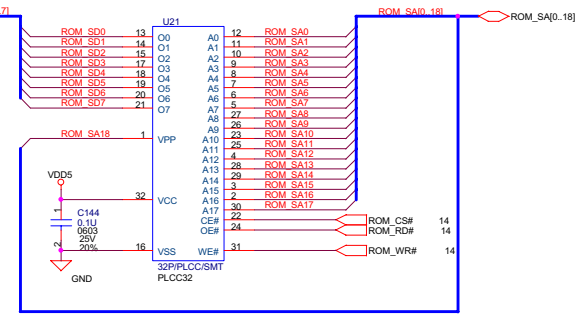
ISA PULL HIGH



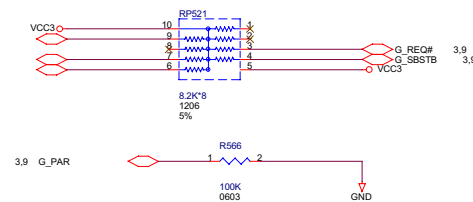
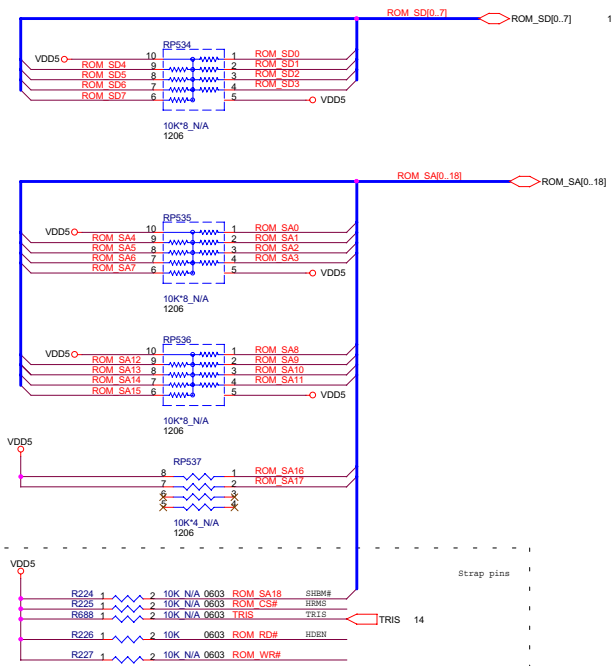
AGP PULL HIGH

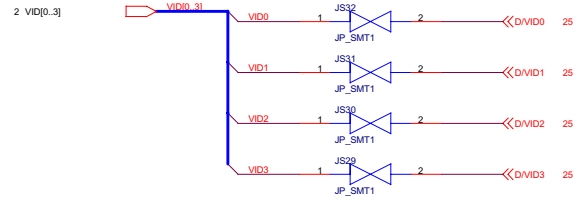
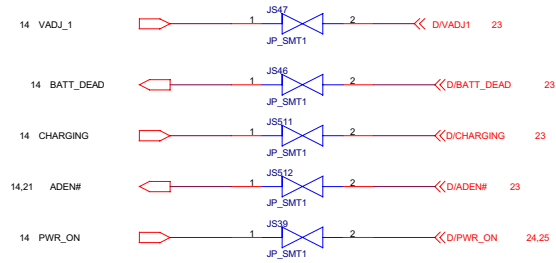
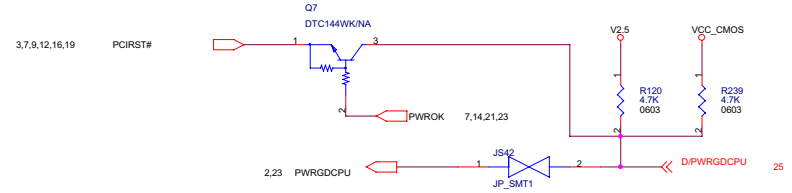
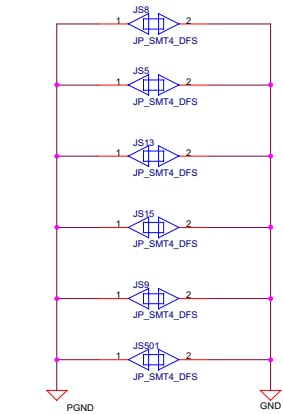
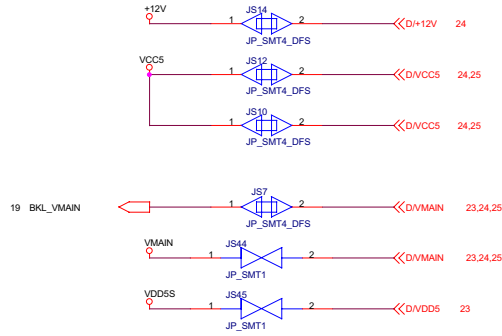
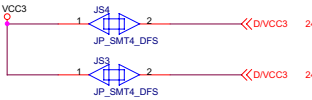
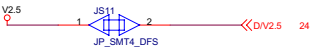
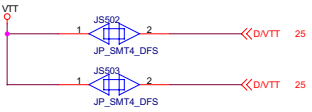
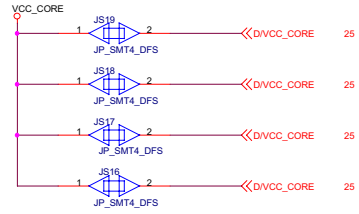


SYSTEM BIOS



Shared Flash ROM Pull Highs





Title			6133XN MBD
Size			Document Number
C			SD411666730001
Date:			Monday, January 17, 2000
Sheet			22 of 25
Rev			03

