

## Software Functional Overview

### 3.1 Overview

The MD02 is an IBM PC/AT compatible Notebook PC, which supports the Intel Micro-PGA Pentium M CPU processors family. The following are the major features that MD02 supports.

- § Microsoft PC99 logo and Win XP logo approval.
- § Offer 1024x768 XGA display with 13.3 XGA LCD panel.
- § Support ACPI 1.0B (or above).
- § Support PCI 2.1 (or above).
- § Support AGP 2.0.
- § Support SMBIOS 2.3.
- § Support DDR266/200 SDRAM.
- § Support 100/133 Mhz CPU front side bus.

### 3.2 Summary of the BIOS Specification

The summary of the BIOS specification is as the below description:

| Controller Chip | Description  |
|-----------------|--|
| BIOS Feature    | <ul style="list-style-type: none"> <li>§ Microsoft PC99 logo and WinXP logo approval.</li> <li>§ Support Boot Block / Crisis Rescue.</li> <li>§ APM 1.2 Compliance</li> <li>§ Support ACPI 1.0B (or above) Spec.</li> <li>§ Support PCI 2.1 (or above) Spec.</li> <li>§ Support SMBIOS 2.3 (or above) Spec</li> <li>§ Support Windows XP.</li> <li>§ Support flash function including both DOS and Windows interface for new BIOS update.</li> <li>§ Support US keyboard .</li> <li>§ Support boot from LAN , USB FDD/FLASH , HDD and CDROM Drive.</li> <li>§ Support Phoenix First BIOS.</li> </ul> |
| CPU             | Auto detecting the CPU type and speed for Intel Dothan based system.<br>Support Intel Geyserville III Technology .   |
| DRAM            | Auto sizing and detection. Support PC-200/266/333 DDR SDRAM.   |
| Cache           | <ul style="list-style-type: none"> <li>§ Level 2 SRAM auto sizing and detection.</li> <li>§ Always enable CPU L1 and L2 cache.</li> </ul>  |
| Shadow          | Always enable VGA and System BIOS shadow   |
| Display         | <ul style="list-style-type: none"> <li>§ System auto detects LCD or CRT presence on boot and lid closed.</li> <li>§ Support Panning while LCD in a display resolution greater than supported.</li> <li>§ Support Microsoft Direct 3D.</li> <li>§ Support AGP 4x BUS.</li> </ul>  |

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|                                      |   |
|--------------------------------------|---|
| Hard Disk                            | <ul style="list-style-type: none"><li>§ Enhanced IDE spec.</li><li>§ Support auto IDE detection.</li><li>§ Support LBA mode for larger capacity HDD.</li><li>§ Support Ultra DMA 33/66/100.</li><li>§ Support Fast PIO mode 1-4 transfer.</li><li>§ Support 32 bit PIO transfer.</li><li>§ Support Multi-Sector transfer.</li><li>§ Support SMART monitoring.</li></ul> |
| Multi Boot                           | Allow the user to select boot from FDD, HDD and CD-ROM  |
| Plug and Play                        | Support PnP Run Time Service and conflict-free allocation of resource during POST   |
| Smart Battery                        | Support BIOS interface to pass battery information to the application via SMBus   |
| Keyboard Controller                  | Support Fn hot keys, one Win95 hot keys, built-in Glide Pad.  |
| PCMCIA                               | Compliant with PCMCIA 2.1 specification   |
| Power Management Support (ACPI Mode) | <p>The power management is compliant with ACPI 1.0B specification and supports the following power state:</p> <ul style="list-style-type: none"><li>§ S0 (Full-On) Mode</li><li>§ S3 (STR) Mode</li><li>§ S4 (STD) Mode</li><li>§ S5 (Soft-Off) Mode</li></ul>  |

### 3.3 Subsystem Software Functions

This section provides introduction on the software functions of the notebook subsystems and BIOS related function.

#### 3.3.1 Key Chipset Summary

Following are the main chipsets used in the notebook:

| Controller Chip     | Vendor    | Description             |
|---------------------|-----------|-------------------------|
| Processor           | Intel     | Mobile Dothan           |
| North Bridge        | Intel     | MontaraGM+              |
| South Bridge        | Intel     | ICH4                    |
| Video Controller    | Intel     | Embedded in MontaraGM+  |
| PCMCIA Controller   | TI        | PCI4510                 |
| Audio Chip          | Intel     | South Bridge Integrated |
| Audio Codec         | Intel     | ICH4                    |
| Keyboard Controller | Misubishi | M38857M8                |
| PMU Controller      | NEC       | PMU08                   |
| ROM BIOS            | SST       | 49LF004A                |
| Clock Generator     | IMI       | CY28346                 |
| Temperature Sensor  | NS        | MAX6690                 |
| IEE 1394            | TI        | PCI4510                 |
| LAN                 | Intel     | ICH4-M+BroadCom BCM4401 |
| Modem               | Intel     | MDC AC'97               |

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## 3.3.2 System Memory

The system memory consists of SDRAM memory on 64-bit bus and the module size options are 128/256/512/1GMB upward. The BIOS will automatically detect the amount of memory in the system and configure CMOS accordingly during the POST (Power-On Self Test) process. This must be done in a way that requires no user interaction.

| Base SO-DIMM DRAM slot<br>(Bank 0&1) | Expansion SO-DIMM DRAM slot<br>(Bank 2&3) | Total Size |
|--------------------------------------|---|------------|
| 128MB                                | NIL                                       | 128MB      |
| 128MB                                | 128MB                                     | 256MB      |
| 128MB                                | 256MB                                     | 384MB      |
| 128MB                                | 512MB                                     | 640MB      |
| 128MB                                | 1GB                                       | 1128MB     |
| 256MB                                | NIL                                       | 256MB      |
| 256MB                                | 128MB                                     | 384MB      |
| 256MB                                | 256MB                                     | 512MB      |
| 256MB                                | 512MB                                     | 768MB      |
| 256MB                                | 1GB                                       | 1256MB     |
| 512MB                                | NIL                                       | 512MB      |
| 512MB                                | 128MB                                     | 640MB      |
| 512MB                                | 256MB                                     | 768MB      |
| 512MB                                | 512MB                                     | 1GB        |
| 1GB                                  | 1GB                                       | 2GB        |

## 3.3.3 Video

The Video subsystem used External DDR memory of Video memory. The system will support the true ZV port, the Microsoft Direct 3D assist, simultaneous display, monitor sense for auto display on boot and VESA Super VGA function call.

### Supported Video Mode

The following is the display modes supported by the Intel Mobility Video control in LCD only, CRT only, and simultaneous mode. The VGA BIOS will allow mode sets of resolutions greater than the panel size but only show as much mode display as will fit on the panel.

### Supported standard VGA modes:

The VGA BIOS supports the IBM VGA Standard 7-bit VGA modes numbers.

| Mode    | Pixel Resolution | Colors | Memory       |
|---------|------------------|--------|--------------|
| 00h/01h | 40*25            | 16     | Text         |
| 02h/03h | 80*25            | 16     | Text         |
| 04h/05h | 320*200          | 4      | 2-bit Planar |
| 06h     | 640*200          | 2      | 1-bit Planar |
| 07h     | 80*25            | Mono   | Text         |
| 0Dh     | 320*200          | 16     | 4-bit Planar |

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|     |         |      |              |
|-----|---------|------|--------------|
| 0Eh | 640*200 | 16   | 4-bit Planar |
| 0Fh | 640*350 | Mono | 1-bit Planar |
| 10h | 640*350 | 16   | 4-bit Planar |
| 11h | 640*480 | 2    | 2-bit Planar |
| 12h | 640*480 | 16   | 4-bit Planar |
| 13h | 320*200 | 256  | 8-bit Planar |

Note: All Standard VGA Modes are limited to the standard VGA refresh rates.

### Supported extended video modes:

CRT device will support all listed VESA mode; and other devices such as PANEL & TV may be limited to the mode support due to their characteristics.

| VESA Mode | Pixel Resolution | Memory Model    | Refresh Rates In (Hz)      | Minimum Memory |
|-----------|------------------|-----------------|----------------------------|----------------|
| 100h      | 640 x 400        | 8-bit Packed    | 70                         | 2MB            |
| 101h      | 640 x 480        | 8-bit Packed    | 60, 72, 75, 85             | 2MB            |
| 102h      | 800 x 600        | 4-bit Planar    | 60, 72, 75, 85, 100        | 2MB            |
| 103h      | 800 x 600        | 8-bit Packed    | 60, 72, 75, 85, 100        | 2MB            |
| 104h      | 1024 x 768       | 4-bit Planar    | 43(I), 60, 70, 75, 85, 100 | 2MB            |
| 105h      | 1024 x 768       | 8-bit Packed    | 43(I), 60, 70, 75, 85, 100 | 2MB            |
| 106h      | 1280 x 1024      | 4-bit Planar    | 43(I), 60, 75, 85          | 2MB            |
| 107h      | 1280 x 1024      | 8-bit Packed    | 43(I), 60, 75, 85          | 2MB            |
| 10Eh      | 320 x 200        | 16-bit Packed   | 70                         | 2MB            |
| 10Fh      | 320 x 200        | 32-bit Unpacked | 70                         | 2MB            |
| 111h      | 640 x 480        | 16-bit Packed   | 60, 72, 75, 85             | 2MB            |
| 112h      | 640 x 480        | 32-bit Unpacked | 60, 72, 75, 85             | 2MB            |
| 114h      | 800 x 600        | 16-bit Packed   | 60, 72, 75, 85, 100        | 2MB            |
| 115h      | 800 x 600        | 32-bit Unpacked | 60, 72, 75, 85, 100        | 2MB            |
| 117h      | 1024 x 768       | 16-bit Packed   | 43(I), 60, 70, 75, 85, 100 | 2MB            |
| 118h      | 1028 x 768       | 32-bit Unpacked | 43(I), 60, 70, 75, 85, 100 | 4MB            |
| 11Ah      | 1280 x 1024      | 16-bit Packed   | 43(I), 60, 75, 85          | 4MB            |
| 11Bh      | 1280 x 1024      | 32-bit Unpacked | 43(I), 60, 75, 85          | 8MB            |
| 11Dh      | 640 x 400        | 16-bit Packed   | 70                         | 2MB            |
| 11Eh      | 640 x 400        | 32-bit Packed   | 70                         | 2MB            |
| 120h      | 1600 x 1200      | 8-bit Packed    | 48(I), 60, 75, 85          | 2MB            |
| 122h      | 1600 x 1200      | 16-bit Packed   | 48(I), 60, 75, 85          | 4MB            |
| 124h      | 1600 x 1200      | 32-bit Unpacked | 48(I), 60, 75, 85          | 8MB            |
| 12Ah      | 640 x 480        | 24-bit Packed   | 60, 72, 75, 85             | 2MB            |
| 12Bh      | 800 x 600        | 24-bit Packed   | 60, 72, 75, 85, 100        | 2MB            |
| 12Ch      | 1024 x 768       | 24-bit Packed   | 43(I), 60, 70, 75, 85, 100 | 4MB            |
| 12Dh      | 1280 x 1024      | 24-bit Packed   | 43(I), 60, 75, 85          | 4MB            |
| 12Eh      | 320 x 200        | 8-bit Packed    | 70                         | 2MB            |
| 131h      | 320 x 200        | 8-bit Packed    | 72                         | 2MB            |
| 133h      | 320 x 200        | 16-bit Packed   | 72                         | 2MB            |

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|       |             |                |        |     |
|-------|-------------|----------------|--------|-----|
| 134h  | 320 x 200   | 32-bit Packed  | 72     | 2MB |
| 13Bh* | 1400 x 1050 | 8-bit Packed   | 60, 75 | 2MB |
| 13Ch* | 1400 x 1050 | 16-bit Packed  | 60, 75 | 4MB |
| 13Eh* | 1400 x 1050 | 32-bitUnpacked | 60, 75 | 8MB |
| 141h  | 400 x 300   | 8-bit Packed   | 72     | 2MB |
| 143h  | 400 x 300   | 16-bit Packed  | 72     | 2MB |
| 144h  | 400 x 300   | 32-bitUnpacked | 72     | 2MB |
| 151h  | 512 x 384   | 8-bit Packed   | 70     | 2MB |
| 153h  | 512 x 384   | 16-bit Packed  | 70     | 2MB |
| 154h  | 512 x 384   | 32-bitUnpacked | 70     | 2MB |
| 171h  | 720 x 480   | 8-bit Packed   | 75     | 2MB |
| 173h  | 720 x 480   | 16-bit Packed  | 75     | 2MB |
| 174h  | 720 x 480   | 24-bit Packed  | 75     | 2MB |
| 175h  | 720 x 480   | 32-bitUnpacked | 75     | 2MB |
| 176h  | 720 x 576   | 8-bit Packed   | 75     | 2MB |
| 178h  | 720 x 576   | 16-bit Packed  | 75     | 2MB |
| 179h  | 720 x 576   | 24-bit Packed  | 75     | 2MB |
| 17Ah  | 720 x 576   | 32-bitUnpacked | 75     | 2MB |

Note: “\*” The modes may not be available. Their availability should be determined by VESA function calls.

## Panel Type Initialization

The VGA BIOS will issue INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPIO pins before the VGA chip initialized, and pass this information to VGA BIOS through INT 15 Function 4E00h.

### LCD Panel ID pin Definition:

| VT82C686B GPI Pins |          |          |          | Panel Type |
|--------------------|----------|----------|----------|------------|
| GPI [23]           | GPI [17] | GPI [11] | GPI [10] |            |
| 0                  | 0        | 0        | 0        |            |
| 0                  | 0        | 0        | 1        | ID0        |
| 0                  | 0        | 1        | 0        | ID1        |
| 0                  | 0        | 1        | 1        |            |
| 0                  | 1        | 0        | 0        | ID2        |
| 0                  | 1        | 0        | 1        |            |
| 0                  | 1        | 1        | 0        |            |
| 0                  | 1        | 1        | 1        |            |
| 1                  | 0        | 0        | 0        | ID3        |
| 1                  | 0        | 0        | 1        |            |
| 1                  | 0        | 1        | 0        |            |
| 1                  | 0        | 1        | 1        |            |
| 1                  | 1        | 0        | 0        |            |

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|   |   |   |   |  |
|---|---|---|---|--|
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

### 3.3.4 Enhanced IDE

The system BIOS must be ready to support 4 IDE devices on two controllers. The BIOS support Ultra DMA33/66/100 and also supports automatic configuration of drives using both the LBA and CHS large drive remapping method. In addition to supporting standard drives through an auto-configuration process that does NOT require user involvement or confirmation. The system should automatically do this at POST time in a way that is transparent to the user. If a drive is connected to the bus, the drive should be automatically recognized, configured and available for use under MS-DOS 6.2x.

### 3.3.5 Audio

The audio subsystem will support the requirements identified by the AC'97 specification. Both software and hardware will control the volume level for the internal audio subsystem. In addition to the volume control, the user will be able to mute the sound to completely cut off the volume using both software and hardware.

### 3.3.7 PCMCIA

The PCMCIA controller chip of the notebook provides the following features:

- Individually accessed, dual-buffer implementation
- Support for 2 separate CardBus slots (one type III or two type II stacked)
- Support for 3.3v, 5v and 12v (flash programming) cards

### 3.3.8 LED Indicator

The table below lists down the functions of the Status LED indicator:

| Indicator            | Function Description  |
|----------------------|---|
| IDE accessing LED    | This LED will turn on while accessing the IDE Device.   |
| Battery Charging LED | Turn on (Blue) – Battery is under charging mode<br>Turn off – Battery full charged or no battery              |
| CapsLock LED         | This LED will turn on when the function of CapsLock is active.  |
| ScrollLock LED       | This LED will turn on when the function of ScrollLock is active.  |
| NumLock LED          | This LED will turn on when the function of NumLock is active.   |
| Power Status LED     | Yellow – System is powered on.<br>Yellow Blinking- System is entered suspend mode.<br>Turn off – Battery Low. |
| Mail LED             | This LED will turn on while Mail was arrived.   |

**i** - These LEDs will be turned off during Suspend mode.

### 3.3.9 Hot Keys Definition

All Hot keys must be active at all times under all operation systems.

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| Function        | Function                            | Handler              |
|-----------------|-------------------------------------|----------------------|
| Fn + F3         | Toggle Display (LCD/CRT/TV/LCD&CRT) | BIOS Handler         |
| Fn + F2         | RF ON/OFF                           | BIOS Handler         |
| Fn + F6         | System Speaker On/Off               | BIOS Handler         |
| Fn + F8         | Brightness Increase                 | Controlled by PMU08  |
| Fn + F9         | Brightness Decrease                 | Controlled by PMU08  |
| ScrLock         | Scroll Lock                         |                      |
| Internet Button | Internet Function Key               | Controlled by Driver |
| Mail Button     | Mail Function Key                   | Controlled by Driver |

### 3.3.10 Plug & Play

The BIOS supports the Plug and Play Specification 1.0A. (Include ESCD)

This section describes the device management. The system board devices and its resources are as follows:

| Device               | Connect Type | Resources                 |           |      |                          |
|----------------------|--------------|---------------------------|-----------|------|--------------------------|
|                      |              | I/O                       | IRQ       | DMA  | Memory                   |
| DMA Controller       | Static       | 00~0F, 81~8F              | -         | DMA5 | -                        |
| Interrupt Controller | Static       | 20~21, A0~A1              | IRQ2      | -    | -                        |
| System Timer         | Static       | 40~43                     | IRQ0      | -    | -                        |
| RTC                  | Static       | 70~71                     | IRQ8      | -    | -                        |
| ISA Bus              | Static       | -                         | -         | -    | -                        |
| System Speaker       | Static       | 61                        | -         | -    | -                        |
| System Board         | Static       | -                         | -         | -    | E0000~FFFFFF             |
| PnP Mother Board     | Static       | 80                        | -         | -    | -                        |
| Keyboard Controller  | Static       | 60, 64                    | IRQ1      | -    | -                        |
| PMU08 Controller     | Static       | 68, 6C                    | -         | -    | -                        |
| Math Coprocessor     | Static       | F0~FF                     | IRQ13     | -    | -                        |
| Glide Pad            | Static       | -                         | IRQ12     | -    | -                        |
| Video Controller     | Static       | 3B0~3BB, 3C0~3DF          | IRQ5      | -    | A0000~BFFFF, C0000~CFFFF |
| Dual IDE Controller  | Static       | 170~177, 1F0~1F7, 3F6     | IRQ14, 15 | -    | -                        |
| CardBus Controller   | Dynamic      | 3E0~3E1                   | IRQ10     | -    | -                        |
| Audio chip           | Dynamic      | 220~22F, 300~301, 388~38B | IRQ5      | DMA3 | -                        |
| IEEE1394             | Dynamic      |                           | IRQ10     |      |                          |
| Modem                | Dynamic      | 3E8~3EF                   | IRQ10     | -    | -                        |
| LAN                  | Dynamic      | 1080~10FF                 | IRQ10     | -    | -                        |
| USB Host Controller  | Dynamic      | EF80~EF9F                 | IRQ5      | -    | -                        |

### 3.3.11 PCI Device

The table below summarizes the PCI IDSEL Pin Allocation:

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| IDSEL Pin | PCI Device    |                 |                |
|-----------|---------------|-----------------|----------------|
|           | Device Number | Function Number | Device Name    |
| AD23      | Device 07     | Function 0      | RICOH Card Bus |
|           |               | Function 1      | RICOH IEEE1394 |
| AD17      | Device 01     | Function 0      | MINI PCI       |

The table below summarizes the INT Pin Allocation:

| INT Pin | PCI Device          |
|---------|---------------------|
| INTA    | CardBus/MiniPCI/LAN |
| INTB    | Cardbus/MiniPCI     |
| INTC    |                     |
| INTD    |                     |

The table below summarizes the PCI bus master Allocation:

| Arbiter | Signal      | Agents (Master) | Function            | Use |
|---------|-------------|-----------------|---------------------|-----|
|         | REQ00/GNT00 |                 |                     |     |
|         | REQ10/GNT10 | RICOH           | Card Bus Controller |     |
|         | REQ20/GNT20 |                 |                     |     |
|         | REQ30/GNT30 |                 |                     |     |
|         |             |                 |                     |     |
|         |             |                 |                     |     |

### 3.3.12 SMBus Devices

The SMBus is a two-wire interface through which the system can communicate with power-related chips. The BIOS should initialize the SMBus devices during POST.

#### ICH4 SMBus Connection Devices

| SMBus Device             | Host/Slave | Address | BIOS Need to Initialization  |
|--------------------------|------------|---------|--|
| SO-DIMM                  | Slave      | A0h/A2h | Memory Auto Sizing (SPD).  |
| CY28346<br>CLK Generator | Slave      | D2h     | Program the desired clock frequency (Pin23 output 24MHz, Pin22 output 48MHz) |

#### PMU 08 SMBus Connection Devices

| SMBus Device                      | Host/Slave | Addresses<br>A7 ~ A1 | BIOS Need to Initialization           |
|-----------------------------------|------------|----------------------|---------------------------------------|
| PMU08                             | Master     | 10h                  | Enable PS01 decode interface          |
| MAX6690 (Thermal sensor)          | Slave      | 9Ch                  | Program the desired temperature range |
| Battery (1 <sup>st</sup> Battery) | Slave      | A8h                  | No Need                               |

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## I/O Map

| Hex Address    | Device                                 |
|----------------|--|
| 000 - 01F      | 8237-1                                 |
| 020 - 021      | 8259-1                                 |
| 022            |  |
| 040 - 05F      | 8254                                   |
| 060 - 064      | Keyboard Controller                    |
| 068 - 06C      | PMU08 Controller                       |
| 070 - 07F      | RTC & NMI Mask                         |
| 080 - 08F      | DMA Page Registers                     |
| 092            | System Control Port                    |
| 0A0 - 0A1      | 8259-2                                 |
| 0B2            | Advanced Power Management Control Port |
| 0B3            | Advanced Power Management Status Port  |
| 0C0 - 0DF      | 8237-2                                 |
| 0F0 - 0FF      | Math Coprocessor                       |
| 170 - 177      | IDE Secondary Command Block            |
| 1F0 - 1F7      | IDE Primary Command Block              |
| 220 - 22F      | Sound Blaster                          |
| 279            | ISA PnP Address                        |
| 330 - 333      | MIDI                                   |
| 376            | IDE Secondary Control Block            |
| 388 - 38B      | FM Synthesizer                         |
| 3B0 - 3DF      | Video Controller                       |
| 3E0 - 3E1      | PCMCIA Controller                      |
| 3F0 - 3F5, 3F7 | Floppy Disk Controller                 |
| 3F6            | IDE Primary Control Block              |
| A79            | ISA PnP Address                        |
| CF8 - CFF      | PCI BUS configuration Register         |

## ISADMA Map

| DMA Channel | Device      |
|-------------|-------------|
| DMA 0       | Unused      |
| DMA 1       | Unused      |
| DMA 2       | Floppy Disk |
| DMA 3       | Audio       |
| DMA 4       | Unused      |
| DMA 5       | Unused      |
| DMA 6       | Unused      |
| DMA 7       | Unused      |

## Memory Map

| Address Range  | Length | Description     |
|----------------|--------|-----------------|
| 00000 - 9FFFFh | 640 KB | System Memory   |
| A0000 - BFFFFh | 128 KB | Video Memory    |
| C0000 - C9FFFh | 40 KB  | Video ROM       |
| CA000 - DBFFFh | 72 KB  | Unused          |
| DC000 - DFFFFh | 16 KB  | DMI information |
| E0000 - FFFFFh | 128 KB | System ROM BIOS |

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## IRQ Map

| IRQ#  | Description                                 |
|-------|---|
| IRQ 0 | System Timer                                |
| IRQ 1 | Keyboard                                    |
| IRQ 2 |   |
| IRQ 3 |   |
| IRQ 4 |   |
| IRQ 5 | Audio/VGA/USB                               |
| IRQ 6 | Floppy Disk Drive                           |
| IRQ 7 |   |
| IRQ 8 | RTC Alarm                                   |
| IRQ 9 | ACPI  |
| IRQ10 | LAN / Modem or Combo, (Card Bus), IEEE 1394 |
| IRQ11 | Reserved for PCMCIA card                    |
| IRQ12 | Glide Pad                                   |
| IRQ13 | FPU (FERR)                                  |
| IRQ14 | Hard Disk Drive                             |
| IRQ15 | CD-ROM or DVD-ROM                           |

## 3.3.13 GPIO Pin Assignment

The GPI and GPO pins connected to system devices. The BIOS can get device's status and control the device via the GPI and GPO pins.

### ICH4 GPI pin assignment

| GPIO Number | Signal Name | Default | I/O | Notes   |
|-------------|-------------|---------|-----|---|
| GPIO0       | PanelID0    |         | I   | Panel ID setting                                  |
| GPIO1       | PanelID1    |         | I   | Panel ID setting                                  |
| GPIO2       | PanelID2    |         | I   | Panel ID setting                                  |
| GPIO3       | PanelID3    |         | I   | Panel ID setting                                  |
| GPIO8       | Q_SMI0      |         | I   | 0:External K/B SMI0<br>1:Normal operation         |
| GPIO11      | LPC_QPME0   | 1       | O   | 0:LPC_QPME0 Event Enable<br>1:Normal operation -- |
| GPIO12      | EC_SCI0     |         | I   | 0:PMU SCI Detect<br>1:PMU SCI not Detect          |
| GPIO13      | PM_RI0      |         | I   | 0:PMU GPIO detect<br>1:PMU GPIO not Detect        |
| GPIO25      | CB_HWSUSP0  | 1       | O   | R5C551 Hardware suspend control pin               |
| GPIO32      | SPDMUX0     | 1       | O   | SMBus select 1                                    |
| GPIO33      | SPDMUX1     | 1       | O   | SMBus select 0                                    |

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## 3.3.14 PMU08 GPIO pin assignment

| GPIO number | Signal Name | Default | I/O | Notes   | Remark |
|-------------|-------------|---------|-----|---|--------|
| GPIO B6     | PM_SLP_S10  | 1       | I   | Suspend Plane A control for ICH4<br>0: POS, STR and STD suspend state.<br>1: not suspend state. |        |
| GPIO B5     | N.C.        | --      | --  | No used   |        |
| GPIO B4     | N.C.        | --      | --  | No used   |        |
| GPIO B1     | N.C.        | 1       | O   | No used   |        |
| GPIO B0     | N.C.        | --      | --  | No use  |        |
| GPIO A7     | N.C.        | --      | --  | No use  |        |
| GPIO A6     | PCMRIO      | 1       | I   | PC Card Ring event<br>0: Ring<br>1: No Ring   |        |
| GPIO A0     | LID0        | 1       | I   | LCD Open/Close Status<br>0: LCD Close<br>1: LCD Open  |        |
| GPIO C1     | NC          | --      | --  | No Use  |        |
| GPIO B7     | PM_RIO      | 1       | O   | Wake Up event request<br>0: Wake SMI(SCI)<br>1: There is no demand.                             |        |
| GPIO B2     | N.C.        | --      | -   | No Use  |        |
| GPIO B0     | N.C.        | --      | --  | No Use  |        |
| GPIO A5     | PRSTMSK0    | 1       | O   | PCI Reset Mask<br>0: Reset Mask<br>1: Reset Enable  |        |
| GPIO A4     | PCMUTE0     | 1       | O   | Mute PC Speaker   |        |
| GPIO A1     | N.C.        | --      | --  | No use  |        |
| GPIO C2     | CHGLED      |         |     | Charge Battery indicator :<br>1 : charging Battery<br>0 : Stop charging Battery                 |        |
| GPIO C3     | N.C.        | --      | --  | No Use  |        |
| GPIO C0     | N.C.        | --      | --  | No Use  |        |

## 3.4 ACPI

### General Requirements

The BIOS must meet the following general Power Management requirements:  
Refers to the portion of the firmware that is compatible with the ACPI 1.0b specifications.  
Support for Power ON(S0 state), Suspend-to-RAM (S3 state) , Suspend-to-Disk mode (S4 state) and Soft OFF(S5 state).

# Software Functional Overview

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## Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user.

Following is a list of the system states:

**G0/S0 - Working:**

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

**G1 - Sleeping:**

A computer state where the computer consumes a small amount of power, user mode threads are not being executed, and the system “appears” to be off (from an end user’s perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state.

**G2/S5 - Soft Off:**

A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is run. This state requires a large latency in order to return to the Working state. The system’s context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

**G3 – Mechanical Off:**

A computer state that is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

## Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state, refer to ACPI specification section 7.5.2. For a detailed definition of the transitions between each of the Sx states, refer to ACPI specification section 9.1.

**S1 Sleeping State:**

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

**S3 Sleeping State:**

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor’s reset vector after the wake-up event.

**S4 Sleeping State:**

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

**S5 Soft Off State:**

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the “SOFT” off state and requires a

# Software Functional Overview

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complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

## System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

### 3.4.1 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

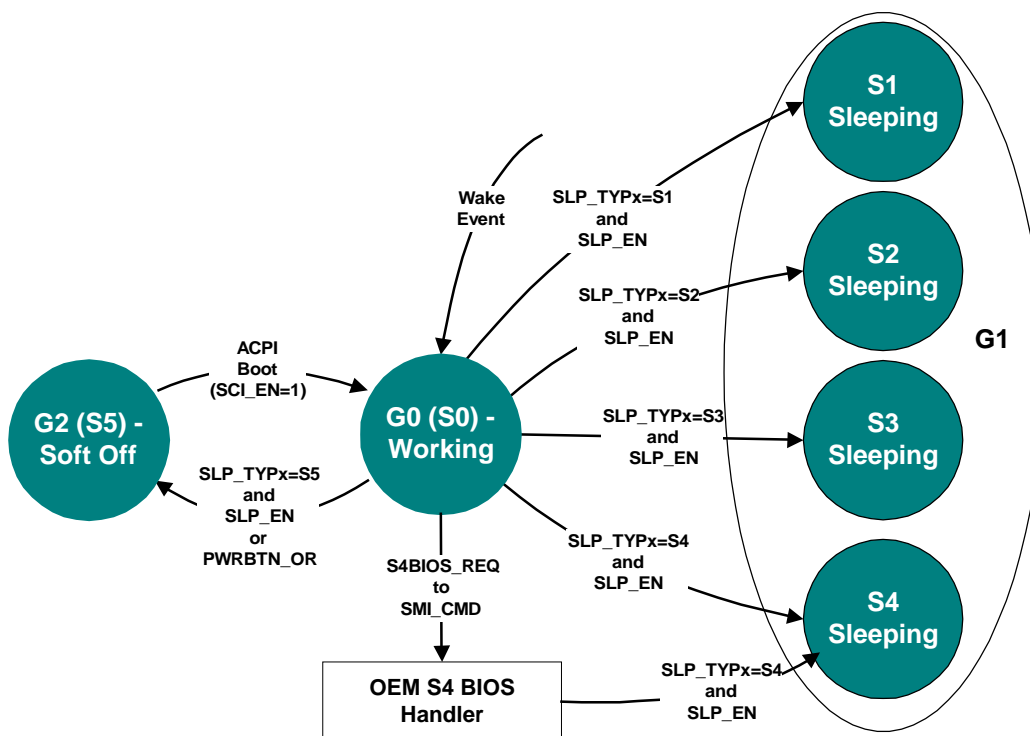
The power plane is divided as following:

| Power Group | Power Control Pin | Controlled Devices  |
|-------------|-------------------|---|
| +B          | Nil               | IMM, (9V~20V)   |
| +3VA        | Nil               | RTC I/F, PMU08  |
| +12V        | PWRON             | PCMCIA Card, AC97 Codec   |
| +5V         | PWRON             | PCMCIA Slot 5V  |
| +3V         | PWRON             | VGA, PCMCIA, PCMCIA Slot 3V, DRAM, Twister(DRAM I/F), M3885x, MAX3243 |
| +5VS        | SUSB#             | FLASH ROM, HDD, CD-ROM, USB, Internal K/B, Glide Pad, Audio AMP, Fan  |
| +3VS        | SUSB#             | ISA I/F Power, Clock Generator & Buffer (W137)                        |
| +RTCVCCS    | Nil               | RTC   |

### 3.4.2 Power Management Mode Transition Flow Chart

From a user-visible level, the system can be thought of as being one of the states in the following diagram:

# Software Functional Overview



## 3.4.3 Power States transition event

The following table summarizes the entry events and wake-up events of each power:

The following table summarize the entry events and wake-up events of each power state

| Power State | Entry Event   | Wake up Event  |
|-------------|---|--|
| S3          | OSPM control<br>Lid Close<br>Power Button<br>Sleep Button<br>Battery Low  | Power Button<br>Ring Wake up<br>RTC Alarm<br>LAN Wake Up<br>Lid open |
| S4          | OSPM control,<br>Power button<br>Sleep button<br>Lid Close<br>Battery Low | Power Button<br>RTC Alarm  |
| S5          | Power Button<br>Battery Low<br>OSPM control                               | Power Button   |

x OSPM: OS-directed Power Management

Device Power Control Methodology

Power state of local devices table

This section illustrates the power control status of each key device/component of the

# Software Functional Overview

system under each power management mode.

| PowerState Component | Doze       | Stand By     | STR                                | STD/SOff                          |
|----------------------|------------|--------------|------------------------------------|-----------------------------------|
| CPU                  | Stop Grant | Stop Clock   | Power Off                          | Power Off                         |
| L2 CACHE             | ON         | Power Down   | Power Off                          | Power Off                         |
| MontaraGM            | ON         | Stop Clock   | Power Off (except Vcc)             | Power Off                         |
| ICH4                 | ON         | ON           | Power Off (except SUSVcc, RTCVcc ) | Power Off (except SUSVcc, RTCVcc) |
| DRAM                 | ON         | Self Refresh | Self Refresh                       | Power Off                         |
| Clock Synthesizer    | ON         | Low Power    | Power Off                          | Power Off                         |
| CDROM                | ON         | Power Down   | Power Off                          | Power Off                         |
| HDD                  | ON         | Power Down   | Power Off                          | Power Off                         |
| FDD                  | ON         | Power Down   | Power Off                          | Power Off                         |
| KBC                  | ON         | ON           | Power Down                         | Power Off                         |
| PMU08                | ON         | ON           | Power Down                         | Power Down                        |
| VGA/VRAM             | ON         | Power Down   | Power Down                         | Power Off                         |
| PCMCIA               | ON         | Power Down   | Power Down                         | Power Off                         |
| AUDIO                | ON         | Power Down   | Power Off                          | Power Off                         |
| Audio AMP            | ON         | Power Down   | Power Off                          | Power Off                         |
| LCD Backlight        | ON         | Power Off    | Power Off                          | Power Off                         |
| LAN                  | ON         | Power Down   | Power Down                         | Power Down                        |
| Internal Modem       | ON         | Power Down   | Power Down                         | Power Down                        |

## Device Power control Methodology During S3 Mode

This section illustrates the control methodology of each device/component and its details under Stand by mode.

| Device            | Power Down Controlled by | Description                               |
|-------------------|--------------------------|---|
| CPU               | Hardware                 | Controlled by SUSB# pin                   |
| L2 CACHE          | Hardware                 | Power off                                 |
| ICH4              | Hardware                 | Controlled by SUSB# pin                   |
| DRAM              | Software                 | Self Refresh                              |
| Clock Synthesizer | Hardware                 | Controlled by SUSB# pin                   |
| CDROM             | Hardware                 | Power off                                 |
| HDD               | Hardware                 | Power off                                 |
| FDD               | Hardware                 | Power off                                 |
| KBC               | Software                 | Controlled by M3885xM8 power down command |
| PMU08             | Software                 | Controlled by PMU08 power down command    |
| VGA/VRAM          | Software                 | Controlled by MontaraGM                   |
| PCMCIA            | Software                 | Controlled by SUSB# pin                   |
| AUDIO             | Hardware                 | Controlled by ICH4                        |
| Audio AMP         | Hardware                 | Controlled by BIOS                        |
| LCD Backlight     | Hardware                 | Power off                                 |
| LAN               | Hardware                 | Controlled by Driver enter Dx status      |
| Internal Modem    | Hardware                 | Controlled by Driver enter Dx status      |

Power Button

The function of Lid Switch is depends on the ACPI aware OS.

# Software Functional Overview

Lid Switch (Cover Switch)

The function of Lid Switch is depends on the ACPI aware OS.

## 3.4.4 Expanding Event Through the Embedded Controller

The following figure shows the relationships between the devices that are wired to the embedded controller, the embedded controller queries, and ACPI general

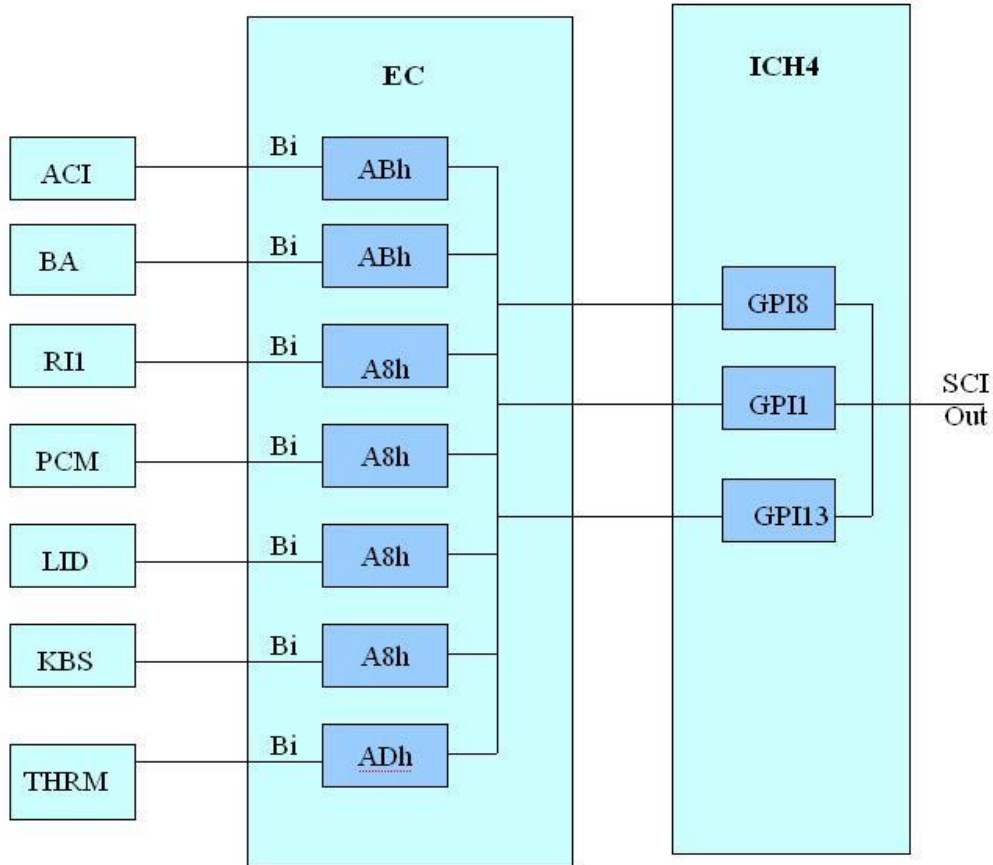


Figure 3-2 The Relationships between ACPI, Controller, and Device

### SCI Source and GPE Event from PMU08

The system will issue a beep to inform user while the following SCI alerted:

| PMU08  | Input Event         | GPE Event | Handler     |
|--------|---------------------|-----------|-------------|
| ADPIN# | AC Plug In/Out      | GPI12     | AML Handler |
| BAT0#  | Battery Plug In/Out | GPI12     | AML Handler |
| GPIOA0 | LID Event           | GPI13     | AML Handler |
| GPIOA3 | Keyboard SMI        | GPI8      | AML Handler |
| GPIOA6 | PCMCIA Ring In      | GPI13     | AML Handler |
| GPIOA7 | COM Port Ring In    | GPI13     | AML Handler |
| THRM   | Thermal Event       | GPI12     | AML Handler |

# Software Functional Overview

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## Control Method Battery Subsystem

EC should support all the battery information to ACPI-OS

- Designed Battery capacity
- Designed Voltage
- Designed Low battery capacity
- Designed Low – Low battery capacity
- Latest Full charged capacity
- Present Remaining capacity
- Present drain rate
- Present voltage
- Present Battery Status

ACPI BIOS should support an independent device object in the name space, and implement the following methods.

### 3.4.5 Thermal Control

There are primary cooling policies that the OS use to control the thermal state of the hardware

| Cooling Policy      | Action             | Temperature Setting |
|---------------------|--------------------|---------------------|
| Action cooling      | Fan On             | Always On           |
| Action cooling      | Fan High On        | Over 70 °C          |
|                     | Fan High Off       | Below 65°C          |
| Passive cooling     | Throttling CPU On  | Over 90 °C          |
|                     | Throttling CPU Off | Below 85°C          |
| Critical trip point | System Shutdown    | Over 110 °C         |

## 3.5 Battery Management

### 3.5.1 Battery Sub-system

§ The charger will stop charge the battery when the following condition is detected.

- The temperature of the system is too high
- The remaining capacity is 95% and more.

Note that the battery life is depending on different configuration running. E.g. with CD-ROM battery life is shorter, document keyin only battery life is longer, PMU disable battery life is short, PMU enable battery life is longer.

- Battery reading methodology is through PMU08 SMBus.

### 3.5.2 Battery Low

When the battery voltage is approaching to the Low level, the PMU08 will generate a battery low SMI. The system will do the following action.

- 1) The Power Indicator will become blinking.

# Software Functional Overview

- 2) The system will issue a Warning beep.

## 3.5.3 Battery Low - Low

When the battery voltage is approaching to the Low-Low level, the PMU08 will generate a battery low-low SMI. The system will do the following action.

- 1) The Power Indicator will keep on Blinking.
- 2) The system will enter Suspend To Disk mode even the power management is disabled. The function of power-on or Resume will be inhibited until the battery Low – Low condition is removed.

## 3.5.4 AC Adapter

When plug in the AC adapter, the system will do the following action:

- The charger will charge the Main Battery, if remaining capacity is not full.
- The Battery Charging Indicator will turn on if the battery is in changing mode.

## 3.6 PMU08

The Embedded controller PMU08 acts as a supplement for power management control. It supports a lot of functions via SMBus interface.

### 3.6.1 The System EC RAM with PMU08

Embedded Controller Command Set

The EC I/F command set allows the OS to communicate with the PMU08.

For detail information refer to ACPI 1.0B specification.

| EC I/F Command                    | Command Byte Encoding | Byte | Register | R/W | Description           | Interrupt          |
|-----------------------------------|-----------------------|------|----------|-----|-----------------------|--------------------|
| Read Embedded Controller (RD_EC)  | 0x80                  | #1   | EC_SC    | W   | Command byte Header   | Interrupt on IBF=0 |
|                                   |                       | #2   | EC_DATA  | W   | Address byte to read  | No Interrupt       |
|                                   |                       | #3   | EC_DATA  | R   | Read data to host     | Interrupt on OBF=1 |
| Write Embedded Controller (WR_EC) | 0x81                  | #1   | EC_SC    | W   | Command byte Header   | Interrupt on IBF=0 |
|                                   |                       | #2   | EC_DATA  | W   | Address byte to write | Interrupt on IBF=0 |

## Software Functional Overview

|   |      |    |         |   |                        |                    |
|---|------|----|---------|---|------------------------|--------------------|
|   |      | #3 | EC_DATA | W | Data to write          | Interrupt on IBF=0 |
| Burst Enable Embedded Controller (BE_EC)  | 0x82 | #1 | EC_SC   | W | Command byte Header    | No Interrupt       |
|   |      | #2 | EC_DATA | R | Burst acknowledge byte | Interrupt on OBF=1 |
| Burst Disable Embedded Controller (BD_EC) | 0x83 | #1 | EC_SC   | W | Command byte Header    | Interrupt on IBF=0 |
| Query Embedded Controller (QR_EC)         | 0x84 | #1 | EC_SC   | W | Command byte Header    | No Interrupt       |
|   |      | #2 | EC_DATA | R | Query value to host    | Interrupt on OBF=1 |

### 3.6.2 PMU08 EC RAM List

The micro controller PMU08 acts as a supplement for power management control. It supports the following functions via SMBus Command ( **0x80** , **0xC0** )

| Function                         | Address | Register Name             | R/W  | Bit Number    |   |   |   |   |   |   |   | Logic | Default | Description   |
|----------------------------------|---------|---------------------------|------|---------------|---|---|---|---|---|---|---|-------|---------|---|
|                                  |         |                           |      | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |         |   |
| 1 <sup>st</sup> Battery [ _BIF ] | 00h *3  | Power unit                | R(W) | DATA[15:0] *1 |   |   |   |   |   |   |   | -     | 0xffff  | 0x0000: mWh [Fixed value]<br>0xffff: Unknown                            |
|                                  | 02h *3  | Design capacity           | R(W) | DATA[15:0] *1 |   |   |   |   |   |   |   | -     | 0xffff  | 0x0000-0xffff(mWh)<br>0xffff: Unknown                                   |
|                                  | 04h *3  | Last Full Charge Capacity | R(W) | DATA[15:0] *1 |   |   |   |   |   |   |   | -     | 0xffff  | 0x0000-0xffff(mWh)<br>0xffff: Unknown                                   |
|                                  | 06h *3  | Battery Technology        | R(W) | DATA[15:0] *1 |   |   |   |   |   |   |   | -     | 0xffff  | 0x0000 : Primary<br>0x0001: Secondary [Fixed value]<br>0xffff: Unknown. |
|                                  | 08h *3  | Design Voltage            | R(W) | DATA[15:0] *1 |   |   |   |   |   |   |   | -     | 0xffff  | 0x0000-0xffff(mV)<br>0xffff: Unknown                                    |

## Software Functional Overview

| Function | Address   | Register Name                  | R/W  | Bit Number                      |   |   |   |                 |   |   |   | Logic | Default | Description  |
|----------|-----------|--------------------------------|------|---------------------------------|---|---|---|-----------------|---|---|---|-------|---------|--|
|          |           |                                |      | 7                               | 6 | 5 | 4 | 3               | 2 | 1 | 0 |       |         |  |
|          | 0Ah<br>*3 | Design capacity of Warning     | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000-0xfffe(mWh)<br>0xffff: Unknown  |
|          | 0Ch<br>*3 | Design capacity of Low         | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000-0xfffe(mWh)<br>0xffff: Unknown  |
|          | 0Eh<br>*3 | Battery capacity Granularity 1 | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000-0xfffe(mWh)<br>0xffff: Unknown  |
|          | 10h<br>*3 | Battery capacity Granularity 2 | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000-0xfffe(mWh)<br>0xffff: Unknown  |
|          | 12h<br>*3 | Model number                   | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000 [Not support]   |
|          | 14h<br>*3 | Serial Number                  | R(W) | DATA[15:0] *1                   |   |   |   |                 |   |   |   | -     | 0xffff  | 0x0000 [Not support]   |
|          | 16h<br>*3 | <b>Battery type</b>            | R(W) | DATA[15:8] *1<br>All bits are 0 |   |   |   | CELL_TYPE [7:0] |   |   |   | -     | 0xffff  | CELL_TYPE [3:0] This code depends on battery data format. In the future, this code may be added.<br>0x00: NiMH<br>0x01: Li-ion<br><b>0x10: Non-rechargeable battery (Reserved)</b> |

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| Function                         | Address    | Register Name              | R/W   | Bit Number                          |   |   |   |              |     |      |   | Logic | Default   | Description   |
|----------------------------------|------------|----------------------------|-------|-------------------------------------|---|---|---|--------------|-----|------|---|-------|---|---|
|                                  |            |                            |       | 7                                   | 6 | 5 | 4 | 3            | 2   | 1    | 0 |       |   |   |
|                                  | 18h<br>*3  | OEM Information            | R(W)  | DATA [15:8]<br>*1<br>All bits are 0 |   |   |   | Vender [7:0] |     |      |   | -     | 0xffff  | Vender [7:0] This code depends on battery data format.<br><br>And the following name should be described in the ASL with the same character code.<br><br>In the future, these codes will be added.<br>0: "MoliEnergy"<br>1: "Panasonic"<br>2: "" (SANYO does not agree the vender name display)<br>3: "TBCL" (Toshiba)<br>4: "Sony" |
| Function                         | Address    | Register Name              | R/W   | Bit Number                          |   |   |   |              |     |      |   | Logic | Default   | Description   |
|                                  |            |                            |       | 7                                   | 6 | 5 | 4 | 3            | 2   | 1    | 0 |       |   |   |
| 1 <sup>st</sup> Battery [ _BST ] | 1Ah<br>*3  | Battery State              | R (W) | DATA[15:3]<br>*1<br>All bits are 0  |   |   |   | CRIT         | CHG | DCHG | - | -     | DCHG=1: The battery is discharged<br>CHG =1: The battery is charged<br>CRIT =1: The battery is critical (Empty) |   |
|                                  | 1Ch<br>*3  | Battery Present rate       | R (W) | DATA[15:0] *1                       |   |   |   |              |     |      |   | -     | 0xffff  | 0x0000-0xfffe(mW)<br>0xffff: Unknown  |
|                                  | 1Eh<br>*3  | Battery Remaining Capacity | R (W) | DATA[15:0] *1                       |   |   |   |              |     |      |   | -     | 0xffff  | 0x0000-0xfffe(mWh)<br>0xffff: Unknown   |
|                                  | 20h<br>*3  | Battery present Voltage    | R (W) | DATA[15:0] *1                       |   |   |   |              |     |      |   | -     | 0xffff  | 0x0000-0xfffe(mV)<br>0xffff: Unknown  |
| 1 <sup>st</sup> Battery [ _BTP ] | 22h        | Battery Trip Point         | R/W   | DATA[15:0] *1                       |   |   |   |              |     |      |   | -     | 0x0000  | 0x0000: Clear the trip point<br>0x0001-0xffff(mWh)  |
| 2 <sup>nd</sup> Battery [ _BIF ] | 24h to 3Ch | *2                         | *2    | *2                                  |   |   |   |              |     |      |   | *2    | *2  | *2  |

## Software Functional Overview

| Function                         | Address       | Register Name              | R/W   | Bit Number |   |   |   |   |   |   |   | Logic | Default | Description  |
|----------------------------------|---------------|----------------------------|-------|------------|---|---|---|---|---|---|---|-------|---------|--|
|                                  |               |                            |       | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |         |  |
|                                  | *3            |                            |       |            |   |   |   |   |   |   |   |       |         |  |
| 2 <sup>nd</sup> Battery [ _BST ] | 3Eh to 44h *3 | *2                         | *2    |            |   |   |   |   |   |   |   | *2    | *2      | *2   |
| 2 <sup>nd</sup> Battery [ _BTP ] | 46h           | *2                         | *2    |            |   |   |   |   |   |   |   | *2    | *2      | *2   |
| -                                | 48h           | Battery data Size          | R (W) |            |   |   |   |   |   |   |   | -     | -       | 0x01: DATA size is 3byte.(PMU06A)<br>0x00: DATA size is 2 byte. (PMU06) *8 |
| 1 <sup>st</sup> Battery [ _BIF ] | 49h           | Design capacity            | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 02/03h. *7 *8                                    |
|                                  | 4Ah           | Last Full Charge Capacity  | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 04/05h. *7 *8                                    |
| 1 <sup>st</sup> Battery [ _BST ] | 4Bh           | Battery Remaining Capacity | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 1E/1Fh. *7 *8                                    |
| 1 <sup>st</sup> Battery [ _BTP ] | 4Ch           | Battery Trip Point         | R (W) |            |   |   |   |   |   |   |   | -     | 0x00    | PMU06A use this data with 22/23h. *7 *8                                    |
| 2 <sup>nd</sup> Battery [ _BIF ] | 4Dh           | Design capacity            | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 26/27h. *7 *8                                    |
|                                  | 4Eh           | Last Full Charge Capacity  | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 28/29h. *7 *8                                    |
| 2 <sup>nd</sup> Battery [ _BST ] | 4Fh           | Battery Remaining Capacity | R (W) |            |   |   |   |   |   |   |   | -     | 0xff    | PMU06A use this data with 42/43h. *7 *8                                    |
| 2 <sup>nd</sup> Battery [ _BTP ] | 50h           | Battery Trip Point         | R (W) |            |   |   |   |   |   |   |   |       | 0x00    | PMU06A use this data with 46/47h. *7 *8                                    |

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| Function   | Address       | Register Name        | R/W    | Bit Number     |       |              |   |   |   |     |   | Logic | Default | Description   |
|------------|---------------|----------------------|--------|----------------|-------|--------------|---|---|---|-----|---|-------|---------|---|
|            |               |                      |        | 7              | 6     | 5            | 4 | 3 | 2 | 1   | 0 |       |         |   |
|            | 51h to 6Bh *3 | Reserved             | R/W    | Don't care     |       |              |   |   |   |     |   | -     | -       |   |
| Function   | Address       | Register Name        | R/W    | Bit Number     |       |              |   |   |   |     |   | Logic | Default | Description   |
|            |               |                      |        | 7              | 6     | 5            | 4 | 3 | 2 | 1   | 0 |       |         |   |
| PMU Access | 6Ch           | PMU_LOW_ADR          | R/W    | DATA [7:0]     |       |              |   |   |   |     |   | -     | -       | These registers are available when PMU slave mode or charger mode is selected.<br><br>For detail information, refer to PMU slave communication section in this document   |
|            | 6Dh           | PMU_HIG_ADR          | R/W    | DATA [15:8]    |       |              |   |   |   |     |   | -     | -       |   |
|            | 6Eh           | CHECK_SUM            | R/W    | DATA [7:0]     |       |              |   |   |   |     |   | -     | -       |   |
|            | 6Fh           | PMU_DATA             | R/W    | DATA [7:0]     |       |              |   |   |   |     |   | -     | -       |   |
| SMBus      | 70h *7        | SMB_PTCL             | R/W    | PROTOCOL [7:0] |       |              |   |   |   |     |   | -     | -       | For detail information, refer to ACPI 1.0 specification [13.9 SMBus Host controller Interface via Embedded controller]<br><br>These registers are not available when PMU slave mode or charger mode is selected.<br><br><b>The PMU06 has access protect function for the EEPROM in the battery, to cancel the protection, set the access protect cancel bit.</b><br><b>For detail, refer to SMBus section</b> |
|            | 71h *7        | SMB_STS              | R/W    | DATA           | ERROR | STATUS [4:0] |   |   |   |     |   | -     | -       |   |
|            | 72h           | SMB_ADDR             | R/W    | ADDRESS [6:0]  |       |              |   |   |   | RES |   | -     | -       |   |
|            | 73h           | SMB_CMD              | R/W    | COMMAND        |       |              |   |   |   |     |   | -     | -       |   |
|            | 74h to 93h    | SMB_DATA [0-31]      | R/W    | DATA           |       |              |   |   |   |     |   | -     | -       |   |
|            | 94h           | SMB_BCNT             | R/W    | RES [7:5]      |       | BCNT [4:0]   |   |   |   |     |   | -     | -       |   |
|            | 95h           | SMB_ALARM_ADDR       | R (/W) | ADDRESS [6:0]  |       |              |   |   |   | RES |   | -     | -       |   |
|            | 96h to 97h    | AMB_ALARM_DATA [0-1] | R (/W) | DATA           |       |              |   |   |   |     |   | -     | -       |   |

## Software Functional Overview

| Function   | Address    | Register Name   | R/W    | Bit Number                      |                       |             |              |   |   |   |     | Logic | Default | Description   |
|------------|------------|-----------------|--------|---------------------------------|-----------------------|-------------|--------------|---|---|---|-----|-------|---------|---|
|            |            |                 |        | 7                               | 6                     | 5           | 4            | 3 | 2 | 1 | 0   |       |         |   |
|            | 98h        | SMB_CNRL        | R/W    | RES [7:1]                       |                       |             |              |   |   |   | PRT |       | 0x00    | PRT =1: The SMBus address (A8-AE) protection is cancelled.  |
| Reserved   | 99h to 9Fh | Reserved        | R/W    | Don't care                      |                       |             |              |   |   |   |     | -     | -       |   |
| Function   | Address    | Register Name   | R/W    | Bit Number                      |                       |             |              |   |   |   |     | Logic | Default | Description   |
|            |            |                 |        | 7                               | 6                     | 5           | 4            | 3 | 2 | 1 | 0   |       |         |   |
| PMU Access | 6Ch        | PMU_LOW_ADR     | R/W    | DATA [7:0]                      |                       |             |              |   |   |   |     | -     | -       | These registers are available when PMU slave mode or charger mode is selected.<br><br>For detail information, refer to PMU slave communication section in this document     |
|            | 6Dh        | PMU_HIG_ADR     | R/W    | DATA [15:8]                     |                       |             |              |   |   |   |     | -     | -       |   |
|            | 6Eh        | CHECK_SUM       | R/W    | DATA [7:0]                      |                       |             |              |   |   |   |     | -     | -       |   |
|            | 6Fh        | PMU_DATA        | R/W    | DATA [7:0]                      |                       |             |              |   |   |   |     | -     | -       |   |
| SMBus      | 70h *7     | SMB_PTCL        | R/W    | PROTOCOL [7:0]                  |                       |             |              |   |   |   |     | -     | -       | For detail information, refer to ACPI 1.0 specification<br>[13.9 SMBus Host controller Interface via Embedded controller]   |
|            | 71h *7     | SMB_STS         | R/W    | D<br>O<br>L<br>E<br>R<br>E<br>M | A<br>L<br>L<br>E<br>M | R<br>E<br>S | STATUS [4:0] |   |   |   |     | -     | -       |   |
|            | 72h        | SMB_ADDR        | R/W    | ADDRESS [6:0]                   |                       |             |              |   |   |   | RES | -     | -       | These registers are not available when PMU slave mode or charger mode is selected.  |
|            | 73h        | SMB_CMD         | R/W    | COMMAND                         |                       |             |              |   |   |   |     | -     | -       |   |
|            | 74h to 93h | SMB_DATA [0-31] | R/W    | DATA                            |                       |             |              |   |   |   |     | -     | -       | The PMU06 has access protect function for the EEPROM in the battery, to cancel the protection, set the access protect cancel bit.<br><br>For detail, refer to SMBus section |
|            | 94h        | SMB_BCNT        | R/W    | RES [7:5]                       |                       |             | BCNT [4:0]   |   |   |   |     | -     | -       |   |
|            | 95h        | SMB_ALARM_ADDR  | R (/W) | ADDRESS [6:0]                   |                       |             |              |   |   |   | RES | -     | -       |   |

## Software Functional Overview

| Function | Address    | Register Name        | R/W    | Bit Number |   |   |   |   |   |   |     | Logic | Default | Description  |
|----------|------------|----------------------|--------|------------|---|---|---|---|---|---|-----|-------|---------|--|
|          |            |                      |        | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0   |       |         |  |
|          | 96h to 97h | AMB_ALARM_DATA [0-1] | R (/W) | DATA       |   |   |   |   |   |   |     | -     | -       |  |
|          | 98h        | SMB_CNRL             | R/W    | RES [7:1]  |   |   |   |   |   |   | PRT |       | 0x00    | PRT =1: The SMBus address (A8-AE) protection is cancelled. |
| Reserved | 99h to 9Fh | Reserved             | R/W    | Don't care |   |   |   |   |   |   |     | -     | -       |  |

| Function | Address | Register Name          | R/W  | Bit Number |     |     |     |     |      |     |     | Logic | Default | Description  |
|----------|---------|------------------------|------|------------|-----|-----|-----|-----|------|-----|-----|-------|---------|--|
|          |         |                        |      | 7          | 6   | 5   | 4   | 3   | 2    | 1   | 0   |       |         |  |
| Status   | A0h *3  | ADP_STS                | R(W) | RES [7:1]  |     |     |     |     |      |     | CON | -     | -       | CON = 1: AC adapter is connected   |
|          | A1h *3  | BAT1_STS (1st Battery) | R(W) |            |     |     |     |     |      |     |     | -     | -       | Battery trip point is detected.<br>BTP =1: Battery is empty.   |
|          | A2h *3  | BAT2_STS (2nd Battery) | R(W) | BTP        | EMP | LOW | WAR | ERR | DCHG | CHG | CON | -     | -       | EMP =1: Battery is Low battery state.<br>WAR=1: Battery is Warning state.<br>ERR =1: Battery is Error state.<br>DCHG=1: Battery is discharged.<br>CHG=1: Battery is charged.<br>CON=1: Battery is connected. |
|          | A3h *3  | Reserved               | R/W  | Don't care |     |     |     |     |      |     |     | -     | -       |  |
|          | A4h *3  | BAT1_CAP               | R(W) | BCAP       |     |     |     |     |      |     |     | -     | -       | 0x00-0x64 = 0-100(%)   |
|          |         |                        |      |            |     |     |     |     |      |     |     |       |         |  |

## Software Functional Overview

| Function | Address | Register Name  | R/W  | Bit Number   |             |                  |                  |             |                  |                  |             | Logic   | Default | Description  |  |
|----------|---------|----------------|------|--------------|-------------|------------------|------------------|-------------|------------------|------------------|-------------|---|---------|--|--|
|          |         |                |      | 7            | 6           | 5                | 4                | 3           | 2                | 1                | 0           |   |         |  |  |
|          | A5h*3   | BAT2_CAP       | R(W) | BCAP         |             |                  |                  |             |                  |                  |             | -   | -       | 0x7F = Unknown<br>0x80 = Not installed   |  |
|          | A6h*3   | Reserved       | R/W  | Don't care   |             |                  |                  |             |                  |                  |             | -   | -       |  |  |
|          | A7h     | SMB_Alert_ADDR | R/W  | ADDRESS[6:0] |             |                  |                  |             |                  |                  | RES         | -   | 0x00    | SMBAlert output device address<br><br>The alert response function is available when this register is cleared (0x00) only.<br><br>When the several devices assert the alert signal at the same time, the least address is stored to this register. And when this register is cleared , next alert address is stored to this register. |  |
|          | A8h*5   | GPIO-A_EVT_STS | R/W  | STS_A [7:0]  |             |                  |                  |             |                  |                  |             | Read<br>0:No event<br>1:EVT detection<br><br>Write<br>0:Clear event<br>1:Ignore | 0x00    | To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only.<br><br>For this operation, this register has special writing manner as follows.<br><b>STS_X        B<br/>(STS_X)     AND<br/>(Written data)</b>   |  |
|          | A9h*5   | GPIO-B_EVT_STS | R/W  | 0            | STS_B [6:0] |                  |                  |             |                  |                  |             |   | 0x00    |  |  |
|          | AAh*5   | GPIO-C_EVT_STS | R/W  | 0            | 0           | 0                | 0                | 0           | 0                | STS_C [1:0]      | 0x00        |   |         |  |  |
|          | ABh*5   | RUN_EVT_STS    | R/W  | B<br>T<br>P  | S<br>M<br>B | A<br>L<br>B<br>R | G<br>P<br>I<br>S | R<br>E<br>S | B<br>A<br>S<br>T | B<br>A<br>T<br>P | A<br>D<br>D | Read<br>0:No event<br>1:EVT detection   | 0x00    | BTP2 =1: BTP2 event is detected<br>SMB =1 : SMBus  |  |

# Software Functional Overview

| Function               | Address | Register Name   | R/W | Bit Number     |     |      |          |   |     |     |      | Logic   | Default | Description   |
|------------------------|---------|-----------------|-----|----------------|-----|------|----------|---|-----|-----|------|---|---------|---|
|                        |         |                 |     | 7              | 6   | 5    | 4        | 3 | 2   | 1   | 0    |   |         |   |
|                        | ACH*5   | WAKE_EVT_STS    | R/W | 2              |     |      |          |   |     | 2   | 1    | detection<br>Write<br>0:Clear event<br>1:Ignore | 0x00    | ALRT=1 : event is detected.<br>GPIO SMBAlert is detected.<br>BATn=1 : GPIO event is detected.<br>ADP=1 : Battery event is detected.<br>TH=1 : event is detected.<br>HIGH=1 : Battery event is detected.<br>LOW=1 : event is detected.<br>ERR=1 : Thermal event is detected.<br>High alarm point is detected.<br>Low alarm point is detected.<br>Polling communication failure with retry. |
|                        | ADh*5   | RUN_EVT_STS_2   | R/W | Reserved [7:1] |     |      |          |   |     |     | TH   |   | 0x00    | To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only.  |
|                        | A Eh*5  | WAKE_EVT_STS_2  | R/W | Reserved [7:1] |     |      |          |   |     |     | TH   |   | 0x00    | For this operation, this register has special writing manner as follows.  |
|                        | AFh*5   | THERMAL_EVT_STS | R/W | Reserved [7:3] |     |      |          |   | ERR | LOW | HIGH |   | 0x00    | <b>STS_X</b> AND <b>(STS_X)</b> (Written data)  |
| Event/<br>GPIO Control | B0h     | EC_RUN_ENB      | R/W | BTP2           | SMB | ALRT | RES[4:1] |   |     |     | ADP  | 0: Disable<br>1: Enable                         | 0x00    | BTP2 : SMBus event.   |
|                        | B1h     | EC_WAKE_ENB     | R/W | BTP2           | SMB | ALRT | RES[4:1] |   |     |     | ADP  | 0: Disable<br>1: Enable                         | 0x00    | ALRT : SMBAlert event.<br>ADP: Adapter event.   |

## Software Functional Overview

| Function | Address | Register Name   | R/W | Bit Number       |                  |     |     |              |     |     |     | Logic                             | Default | Description   |
|----------|---------|-----------------|-----|------------------|------------------|-----|-----|--------------|-----|-----|-----|-----------------------------------|---------|---|
|          |         |                 |     | 7                | 6                | 5   | 4   | 3            | 2   | 1   | 0   |                                   |         |   |
|          | B2h     | BATT_RUN_ENB    | R/W |                  |                  |     |     |              |     |     |     | 0: Disable<br>1: Enable           | 0x00    | Battery trip point<br>BTP: Empty.<br>EMP: Low battery<br>LOW: Warning<br>WAR: Error<br>ERR: Capacity<br>CAP: learning<br>C/D: Charge/Disc<br>CON: harge<br>Battery presence |
|          | B3h     | BATT_WAKE_ENB   | R/W | BTP              | EMP              | LOW | WAR | ERR          | CAP | C/D | CON | 0: Disable<br>1: Enable           | 0x00    |   |
|          | B4h     | GPIO-A_IO_CONF  | R/W | CONF_A [7:0]     |                  |     |     |              |     |     |     | 0: Input<br>1: Output             | 0x00    | For detail information, refer to GPIO section in this document.   |
|          | B5h     | GPIO-A_DATA     | R/W | DATA_A [7:0]     |                  |     |     |              |     |     |     |                                   | -       |   |
|          | B6h     | GPIO-A_RUN_ENB  | R/W | RUN_ENB_A [7:0]  |                  |     |     |              |     |     |     | 0: Disable<br>1: Enable           | 0x00    |   |
|          | B7h     | GPIO-A_EVT_POL  | R/W | POL_A [7:0]      |                  |     |     |              |     |     |     | 0: Falling edge<br>1: Rising edge | 0x00    |   |
|          | B8h     | GPIO-A_WAKE_ENB | R/W | WAKE_ENB_A [7:0] |                  |     |     |              |     |     |     | 0: Disable<br>1: Enable           | 0x00    |   |
|          | B9h     | GPIO-B_IO_CONF  | R/W | 1                | CONF_B [6:0]     |     |     |              |     |     |     | 0: Input<br>1: Output             | 0x80    |   |
|          | BAh     | GPIO-B_DATA     | R/W | 0                | DATA_B [6:0]     |     |     |              |     |     |     |                                   | -       |   |
|          | BBh     | GPIO-B_RUN_ENB  | R/W | 0                | RUN_ENB_B [6:0]  |     |     |              |     |     |     | 0: Disable<br>1: Enable           | 0x00    |   |
|          | BCh     | GPIO-B_EVT_POL  | R/W | 0                | POL_B [6:0]      |     |     |              |     |     |     | 0: Falling edge<br>1: Rising edge | 0x00    |   |
|          | BDh     | GPIO-B_WAKE_ENB | R/W | 0                | WAKE_ENB_B [6:0] |     |     |              |     |     |     | 0: Disable<br>1: Enable           | 0x00    |   |
|          | BEh     | GPIO-C_DATA     | R/W | RES [7:4]<br>*4  |                  |     |     | DATA_C [3:0] |     |     |     |                                   | -       |   |

## Software Functional Overview

| Function               | Address | Register Name            | R/W | Bit Number |   |   |   |   |   |          |                         | Logic                             | Default | Description |
|------------------------|---------|--------------------------|-----|------------|---|---|---|---|---|----------|-------------------------|-----------------------------------|---------|-------------|
|                        |         |                          |     | 7          | 6 | 5 | 4 | 3 | 2 | 1        | 0                       |                                   |         |             |
|                        | BFh     | <b>GPIO-C_RUN_ENB</b>    | R/W | 0          | 0 | 0 | 0 | 0 | 0 | <b>0</b> | <b>RUN_ENB_C [1:0]</b>  | 0: Disable<br>1: Enable           | 0x00    |             |
| Event/<br>GPIO Control | C0h     | <b>GPIO-C_EVT_POL</b>    | R/W | 0          | 0 | 0 | 0 | 0 | 0 | <b>0</b> | <b>POL_C [1:0]</b>      | 0: Falling edge<br>1: Rising edge | 0x00    |             |
|                        | C1h     | <b>GPIO-C_WAKE_ENB_C</b> | R/W | 0          | 0 | 0 | 0 | 0 | 0 | <b>0</b> | <b>WAKE_ENB_C [1:0]</b> | 0: Disable<br>1: Enable           | 0x00    |             |

# Software Functional Overview

| Function | Address | Register Name | R/W | Bit Number |      |     |      |     |      |     |      | Logic | Default                 | Description   |
|----------|---------|---------------|-----|------------|------|-----|------|-----|------|-----|------|-------|-------------------------|---|
|          |         |               |     | 7          | 6    | 5   | 4    | 3   | 2    | 1   | 0    |       |                         |   |
|          |         |               |     |            |      |     |      |     |      |     |      |       |                         | <p>=0: Wake# output is "Level".</p> <p>=1: Wake# output is "Pulse".</p> <p>=0: SCI is always output by event detection and SCI_EVT shows the query data is stored. And next SCI is not output until SCI_EVT is cleared.</p> <p>=1: SCI is output when the</p> <p>WAKE</p> <p>SCI</p> <p>command set is not executed and OBF=0.</p> <p>SCI_EVT shows the output</p> <p>SCI is for event notification.</p> <p>=0: Runtime event status is</p> <p>reflected to RUN_EVT_STS</p> <p>WAKE_OUT</p> <p>register.</p> <p>=1: Runtime event status is</p> |
|          | C2h     | EVT_COUNT     | R/W | RES [7:6]  | WAKE | SCI | WAKE | RES | WAKE | SCI | WAKE |       | 0x00                    | <p>Q_RUN</p> <p>WAKE_OUT</p> <p>reflected to</p> <p>Query data.</p>   |
| 3-30     |         |               |     |            |      |     |      |     |      |     |      |       | FIC MD02-Service Manual | <p>3-30</p> <p>reflected to</p>   |

# Software Functional Overview

| Function        | Address    | Register Name | R/W | Bit Number                     |   |   |   |   |   |   |   | Logic                   | Default | Description  |
|-----------------|------------|---------------|-----|--------------------------------|---|---|---|---|---|---|---|-------------------------|---------|--|
|                 |            |               |     | 7                              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                         |         |  |
|                 | C3h        | EC_RUN_ENB_2  | R/W | Reserved [7:1]                 |   |   |   |   |   |   |   | 0: Disable<br>1: Enable | 0x00    | TH: Thermal event  |
|                 | C4h        | EC_WAKE_ENB_2 | R/W |                                |   |   |   |   |   |   |   | 0: Disable<br>1: Enable | 0x00    |  |
|                 | C5h To C7h | Reserved      | R/W | Don't care                     |   |   |   |   |   |   |   | -                       | -       |  |
|                 | C8h *6     | GPI_AD0       | R   | AD0_DATA [7:0]                 |   |   |   |   |   |   |   | -                       | -       | For detail information, refer to GPIO section in this document.  |
|                 | C9h *6     | GPI_AD1       | R   | AD1_DATA [7:0]                 |   |   |   |   |   |   |   | -                       | -       |  |
|                 | CAh *6     | Reserved      | R/W | Don't care                     |   |   |   |   |   |   |   | -                       | -       |  |
|                 | CBh        | D/A_CONVERT   | R/W | DATA [7:0]                     |   |   |   |   |   |   |   | -                       | 0xff    | 0x00-0xfe: D/A converter output data<br>0xff : Battery capacity(%) output  |
| Battery control | D0h        | BAT_CHG_CONT  | R/W | RES[7:5] CHG_RDY# [3:2] CHG2 1 |   |   |   |   |   |   |   | -                       | -       | CHG_RDY# =0 : Charge ready<br>CHGn =1 : The nth battery is charged   |
|                 | D1h        | BAT_DISCH_PRI | R/W | RES[7:3] PAT [2:0]             |   |   |   |   |   |   |   | -                       | 0x00    | Battery discharge priority<br>0 : 2 1<br>1 : 1 2<br>2 : 2 1<br>3 : 2 1<br>4 : 1 2<br>5 : 1 2<br>6 : Same as 0<br>7 : Simultaneously discharge (Read only :<br>This data can be set using PMU register) |

## Software Functional Overview

| Function | Address   | Register Name        | R/W | Bit Number    |   |   |   |   |   |   |                                 | Logic                               | Default    | Description  |
|----------|-----------|----------------------|-----|---------------|---|---|---|---|---|---|---------------------------------|-------------------------------------|------------|--|
|          |           |                      |     | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0                               |                                     |            |  |
|          | D2h       | BAT_DC<br>H_<br>CONT | R/W | RES[7:2]      |   |   |   |   |   |   | D D<br>C C<br>H H<br>G G<br>2 1 | 0: Not<br>discharge<br>1: Discharge | -          | The discharge battery can be selected one of the batteries can be discharged.  |
|          | D3h       | BAT_WA<br>R_<br>ABS  | R/W | DATA[15:0] *1 |   |   |   |   |   |   |                                 | -                                   | 0x00<br>00 | Absolute capacity battery Warning detection point<br>0x0000-0xffff (mWh)   |
|          | D5h       | BAT_LO<br>W_<br>ABS  | R/W | DATA[15:0] *1 |   |   |   |   |   |   |                                 | -                                   | 0x00<br>00 | Absolute capacity battery Low detection point<br>0x0000-0xffff (mWh)   |
|          | D7h       | BAT_WA<br>R_<br>REL  | R/W | DATA [7:0]    |   |   |   |   |   |   |                                 | -                                   | 0x10       | Relative capacity battery Warning detection point<br>00-C8h (0-100% step 0.5%)   |
|          | D8h       | BAT_LO<br>W_<br>REL  | R/W | DATA [7:0]    |   |   |   |   |   |   |                                 | -                                   | 0x06       | Relative capacity battery Low detection point<br>00-C8h (0-100% step 0.5%)   |
|          | D9h<br>*3 | FULL_D<br>ATA        | R/W | DATA [7:0]    |   |   |   |   |   |   |                                 | -                                   | 0xbe       | Full charge cancel point<br>00-C8h (0-100% step 0.5%)  |
|          | Dah       | CC_CUR<br>_<br>DATA  | R   | DATA [7:0]    |   |   |   |   |   |   |                                 | -                                   | 0x00       | Battery charging current setting<br>0x01-0xff (0.02-5.10A step 0.02A)<br>0x00 Depends on the battery<br>This register is "read only", to change the value, use the register in PMU registers area. |

## Software Functional Overview

| Function    | Address    | Register Name | R/W | Bit Number  |   |   |   |   |   |   |   | Logic | Default | Description  |
|-------------|------------|---------------|-----|-------------|---|---|---|---|---|---|---|-------|---------|--|
|             |            |               |     | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |         |  |
|             | DBh To DCh | BTP2          | R/W | DATA [15:0] |   |   |   |   |   |   |   | -     | 0x0000  | 0x0000: Clear the trip point<br>0x0001-0xffff : (mWh)<br>When all of the battery's capacities lesser than this setting value, the BTP2 is detected if event is enabled.                            |
|             | DDh To DFh | Reserved      | R/W | Don't care  |   |   |   |   |   |   |   | -     | -       |  |
| PMU control | E0h        | PMU_CONTROL   | R/W | RES[7:3]    |   |   |   |   |   |   |   | -     | 0x00    | PMU does not initialize EC register when system power is off.<br>EC_REG = 1:<br>PMU indicates the Battery discharge status to the LED_BAY#n, when the battery is installed.<br>The Power LED blink |
|             | E1h        | ACPI_AC_C_ENB | R/W | RES [7:1]   |   |   |   |   |   |   |   | -     | 0x00    | OS_STS = 1: ACPI mode<br>= 0: Legacy mode  |

## Software Functional Overview

| Function               | Address    | Register Name      | R/W  | Bit Number          |   |   |   |   |   |   |   | Logic        | Default | Description  |
|------------------------|------------|--------------------|------|---------------------|---|---|---|---|---|---|---|--------------|---------|--|
|                        |            |                    |      | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |              |         |  |
|                        | E2h        | OFF_TIME           | R/W  | DATA [7:0]          |   |   |   |   |   |   |   | -            | 0x64    | Power switch override function timer<br>01h-FFh (0.1-25.5esc step 0.1sec)<br>00h : Reserved                |
| Thermal Sensor Polling | E3h        | POLLING_ADDRESS    | R/W  | Slave Address [6:0] |   |   |   |   |   |   |   |              | 0x00    | Address: 0x00-0x7F<br>The polling slave address setting<br>If this address is 00, the Polling is disabled. |
|                        | E4h        | HIGH_ALARM         | R/W  | DATA [7:0]          |   |   |   |   |   |   |   | Signed value | 0x00    | If the received data GE this value, the event will be detected.  |
|                        | E5h        | LOW_ALARM          | R/W  | DATA [7:0]          |   |   |   |   |   |   |   | Signed value | 0x00    | If the received data LE this value, the event will be detected.  |
|                        | E6h        | POLLING_INTERVAL   | R/W  | DATA [7:0]          |   |   |   |   |   |   |   |              | 0x00    | 0x00 :Polling disable<br>0x01 – 0xFF [x 250ms] (250ms to 63.75sec)   |
|                        | E7h        | POLLING_DATA       | R(W) | DATA [7:0]          |   |   |   |   |   |   |   | Signed value | 0x00    | This register shows data at latest polling.  |
|                        | E8h        | HARDWARE_SHUT_DOWN | R/W  | DATA [7:0]          |   |   |   |   |   |   |   | Signed value | 0x7D    | If the thermal sensor read value GE this value, the PMU automatically off the power.                       |
|                        | E9h        | POLLING_COMMAND    | R/W  | DATA [7:0]          |   |   |   |   |   |   |   |              | 0x00    | Polling command (data register) address.   |
|                        | EAh        | RETRY_COUNT        | R/W  | DATA [7:0]          |   |   |   |   |   |   |   |              | 0x10    | 0x00 - 0xFF: Retry count value (0-255)   |
|                        | EBh To EFh | Reserved           | R/W  | Don't care          |   |   |   |   |   |   |   |              |         |  |
| PMU control            | F0h        | BURST_FLG_CLR      | R/W  | DATA [7:0]          |   |   |   |   |   |   |   | -            | -       | After writing to the register addressed A8h-AFh, Set the 00h to this register.                             |

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| Function | Address          | Register Name | R/W | Bit Number |   |   |   |   |   |   |   | Logic | Default | Description |
|----------|------------------|---------------|-----|------------|---|---|---|---|---|---|---|-------|---------|-------------|
|          |                  |               |     | 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |         |             |
|          | F1h<br>To<br>FFh | Reserved      | R/W | Don't care |   |   |   |   |   |   |   |       |         |             |

## 3.6.3 Security

The user may enter up to eight standard text characters for a password. The password includes two levels. The higher priority is the Supervisor Password. The lower priority is the User Password. The Supervisor Password can access all the system resource, while the User Password may not access the floppy disk when it is protected by Supervisor Password. Also, the User Password may not access the floppy disk when the Supervisor Password protects it.

When the security function is enabled, the system will request the user to enter password during the following situation:

- Power On → The system will prompt the user to enter the password before booting the OS. If the user key in the wrong password for 3 times, then the system will halt..
- Entering CMOS Setup → The system will prompt the user to enter the password before entering the CMOS Setup. If the user keys in the wrong password for 3 times, then the system will halt.

## 3.7 CMOS Setup Utility

The Setup utility is used to configure the system. The Setup contains the information regarding the hardware for boot purpose. The changed settings will take effect after the system rebooted. Refer to Chapter 1 on running BIOS Setup Program for more detailed information.

## 3.8 Definitions of Terms

**10Base-T (Ethernet)** - A networking standard that supports data transfer rates up to 10Mbps (10 megabits per second).

**100Base-T (Fast Ethernet)** - A relatively new networking standard that supports data transfer rates up to 100Mbps.

**ACPI** - Advanced Configuration and Power Management Interface, a power management specification developed by Intel, Microsoft, and Toshiba.

**CardBus** - The 32-bit version of the PCMCIA PC Card standard. In addition to supporting a wider bus (32 bits instead of 16 bits), CardBus also supports bus mastering and operation speeds up to 33MHz.

**Clock Throttling** – South bridge function that allows the CPU clock to be stopped and started at a known duty cycle using the STPCLK# pin to enter and exit Stop Grant mode. Clock throttling is used for power saving, thermal management, and reducing the processing speed.

**DIMM (SODIMM)** - Dual In-line Memory Module, a small circuit board that holds memory chips. A Single In-line Memory Module (SIMM) has a 32-bit path to the memory chips whereas a DIMM has 64-bit path. Because the Pentium processor requires a 64-bit path to memory, you need to install SIMMs two at a time. With DIMMs, you can install one DIMM at a time. SODIMM is Small Outline Dual In-line Memory Module used in notebook computers.

**DMI** - Desktop Management Interface, an API to enable software to collect information

# Software Functional Overview

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about a computer environment about a computer environment. For example, using DMI a program can determine what hardware and expansion boards are installed on a computer.

**GPI** - General Purpose Input.

**GPO** - General Purpose Output.

**Lid Switch** - A switch that indicates the notebook LCD Panel has been closed and it can be turned off.

**MPEG-2** - Moving Picture Experts Group, a working group of ISO. The term also refers to the family of digital video compression standards developed by the group. There are two major MPEG standards : MPEG-1 and MPEG-2. The most common implementations of the MPEG-1 standard provide a video resolution 352x240 at 30 frames per second(fps). A newer standard, MPEG-2, offers resolution of 720x480 and 1280x720 at 60 fps, with full CD-quality audio.

**North Bridge** - The CPU to PCI interface, also contains the memory and cache controllers.

**South Bridge** - The PCI to ISA interface, also contains many legacy devices.

**SMM** - System Management Mode, Mode of operation while an SMI is active.

**SMI** - System Management Interrupt, non-maskable interrupt that causes the system to enter SMM. SMM functions include power management, USB legacy keyboard control, security, hot keys, and thermal monitoring.

**SMB** - System Management Bus, that is used for managing smart batteries, reading SDRAM configuration information, and other miscellaneous system function.

**TBD** -To Be Discussed. The mentioned specification is not final that should be discussed with related engineers.

**Ultra DMA-33** - A protocol developed by Quantum Corporation and Intel that supports burst mode data transfer rates of 33.3 MBps.

**USB** - A new external bus standard that supports data transfer rates of 12 MBps. A single USB port can be used to connect up to 127 peripheral devices, such as mice, modems, and keyboards. USB also supports Plug-and-Play installation and hot plugging.