



First International Computer, Inc.

Model	MB02		
Version	0.3A	Date	01/28/2003

BIOS Technical Spec.

--

Manager :	Leader :	Initial :
------------------	-----------------	------------------

Revision History:

Date	Revision	Author	Revised Comments
01/28/2003	0.3A	Ray Chen	Draft

Headline Of Contents

1. OVERVIEW	7
2. SUMMARY OF H/W RELATED SPEC.	7
2.1 H/W KEY PART LIST	12
2.2 MARKETING RELATED SPEC.....	12
3. SUMMARY OF BIOS SPEC.....	15
4. SYSTEM	17
4.1 SYSTEM MEMORY	17
4.2 VIDEO	17
4.2.1 Supported Video Mode.....	18
4.2.2 Panel Type Initialization.....	20
4.3 ENHANCED IDE	21
4.4 AUDIO	21
4.5 SUPER I/O	錯誤! 尚未定義書籤。
4.6 PCMCIA	22
4.7 LED INDICATOR	22
4.8 HOT KEYS DEFINITION	22
4.8.1 Hot Keys by Internal Keyboard.....	23
4.9 PORT REPLICATOR	錯誤! 尚未定義書籤。
4.10 PLUG & PLAY.....	23
4.11 PCI DEVICE	24
4.12 SMBUS DEVICES.....	26
4.12.1 ICH4 SMBus Connection Devices	26
4.12.2 PMU 08 SMBus Connection Devices	26
4.13 RESOURCE ALLOCATION	26
4.13.1 I/O Map.....	26
4.13.2 ISA DMA Map	28
4.13.3 Memory Map.....	28
4.13.4 IRQ Map	28

4.14 GPIO PIN ASSIGNMENT.....	29
4.14.1 ICH4 GPI pin assignment.....	29
4.14.2 ICH4 GPO pin assignment	錯誤! 尚未定義書籤。
4.14.3 PMU08 GPIO pin assignment	30
4.14.4 M3885X GPIO pin assignment.....	錯誤! 尚未定義書籤。
5. ACPI.....	31
5.1 GENERAL REQUIREMENTS.....	31
5.2 GLOBAL SYSTEM STATE DEFINITIONS.....	32
5.3 SLEEPING STATE DEFINITIONS	33
5.4 SYSTEM POWER PLANE.....	33
5.5 POWER MANAGEMENT MODE TRANSITION FLOW CHART.....	35
5.6 POWER STATES TRANSITION EVENT.....	35
5.7 DEVICE POWER CONTROL METHODOLOGY	36
5.7.1 Power state of local devices table	36
5.7.2 Device Power control Methodology During S2(Stand by) Mode	錯誤! 尚未定義書籤。
5.7.3 Device Power Control Methodology During S3(Suspend to RAM) Mode....	37
5.8 POWER BUTTON.....	38
5.9 LID SWITCH (COVER SWITCH).....	38
5.10 EXPANDING EVENT THROUGH THE EMBEDDED CONTROLLER.....	39
5.10.1 SCI Source and GPE Event from PMU08.....	40
5.10.2 Control Method Battery Subsystem	40
5.11 THERMAL CONTROL.....	40
6. BATTERY MANAGEMENT.....	42
6.1 SPEEDSTEP.....	錯誤! 尚未定義書籤。
6.1.1 Battery-Powered Mode.....	錯誤! 尚未定義書籤。
6.1.2 AC-Powered Mode	錯誤! 尚未定義書籤。
6.2 BATTERY SUB-SYSTEM.....	42
6.3 BATTERY LOW	42
6.4 BATTERY LOW - LOW	42
6.5 AC ADAPTER	42

7. PMU08	錯誤! 尚未定義書籤。
7.1 THE SYSTEM EC RAM WITH PMU08	44
7.2 PMU08 EC RAM LIST	46
8. MISCELLANEOUS	74
8.1 SECURITY	74
9. CMOS SETUP UTILITY	錯誤! 尚未定義書籤。
9.1 MAIN MENU DEFAULT	錯誤! 尚未定義書籤。
<i>9.1.1 Internal HDD Sub-Menu Default.....</i>	<i>錯誤! 尚未定義書籤。</i>
9.2 ADVANCED MENU DEFAULT	錯誤! 尚未定義書籤。
<i>9.2.1 I/O Device Sub-Menu Default</i>	<i>錯誤! 尚未定義書籤。</i>
9.3 SECURITY MENU DEFAULT	錯誤! 尚未定義書籤。
9.4 BOOT MENU DEFAULT	錯誤! 尚未定義書籤。
9.5 EXIT MENU	錯誤! 尚未定義書籤。
10. DEFINITIONS OF TERMS	86

1. Overview

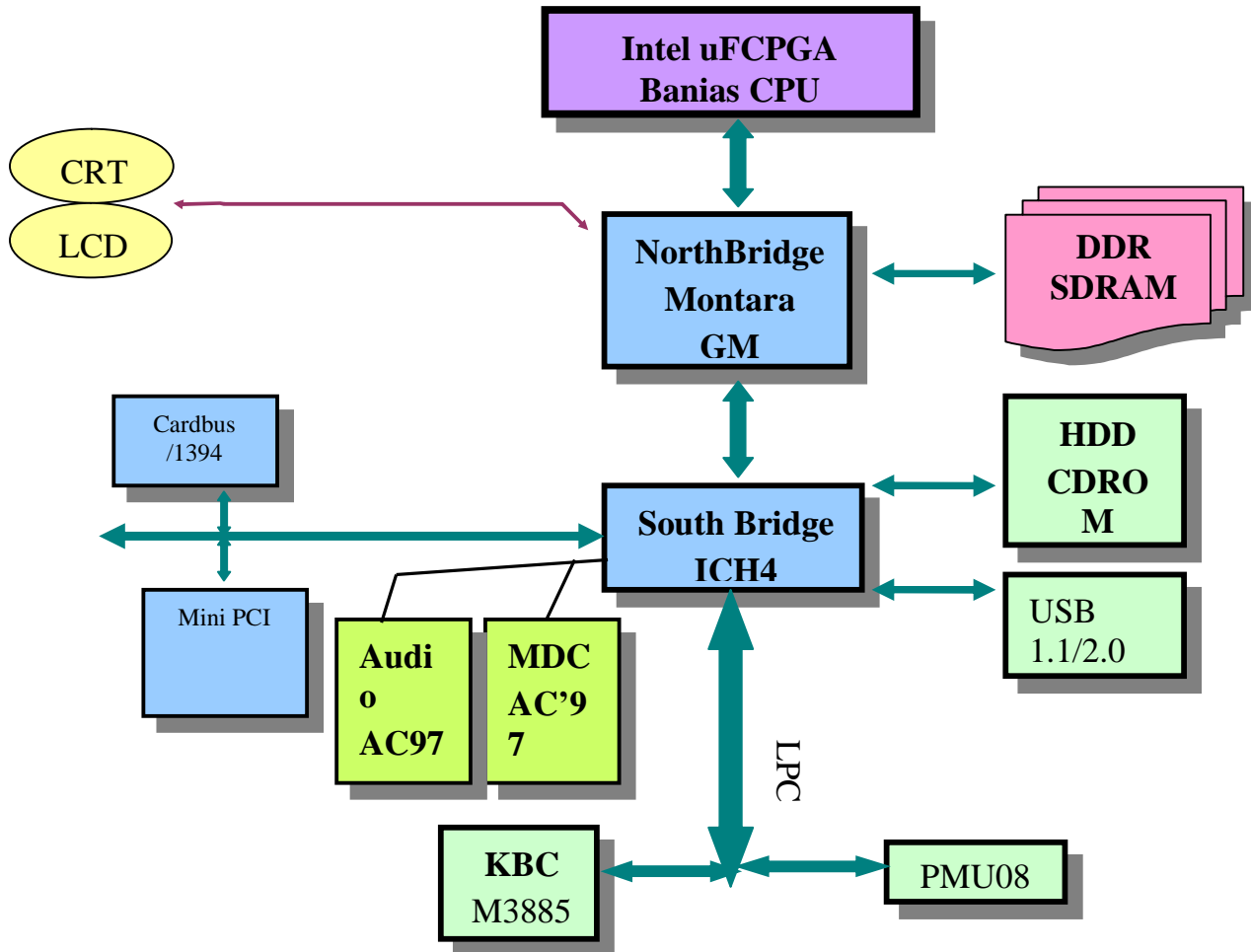
The MB02 is an IBM PC/AT compatible Notebook PC which supports the Intel uFCPGA Socket. The following are the major features that MB02 supports.

- § Microsoft PC99 logo and WinXP logo approval.
- § 14.1" XGA panel support.
- § Support ACPI 1.0B (or above).
- § Support PCI 2.2 (or above).
- § Support USB 1.1/2.0.
- § Support SMBIOS 2.3.(or above)

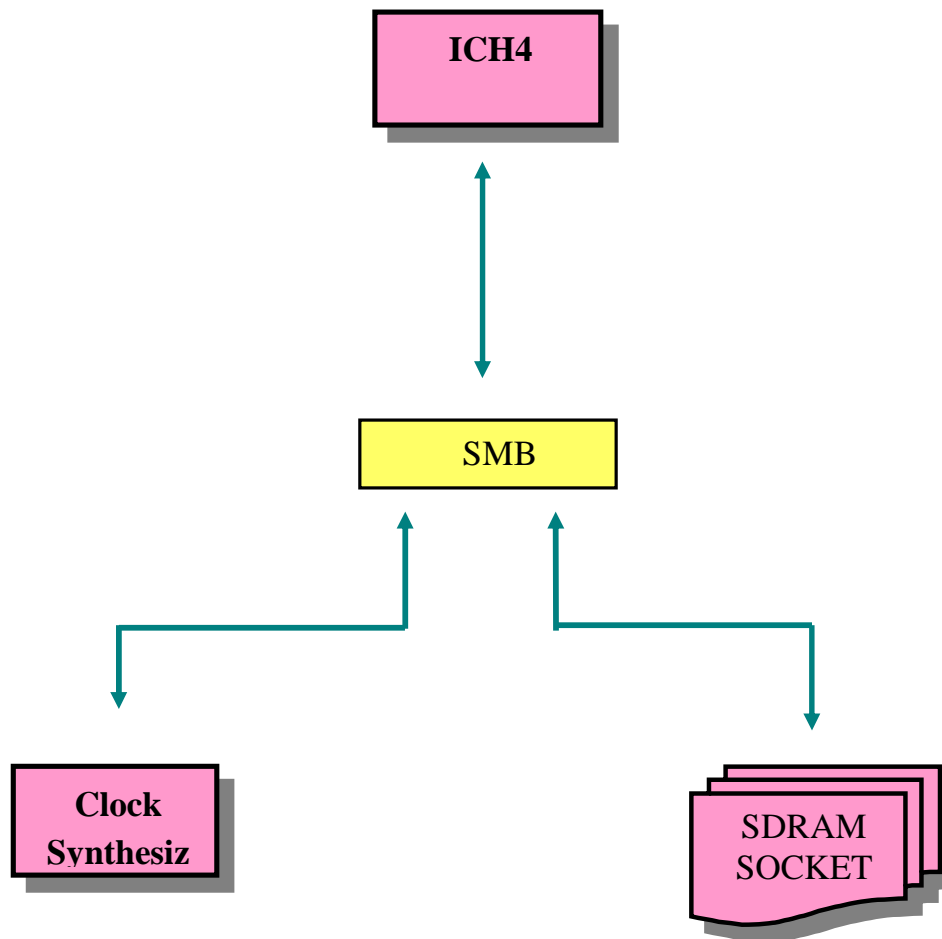
2. Summary of H/W Related Spec.

This section describes about the key component list that using on MB02 machine and it's related marketing specification.

Main components block diagram:

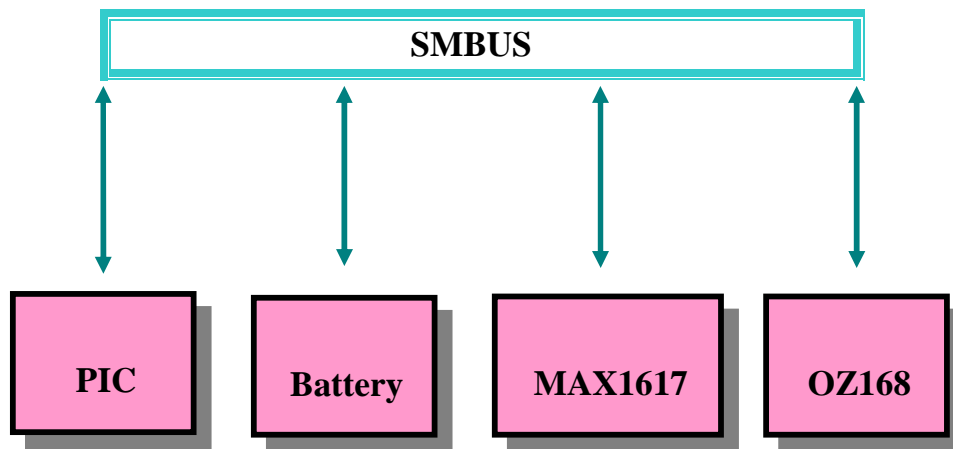


ICH4 SMBUS block diagram:



PMU08 SMBUS block diagram:

PMU08



2.1 H/W Key Part List

Controller Chip	Vender	Description
Processor	Intel	Mobile Banias
North Bridge	Intel	MontaraGM
South Bridge	Intel	ICH4
Video Controller	Intel	Embedded in MontaraGM
PCMCIA Controller	RICOH	R5C551
Audio Controller	Intel	South Bridge Integrated
Audio Codec	Intel	ICH4
Keyboard Controller	Misubishi	M3885x
Power Management	NEC	PMU08
ROM BIOS	SST	49LF004A
Clock Generator	IMI	CY28346
Temperature Sensor	NS	MAX6690
IEEE 1394	RICOH	R5C551
LAN	Intel	ICH4
Modem	Intel	MDC AC'97

2.2 Marketing Related Spec.

Controller Chip	Description
CPU	Intel uFCPGA Banias
Level 2 Cache	1024KB L2 Cache

System Memory	§ Two SO-DIMM sockets that can support up to 512MB (Max) § PC-200/266 DDR SDRAM Specification § Base socket: 128/256/512MB, Expansion socket: 128/256/512MB
Video RAM	UMA (8 ~32MB)
BIOS ROM	512KB flash ROM with boot block
HDD	2.5" 9.5mmH Pack
CD-ROM	24x CD-ROM
CD-R/W	8x CD-R, CD-RW
Combo	8x DVD, 8x CD-R, CD-RW write, 20x CD-ROM(read only)
DVD-ROM	8x DVD
LCD Panel	§ 14.1" XGA LCD
Audio	Software Audio , compliant with AC97
PCMCIA/1394	PCMCIA-Hot plug w/o external buffer/IEEE1394-Data rate 100/200/400 Mbits per second.
Keyboard	Support 2 extra Win 95 hot keys (87/88 KEYS)
Pointing Device	Built-in glide pad with 2 buttons
Modem	AC97 Modem
LED Indicators	§ IDE accessing LED (Blue) § Caps lock LED (Blue) § Scroll lock LED (Blue) § Num lock LED (Blue) § Battery in charging LED (Blue) § Power Status LED (Blue when power on, Blue Blinking when system enter suspend mode, Turn off when Battery Low)

Ports	CRT USB IEEE1394 Cardbus Mic In Modem LAN	D-sub 15pin*1 3pin*2 port (Ver1.1/2.0) One port One port Min Jack *1 RJ11*1 RJ45*1
Switches and Buttons	§ Power switch (Power/Suspend button) § Lid switch (Cover switch)	
Options	§ Expanded RAM module (SO-DIMM type) § Battery pack § AC Adapter	

3. Summary Of BIOS Spec.

Controller Chip	Description
BIOS Feature	<p>§ Microsoft PC99 logo and WinXP logo approval.</p> <p>§ Support Boot Block / Crisis Rescue.</p> <p>§ APM 1.2 Compliance</p> <p>§ Support ACPI 1.0B (or above) Spec.</p> <p>§ Support PCI 2.1 (or above) Spec.</p> <p>§ Support SMBIOS 2.3 (or above) Spec</p> <p>§ Support Windows XP.</p> <p>§ Support flash function including both DOS and Windows interface for new BIOS update.</p> <p>§ Support US keyboard .</p> <p>§ Support boot from LAN , USB FDD/FLASH , HDD and CDROM Drive.</p> <p>§ Support Phoenix First BIOS.</p>
CPU	<p>Auto detecting the CPU type and speed for Intel Baniass based system.</p> <p>Support Intel Geyserville III Technology .</p>
DRAM	Auto sizing and detection. Support PC-200/266 DDR SDRAM.
Cache	<p>§ Level 2 SRAM auto sizing and detection.</p> <p>§ Always enable CPU L1 and L2 cache.</p>
Shadow	Always enable VGA and System BIOS shadow.
Display	<p>§ System auto detects LCD or CRT presence on boot .</p> <p>§ Up to 32 MB of Dynamic Video Memory Allocation.</p>

Hard Disk	<p>§ Enhanced IDE spec.</p> <p>§ Support auto IDE detection.</p> <p>§ Support LBA mode for larger capacity HDD.</p> <p>§ Support Ultra DMA 33/66/100.</p> <p>§ Support Fast PIO mode 1-4 transfer.</p> <p>§ Support 32 bit PIO transfer.</p> <p>§ Support Multi-Sector transfer.</p> <p>§ Support SMART monitoring.</p>
Multi Boot	Allow the user to select boot from USB FDD/FLASH, HDD LAN and CD-ROM.
Plug and Play	Support PnP Run Time Service and conflict-free allocation of resource during POST
Smart Battery	Support BIOS interface to pass battery information to the application via SMBus.
Keyboard Controller	Support Fn hot keys, two Win95 hot keys, built-in Glide Pad.
PCMCIA	Compliant with PCMCIA 2.1 specification.
Power Management Support (ACPI Mode)	<p>The power management is compliant with ACPI 1.0B specification and supports the following power state:</p> <p>§ S0 (Full-On) Mode</p> <p>§ S3 (STR) Mode</p> <p>§ S4 (STD) Mode</p> <p>§ S5 (Soft-Off) Mode</p>

4. System

4.1 System Memory

The system memory consists of DDR SDRAM memory on 64-bit bus and the size options are 64/128/256MB. The BIOS will automatically detect the amount of memory in the system and configure CMOS accordingly during the POST (Power On Self Test) process. This must be done in a way that requires no user interaction.

DRAM Combination Configuration

Base SO-DIMM DRAM slot (Bank 0&1)	Expansion SO-DIMM DRAM slot (Bank 2&3)	Total Size
NIL	128MB	128MB
NIL	256MB	256MB
NIL	512MB	512MB
128MB	NIL	128MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	NIL	256MB
256MB	128MB	384MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	NIL	512MB
512MB	128MB	640MB
512MB	256MB	768MB
512MB	512MB	1024MB

4.2 Video

4.2.1 Supported Video Mode

The following is the display modes supported by the INTEL Mobility Video control in LCD only, CRT only, and simultaneous mode. The VGA BIOS will allow mode sets of resolutions greater than the panel size but only show as much mode display as will fit on the panel.

Supported standard VGA modes:

The VGA BIOS supports the IBM VGA Standard 7-bit VGA modes numbers.

Mode	Pixel Resolution	Colors	Memory
00h/01h	40*25	16	Text
02h/03h	80*25	16	Text
04h/05h	320*200	4	2-bit Planar
06h	640*200	2	1-bit Planar
07h	80*25	Mono	Text
0Dh	320*200	16	4-bit Planar
0Eh	640*200	16	4-bit Planar
0Fh	640*350	Mono	1-bit Planar
10h	640*350	16	4-bit Planar
11h	640*480	2	2-bit Planar
12h	640*480	16	4-bit Planar
13h	320*200	256	8-bit Planar

Note: All Standard VGA Modes are limited to the standard VGA refresh rates.

Supported extended video modes:

CRT device will support all listed VESA mode; and other devices such as PANEL & TV may be limited to the mode support due to their characteristics.

VESA Mode	Pixel Resolution	Memory Model	Refresh Rates In (Hz)	Minimum Memory
100h	640 x 400	8-bit Packed	70	2MB
101h	640 x 480	8-bit Packed	60, 72, 75, 85	2MB
102h	800 x 600	4-bit Planar	60, 72, 75, 85, 100	2MB

103h	800 x 600	8-bit Packed	60, 72, 75, 85, 100	2MB
104h	1024 x 768	4-bit Planar	43(I), 60, 70, 75, 85, 100	2MB
105h	1024 x 768	8-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
106h	1280 x 1024	4-bit Planar	43(I), 60, 75, 85	2MB
107h	1280 x 1024	8-bit Packed	43(I), 60, 75, 85	2MB
10Eh	320 x 200	16-bit Packed	70	2MB
10Fh	320 x 200	32-bit Unpacked	70	2MB
111h	640 x 480	16-bit Packed	60, 72, 75, 85	2MB
112h	640 x 480	32-bit Unpacked	60, 72, 75, 85	2MB
114h	800 x 600	16-bit Packed	60, 72, 75, 85, 100	2MB
115h	800 x 600	32-bit Unpacked	60, 72, 75, 85, 100	2MB
117h	1024 x 768	16-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
118h	1028 x 768	32-bit Unpacked	43(I), 60, 70, 75, 85, 100	4MB
11Ah	1280 x 1024	16-bit Packed	43(I), 60, 75, 85	4MB
11Bh	1280 x 1024	32-bit Unpacked	43(I), 60, 75, 85	8MB
11Dh	640 x 400	16-bit Packed	70	2MB
11Eh	640 x 400	32-bit Packed	70	2MB
120h	1600 x 1200	8-bit Packed	48(I), 60, 75, 85	2MB
122h	1600 x 1200	16-bit Packed	48(I), 60, 75, 85	4MB
124h	1600 x 1200	32-bit Unpacked	48(I), 60, 75, 85	8MB
12Ah	640 x 480	24-bit Packed	60, 72, 75, 85	2MB
12Bh	800 x 600	24-bit Packed	60, 72, 75, 85, 100	2MB
12Ch	1024 x 768	24-bit Packed	43(I), 60, 70, 75, 85, 100	4MB
12Dh	1280 x 1024	24-bit Packed	43(I), 60, 75, 85	4MB
12Eh	320 x 200	8-bit Packed	70	2MB
131h	320 x 200	8-bit Packed	72	2MB

133h	320 x 200	16-bit Packed	72	2MB
134h	320 x 200	32-bit Packed	72	2MB
13Bh*	1400 x 1050	8-bit Packed	60, 75	2MB
13Ch*	1400 x 1050	16-bit Packed	60, 75	4MB
13Eh*	1400 x 1050	32-bitUnpacked	60, 75	8MB
141h	400 x 300	8-bit Packed	72	2MB
143h	400 x 300	16-bit Packed	72	2MB
144h	400 x 300	32-bitUnpacked	72	2MB
151h	512 x 384	8-bit Packed	70	2MB
153h	512 x 384	16-bit Packed	70	2MB
154h	512 x 384	32-bitUnpacked	70	2MB
171h	720 x 480	8-bit Packed	75	2MB
173h	720 x 480	16-bit Packed	75	2MB
174h	720 x 480	24-bit Packed	75	2MB
175h	720 x 480	32-bitUnpacked	75	2MB
176h	720 x 576	8-bit Packed	75	2MB
178h	720 x 576	16-bit Packed	75	2MB
179h	720 x 576	24-bit Packed	75	2MB
17Ah	720 x 576	32-bitUnpacked	75	2MB

Note: “*” The modes may not be available. Their availability should be determined by VESA function calls.

4.2.2 Panel Type Initialization

The VGA BIOS will issue INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPIO pins before the VGA chip initialized, and pass this information to VGA BIOS through INT 15 Function 5F40h.

LCD Panel ID pin Definition:

ICH4 GPI Pins				Panel Type
GPIO 3	GPIO 2	GPIO 1	GPIO 0	
0	0	0	0	
0	0	0	1	ID0
0	0	1	0	ID1
0	0	1	1	
0	1	0	0	ID2
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	ID3
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

4.3 Enhanced IDE

The system BIOS must be ready to support 4 IDE devices on two controllers. The BIOS support Ultra DMA33/66/100 and also supports automatic configuration of drives using both the LBA and CHS large drive remapping method. In addition to supporting standard drives through an auto-configuration process that does NOT require user involvement or confirmation. The system should automatically do this at POST time in a way that is transparent to the user. If a drive is connected to the bus, the drive should be automatically recognized, configured and available for use under MS-DOS 6.2x.

4.4 Audio

The audio subsystem will support the requirements identified by the AC 97 specification. Both software and hardware will control the volume level for the internal audio subsystem. In addition to volume control, the user will be able to

mute the sound to completely cut off the volume using both software and hardware.

4.5 PCMCIA/IEEE 1394

R5C551 is the single chip solution offering PCI bus-PC Card bridge and PCI bus-IEEE 1394 OHCI bridge with integrated PHY. The R5C551 is compliant with the latest specification in both PC card and IEEE 1394.

4.6 LED Indicator

Indicator	Function Description
IDE accessing LED	This LED will turn on while accessing the IDE Device.
Battery Charging LED	Turn on (Blue) – Battery is under charging mode Turn off – Battery full charged or no battery
CapsLock LED	This LED will turn on when the function of CapsLock is active.
ScrollLock LED	This LED will turn on when the function of ScrollLock is active.
NumLock LED	This LED will turn on when the function of NumLock is active.
Power Status LED	Blue – System is powered on. Blue Blinking- System is entered suspend mode. Turn off – Battery Low.
Mail LED	This LED will turn on while Mail was arrived.

Note: These LEDs will be turned off during Suspend mode.

4.7 Hot Keys Definition

All Hot keys must be active at all times under all operation systems.

4.7.1 Hot Keys by Internal Keyboard

Function	Function	Handler
Fn + F3	Toggle Display (LCD/CRT/TV/LCD&CRT)	BIOS Handler
Fn + F2	RF ON/OFF	BIOS Handler
Fn + F6	System Speaker On/Off	BIOS Handler
Fn + F8	Brightness Increase	Controlled by PMU08
Fn + F9	Brightness Decrease	Controlled by PMU08
ScrLock	Scroll Lock	
Internet Button	Internet Function Key	Controlled by Driver
Mail Button	Mail Function Key	Controlled by Driver

Note: The scale parameters of the brightness will be saved in CMOS before Suspend to Disk and SoftOff.

4.8 Plug & Play

The BIOS supports the Plug and Play Specification 1.0A. (Include ESCD)

This section describes the device management. The system board devices and its resources are as follows.

Device	Connect Type	Resources			
		I/O	IRQ	DMA	Memory
DMA Controller	Static	00~0F, 81~8F	-	DMA 5	-
Interrupt Controller	Static	20~21, A0~A1	IRQ2	-	-
System Timer	Static	40~43	IRQ0	-	-
RTC	Static	70~71	IRQ8	-	-
ISA Bus	Static	-	-	-	-

System Speaker	Static	61	-	-	-
System Board	Static	-	-	-	E0000~FFFF
PnP Mother Board	Static	80	-	-	-
Keyboard Controller	Static	60, 64	IRQ1	-	-
PMU08 Controller	Static	68, 6C	-	-	-
Math Coprocessor	Static	F0~FF	IRQ13	-	-
Glide Pad	Static	-	IRQ12	-	-
Video Controller	Static	3B0~3BB, 3C0~3DF	IRQ5	-	A0000~BFFFF, C0000~CFFFF
Dual IDE Controller	Static	170~177, 1F0~1F7, 3F6	IRQ14, 15	-	-
CardBus Controller	Dynamic	3E0~3E1	IRQ10	-	-
Audio chip	Dynamic	220~22F, 300~301, 388~38B	IRQ5	DMA 3	-
IEEE1394	Dynamic		IRQ10		
Modem	Dynamic	3E8~3EF	IRQ10	-	-
LAN	Dynamic	1080~10FF	IRQ10	-	-
USB Host Controller	Dynamic	EF80~EF9F	IRQ5	-	-

4.9 PCI Device

IDSEL Pin Allocation:

IDSEL Pin	PCI	Device
------------------	------------	---------------

	Device Number	Function Number	Device Name
AD23	Device 07	Function 0	RICOH Card Bus
		Function 1	RICOH IEEE1394
AD17	Device 01	Function 0	MINI PCI

INT Pin Allocation:

INT Pin	PCI Device
INTA	CardBus/MiniPCI/LAN
INTB	Cardbus/MiniPCI
INTC	
INTD	

PCI Bus Master Allocation:

Arbiter	Signal	Agents (Master)	Function	Use
	REQ00/GNT00			
	REQ10/GNT10	RICOH	Card Bus Controller	
	REQ20/GNT20			
	REQ30/GNT30			

4.10 SMBus Devices

The SMBus is a two-wire interface through which the system can communicate with power-related chips. The BIOS should initialize the SMBus devices during POST.

4.10.1 Ich4 SMBus Connection Devices

SMBus Device	Host/Slave	Address	BIOS Need to Initialization
SO-DIMM	Slave	A0h/A2h	Memory Auto Sizing (SPD).
CY28346 CLK Generator	Slave	D2h	Program the desired clock frequency (Pin23 output 24MHz, Pin22 output 48MHz)

4.10.2 PMU 08 SMBus Connection Devices

SMBus Device	Host/Slave	Address A7 ~ A1	BIOS Need to Initialization
PMU08	Master	10h	Enable PS01 decode interface
MAX6690 (Thermal sensor)	Slave	9Ch	Program the desired temperature range
Battery (1st Battery)	Slave	A8h	No Need

4.11 Resource Allocation

4.11.1 I/O Map

Hex Address	Device
000 - 01F	8237-1
020 - 021	8259-1
022	
040 - 05F	8254
060 - 064	Keyboard Controller
068 - 06C	PMU08 Controller
070 - 07F	RTC & NMI Mask
080 - 08F	DMA Page Registers
092	System Control Port
0A0 - 0A1	8259-2
0B2	Advanced Power Management Control Port
0B3	Advanced Power Management Status Port
0C0 - 0DF	8237-2
0F0 - 0FF	Math Coprocessor
170 - 177	IDE Secondary Command Block
1F0 - 1F7	IDE Primary Command Block
220 - 22F	Sound Blaster
279	ISA PnP Address
330 - 333	MIDI
376	IDE Secondary Control Block
388 - 38B	FM Synthesizer
3B0 - 3DF	Video Controller
3E0 - 3E1	PCMCIA Controller
3F0 - 3F5, 3F7	Floppy Disk Controller
3F6	IDE Primary Control Block
A79	ISA PnP Address
CF8 - CFF	PCI BUS configuration Register

4.11.2 ISA DMA Map

DMA Channel	Device
DMA 0	Unused
DMA 1	Unused
DMA 2	Floppy Disk
DMA 3	Audio
DMA 4	Unused
DMA 5	Unused
DMA 6	Unused
DMA 7	Unused

4.11.3 Memory Map

Address Range	Length	Description
00000 - 9FFFFh	640 KB	System Memory
A0000 – BFFFFh	128 KB	Video Memory
C0000 – C9FFFh	40 KB	Video ROM
CA000 – DBFFFh	72 KB	Unused
DC000 - DFFFFh	16 KB	DMI information
E0000 – FFFFFh	128 KB	System ROM BIOS

4.11.4 IRQ Map

IRQ#	Description
IRQ 0	System Timer
IRQ 1	Keyboard
IRQ 2	
IRQ 3	
IRQ 4	
IRQ 5	Audio/VGA/USB
IRQ 6	Floppy Disk Drive
IRQ 7	

IRQ 8	RTC Alarm
IRQ 9	ACPI
IRQ10	LAN / Modem or Combo, (Card Bus), IEEE 1394
IRQ11	Reserved for PCMCIA card
IRQ12	Glide Pad
IRQ13	FPU (FERR)
IRQ14	Hard Disk Drive
IRQ15	CD-ROM or DVD-ROM

4.12 GPIO Pin Assignment

The GPI and GPO pins connected to system devices. The BIOS can get device's status and control the device via the GPI and GPO pins.

4.12.1 ICH4 GPIOs pin assignment

GPIO Number	Signal Name	Default	I/O	Notes
GPIO0	PanelID0		I	Panel ID setting
GPIO1	PanelID1		I	Panel ID setting
GPIO2	PanelID2		I	Panel ID setting
GPIO3	PanelID3		I	Panel ID setting
GPIO8	Q_SMI0		I	0:External K/B SMI0 1:Normal operation
GPIO11	LPC_QPME0	1	O	0:LPC_QPME0 Event Enable 1:Normal operation --
GPIO12	EC_SCI0		I	0:PMU SCI Detect 1:PMU SCI not Detect
GPIO13	PM_RI0		I	0:PMU GPIO detect 1:PMU GPIO not Detect

GPIO25	CB_HWSU SP0	1	O	R5C551 Hardware suspend control pin
GPIO32	SPDMUX0	1	O	SMBus select 1
GPIO33	SPDMUX1	1	0	SMBus select 0

4.14.2 PMU08 GPIO pin assignment

GPIO number	Signal Name	Default	I/O	Notes	Remark
GPIO B6	PM_SLP_ S10	1	I	Suspend Plane A control for ICH4 0: POS, STR and STD suspend state. 1: not suspend state.	
GPIO B5	N.C.	--	--	No used	
GPIO B4	N.C.	--	--	No used	
GPIO B1	N.C.	1	O	No used	
GPIO B0	N.C.	--	--	No use	
GPIO A7	N.C	--	--	No use	
GPIO A6	PCMRI0	1	I	PC Card Ring event 0: Ring 1: No Ring	
GPIO A0	LID0	1	I	LCD Open/Close Status 0: LCD Close 1: LCD Open	

GPIO C1	NC	--	--	No Use	
GPIO B7	PM_RI0	1	O	Wake Up event request 0: Wake SMI(SCI) 1: There is no demand.	
GPIO B2	N.C.	--	-	No Use	
GPIO B0	N.C.	--	--	No Use	
GPIO A5	PRSTMS K0	1	O	PCI Reset Mask 0: Reset Mask 1: Reset Enable	
GPIO A4	PCMUTE 0	1	O	Mute PC Speaker	
GPIO A1	N.C.	--	--	No use	
GPIO C2	CHGLED			Charge Battery indicator : 1 : charging Battery 0 : Stop charging Battery	
GPIO C3	N.C.	--	--	No Use	
GPIO C0	N.C.	--	--	No Use	

5. ACPI

5.1 General Requirements

The BIOS must meet the following general Power Management requirements:

Refers to the portion of the firmware that is compatible with the ACPI 1.0b specifications.

Support for Power ON(S0 state), Suspend-to-RAM (S3 state) , Suspend-to-Disk

mode (S4 state) and Soft OFF(S5 state).

5.2 Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user.

Following is a list of the system states:

G0/S0 - Working:

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

G1 - Sleeping:

A computer state where the computer consumes a small amount of power, user mode threads are not being executed, and the system “appears” to be off (from an end user’s perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state.

G2/S5 - Soft Off:

A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is run. This state requires a large latency in order to return to the Working state. The system’s context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

G3 – Mechanical Off:

A computer state that is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be

restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

5.3 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state, refer to ACPI specification section 7.5.2. For a detailed definition of the transitions between each of the Sx states, refer to ACPI specification section 9.1.

S1 Sleeping State:

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

S3 Sleeping State:

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor's reset vector after the wake-up event.

S4 Sleeping State:

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

S5 Soft Off State:

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the "SOFT" off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

5.4 System Power Plane

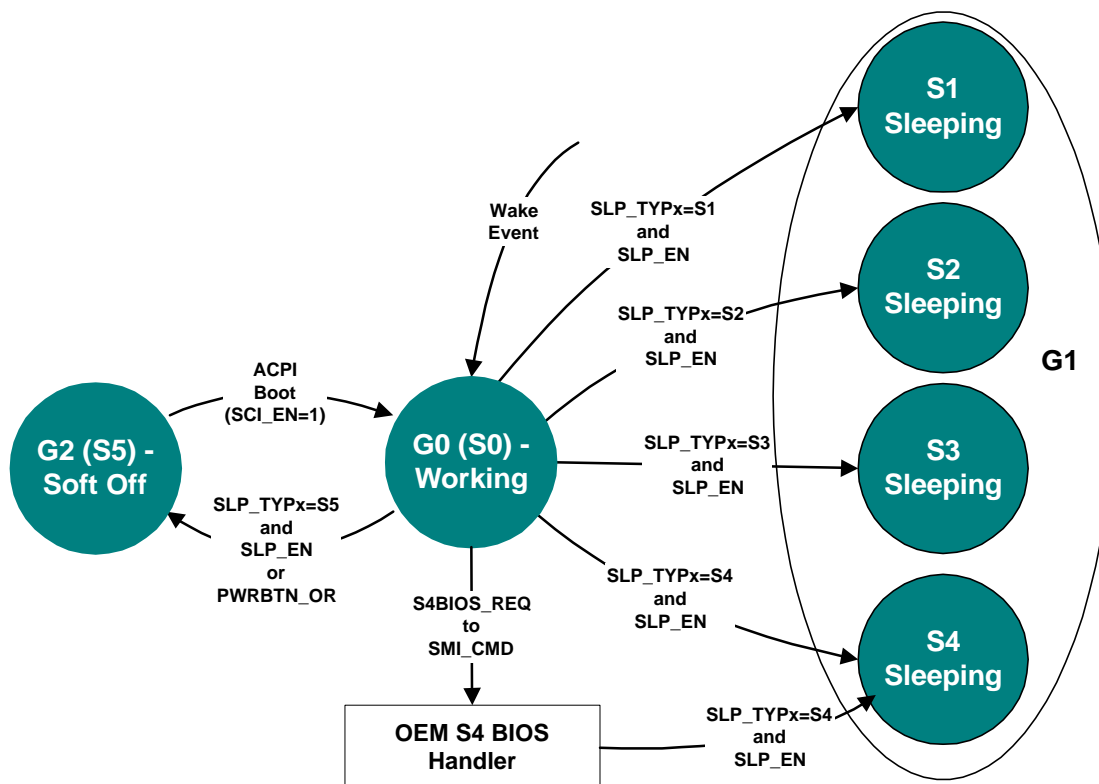
The system components are grouped as the following parties to let the system to control the On/Off

of power under different power management modes.

The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
+B	Nil	IMM, (9V~20V)
+3VA	Nil	RTC I/F, PMU08
+12V	PWRON	PCMCIA Card, AC97 Codec
+5V	PWRON	PCMCIA Slot 5V
+3V	PWRON	VGA, PCMCIA, PCMCIA Slot 3V, DRAM, Twister(DRAM I/F), M3885x, MAX3243
+5VS	SUSB#	FLASH ROM, HDD, CD-ROM, USB, Internal K/B, Glide Pad, Audio AMP, Fan
+3VS	SUSB#	ISA I/F Power, Clock Generator & Buffer (W137)
+RTCVCS	Nil	RTC

5.5 Power Management Mode Transition Flow Chart



5.6 Power States transition event

The following table summarize the entry events and wake-up events of each power state

Power State	Entry Event	Wake up Event
S3	OSPM control Lid Close Power Button Sleep Button Battery Low	Power Button Ring Wake up RTC Alarm LAN Wake Up Lid open

S4	OSPM control, Power button Sleep button Lid Close Battery Low	Power Button RTC Alarm
S5	Power Button Battery Low OSPM control	Power Button

x OSPM: OS-directed Power Management

5.7 Device Power Control Methodology

5.7.1 Power state of local devices table

This section illustrates the power control status of each key device/component of the system under each power management mode.

PowerState Component	Doze	Stand By	STR	STD/SOff
CPU	Stop Grant	Stop Clock	Power Off	Power Off
L2 CACHE	ON	Power Down	Power Off	Power Off
MontaraGM	ON	Stop Clock	Power Off (except Vcc)	Power Off
ICH4	ON	ON	Power Off (except SUSVcc, RTCVcc)	Power Off (except SUSVcc, RTCVcc)
DRAM	ON	Self Refresh	Self Refresh	Power Off
Clock Synthesizer	ON	Low Power	Power Off	Power Off
CDROM	ON	Power Down	Power Off	Power Off

HDD	ON	Power Down	Power Off	Power Off
FDD	ON	Power Down	Power Off	Power Off
KBC	ON	ON	Power Down	Power Off
PMU08	ON	ON	Power Down	Power Down
VGA/VRAM	ON	Power Down	Power Down	Power Off
PCMCIA	ON	Power Down	Power Down	Power Off
AUDIO	ON	Power Down	Power Off	Power Off
Audio AMP	ON	Power Down	Power Off	Power Off
LCD Backlight	ON	Power Off	Power Off	Power Off
LAN	ON	Power Down	Power Down	Power Down
Internal Modem	ON	Power Down	Power Down	Power Down

5.7.2 Device Power Control Methodology During S3(Suspend to RAM) Mode

This section illustrates the control methodology of each device/component and its details under Suspend to RAM mode.

Device	Power Down Controlled by	Description
CPU	Hardware	Controlled by SUSB# pin
L2 CACHE	Hardware	Power off
ICH4	Hardware	Controlled by SUSB# pin
DRAM	Software	Self Refresh
Clock Synthesizer	Hardware	Controlled by SUSB# pin

CDROM	Hardware	Power off
HDD	Hardware	Power off
FDD	Hardware	Power off
KBC	Software	Controlled by M3885xM8 power down command
PMU08	Sofeware	Controlled by PMU08 power down command
VGA/VRAM	Software	Controlled by MontaraGM
PCMCIA	Software	Controlled by SUSB# pin
AUDIO	Hardware	Controlled by ICH4
Audio AMP	Hardware	Controlled by BIOS
LCD Backlight	Hardware	Power off
LAN	Hardware	Controlled by Driver enter Dx status
Internal Modem	Hardware	Controlled by Driver enter Dx ststus

5.8 Power Button

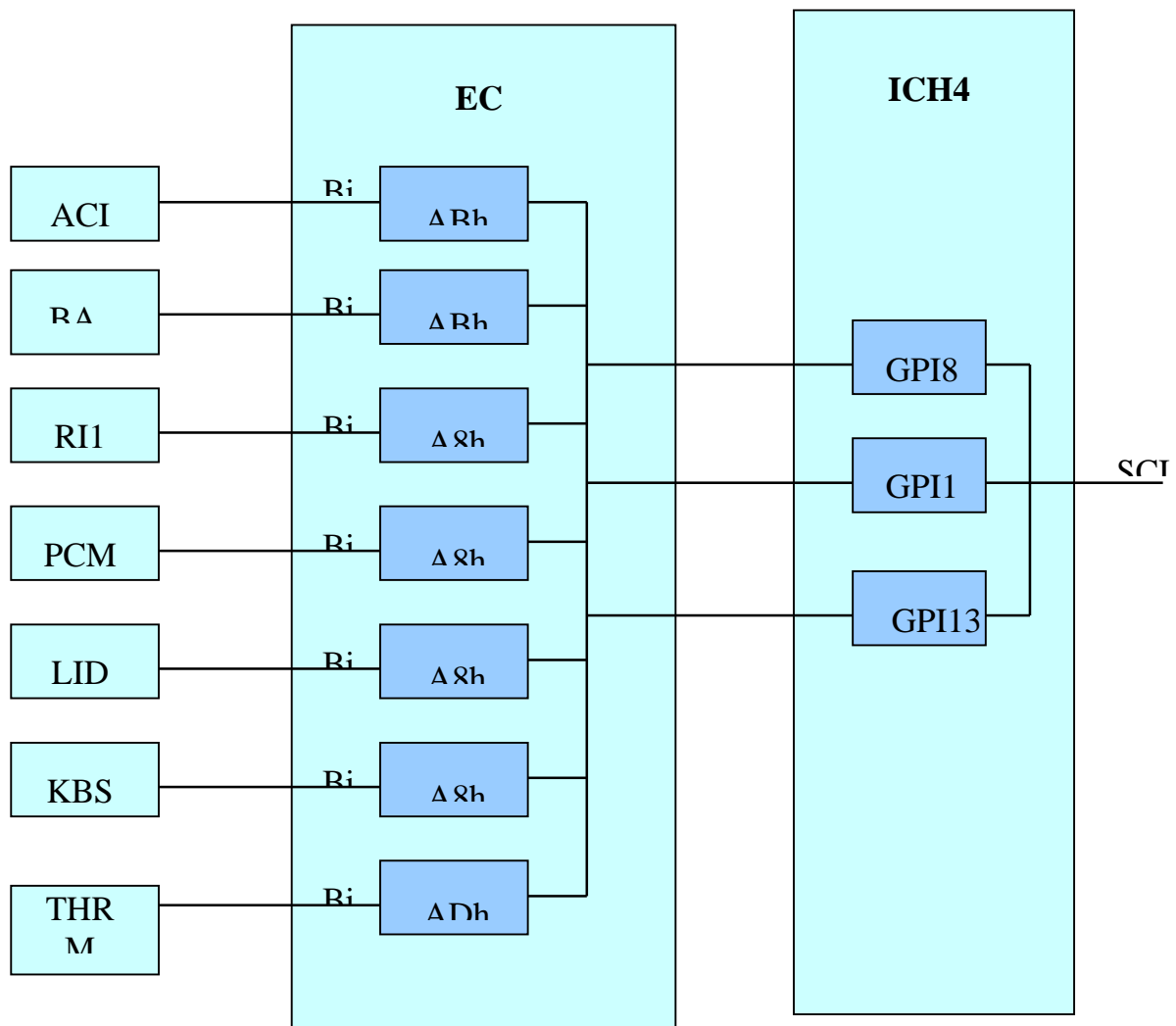
The function of Lid Switch is depends on the ACPI aware OS.

5.9 Lid Switch (Cover Switch)

The function of Lid Switch is depends on the ACPI aware OS.

5.10 Expanding Event Through the Embedded Controller

The following figure shows the relationships between the devices that are wired to the embedded controller, the embedded controller queries, and the ACPI specified General



5.10.1 SCI Source and GPE Event from PMU08

PMU08	Input Event	GPE Event	Handler
ADPIN#	AC Plug In/Out	GPI12	AML Handler
BAT0#	Battery Plug In/Out	GPI12	AML Handler
GPIOA0	LID Event	GPI13	AML Handler
GPIOA3	Keyboard SMI	GPI8	AML Handler
GPIOA6	PCMCIA Ring In	GPI13	AML Handler
GPIOA7	COM Port Ring In	GPI13	AML Handler
THRM	Thermal Event	GPI12	AML Handler

5.10.2 Control Method Battery Subsystem

EC should support all the battery information to ACPI-OS

Designed Battery capacity

Designed Voltage

Designed battery warning capacity

Designed battery low capacity

Latest Full charged capacity

Present Remaining capacity

Present drain rate

Present voltage

Present Battery Status

5.11 Thermal Control

There are three primary cooling policies that the OS use to control the thermal state of the hardware.

Cooling Policy	Action	Temperature Setting
Action cooling	Fan On	Always On
Action cooling	Fan High On	Over 70 °C
	Fan High Off	Below 65°C

Passive cooling	Throttling CPU On	Over 90 °C
	Throttling CPU Off	Below 85°C
Critical trip point	System Shutdown	Over 110 °C

6. Battery Management

6.1 Battery Sub-system

§ The charger will stop charge the battery when the following condition is detected.

- The temperature of the system is too high
- The remaining capacity is 95% and more.

Note that the battery life is depend on different configuration running. E.g. with CD-ROM battery life is shorter, document keyin only battery life is longer, PMU disable battery life is short, PMU enable battery life is longer.

- Battery reading methodology is through PMU08 SMBus.

6.2 Battery Warning

When the battery voltage is approaching to the Low level, the PMU08 will generate a battery low SMI/SCI. The system will do the following action.

DOS Mode:

- 1) The Power Indicator will become blinking.**
- 2) The system will issue a Warning beep.

ACPI Mode:

Depends on user setting .

6.3 Battery Low

When the battery voltage is approaching to the Low level, the PMU08 will generate a battery low SMI/SCI. The system will do the following action.

DOS Mode:

- 1) The Power Indicator will keep on Blinking.**
- 2) The system will be power off.

ACPI Mode:

Depends on User setting .

6.4 AC Adapter

When plug in the AC adapter, the system will do the following action:

- The charger will charge the Main Battery, if remaining capacity is not full.

- The Battery Charging Indicator will turn on if the battery is in changing mode.

7. PMU08

The Embedded controller PMU08 acts as a supplement for power management control. It supports a lot of functions via SMBus interface.

7.1 The System EC RAM With PMU08

Embedded Controller Command Set

The EC I/F command set allows the OS to communicate with the PMU08.

For detail information refer to ACPI 1.0B specification.

EC I/F Command	Comm and Byte Encodi ng	By te	Regis ter	R / W	Description	Interrupt
Read Embedded Controller (RD_EC)	0x80	#1	EC_S C	W	Command byte Header	Interrupt on IBF=0
		#2	EC_ DAT A	W	Address byte to read	No Interrupt
		#3	EC_ DAT A	R	Read data to host	Interrupt on OBF=1
Write Embedded Controller (WR_EC)	0x81	#1	EC_S C	W	Command byte Header	Interrupt on IBF=0
		#2	EC_ DAT A	W	Address byte to write	Interrupt on IBF=0
		#3	EC_ DAT A	W	Data to write	Interrupt on IBF=0
Burst Enable Embedded	0x82	#1	EC_S C	W	Command byte Header	No Interrupt

		#2	EC_ DAT A	R	Burst acknowledge byte	Interrupt on OBF=1
Burst Disable Embedded Controller (BD_EC)	0x83	#1	EC_S C	W	Command byte Header	Interrupt on IBF=0
Query Embedded Controller (QR_EC)	0x84	#1	EC_S C	W	Command byte Header	No Interrupt
		#2	EC_ DAT A	R	Query value to host	Interrupt on OBF=1

7.2 PMU08 EC RAM List

The micro controller PMU08 acts as a supplement for power management control. It supports the following functions via SMBus Command (0x80 , 0xC0)

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
1 st Battery [_BIF]	00h*3	Power unit	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000: mWh [Fixed value] 0xffff: Unknown
	02h*3	Design capacity	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	04h*3	Last Full Charge Capacity	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	06h*3	Battery Technology	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000 : Primary 0x0001: Secondary [Fixed value] 0xffff: Unknown.
	08h*3	Design Voltage	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mV) 0xffff: Unknown
	0Ah*3	Design capacity of Warning	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	0Ch*3	Design capacity of Low	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	0Eh*3	Battery capacity Granularity 1	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	10h*3	Battery capacity Granularity 2	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	12h*3	Model number	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]
	14h*3	Serial Number	R(/ W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]

Func tion	A dd re ss	Registe r Name	R/ W	Bit Number								Logic	De fau lt	Description
				7	6	5	4	3	2	1	0			
	16 h *3	Batter y type	R(/ W)	DAT A[15: 8] *1 All bits are 0				CEL L_TY PE [7:0]				-	0xf fff	CELL_TYPE [3:0] This code depends on battery data format. In the future, this code may be added. 0x00: NiMH 0x01: Li-ion 0x10: Non-rechargeable battery (Reserved)
	18 h *3	OEM Inform ation	R(/ W)	DA TA [15: 8] *1 All bits are 0				Vender[7:0]				-	0xf fff	Vender [7:0] This code depends on battery data format. And the following name should be described in the ASL with the same character code. In the future, these codes will be added. 0: "MoliEnergy" 1: "Panasonic" 2: "" (SANYO does not agree the vender name display) 3: "TBCL" (Toshiba) 4: "Sony"

*1: The register type is word.

*3: This register is not cleared if the system is in S4-S5 state.

R(W): This is the read only register, but the written data will be able to read back

till PMU updates the data periodically, or PMU detects the status change.

Func tion	Ad dres s	Regis ter Nam e	R/ W	Bit Number								Logic	De fau lt	Description
				7	6	5	4	3	2	1	0			
1 st Batte ry [_BS T]	1A h *3	Batte ry State	R(/ W)	DATA[15:3] *1 All bits are 0				C R I T	C H G =1	D C H G =1		-	-	DC HG= 1: CH G =1 : CRI T =1 : The battery is discharged The battery is charged The battery is critical (Empty)
	1C h *3	Batte ry Prese nt rate	R(/ W)	DATA[15:0] *1								-	0xf fff	0x0000-0xfffe(mW) 0xffff: Unknown
	1E h *3	Batte ry Rem ainin g Capa city	R(/ W)	DATA[15:0] *1								-	0xf fff	0x0000-0xfffe(mWh) 0xffff: Unknown
	20h *3	Batte ry prese nt Volta ge	R(/ W)	DATA[15:0] *1								-	0xf fff	0x0000-0xfffe(mV) 0xffff: Unknown

Func tion	Ad dres s	Regis ter	R/ W	Bit Number								Logic	De fau lt	Description
		Nam e		7	6	5	4	3	2	1	0			
1 st Batte ry [_BT P]	22h	Batte ry Trip Point	R/ W	DATA[15:0] *1								-	0x 00 00	0x0000 :Clear the trip point 0x0001-0xffff(mWh)
2 nd Batte ry [_BI F]	24h to 3C h *3	*2	*2	*2								*2	*2	*2
2 nd Batte ry [_BS T]	3E h to 44h *3	*2	*2	*2								*2	*2	*2
2 nd Batte ry [_BT P]	46h	*2	*2	*2								*2	*2	*2
-	48h	Batte ry data Size	R(/ W)	DATA[7:0]								-	-	0x01 : DATA size is 3byte.(PMU06A) 0x00 :DATA size is 2 byte. (PMU06) *8
1 st Batte ry [_BI	49h	Desig n capac ity	R(/ W)	DATA[23:16] *1 *7								-	0xf f	PMU06A use this data with 02/03h. *7 *8

Func tion	Ad dres s	Regis ter	R/ W	Bit Number								Logic	De fau lt	Description
		Nam e		7	6	5	4	3	2	1	0			
	4A h	Last Full Char ge Capa city	R(/ W)	DATA[23:16] *1 *7								-	0xf f	PMU06A use this data with 04/05h. *7 *8
1 st Batte ry [_BS T]	4B h	Batte ry Rem ainin g Capa city	R(/ W)	DATA[23:16] *1 *7								-	0xf f	PMU06A use this data with 1E/1Fh. *7 *8
1 st Batte ry [_BT P]	4C h	Batte ry Trip Point	R(/ W)	DATA[23:16] *1 *7								-	0x 00	PMU06A use this data with 22/23h. *7 *8
2 nd Batte ry [_BI F]	4D h	Desig n capac ity	R(/ W)	DATA[23:16] *1 *7								-	0xf f	PMU06A use this data with 26/27h. *7 *8
	4E h	Last Full Char ge Capa city	R(/ W)	DATA[23:16] *1 *7								-	0xf f	PMU06A use this data with 28/29h. *7 *8

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
2 nd Battery [BST]	4Fh	Battery Remaining Capacity	R(/W)	DATA[23:16] *1 *7								-	0xf	PMU06A use this data with 42/43h. *7 *8
2 nd Battery [BTP]	50h	Battery Trip Point	R(/W)	DATA[23:16] *1 *7									0x00	PMU06A use this data with 46/47h. *7 *8
	51h to 6Bh *3	Reserved	R/W	Don't care								-	-	

*1: The register type is word.

*2: Same as 1st Battery CMBatt Data

*3: This register is not cleared if the system is in S4-S5 state.

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
PMU Access	6Ch	PMU_LOW-ADR	R/W	DATA [7:0]								-	-	These registers are available when PMU slave mode or charger mode is selected. For detail information, refer to PMU slave communication section in this document
	6Dh	PMU_HIG-ADR	R/W	DATA [15:8]								-	-	
	6Eh	CHECK-SUM	R/W	DATA [7:0]								-	-	
	6Fh	PMU_DATA	R/W	DATA [7:0]								-	-	
SMBus	70h*7	SMB_PTCL	R/W	PROTOCOL[7:0]								-	-	For detail information, refer to ACPI 1.0 specification [13.9 SMBus Host controller Interface via Embedded controller] These registers are not available when PMU slave mode or charger mode is selected. The PMU06 has access protect function for the
	71h*7	SMB_STS	R/W	D A T A	C L E A R	R E S E T	STATUS [4:0]					-	-	
	72h	SMB_ADDR	R/W	ADDRESS [6:0]							R E S	-	-	
	73h	SMB_CMD	R/W	COMMAND								-	-	

Func tion	A dd re ss	Regist er	R/ W	Bit Number								Logic	De fau lt	Description
		Name		7	6	5	4	3	2	1	0			
	74 h to 93 h	SMB_ DATA [0-31]	R/ W	DATA								-	-	
	94 h	SMB_ BCNT	R/ W	RE S[7: 5]		BCNT[4:0]						-	-	
	95 h	SMB_ ALAR M_ ADD R	R(/ W)	ADDRESS[6:0]						R E S	-	-		
	96 h to 97 h	AMB_ ALAR M_ DATA [0-1]	R(/ W)	DATA								-	-	
	98 h	SMB_ CNRL	R/ W	RES[7:1]						P R T		0x 00	PR T =1 :	
Reser ved	99 h to 9F h	Reser ved	R/ W	Don't care								-	-	

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the

status change.

***7: When this register is checked by polling, the interval time is necessary more than 500usec.**

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
Status	A0h*3	ADP_STS	R/W	RES[7:1]								-	-	CON=1: AC adapter is connected
	A1h*3	BAT1_STS (1st Battery)	R/W									-	-	BTP=1: EM P=1: Battery trip point is detected.
	A2h*3	BAT2_STS (2nd Battery)	R/W									-	-	LOW=1: Battery is empty. Battery is Low battery state. WA R=1: Battery is Warning state. ERR=1: Battery is Error state. DC HG=1: Battery is discharged. Battery is charged. CH G=1: Battery is connected.
	A3h*3	Reserved	R/W	Don't care								-	-	
	A4h*3	BAT1_CAP	R/W	BCAP								-	-	0x00-0x64 = 0-100(%) 0x7F = Unknown

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
	A5h*3	BAT2_CAP	R(/W)	BCAP								-	-	
	A6h*3	Reserved	R/W	Don't care								-	-	
	A7h	SMB_Alert_ADD R	R/W	ADDRESS[6:0]								-	0x00	<p>SMBAlert output device address</p> <p>The alert response function is available when this register is cleared (0x00) only.</p> <p>When the several devices assert the alert signal at the same time, the least address is stored to this register. And when this register is cleared, next alert address is stored to this register.</p>
	A8h*5	GPIO-A_EVT_STS	R/W	STS_A [7:0]								Read 0:No event 1:EVT detection	0x00	<p>To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only.</p> <p>For this operation, this register has special writing manner as follows.</p>
	A9h*5	GPIO-B_EVT_STS	R/W	0	STS_B [6:0]							Write 0:Clear	0x00	

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	AAh*5	GPIO-C_EVT_STS	R/W	0	0	0	0	0	0	0	STS [1:0]		0x00	
	ABh*5	RUN_EVT_STS	R/W										0x00	BTP2=1: BTP2 event is detected SMB=1: SMBus event is detected.
	ACH*5	WAKE_EVT_STS	R/W	BTP2	SLP	ACLRIS	GRPTS	BATT	BATT	BATT	ADP	Read 0:No event 1:EVT detection Write 0:Clear event 1:Ignore	0x00	ALR=1: SMBAlert is detected. GPIO=1: GPIO event is detected. BATn=1: Battery event is detected. ADP=1: Battery event is detected. TH=1: Thermal event is detected HIG=1: High alarm point is detected. LOW=1: Low alarm point is detected. ERR=1: Polling communication failure with retry.

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
	ADh*5	RUN_EVT_STS_2	R/W	Reserved [7:1]							1		0x00	To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only. For this operation, this register has special writing manner as follows. STS_X B (STS_X) AND (Written data)
	A Eh*5	WAKE_EVT_STS_2	R/W	Reserved [7:1]							1		0x00	
	A Fh*5	THE_RMA_L_EVT_STS	R/W	Reserved [7:3]							ELRCRV		0x00	

*3: This register is not cleared if the system is in S4-S5 state.

R(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

*5: After writing to this register, Set the “00h” to the BURST_FLG_CLR register.

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description	
				7	6	5	4	3	2	1	0				
Event/ GPIO Control	B0h	EC_RUN_ENB	R/W	BTP2	SILR	A	RES[4:1]				ADP	0: Disable 1: Enable	0x00	BTP2: SMB : ALRT : ADP:	BTP2 event SMBus event. SMBAlert event. Adapter event.
	B1h	EC_WAKE_ENB	R/W									0: Disable 1: Enable	0x00		
	B2h	BATT_RUN_ENB	R/W	BTP2	SILR	A	RES[4:1]				ADP	0: Disable 1: Enable	0x00	BTP: EMP: LOW: WAR: : ERR: CAP: C/D: CON:	Battery trip point Empty. Low battery Warning Error Capacity learning Charge/Discharge Battery presence
	B3h	BATT_WAKE_ENB	R/W									0: Disable 1: Enable	0x00		

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	B4h	GPIO-A_IO_CONF	R/W	CONF_A [7:0]								0: Input 1: Output	0x00	For detail information, refer to GPIO section in this document.
	B5h	GPIO-A_DATA	R/W	DATA_A [7:0]									-	
	B6h	GPIO-A_RUN_ENB	R/W	RUN_ENB_A [7:0]								0: Disable 1: Enable	0x00	
	B7h	GPIO-A_EVT_POL	R/W	POL_A [7:0]								0: Falling edge 1: Rising edge	0x00	
	B8h	GPIO-A_WAKE_ENB	R/W	WAKE_ENB_A [7:0]								0: Disable 1: Enable	0x00	
	B9h	GPIO-B_IO_CONF	R/W	1	CONF_B [6:0]							0: Input 1: Output	0x80	
	BAh	GPIO-B_DATA	R/W	0	DATA_B [6:0]								-	

Function	Address	Register	R/W	Bit Number								Logic	Default	Description	
		Name								7	6				5
	B Bh	GPIO-B_RUN_ENB	R/W	0	RUN_ENB_B [6:0]								0: Disable 1: Enable	0x00	
	B Ch	GPIO-B_EVT_POL	R/W	0	POL_B [6:0]								0: Falling edge 1: Rising edge	0x00	
	B Dh	GPIO-B_WAKE_ENB	R/W	0	WAKE_ENB_B [6:0]								0: Disable 1: Enable	0x00	
	B Eh	GPIO-C_DATA	R/W	RES [7:4] *4				DATA_C [3:0]					-		
	B Fh	GPIO-C_RUN_ENB	R/W	0	0	0	0	0	0	0	0	RUN_ENB_C [1:0]	0: Disable 1: Enable	0x00	

*4: Should be 0.

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
Event/ GPIO Control	C0h	GPIO-C_EVT_P OL	R/W	0	0	0	0	0	0	0	POL-C [1:0]	0: Falling edge 1: Rising edge	0x00	
	C1h	GPIO-C_WAKE_ENB	R/W	0	0	0	0	0	0	0	WAKE-ENB-C [1:0]	0: Disable 1: Enable	0x00	

Function	Address	Register	R/W	Bit Number								Logic	Default	Description		
		Name		7	6	5	4	3	2	1	0					
	C2h	EVT_CONT	R/W	RES [7:6]	WAKE	SCI	*4	RES	NOX	UT	-65-	0x00	WAKE SCI	Q_RUN	WAKE_OUT	<p>=0: Wake# output is “Level”. =1: Wake# output is “Pulse”. =0: SCI is always output by event detection and SCI_EVT shows the query data is stored. And next SCI is not output until SCI_EVT is cleared. =1: SCI is output when the command set is not executed and OBF=0. SCI_EVT shows the output SCI is for event notification. =0: Runtime event ststus is reflected to RUN_EVT_STS register. =1: Runtime</p>

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	C3h	EC_RUN_ENB_2	R/W	Reserved [7:1]								0: Disable 1: Enable	0x00	TH: Thermal event
	C4h	EC_WAKE_ENB_2	R/W									0: Disable 1: Enable	0x00	
	C5h To C7h	Reserved	R/W	Don't care								-	-	
	C8h *6	GPI_AD0	R	AD0_DATA [7:0]								-	-	For detail information, refer to GPIO section in this document.
	C9h *6	GPI_AD1	R	AD1_DATA [7:0]								-	-	
	CAh *6	Reserved	R/W	Don't care								-	-	
	CBh	D/A_CONVERT	R/W	DATA [7:0]								-	0xff	0x00-0xfe: D/A converter output data 0xff : Battery capacity(%) output

Func tion	A dd re ss	Registe r Name	R/ W	Bit Number								Logic	Def aul t	Description
				7	6	5	4	3	2	1	0			
	Ch	WAKE_DIS	R/W	DATA [7:0]								-	0x00	0x01 : WAKE# output enable 0x01 : WAKE# output disable

*4: Should be 0.

*6: This register's response time is 150usec max.

Func tion	A dd re ss	Registe r Name	R/ W	Bit Number								Logic	Def aul t	Description
				7	6	5	4	3	2	1	0			
Batte ry contr ol	0h	BAT_CHG_CONT	R/W	RE S[7: 5]								-	-	CHG_RDY# =0 : Charge ready CHGn =1 : The nth battery is charged

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
	D1h	BAT_DCH_PRI	R/W	RES[7:3]				PAT[2:0]				-	0x00	Battery discharge priority 0 : 2 1 1 : 1 2 2 : 2 1 3 : 2 1 4 : 1 2 5 : 1 2 6 : Same as 0 7 : Simultaneously discharge (Read only : This data can be set using PMU register)
	D2h	BAT_DCH_CONT	R/W	RES[7:2]				DDCCFFCC	DDCCFFCC	DDCCFFCC	0: Not discharge 1: Discharge	-	The discharge battery can be selected one of the batteries can be discharged.	
	D3h	BAT_WAR_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Warning detection point 0x0000-0xffff (mWh)
	D5h	BAT_LOW_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Low detection point 0x0000-0xffff (mWh)
	D7h	BAT_WAR_REL	R/W	DATA [7:0]								-	0x10	Relative capacity battery Warning detection point 00-C8h (0-100% step 0.5%)

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
	D8h	BAT_LOW_REL	R/W	DATA [7:0]								-	0x06	Relative capacity battery Low detection point 00-C8h (0-100% step 0.5%)
	D9h*3	FULL_DATA	R/W	DATA [7:0]								-	0xbe	Full charge cancel point 00-C8h (0-100% step 0.5%)
	Dah	CC_CUR_DATA	R	DATA [7:0]								-	0x00	Battery charging current setting 0x01-0xff (0.02-5.10A step 0.02A) 0x00 Depends on the battery This register is “read only”, to change the value, use the register in PMU registers area.
	DBh To DCh	BTP2	R/W	DATA [15:0]								-	0x0000	0x0000: Clear the trip point 0x0001-0xffff : (mWh) When all of the battery’s capacities lesser than this setting value, the BTP2 is detected if event is enabled.

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	DDh To Dfh	Reserved	R/W	Don't care								-	-	

*3: This register is not cleared if the system is in S4-S5 state.

R(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
PMU control	E0h	PMU_CONT	R/W	RES[7:3]				EC_REG	BATTERY	POWER_LED		-	0x00	<p>PMU does not initialize EC register when system power is off.</p> <p>BATTERY_LED =1: PMU indicates the Battery discharge status to the LED_BAY#n, when the battery is installed.</p> <p>POWER_LED =1: The Power LED blink</p>

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	E1h	ACPI_ACC_ENB	R/W	RES [7:1]								-	0x00	OS_STS = 1: ACPI mode = 0: Legacy mode
	E2h	OFF_TIMER	R/W	DATA [7:0]								-	0x64	Power switch over ride function timer 01h-FFh (0.1-25.5sec step 0.1sec) 00h : Reserved
Thermal Sensor Polling	E3h	POLLING_ADDRESS	R/W	Slave Address [6:0]									0x00	Address: 0x00-0x7F The polling slave address setting If this address is 00, the Polling is disabled.
	E4h	HIGH_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data GE this value, the event will be detected.
	E5h	LOW_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data LE this value, the event will be detected.
	E6h	POLLING_INTERVAL	R/W	DATA [7:0]									0x00	0x00 : Polling disable 0x01 – 0xFF [x 250ms] (250ms to 63.75sec)

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
	E7h	POLLING_DATA	R/W	DATA [7:0]								Signed value	0x00	This register shows data at latest polling.
	E8h	HARDWARE_SHUT_DOWN	R/W	DATA [7:0]								Signed value	0x7D	If the thermal sensor read value GE this value, the PMU automatically off the power.
	E9h	POLLING_COMMAND	R/W	DATA [7:0]									0x00	Polling command (data register) address.
	EAh	RETRY_COUNT	R/W	DATA [7:0]									0x10	0x00 - 0xFF: Retry count value (0-255)
	EBh To EFh	Reserved	R/W	Don't care										
PMU control	F0h	BURST_FLG_CLR	R/W	DATA [7:0]								-	-	After writing to the register addressed A8h-AFh, Set the 00h to this register.

Function	Address	Register	R/W	Bit Number								Logic	Default	Description
		Name		7	6	5	4	3	2	1	0			
	F1h To Fh	Reserved	R/W	Don't care										

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

8. Miscellaneous

8.1 Security

The user may enter up to 8 standard text characters for a password. The password includes two levels. The higher priority is the Supervisor Password. The lower priority is the User Password. The Supervisor Password can access all the system resource, while the User Password may not access the floppy disk when it is protected by Supervisor Password. When the security function is enabled, the system will request the user to enter password during the following situation.

I. **Power On:** The system will prompt the user to enter the password before booting the OS. If the user key in the wrong password for 3 times, then the system will halt.

II. **Resume:** The system will prompt the user to enter password while resuming from STR or STD mode. If the user keys in the wrong password for 3 times, the system will not resume and should return to Suspend mode again.

III. **Entering CMOS Setup:** The system will prompt the user to enter the password before entering the CMOS Setup. If the user keys in the wrong password for 3 times, then the system will halt.

8.2 Phoenix FirstBIOS Security.

9. CMOS Setup Utility

The Setup utility is used to configure the system. The Setup contains the information regarding the hardware for boot purpose. The changed settings will take effect after the system rebooted.

9.1 Main Menu Default

PhoenixBIOS Setup Utility

Main	Advanced	Security	Boot	Exit
			Item Specific Help	
<div>System Time : [12: 00 : 00]</div> <div>System Date : [01 / 01 / 2003]</div> <div>Language: [English (US)]</div> <div>▶ Boot Display Device [Both]</div> <div>Primary Master [HITACHI_DK23DA-30-(P M)]</div> <div>Secondary Master Installed CD/DVD</div> <div>System Memory: 640 KB</div> <div>Extended Memory: 228352 KB</div> <div>CPU Type Genuine Intel Processor-M</div> <div>CPU Speed 1500 MHz</div> <div>BIOS Version: 0.1A-2834-0812</div>			Select the display device	
Help	Select Item		Change Values	

Setup Defaults

Exit **Select Menu** ► **Select** **Sub-Menu**
Save and Exit

System Time:	[12:00:00]	<Tab>, <Shift-Tab>, or <Enter> selects Field.
System Date:	[01/01/2003]	<Tab>, <Shift-Tab>, or <Enter> selects field.
Primary Master	[30006MB]	
Primary Slave	[None]	
Secondary Master	[CD-ROM]	
Secondary Slave	[None]	
System Memory	640 KB	(BIOS auto detect, display for information only)
Extended Memory	227328 KB	(BIOS auto detect, display for information only)
CPU Type	Intel Banias Processor	(BIOS auto detect, display for information only)
CPU Speed	1600 MHz	(BIOS auto detect, display for information only)
BIOS Version	0.3A-2869-0812	(BIOS-VGA-uP version, display for information only)

9.1.1 Internal HDD Sub-Menu Default

PhoenixBIOS Setup Utility

Main

Primary Master [HITACHI_DK23DA-30-(PM)]		Item Specific Help
Type:	[Auto]	Select the drive type fixed disk installed in your system. If type USER is selected, Cylinders, Heads & Sectors can be edited directly.
LBA Format		
Total Sectors:	58605120	
Maximum Capacity:	30006MB	
Multi-Sector Transfers:	16 Sectors	
LBA Mode Control:	Enabled	
32 Bit I/O:	[Disabled]	
Transfer Mode:	Fast PIO 4	
Ultra DMA Mode:	Mode 5	
Help	Select Item	Change Values
	Setup Defaults	
Exit	Select Menu ►	Select Sub-Menu
	Save and Exit	

Type:	[Auto] / [None] / [ATAPI Removable] / [CD-ROM] / [User]	Select the drive type corresponding to the
LBA Format		USER is selected, Cylinders, Heads & Sectors
Total Sectors:	58605120	edited directly.
Maximum Capacity:	30006MB	
Multi-Sector Transfers:	[16 Sectors] / [Disabled] / [2 Sectors] / [4 Sectors] / [8 Sectors]	Determine the number of sectors per block for multiple sector transfers.
LBA Mode Control:	[Enabled] / [Disabled]	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads & Sectors
32 Bit I/O :	[Disabled] / [Enabled]	This setting enables or disables 32 bit IDE data transfers
Transfer Mode:	[Standard] / [Fast PIO 1] / [Fast PIO 2] / [Fast PIO 3] / [Fast PIO 4] / [FPIO 3 / DMA 1] / [FPIO 4 / DMA 2]	Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode
Ultra DMA Mode:	Mode 2	(BIOS auto detect, display for information only)

Advanced Menu Default

PhoenixBIOS Setup Utility

Main	Advanced	Security	Boot	Exit	Item Specification Help
Installed o/s					<p>Select the operating System installed</p> <p>On your system which you will use most commonly.</p>
Reset Date:	Configuration	[No]	<p>Select 'Yes' if you Want to clear the Extended System Configuration Date (ESCD) area.</p>		
Legacy Disk Access Mode:		[DOS]	<p>UNIX,Novell Netware Or other operating System,select 'other'.</p> <p>If you are installing new software and the drive fail ,change this selection and try again</p> <p>Different operating system require different representations of drive geometries.</p>		

Help	Select Item	Change Values
Exit	Setup Defaults	
	Select Menu ►	Select Sub-Menu
	Save and Exit	
Boot-time Diagnostic Screen :	[Disable]	Display the diagnostic Screen during boot
Legacy USB Support:	[Enable]	Enable support for legacy Universal Serial Bus

9.2 Security Menu Default

PhoenixBIOS Setup Utility		
Main	Advanced	Security
Supervisor Password Is:		Clear
User Password Is:		Clear
Set Supervisor Password		[Enter]
Set User Password		[Enter]
Fixed disk boot sector:		[Normal]
Password on boot:		[Disabled]
Help		Change Values
Exit		Select Sub-Menu
Select Item		Save and Exit
Setup Defaults		
Select Menu		

Item Specification Help
Supervisor Password controls access to the setup utility.
Write protect boot sector on hard disk to protect against viruses.

Set Supervisor Password	Enter New Password	Supervisor Password controls access to the setup utility.
-------------------------	--------------------	---

	Confirm New Password	
Set User Password	Press Enter	User Password controls access to the system.
Fixed disk boot sector:	[Normal]/[Write Protect]	Write protects boot sector on hard disk to protect against viruses.
Password on boot	[Disabled] / [Enabled]	Enabled password entry on boot

9.3 Boot Menu Default

PhoenixBIOS Setup Utility

Main		Advanced	Security	Boot	Exit
				Item Specific Help	
1.	Removable Device			<p>Key used to view or configure Device: <Enter> expands or collapses devices with a + or - <Ctrl + Enter> expands all <Shift + 1> enables or disable a device. <+> and <-> moves the device up or down. <n> May move removable device between Hard Disk or Removable Disk <d> Remove a device that is not installed.</p>	
2.	+ Hard Drive				
3.	CD-ROM Driver				
4.	IBA FE Slot 0240 v4109				
Help		Select Item		Change Values	
		Setup Defaults			
Exit		Select Menu ►		Select Sub-Menu	
		Save and Exit			

9.4 Exit Menu

PhoenixBIOS Setup Utility

Main	Advanced	Security	Boot	Exit
			Item Specific Help	
Exit Saving Changes Exit Discarding Changes Load Setup Defaults Discard Changes Save Changes Battery Refresh			Exit System Setup and save your changes to CMOS.	
Help	Select Item	Change Values		
	Setup Defaults			
Exit	Select Menu ▶	Select	Sub-Menu	
	Save and Exit			

Exit Saving Changes	Exit System Setup and save your changes to CMOS.
Exit Discarding Changes	Exit utility without saving Setup data to CMOS.
Load Setup Defaults	Load default values for all SETUP items.
Discard Changes	Load previous values from CMOS for all SETUP items.
Save Changes	Save Setup Data to CMOS.

Battery Refresh

Reactivate the battery.
(This utility used for Ni-MH battery only.)

10. Definitions of Terms

10Base-T (Ethernet) - A networking standard that supports data transfer rates up to 10Mbps (10 megabits per second).

100Base-T (Fast Ethernet) - A relatively new networking standard that supports data transfer rates up to 100Mbps.

ACPI - Advanced Configuration and Power Management Interface, a power management specification developed by Intel, Microsoft, and Toshiba.

CardBus - The 32-bit version of the PCMCIA PC Card standard. In addition to supporting a wider bus (32 bits instead of 16 bits), CardBus also supports bus mastering and operation speeds up to 33MHz.

Clock Throttling – South bridge function that allows the CPU clock to be stopped and started at a known duty cycle using the STPCLK# pin to enter and exit Stop Grant mode. Clock throttling is used for power saving, thermal management, and reducing the processing speed.

DIMM (SODIMM) - Dual In-line Memory Module, a small circuit board that holds memory chips. A Single In-line Memory Module (SIMM) has a 32-bit path to the memory chips whereas a DIMM has 64-bit path. Because the processor requires a 64-bit path to memory, you need to install SIMMs two at a time. With DIMMs, you can install one DIMM at a time. SODIMM is Small Outline Dual In-line Memory Module used in notebook computers.

DMI - Desktop Management Interface, an API to enable software to collect information about a computer environment about a computer environment. For example, using DMI a program can determine what hardware and expansion boards are installed on a computer.

GPI - General Purpose Input.

GPO - General Purpose Output.

Lid Switch - A switch that indicates the notebook LCD Panel has been closed and it can be turned off.

MPEG-2 - Moving Picture Experts Group, a working group of ISO. The term also refers to the family of digital video compression standards developed by the group. There are two major MPEG standards : MPEG-1 and MPEG-2. The most common implementations of the MPEG-1 standard provide a video resolution 352x240 at 30 frames per second(fps). A newer standard, MPEG-2, offers resolution of 720x480 and 1280x720 at 60 fps, with full CD-quality audio.

North Bridge - The CPU to PCI interface, also contains the memory and cache controllers.

South Bridge - The PCI to ISA interface, also contains many legacy devices.

SMM - System Management Mode, Mode of operation while an SMI is active.

SMI - System Management Interrupt, non-maskable interrupt that causes the system to enter SMM. SMM functions include power management, USB legacy keyboard control, security, hot keys, and thermal monitoring.

SMB - System Management Bus, that is used for managing smart batteries, reading SDRAM configuration information, and other miscellaneous system function.

TBD -To Be Discussed. The mentioned specification is not final that should be discussed with related engineers.

Ultra DMA-33 - A protocol developed by Quantum Corporation and Intel that supports burst mode data transfer rates of 33.3 MBps.

USB - A new external bus standard that supports data transfer rates of 12 MBps. A single USB

port can be used to connect up to 127 peripheral devices, such as mice, modems, and keyboards. USB also supports Plug-and-Play installation and hot plugging.