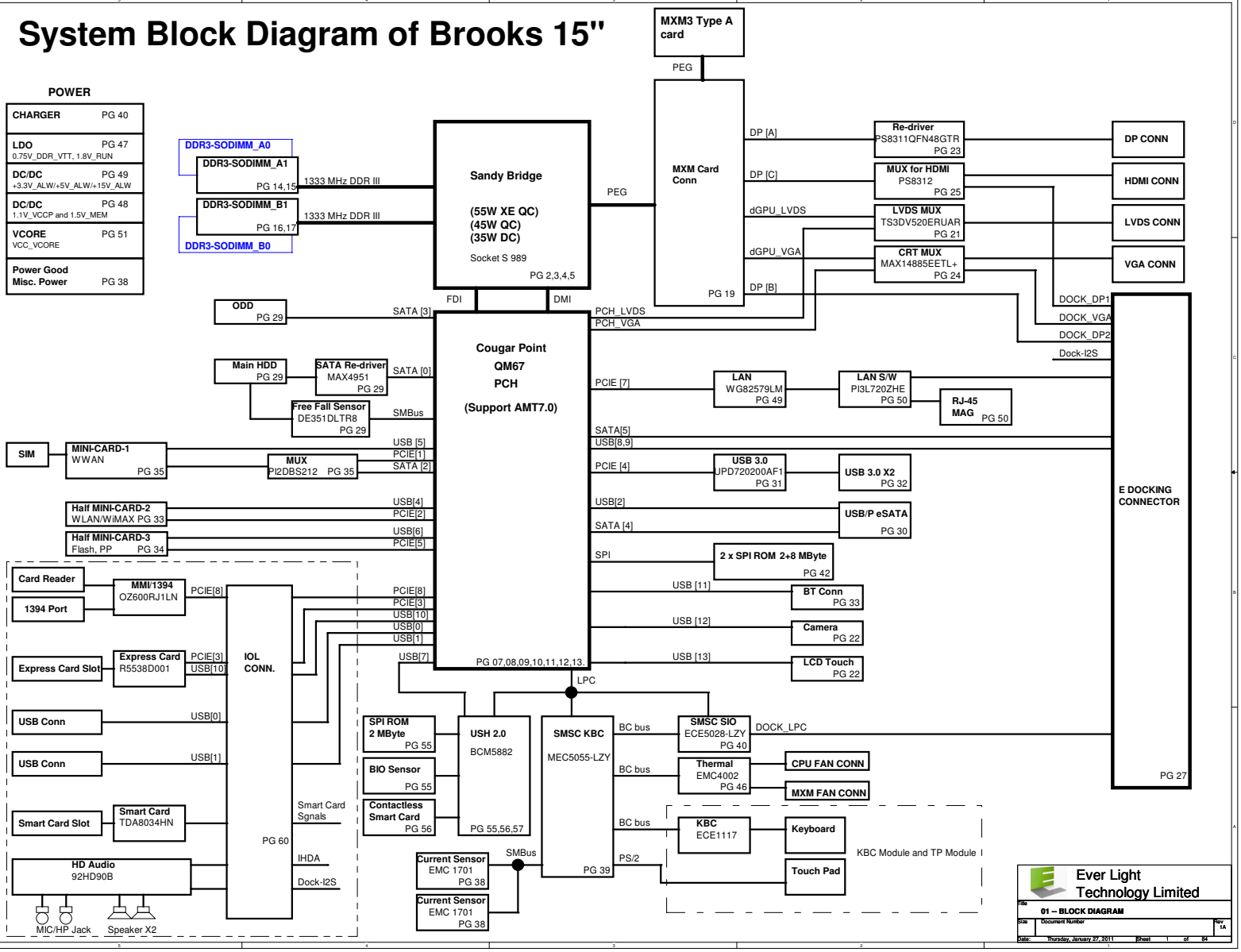
System Block Diagram of Brooks 15"



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File: 01 -- BLOCK DIAGRAM

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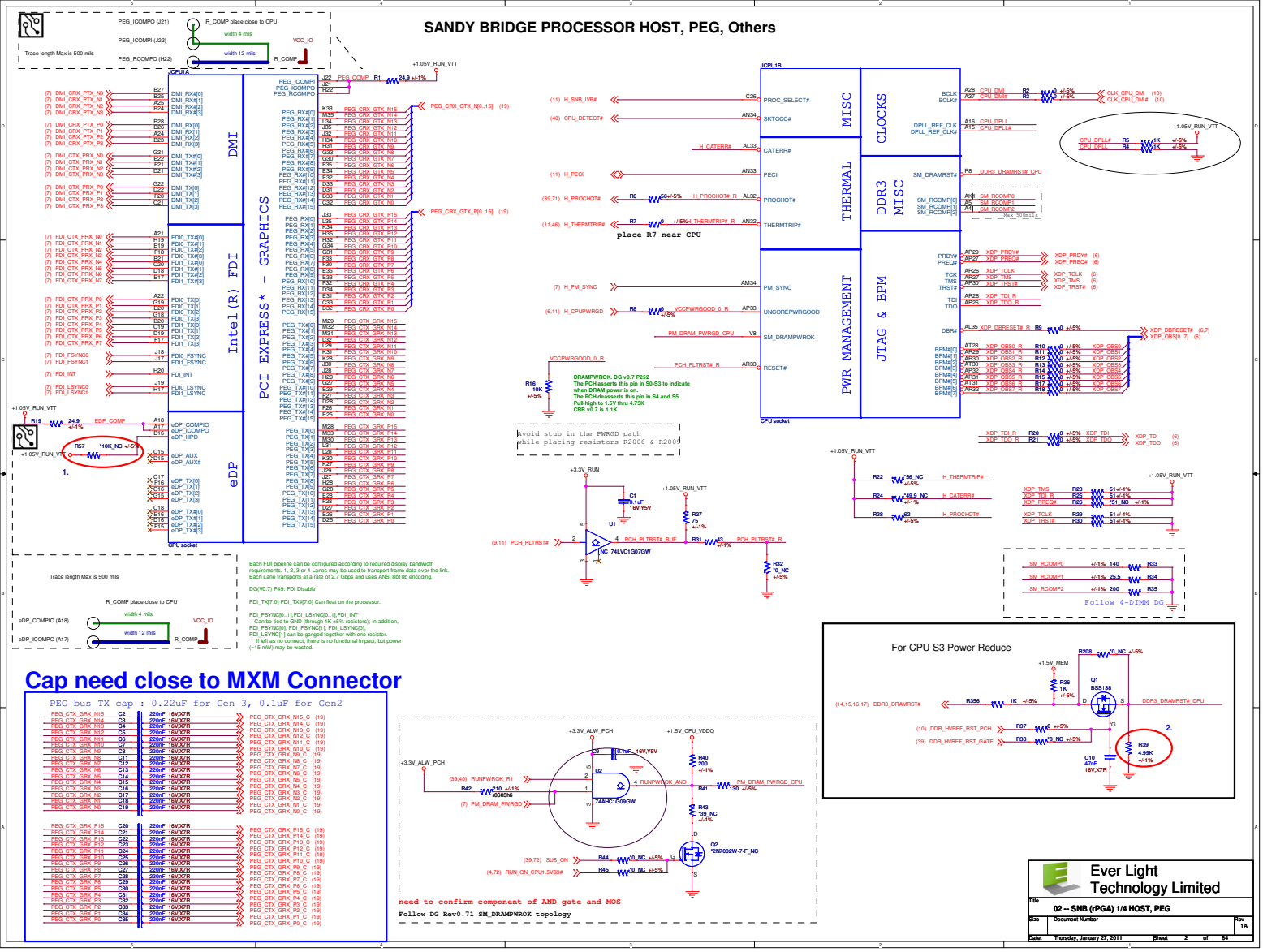
SANDY BRIDGE PROCESSOR HOST, PEG, Others



Cap need close to MXM Connector

PEG bus TX cap : 0.22uF for Gen 3, 0.1uF for Gen2

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Title	02 – SNB (rPGA) 1/4 HOST, PEG	
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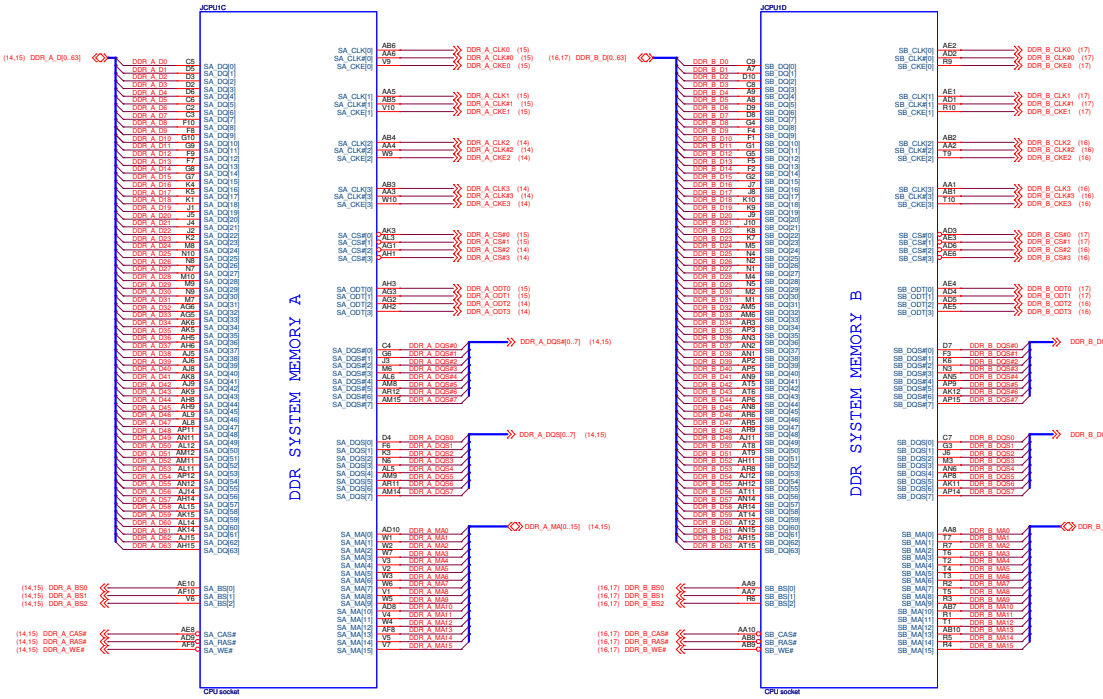
SANDY BRIDGE PROCESSOR (DDR3)



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Title	03 -- SNB (rPGA) 2/4 DDR		
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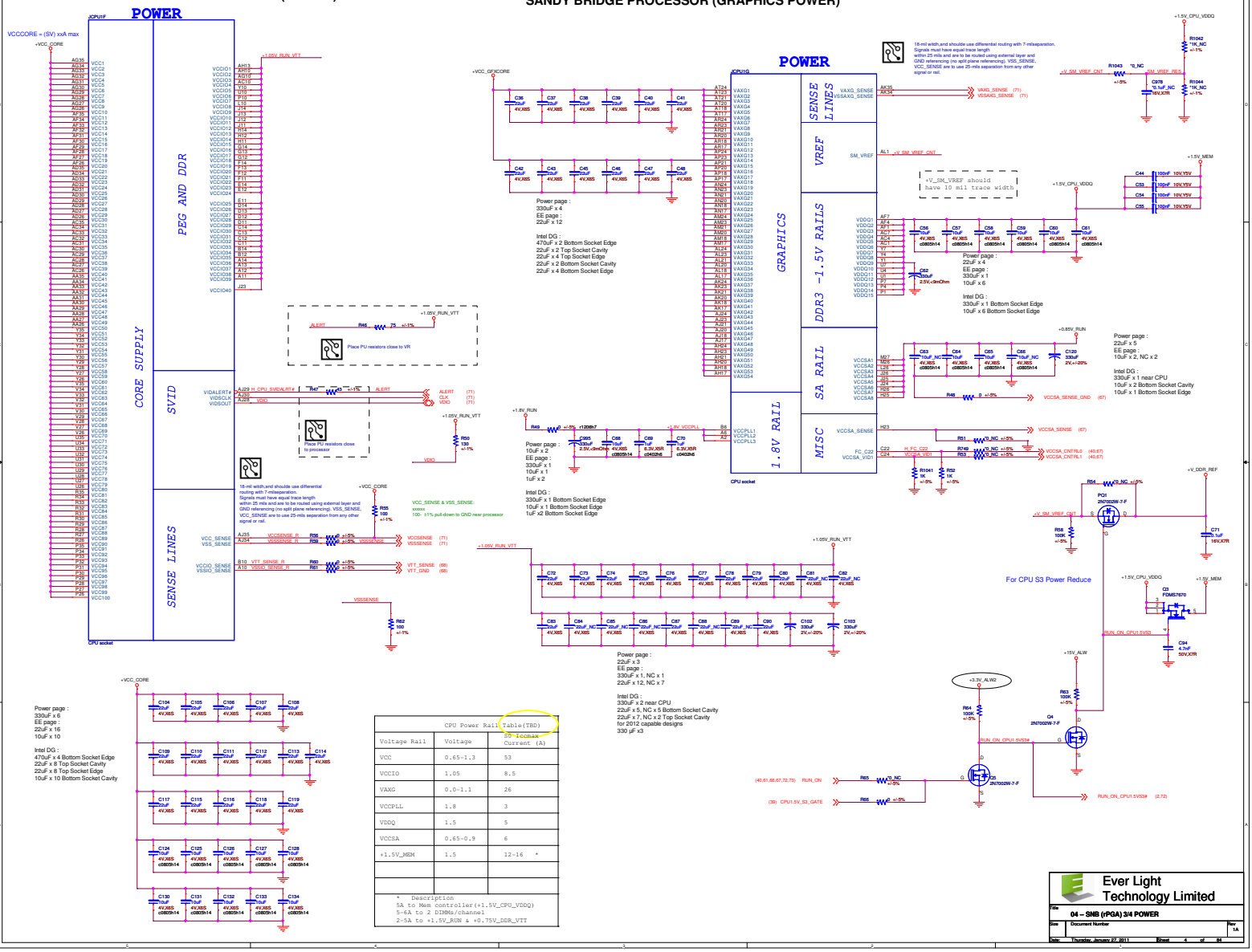
SANDY BRIDGE PROCESSOR (POWER)

SANDY BRIDGE PROCESSOR (GRAPHICS POWER)



Power page : 330uF x 6 EE page : 22uF x 16 10uF x 10

Intel DG : 470uF x 4 Bottom Socket Edge 22uF x 8 Top Socket Cavity 22uF x 8 Top Socket Edge 10uF x 10 Bottom Socket Cavity

Power page : 330uF x 4 EE page : 22uF x 12

Intel DG : 470uF x 2 Bottom Socket Edge 22uF x 2 Top Socket Cavity 22uF x 4 Top Socket Edge 22uF x 2 Bottom Socket Cavity 22uF x 4 Bottom Socket Edge

Power page : 10uF x 2 EE page : 330uF x 1 10uF x 1 1uF x 2

Intel DG : 330uF x 1 Bottom Socket Edge 10uF x 1 Bottom Socket Edge 1uF x2 Bottom Socket Edge

Power page : 22uF x 3 EE page : 330uF x 1, NC x 1 22uF x 12, NC x 7

Intel DG : 330uF x 2 near CPU 22uF x 5, NC x 5 Bottom Socket Cavity 22uF x 7, NC x 2 Top Socket Cavity for 2012 capable designs 330 µF x3

Power page : 22uF x 4 EE page : 330uF x 1 10uF x 6

Intel DG : 330uF x 1 Bottom Socket Edge 10uF x 6 Bottom Socket Edge

Power page : 22uF x 5 EE page : 10uF x 2, NC x 2

Intel DG : 330uF x 1 near CPU 10uF x 2 Bottom Socket Cavity 10uF x 1 Bottom Socket Edge

CPU Power Rail Table(TBD)		
Voltage Rail	Voltage	50 Icmax Current (A)
VCC	0.65~1.3	53
VCCIO	1.05	8.5
VAXG	0.0~1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65~0.9	6
+1.5V_MEM	1.5	12~16 *

* Description
5A to Mem controller(+1.5V_CPU_VDDQ)
5~6A to 2 DIMMs/channel
2~5A to +1.5V_RUN & +0.75V_DDR_VTT

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Title	04 – SNB (rPGA) 3/4 POWER
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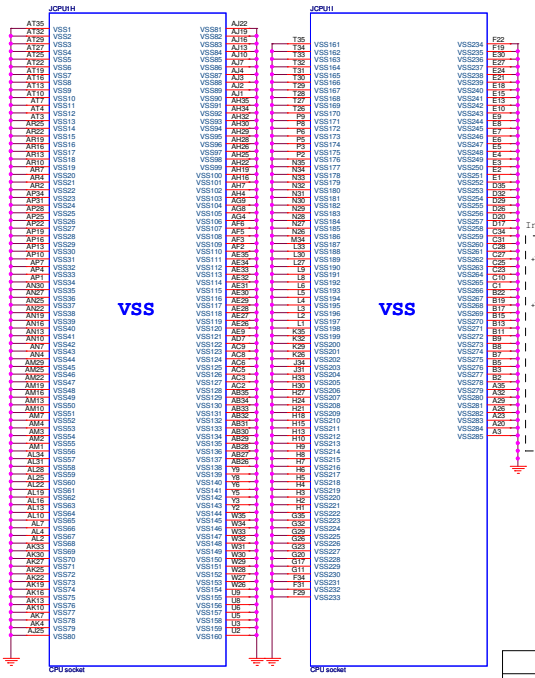
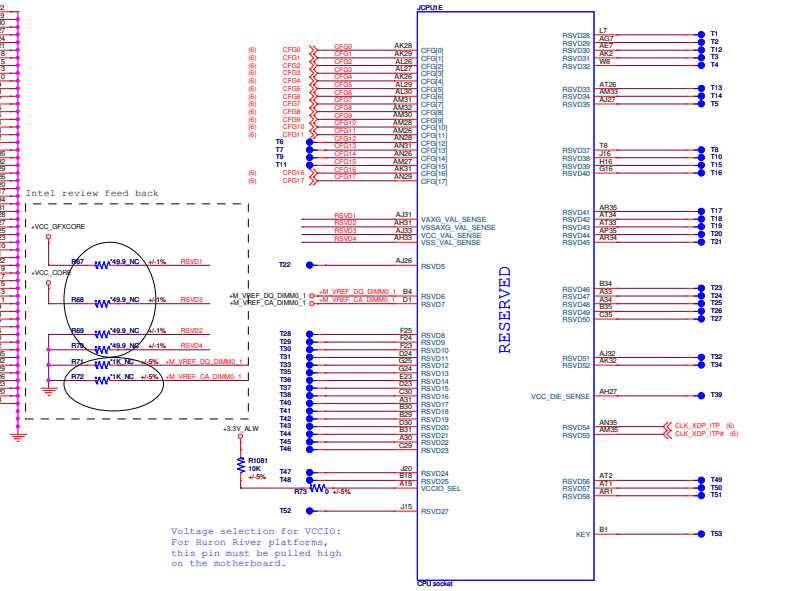
SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)



	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 (PEG Defer Training)	PEG Train immediately following xxRESETB de assertion (Default Value)	PEG Wait for BIOS for training

CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable (Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable

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Title	05 -- SNB (rPGA) 4/4(GND)	
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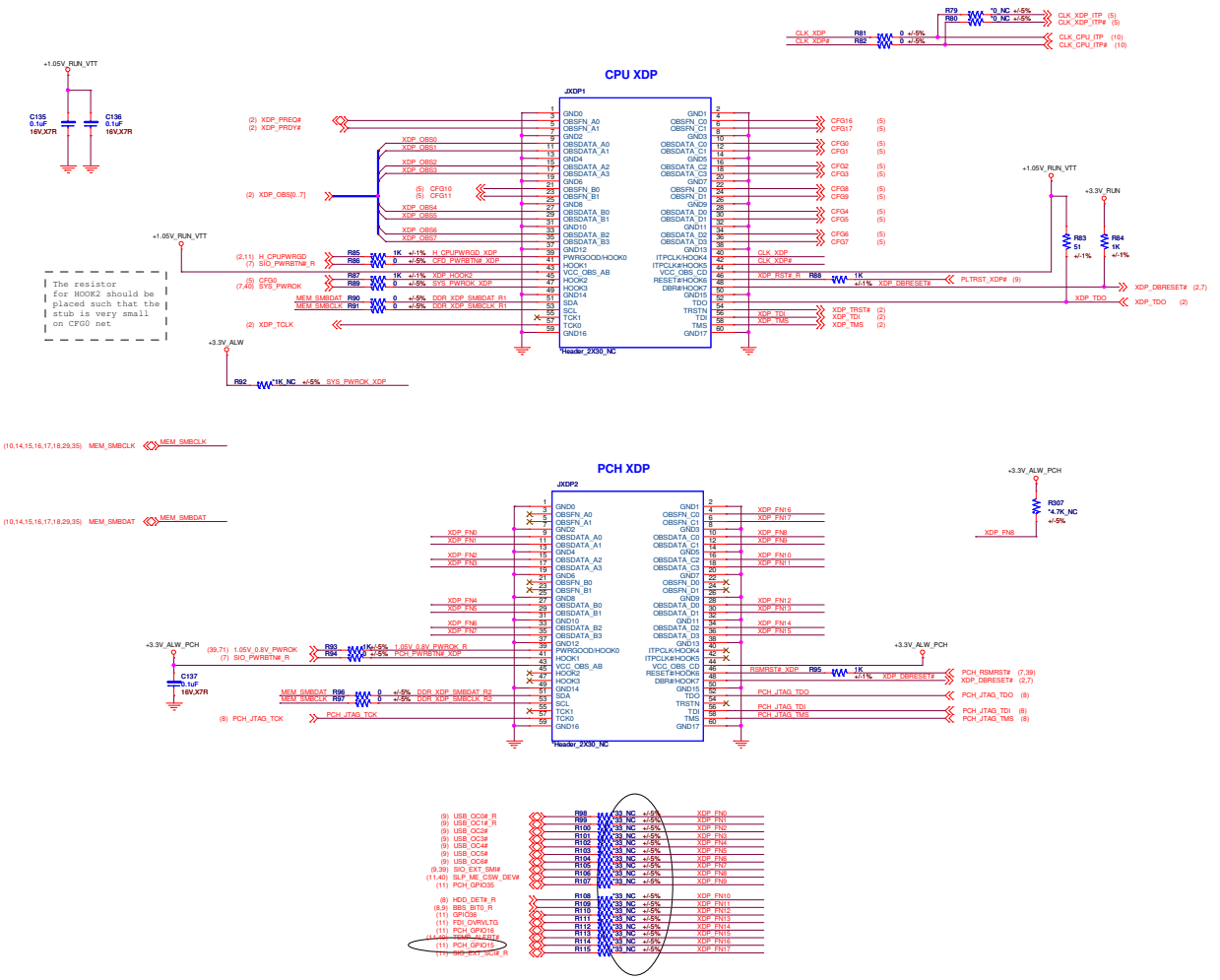

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Title	06 -- XDP Connector	
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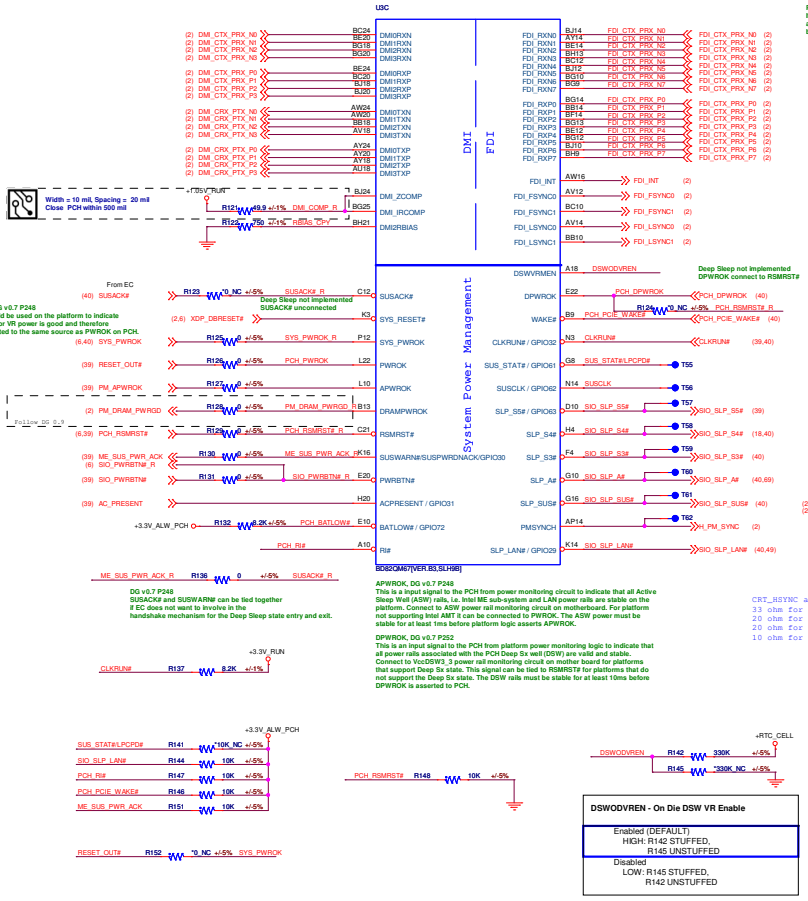
COUGAR POINT (DMI,FDI,GPIO)



DSWODVREN - On Die DSW VR Enable

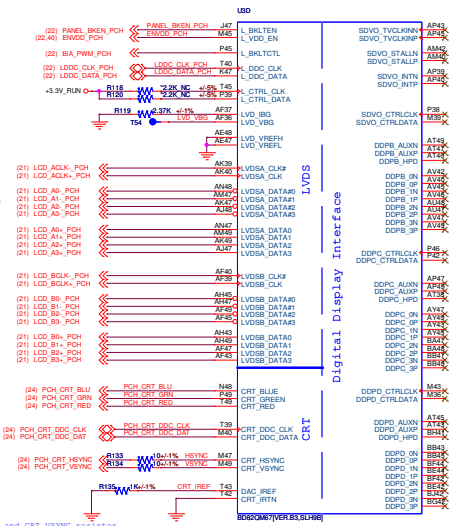
Enabled (DEFAULT)
HIGH: R142 STUFFED,
R145 UNSTUFFED

Disabled
LOW: R145 STUFFED,
R142 UNSTUFFED

R116 100K +/-5% ENVDD_PCH
R117 100K +/-5% PANEL_BKEN_PCH

PDG v0.7 P166
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects

COUGAR POINT (LVDS,DDI)



CRT_HSYNC and CRT_VSYNC resistor
33 ohm for Direct Connect
20 ohm for Dock Support
20 ohm for Switchable Graphics Device Down Topology
10 ohm for Switchable Graphics Dock Support

PCH_CRT_BLU R138 150 +/-1%
PCH_CRT_GRN R139 150 +/-1%
PCH_CRT_RED R140 150 +/-1%

PCH_CRT_DDC_DAT R149 2.2K +/-5%
PCH_CRT_DDC_CLK R150 2.2K +/-5%
LDDC_CLK_PCH R1106 2.2K +/-5%
LDDC_DATA_PCH R1107 2.2K +/-5%

+3.3V_RUN

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Title	07 -- CBT 1/6 (DMI&VIDEO)	
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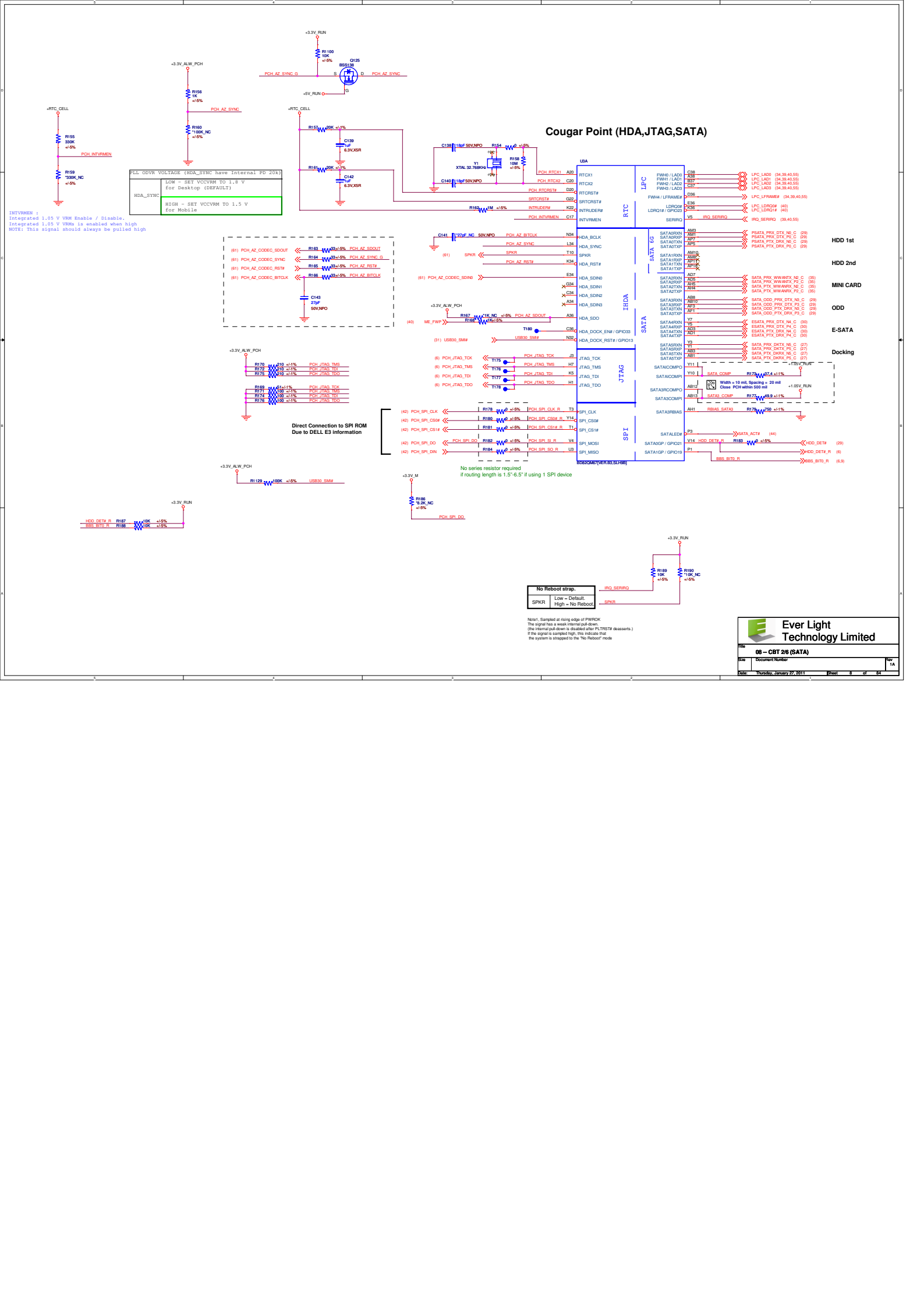
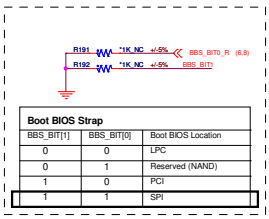
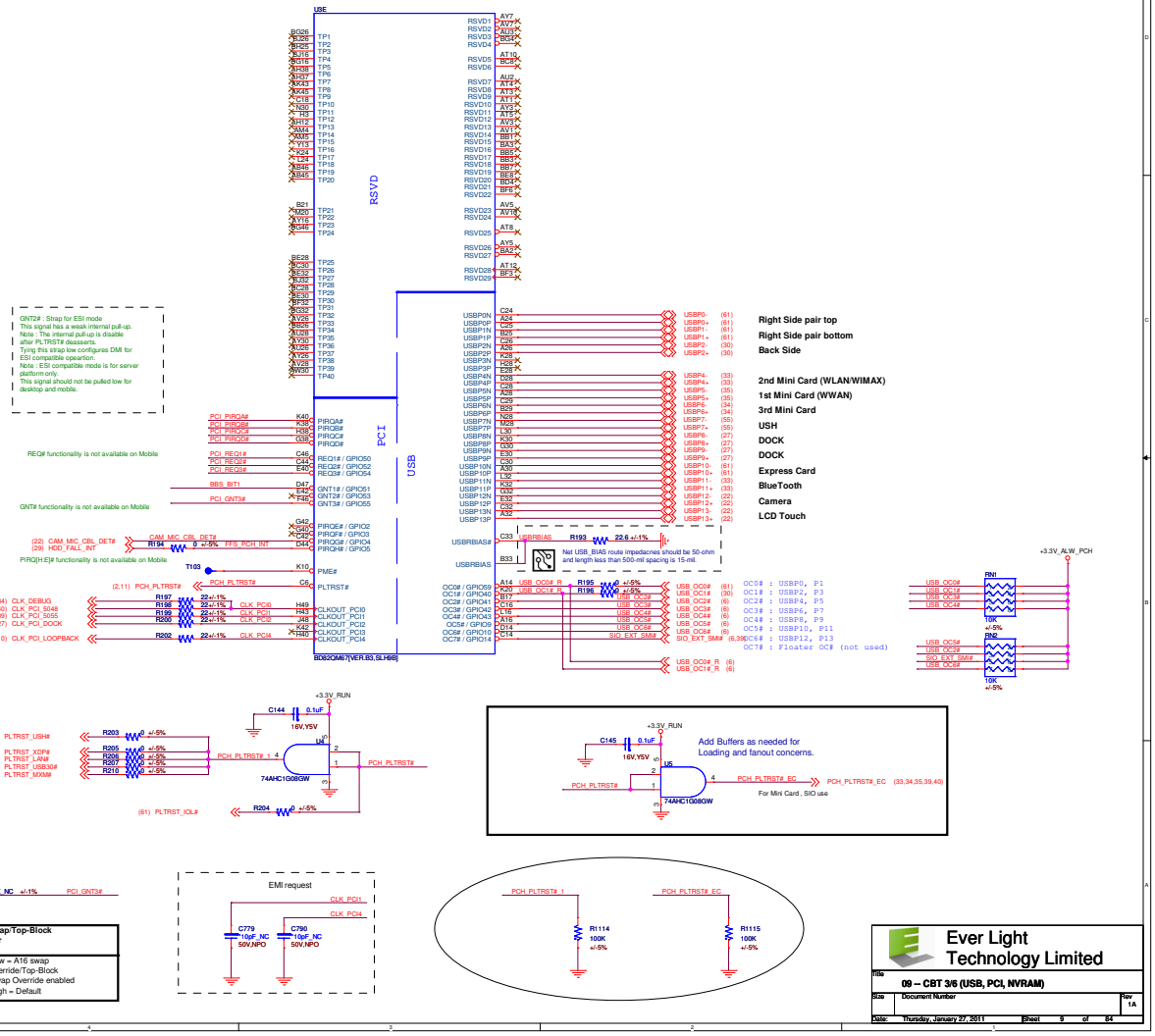

Cougar Point (HDA,JTAG,SATA)
PLL ODVR VOLTAGE (HDA_SYNC have Internal PD 20k)
HDA_SYNC
LOW - SET VCCVRM TO 1.8 V for Desktop (DEFAULT)
HIGH - SET VCCVRM TO 1.5 V for Mobile
INTVRMEN :
Integrated 1.05 V VRM Enable / Disable.
Integrated 1.05 V VRMs is enabled when high
NOTE: This signal should always be pulled high
Direct Connection to SPI ROM
Due to DELL E3 information
No series resistor required
if routing length is 1.5"-6.5" if using 1 SPI device
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
Note1, Sampled at rising edge of PWROK
The signal has a weak internal pull-down.
(the internal pull-down is disabled after PLTRST# deasserts.)
If the signal is sampled high, this indicate that
the system is strapped to the "No Reboot" mode
HDD 1st
HDD 2nd
MINI CARD
ODD
E-SATA
Docking
Ever Light Technology Limited
08 -- CBT 2/6 (SATA)
Thursday, January 27, 2011

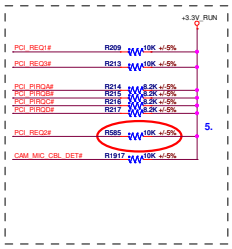
Cougar Point (PCI,USB,NVRAM)



Boot BIOS Strap

BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI





A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Title	09 -- CBT 3/6 (USB, PCI, NVRAM)
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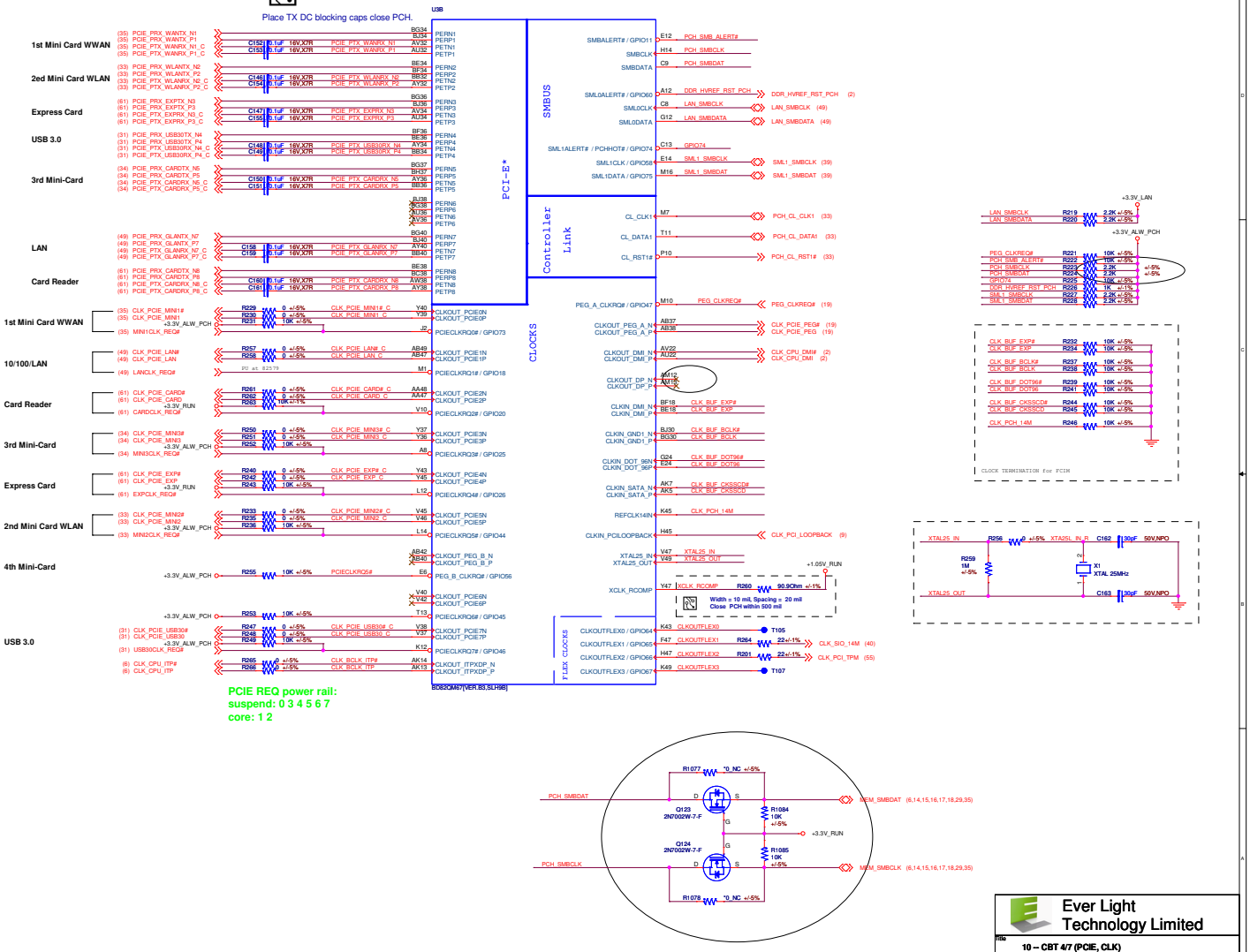
Cougar Point (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



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Title	10 – CBT 4/7 (PCIE, CLK)	
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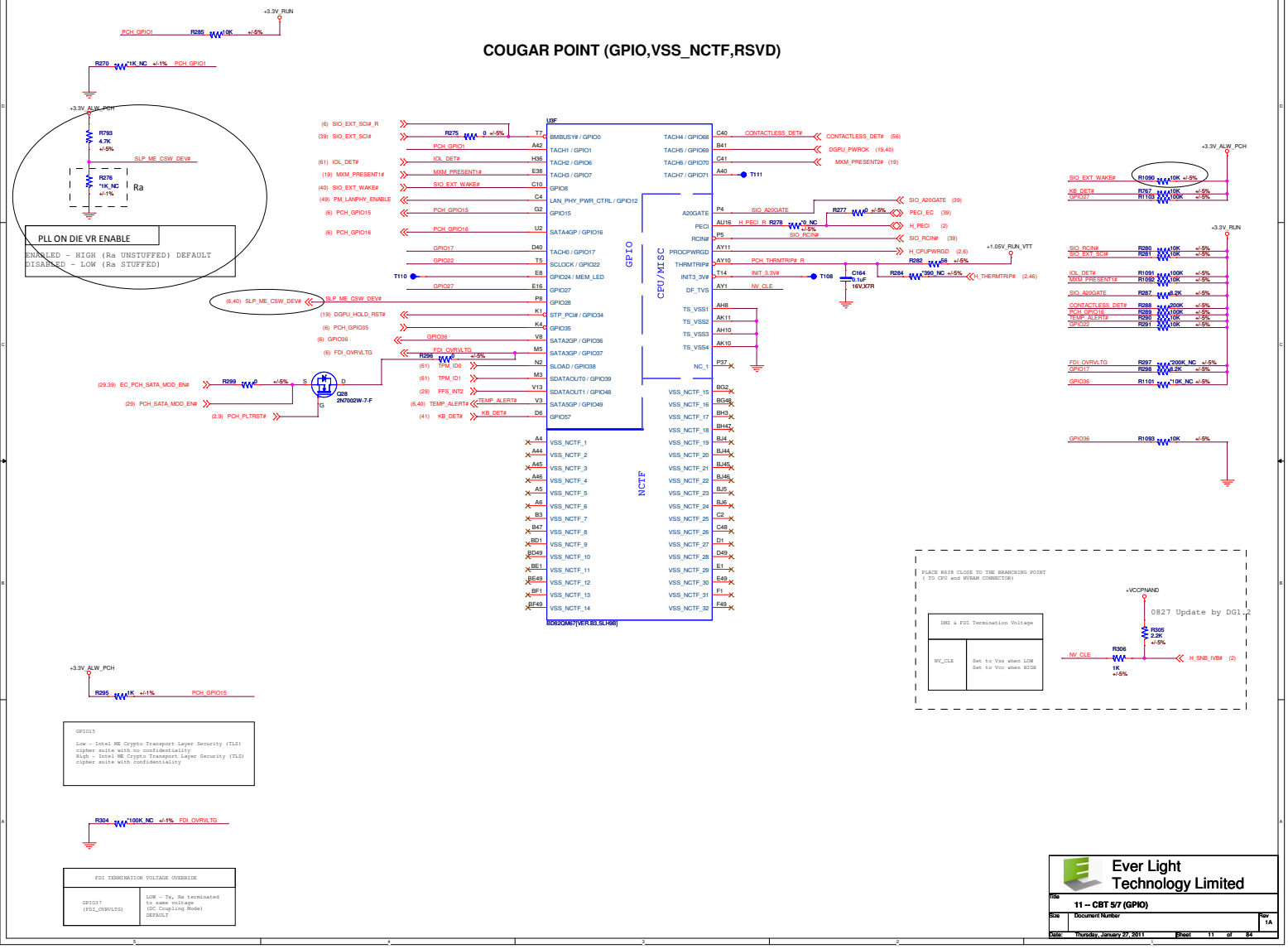
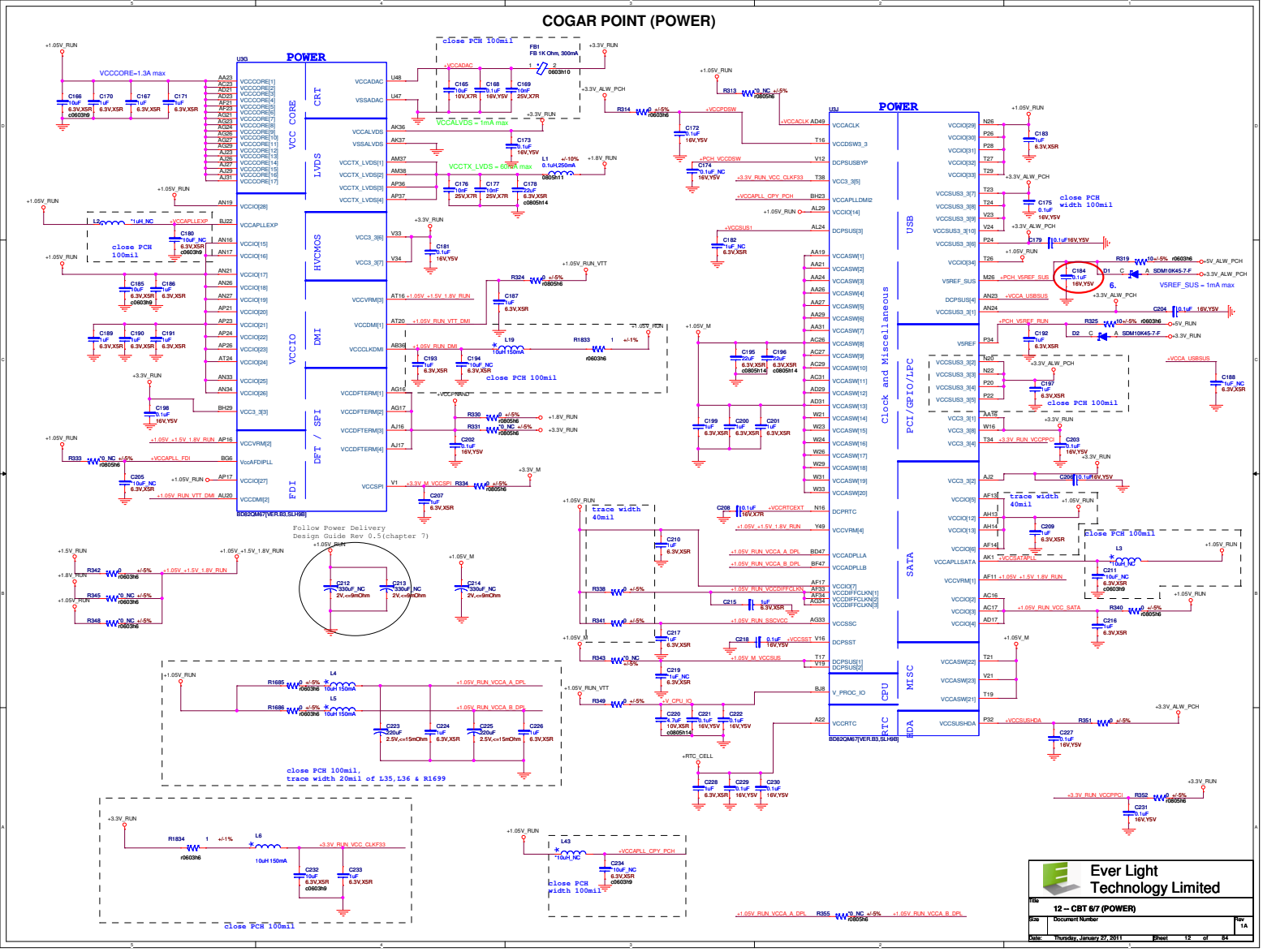
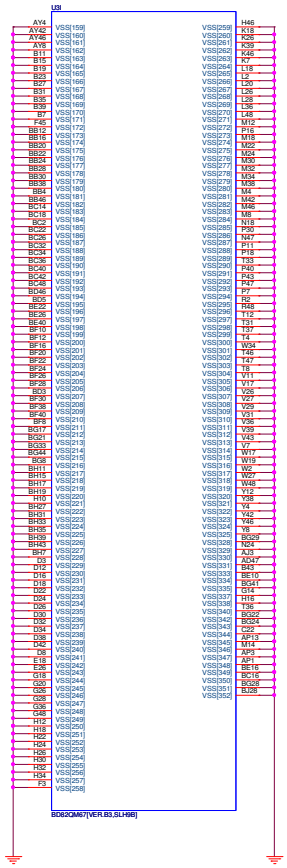
COUGAR POINT (GPIO,VSS_NCTF,RSVD)

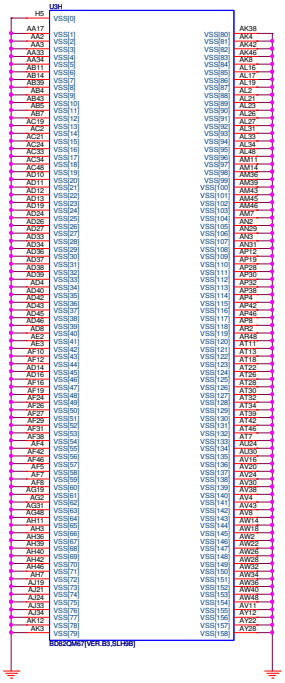


COGAR POINT (POWER)



Cougar Point (GND)





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Title	13 – CBT 7/7 (GND)	
Size	Document Number	Rev 1A
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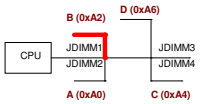
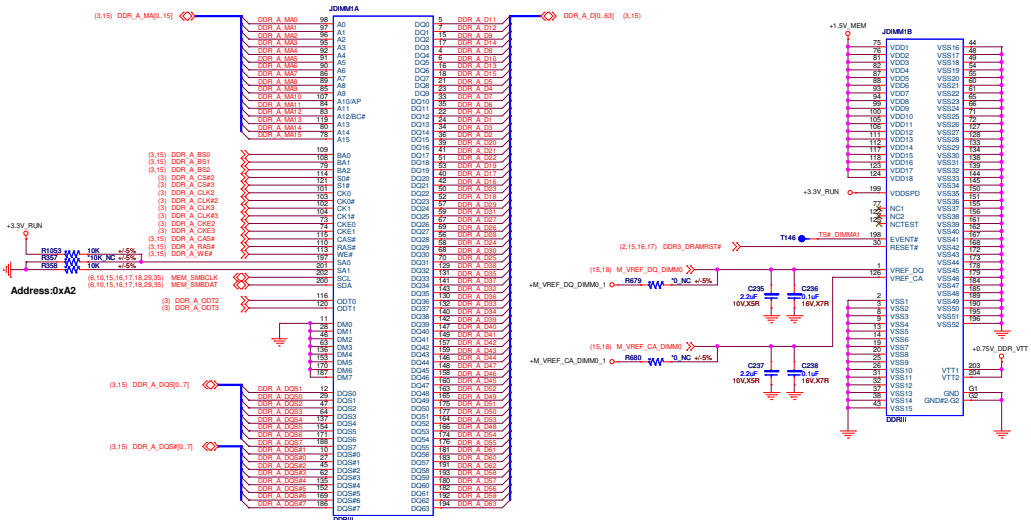
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



CHA_DIMM1_TOP_SIDE

JDIMM1 is STD type. (H=60)

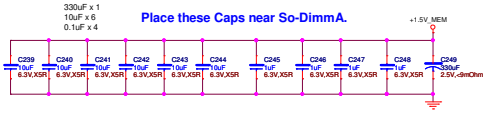


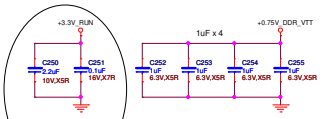
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

330uF x 1
10uF x 6
0.1uF x 4

Place these Caps near So-DimmA.





For VDDSPD

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Title	15 -- SODIMM-204P-A1	
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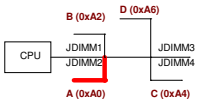
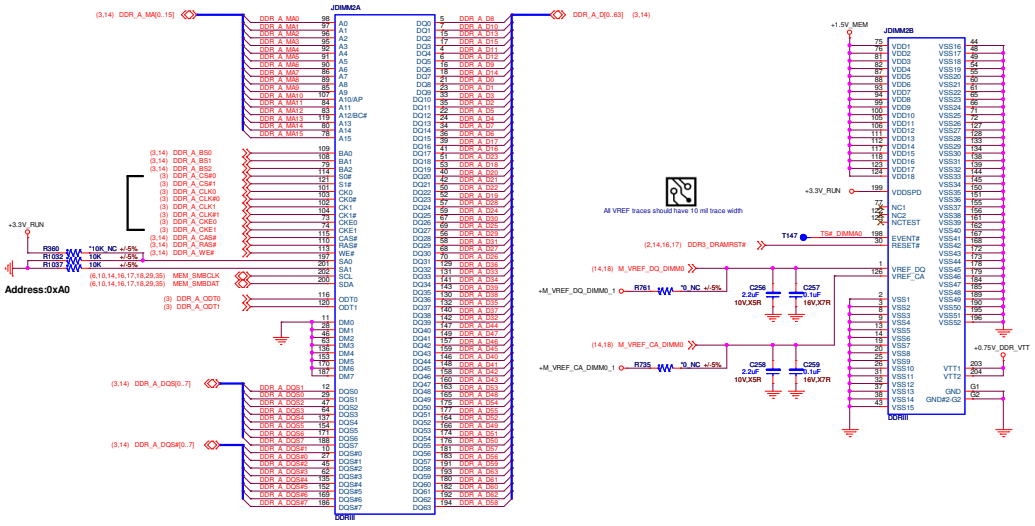
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



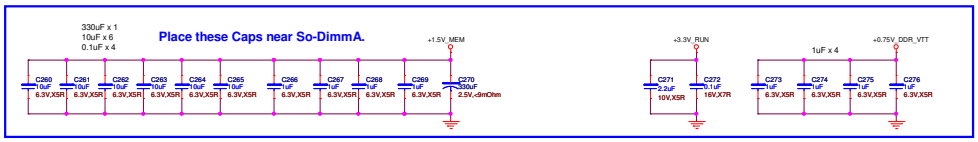
CHA_DIMM0_BOT_SIDE

JDIMM2 is RVS type.(H=60)



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector



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Title	14 -- SODIMM-204P-A0		
Size	Document Number: Thunder		Rev: 1A
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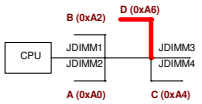
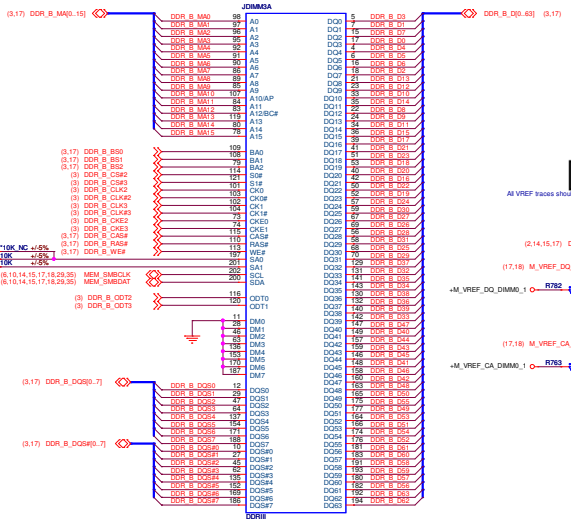
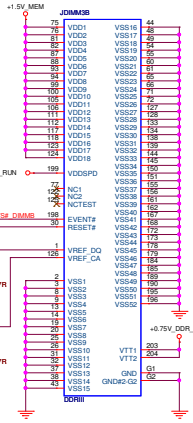
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



CHB_DIMM1_TOP_SIDE

JDIMM3 is STD type.





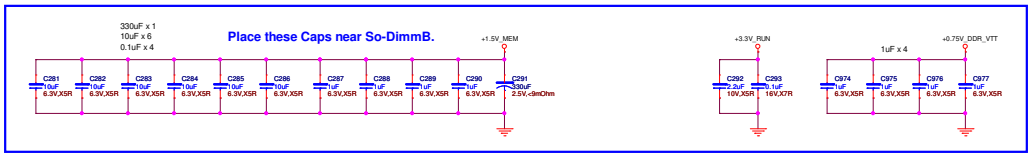
All VREF traces should have 10 mil trace width

Address:0xA6

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Place these Caps near So-DimmB.



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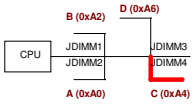
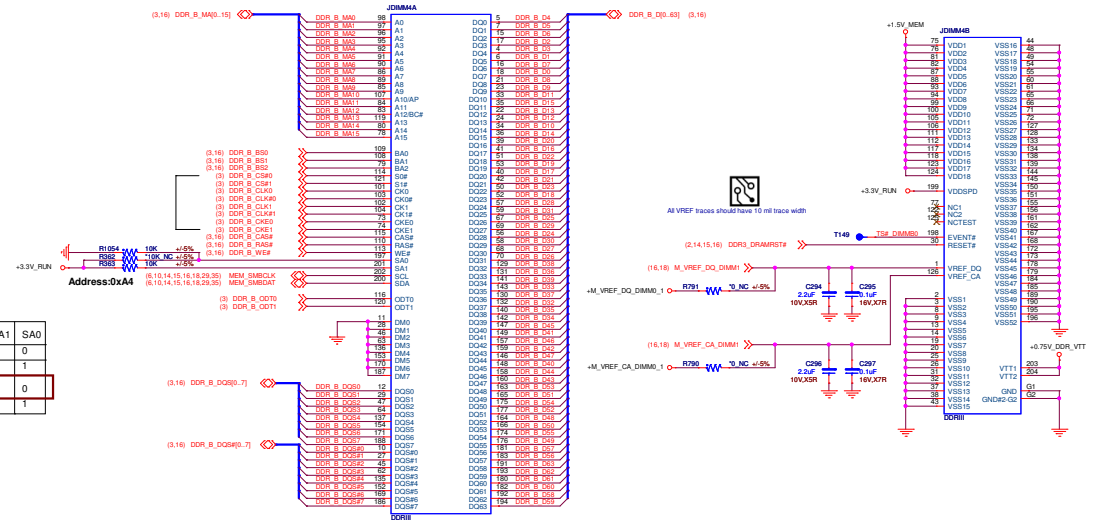
Title: 17 – SODIMM-204P-B0			
Size	Document Number: Thunder		Rev: 1A
Date: Thursday, January 27, 2011	Sheet 16 of 84		

DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



CHB_DIMM0_BOT_SIDE

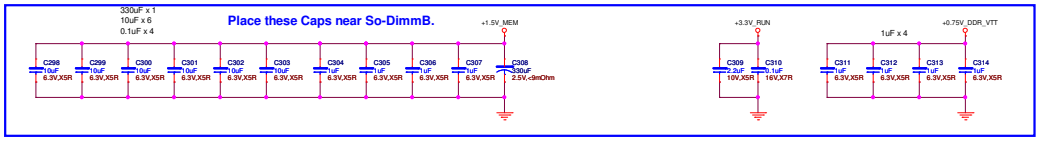
JDIMM4 is STD type.



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals
Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector

Place these Caps near So-DimmB.



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Title	16 -- SODIMM-204P-B0	
Size	Document Number: Thunder	Rev: 1A
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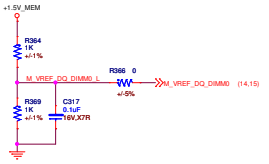
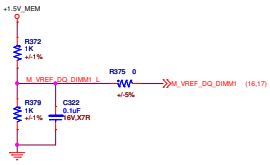
M1: Fixed SO-DIMM VREF_DQ (Default)

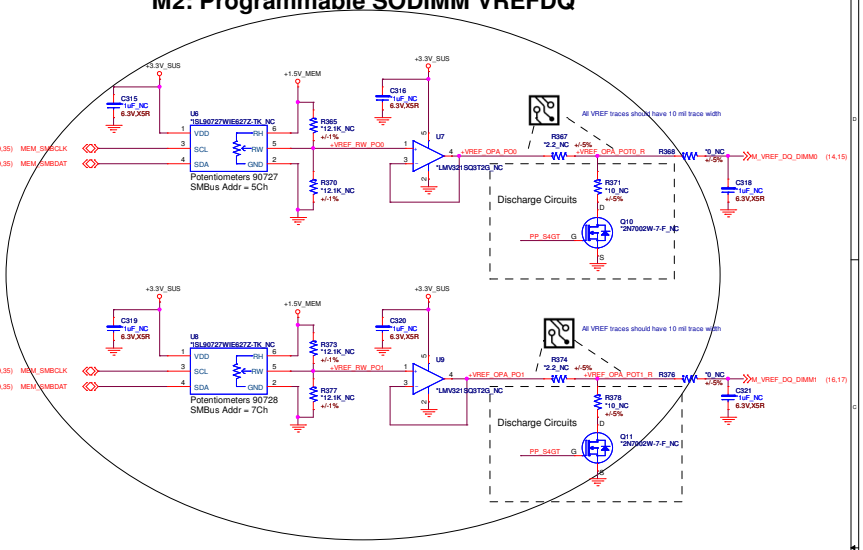


For CH A SO-DIMM VREF_DQ

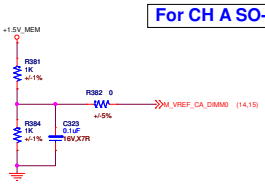


For CH B SO-DIMM VREF_DQ

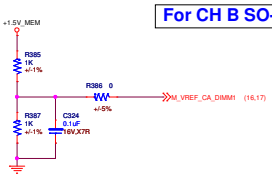
M2: Programmable SODIMM VREFDQ

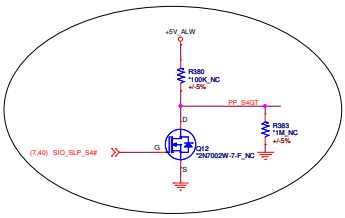


For CH A SO-DIMM VREF_CA



For CH B SO-DIMM VREF_CA





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Title	18 -- DDR3 VREF	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 18 of 84	

MXM 3.0 C0NNECTOR

MXM SPEC:
7~20V, Up to 10A

0607GC: CIS OK

2.5 A

PEX swing select
0: High swing
NC: Lowing swing

to 5048

CEC MXM Internal PU.

Mechanical Key

CONN-PCI-X

To GPIO module side is GND

GPU internal PU.

PEX_TX : connect to CPU TX
connect to MXM RX
PEX_RX : connect to CPU RX
connect to MXM TX

DOCK DP1
MB HDMI

MB DP Port

PU at PCH.

To GPIO module side is GND

DOCK DP2

1 A

From PCH

From 5048

1.Whole TX & RX AC decoupling Cap(64 pcs) need to place within 0.5" of MXM Conn
2.TX cap at CPU Side

MXM PEG SPEC
Length Low swing: 7 inches High swing: 10 inches

Thermal Trip

Thermal Alert

GPU internal PU.

GPU internal PU.

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Title	19 – MXM3.0 Connector	
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Title	20 – 17" eDP for PANEL	
Size	Document Number Thunder	Rev 1A
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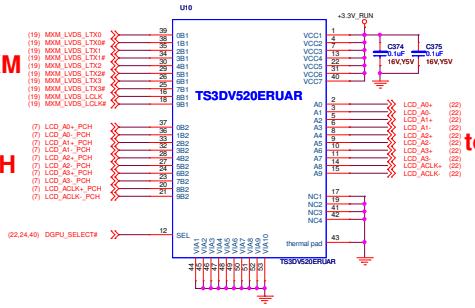
LVDS MUX for Panel

from MXM

from PCH

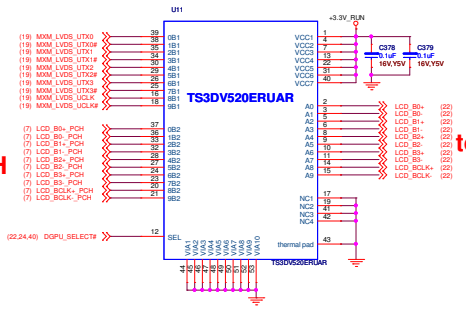


to Panel

SEL = L , Port B1 active.
SEL = H , Port B2 active.

from MXM

from PCH



to Panel

SEL = L , Port B1 active.
SEL = H , Port B2 active.

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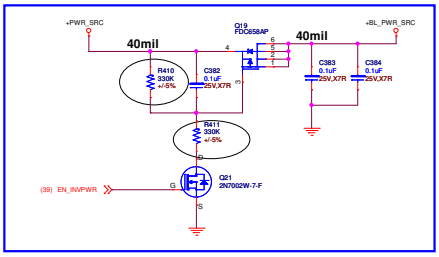
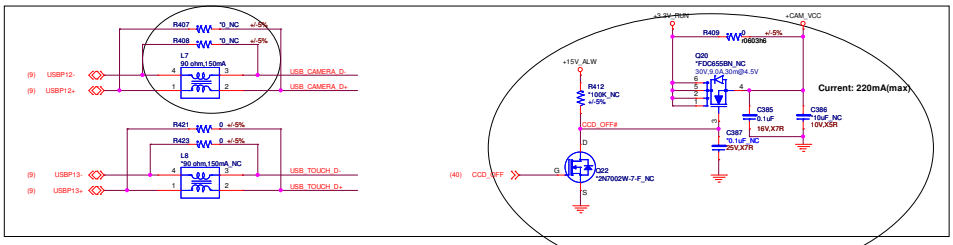
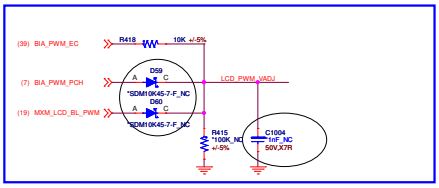
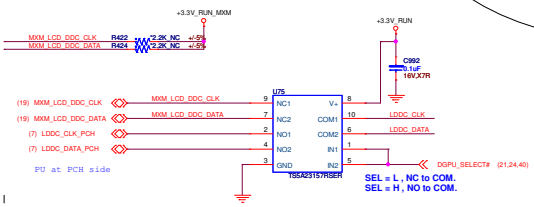
Title	21 -- LVDS MUX for PANEL	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 21 of 84	

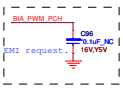

+PWR_SRC
40mil
Q19
FDC658AP
40mil
+BL_PWR_SRC
R418
330K
+/-5%
C382
0.1uF
25V,X7R
C383
0.1uF
25V,X7R
C384
0.1uF
25V,X7R
R411
330K
+/-5%
(39) EN_INVPWR
Q21
2N7002W-7-F

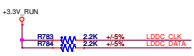

R407 *0_NC +/-5%
R408 *0_NC +/-5%
L7
90 ohm,150mA
(9) USBP12-
(9) USBP12+
USB_CAMERA_D-
USB_CAMERA_D+
R421 0 +/-5%
R423 0 +/-5%
L8
*90 ohm,150mA_NC
(9) USBP13-
(9) USBP13+
USB_TOUCH_D-
USB_TOUCH_D+

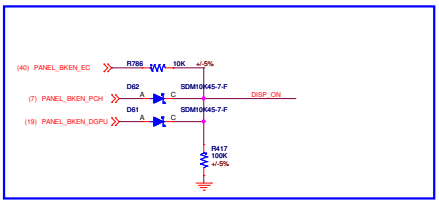
+3.3V_RUN
+CAM_VCC
R409 0 +/-5%
r0603hs
+15V_ALW
R412 *100K_NC +/-5%
Q20
*FDC655BN_NC
30V,9.0A,30m@4.5V
Current: 220mA(max)
C385 0.1uF 16V,X7R
C396 10uF_NC 10V,X5R
C387 *0.1uF_NC 25V,X7R
CCD_OFF#
(40) CCD_OFF
Q22
*2N7002W-7-F_NC


(39) BIA_PWM_EC
R418 10K +/-5%
D59
SDM10K45-7-F_NC
D60
SDM10K45-F_NC
(7) BIA_PWM_PCH
(19) MXM_LCD_BL_PWM
LCD_PWM_VADJ
R415 *100K_NC +/-5%
C1004 *1nF_NC 50V,X7R

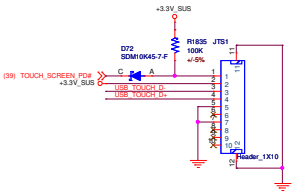

+3.3V_RUN_MXM
MXM_LCD_DDC_CLK R422 *2.2K_NC +/-5%
MXM_LCD_DDC_DATA R424 *2.2K_NC +/-5%
+3.3V_RUN
C992 0.1uF 16V,X7R
U75
(19) MXM_LCD_DDC_CLK
(19) MXM_LCD_DDC_DATA
(7) LDDC_CLK_PCH
(7) LDDC_DATA_PCH
NC1
NC2
NO1
NO2
GND
V+
COM1
COM2
IN1
IN2
LDDC_CLK
LDDC_DATA
DGPU_SELECT# (21,24,40)
TS5A23157RSER
PU at PCH side
SEL = L , NC to COM.
SEL = H , NO to COM.

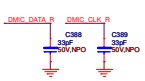

BIA_PWM_PCH
EMI request.
C86 *0.1uF_NC 16V,Y5V

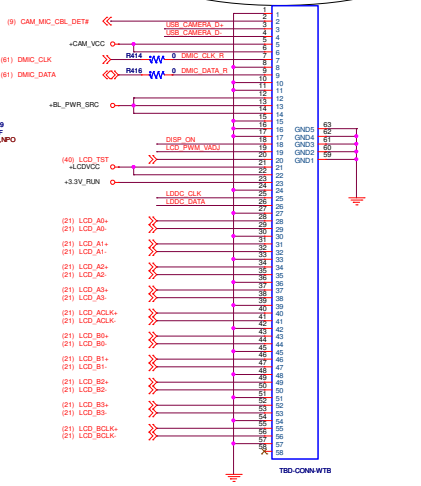

+3.3V_RUN
R783 2.2K +/-5%
R784 2.2K +/-5%
LDDC_CLK
LDDC_DATA

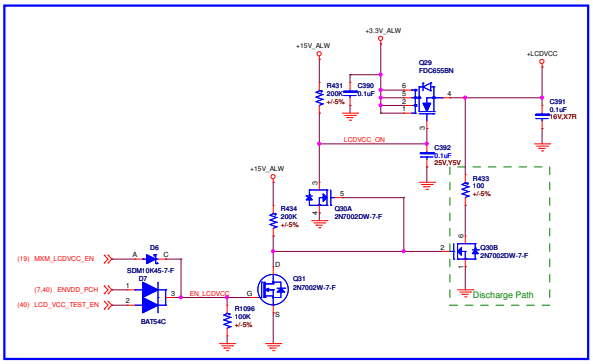

(40) PANEL_BKEN_EC
R786 10K +/-5%
D62
SDM10K45-7-F
(7) PANEL_BKEN_PCH
DISP_ON
D61
SDM10K45-7-F
(19) PANEL_BKEN_DGPU
R417 100K +/-5%


LVDS
0817GC: Need to update CIS.
cable loopback


+3.3V_SUS
R1635 100K +/-5%
D72
SDM10K45-7-F
(39) TOUCH_SCREEN_PD#
+3.3V_SUS
USB_TOUCH_D-
USB_TOUCH_D+
JTS1
Header_1X10


DMIC_DATA_R
DMIC_CLK_R
C388 33pF 50V,NPO
C389 33pF 50V,NPO


JLVDS1
(9) CAM_MIC_CBL_DET#
USB_CAMERA_D+
USB_CAMERA_D-
+CAM_VCC
(61) DMIC_CLK
(61) DMIC_DATA
R414 0 DMIC_CLK_R
R416 0 DMIC_DATA_R
+BL_PWR_SRC
DISP_ON
LCD_PWM_VADJ
(40) LCD_TST
+LCDVCC
+3.3V_RUN
LDDC_CLK
LDDC_DATA
(21) LCD_A0+
(21) LCD_A0-
(21) LCD_A1+
(21) LCD_A1-
(21) LCD_A2+
(21) LCD_A2-
(21) LCD_A3+
(21) LCD_A3-
(21) LCD_ACLK+
(21) LCD_ACLK-
(21) LCD_B0+
(21) LCD_B0-
(21) LCD_B1+
(21) LCD_B1-
(21) LCD_B2+
(21) LCD_B2-
(21) LCD_B3+
(21) LCD_B3-
(21) LCD_BCLK+
(21) LCD_BCLK-
GND5
GND4
GND3
GND2
GND1
TBD-CONN-WTB


+15V_ALW
+3.3V_ALW
+LCDVCC
Q29
FDC655BN
R431 200K +/-5%
C390 0.1uF
C391 0.1uF 16V,X7R
LCDVCC_ON
C392 1uF 25V,Y5V
+15V_ALW
R434 200K +/-5%
Q30A
2N7002DW-7-F
R433 100 +/-5%
Q30B
2N7002DW-7-F
(19) MXM_LCDVCC_EN
D6
SDM10K45-7-F
D7
BAT54C
(7,40) ENVDD_PCH
(40) LCD_VCC_TEST_EN
EN_LCDVCC
Q31
2N7002W-7-F
R1096 100K +/-5%
Discharge Path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Title
22 -- LCD,Camera,Touch Conn
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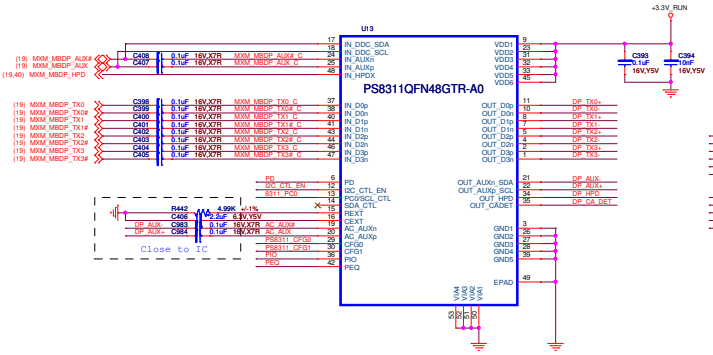
From dGPU Direct



PC0 : Internal pull down 150k
L : automatic equalization enable
H : automatic equalization disable

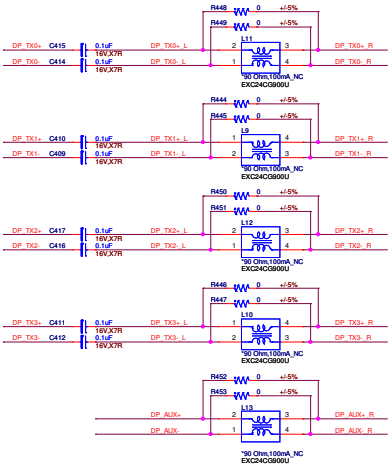
PD : Power down control, Internal pull down 150k
L : Normal operation
H : Chip power down

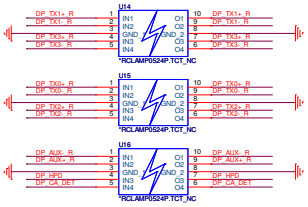
PIO :
Internal pull down 150k
L : IN_HPDX=OUT_HPD, 3.3V CMOS output
H : IN_HPDX=OUT_HPD#, inverted HPD, 0.9V output

I2C_CTL_EN :
Internal pull down 150k
LOW : PIN control
HIGH : I2C control

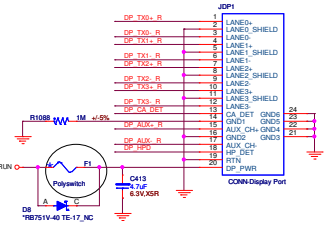
Chip operation mode, Internal pull down 150k
CFG0
L : AUX CH is off when chip is in automatic power down
H : AUX CH is operational when chip is in automatic power down
CFG1
L : Normal AUX interception operation
H : AUX interception with fixed output swing of 600mV and no pre-emphasis

PEQ : Programmable input equalization level pre-setting
Internal pull down 150k
L : Low RX EQ setting (LEQ)
H : High RX EQ setting (HEQ)





0524GC:CIS OK



Ever Light Technology Limited			
Title: 22 – Display Port & Re-Driver			
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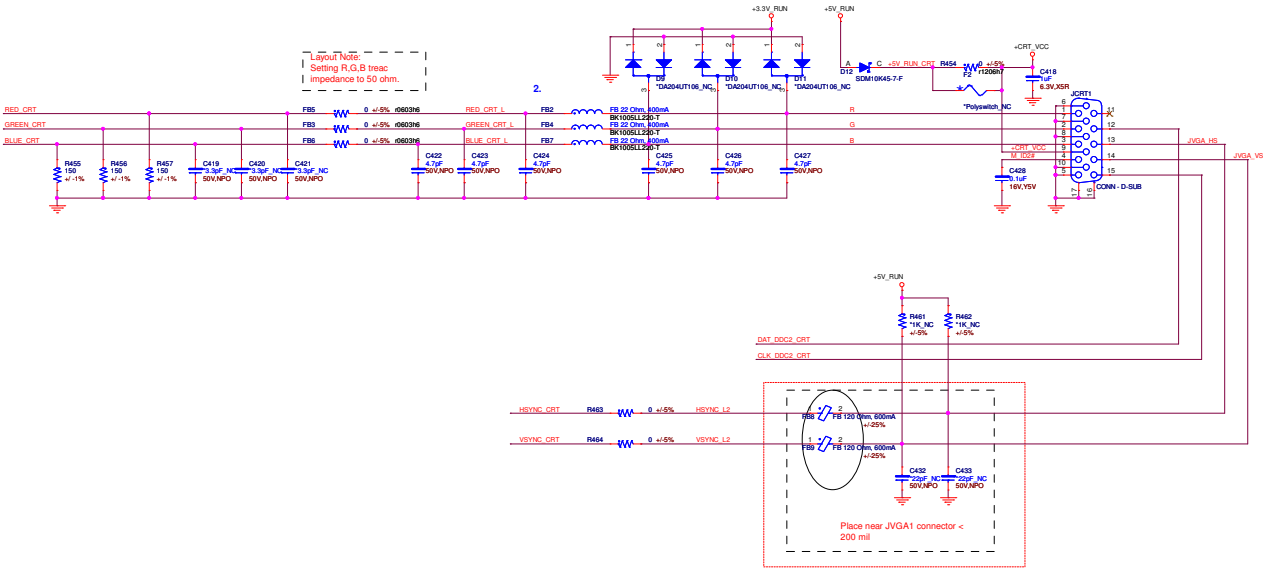
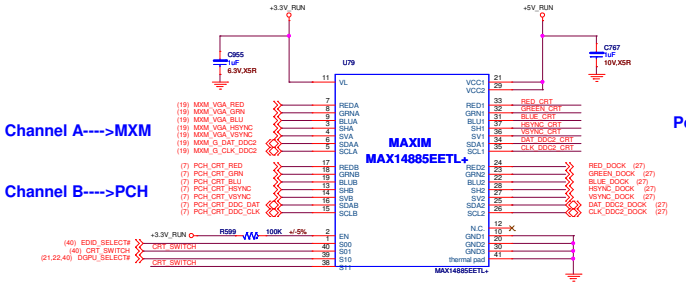
CRT





Truth table

	A-->Port 1	B-->Port 1	A-->Port 2	B-->Port 2
S01/S11 (CRT_SWITCH)	0	0	1	1
S10 (DGPU_SELECT#)	0	1	0	1
S00 (EDID_SELECT#)	0	1	0	1

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Title	23 -- CRT & MUX	
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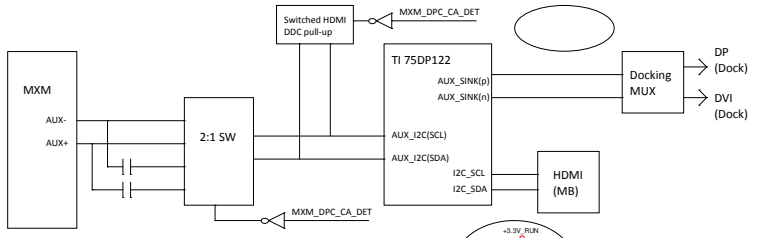
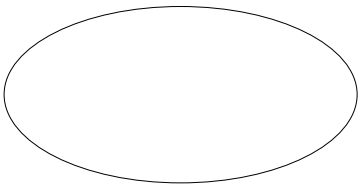
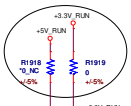
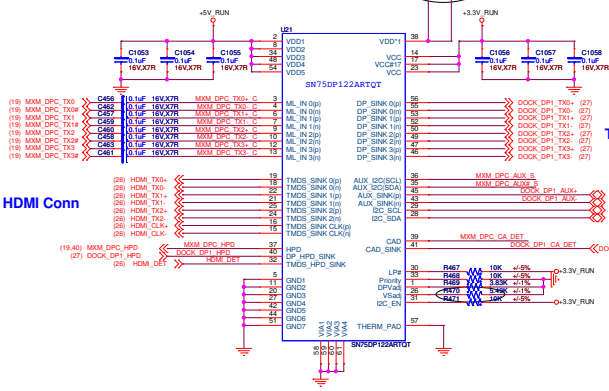




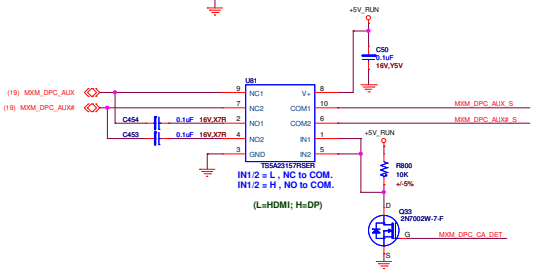


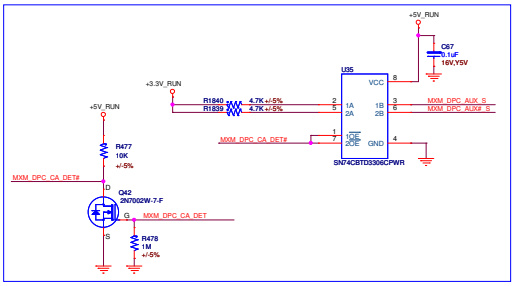
From dGPU



To Docking DP1 Port

TO MB HDMI Conn





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Title	24 -- MUX for HDMI		
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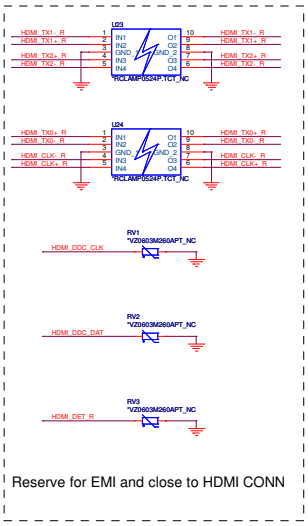
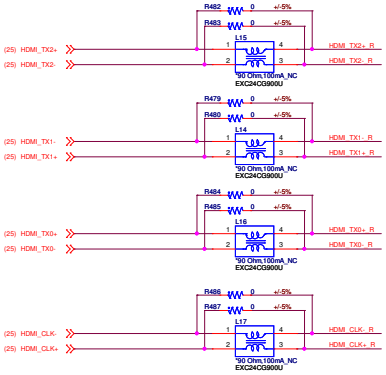
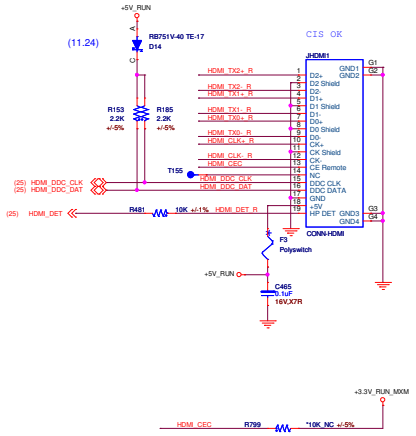
HDMI CONN



Reserve for EMI and close to HDMI CONN





Ever Light Technology Limited

Title	25 -- HDMI	
Size	Document Number: Thunder	Rev: 1A
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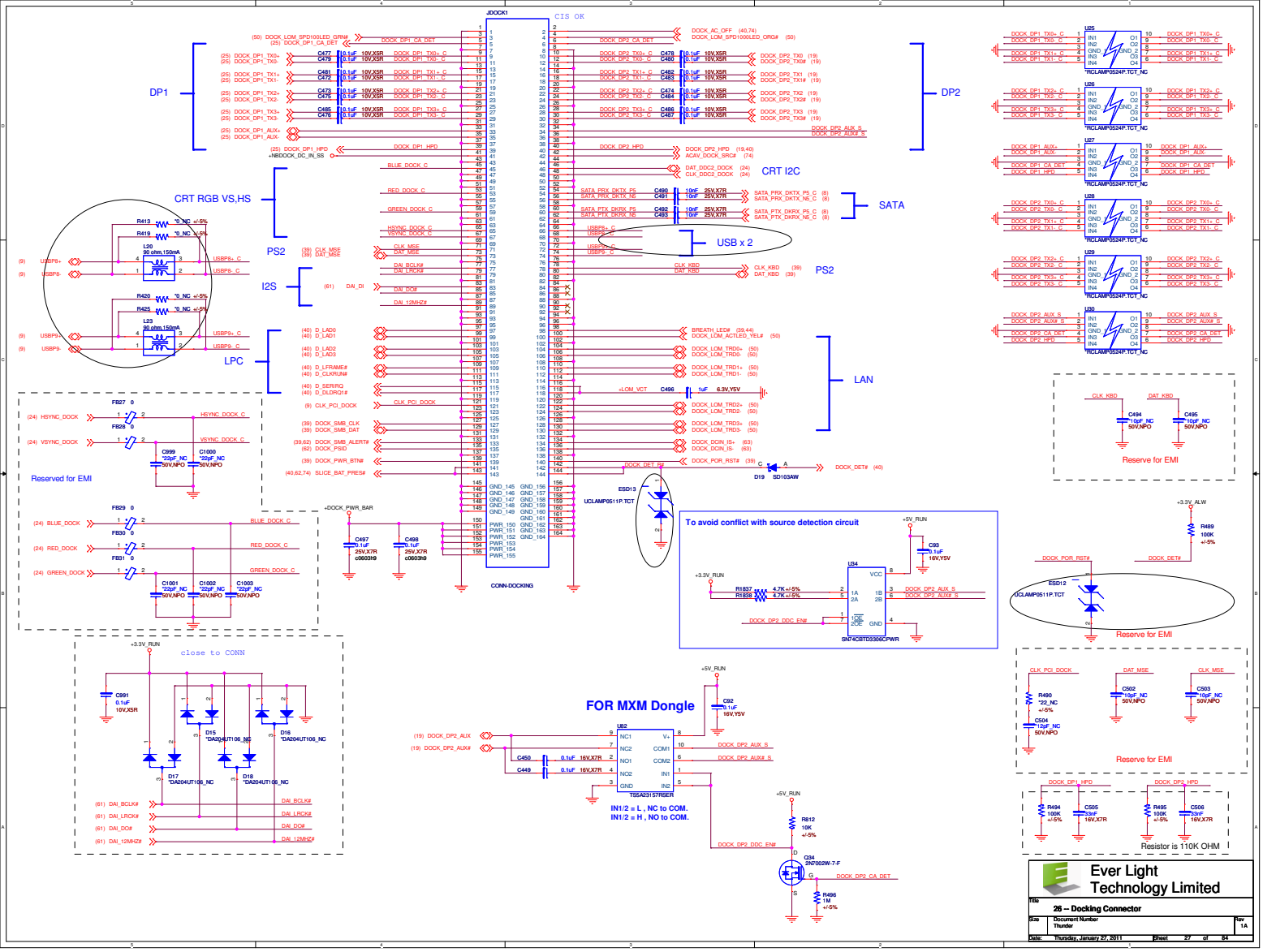
JDOCK1
CIS OK
DP1
DP2
CRT RGB VS,HS
CRT I2C
SATA
PS2
USB x 2
I2S
LPC
LAN
Reserved for EMI
CONN-DOCKING
ESD13
UCLAMP0511P.TCT
To avoid conflict with source detection circuit
SN74CBTD3306CPWR
FOR MXM Dongle
TS5A23157RSER
IN1/2 = L , NC to COM.
IN1/2 = H , NO to COM.
close to CONN
Reserve for EMI
Resistor is 110K OHM
Ever Light Technology Limited
26 -- Docking Connector
Document Number
Thunder
Rev 1A
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Ever Light
Technology Limited

Title	28 – 17" HDD, ODD, G-SENSOR	
Size	Document Number Thunder	Rev 1A
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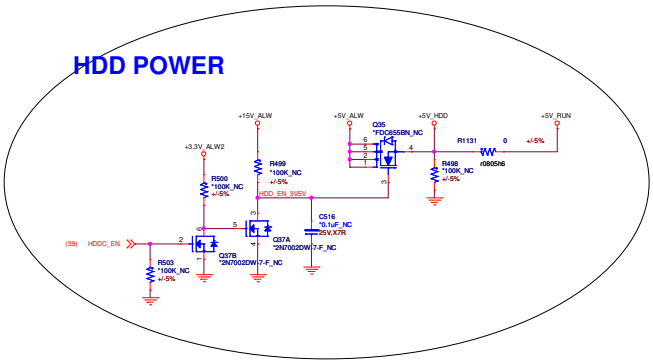
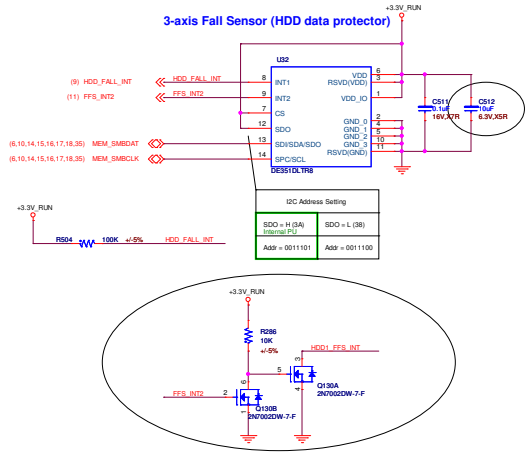
HDD POWER

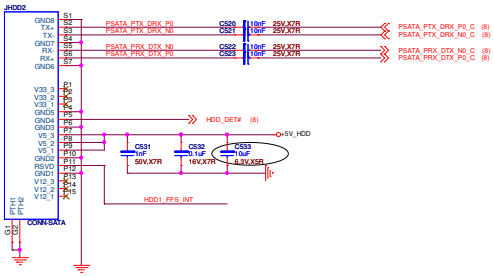


3-axis Fall Sensor (HDD data protector)

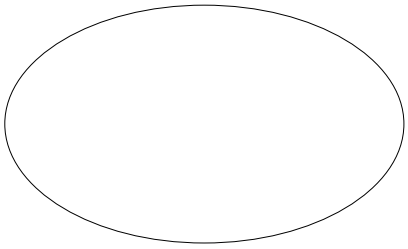


HDD Connector

Main HDD

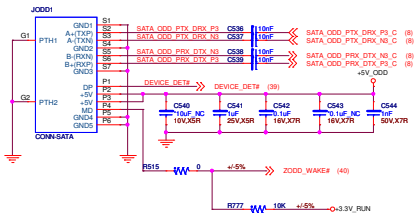


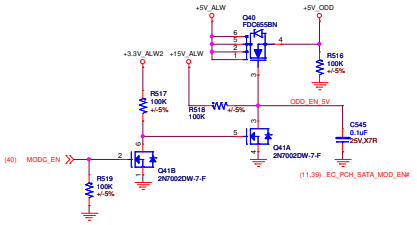
SATA3 Re-Driver For main HDD

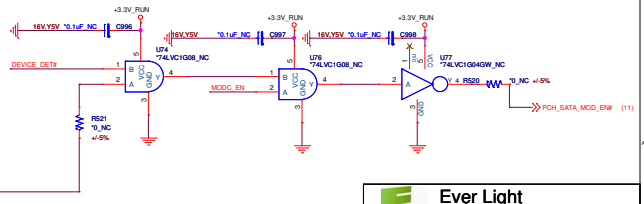


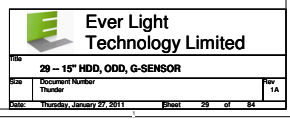
ODD Connector

SATA port 3

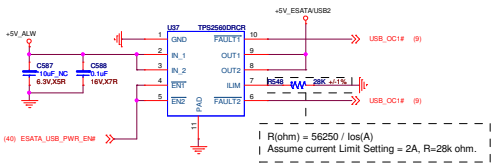


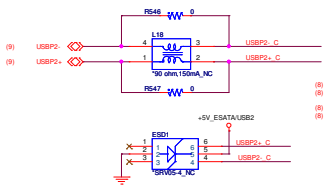






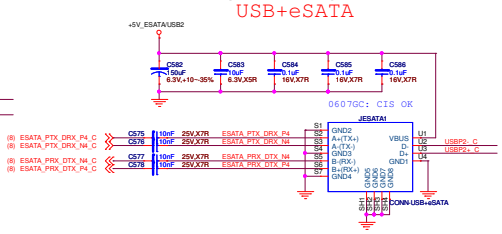
USB Power





USB(Back Side)

USB+eSATA



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Title	29 -- eSATA/USB, USB x 2	
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Note:
1. Every Power trace (3.3V, 1.05V, A0,3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly - by tracing shortly and broadly.
5. For signal traces, routing priority is as follows; USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
   > Remove any impairment or discontinuity.
   > Keep same length by each other.
   > Keep same width and spacing.

For more information please refer to 'USB3.0 Board Design Guide' in design kit.

uPD720200

USB3.0 Trace need routing 90-ohms Diff

USB3.0 Trace need routing 90-ohms Diff

Power on Reset

uPD720200 : Pop R563, De-pop R584
uPD720200A : Pop R584, De-pop R563

Put R2 close to U1
Short and broad connection to GND
Don't split R2 into multiple resistors.

0 : 24MHz Crystal
1 : 48MHz clock in

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Title	30 -- NEC USB 3.0 Chip & Power
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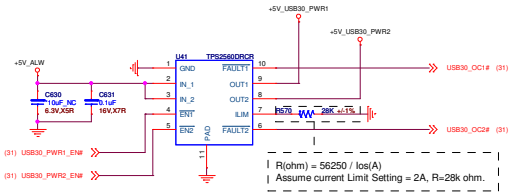

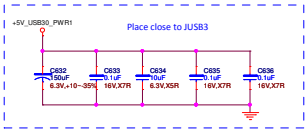

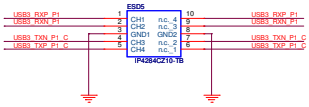

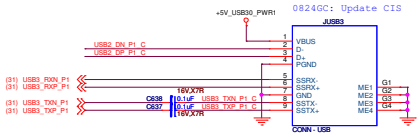

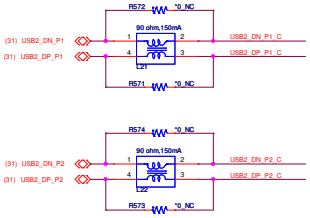

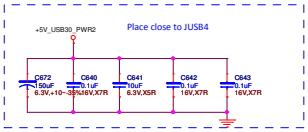

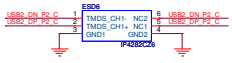

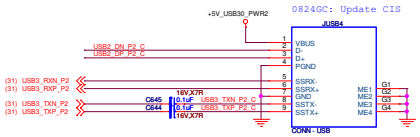

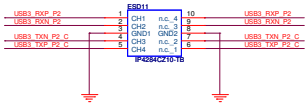

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Title	31 -- USB 3.0 Connector x 2	
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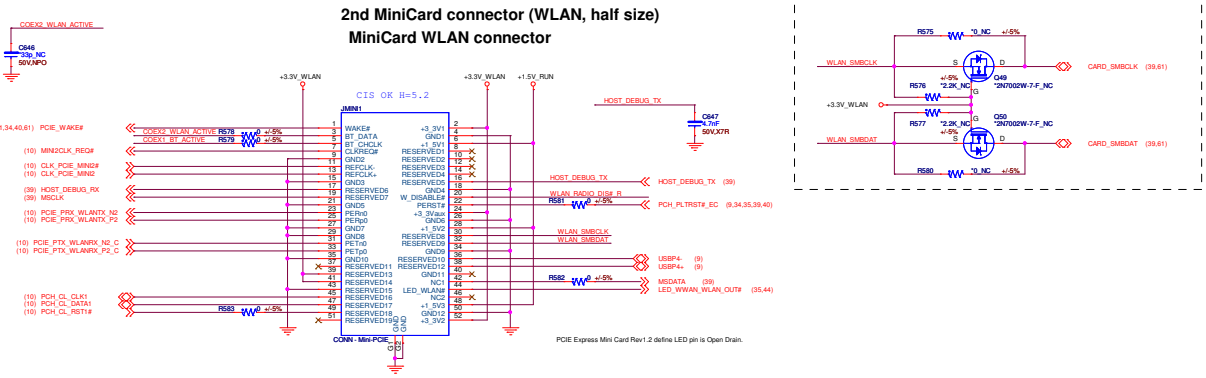
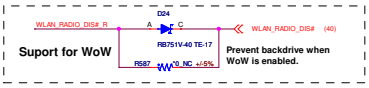
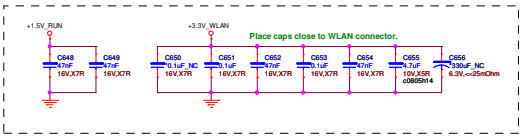
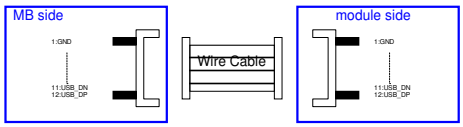
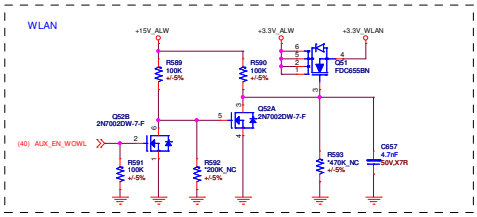
2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector

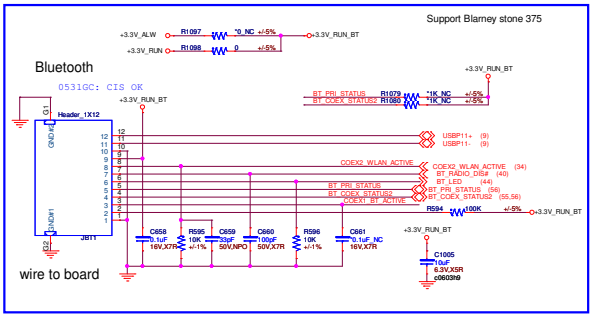


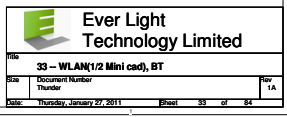




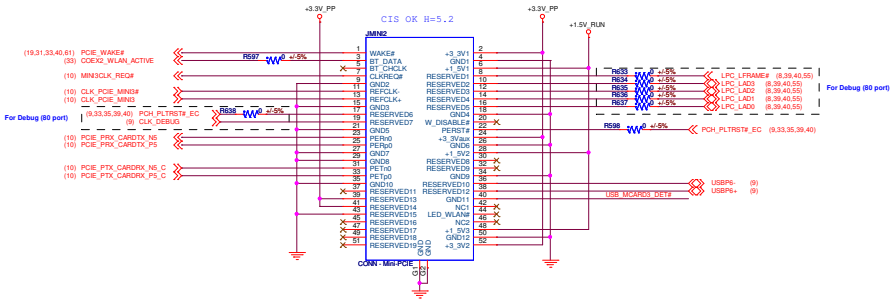


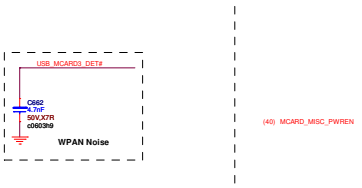


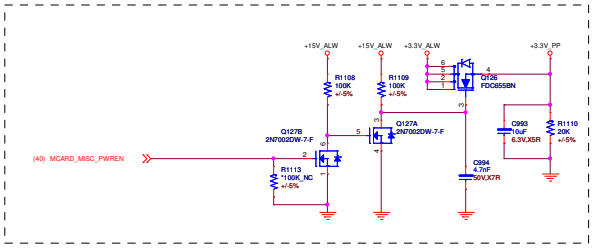


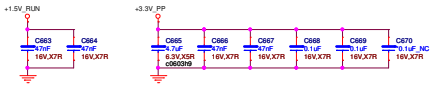


3rd MiniCard connector (Flash, half size)
MiniCard connector









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Title	34 -- Flash /PP(1/2Mini cad)	
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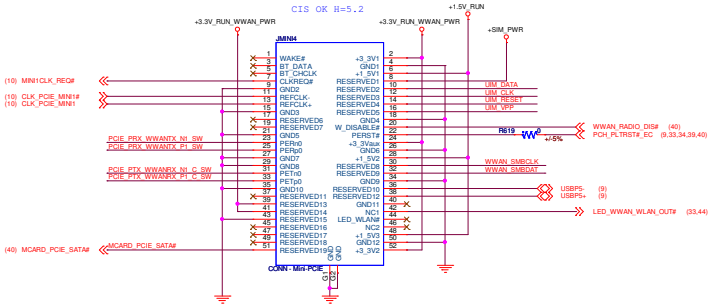
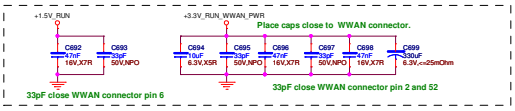
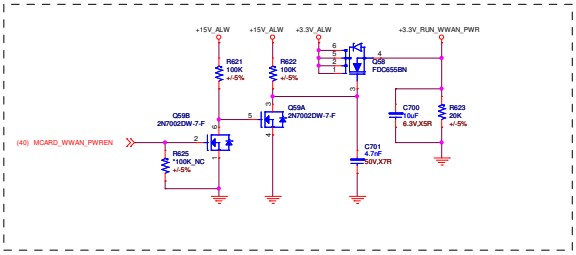
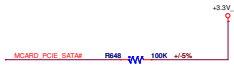
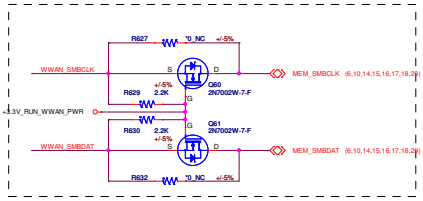
MiniCard WWAN connector

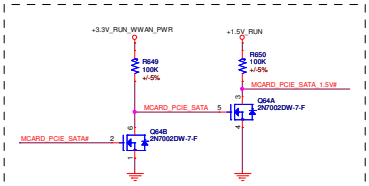






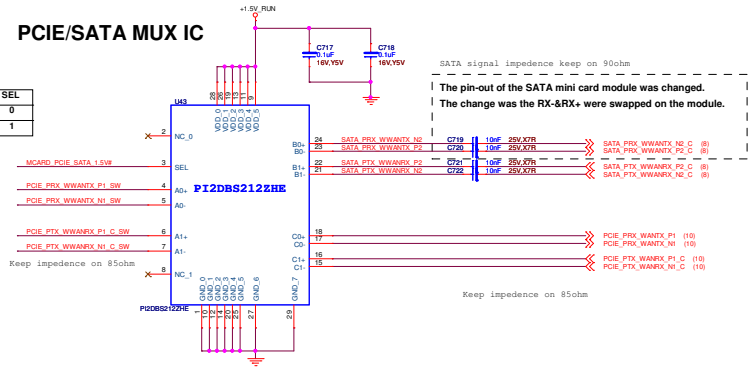




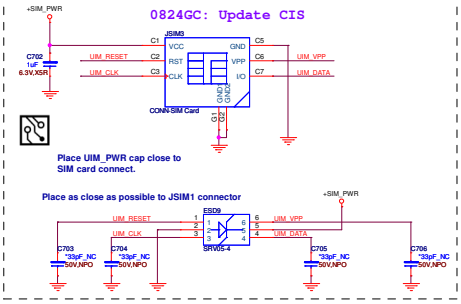


PCIE/SATA MUX IC

Function	SEL
Port A to Port B	0
Port A to Port C	1



SIM CARD



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
	+-9%	330	250	250 (wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

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Title	35 -- 15" WWAN+ SIM+MUX		
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Title	36 -- 17" WWAN+ SIM	
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Title	37 – 17" NVRAM+MUX	
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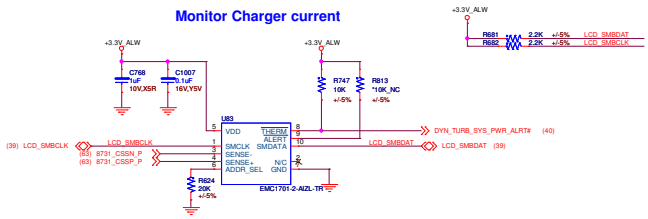
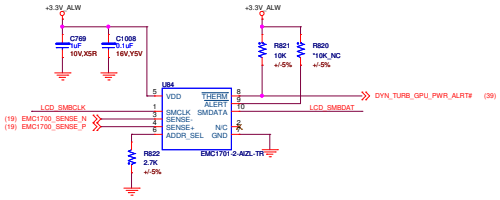
Monitor Charger current



RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS	
0	1001_100(r/w)	1600	0101_000(r/w)	
100	1001_101(r/w)	2000	0101_001(r/w)	
180	1001_110(r/w)	2700	0101_010(r/w)	U84
300	1001_111(r/w)	3600	0101_011(r/w)	
430	1001_000(r/w)	5600	0101_100(r/w)	
560	1001_001(r/w)	9100	0101_100(r/w)	
750	1001_010(r/w)	20000	0101_101(r/w)	U83
1270	1001_011(r/w)	Open	0111_000(r/w)	

Monitor PWR_SRC_MXM



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Title	38 -- Express Card & Power	
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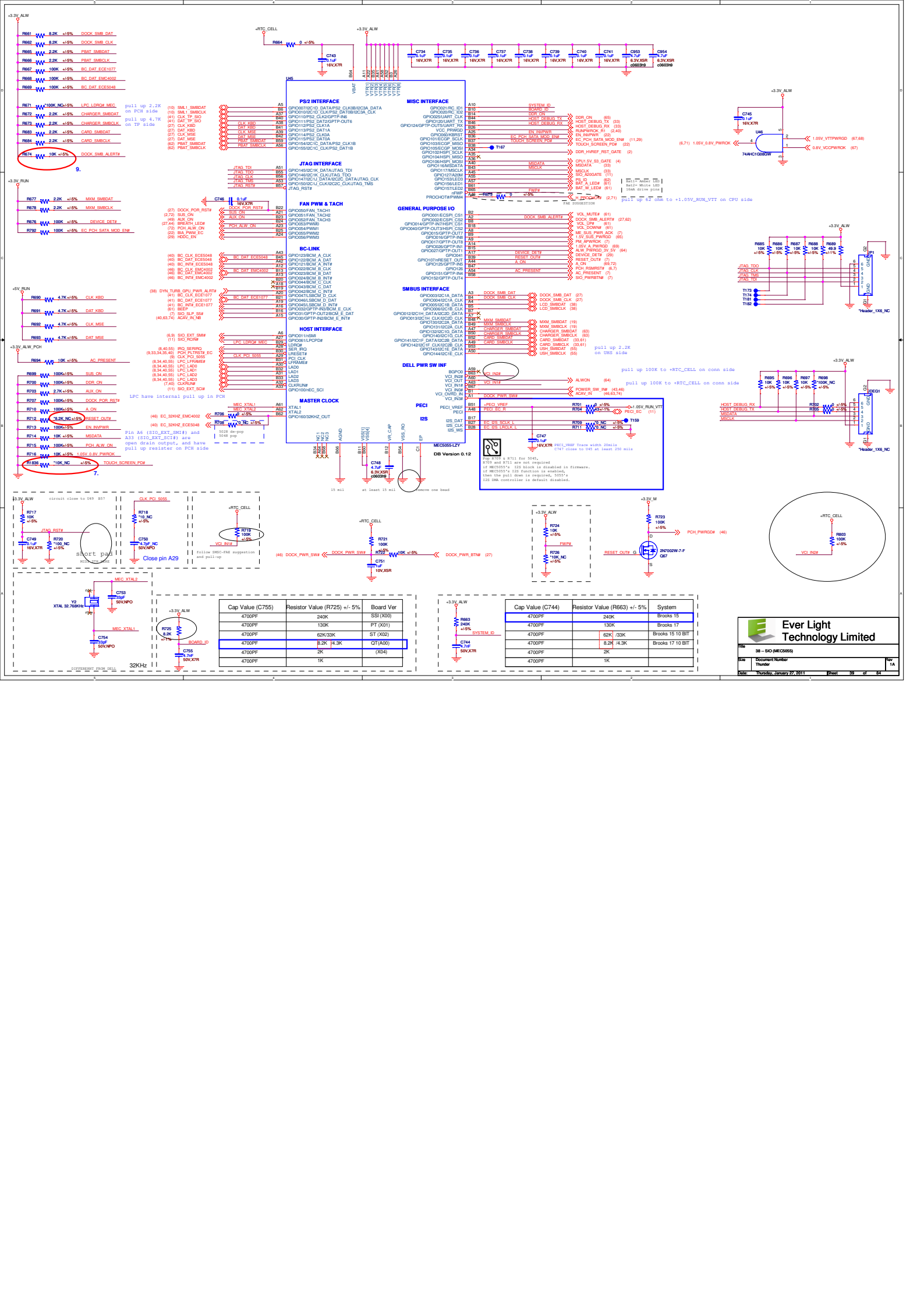
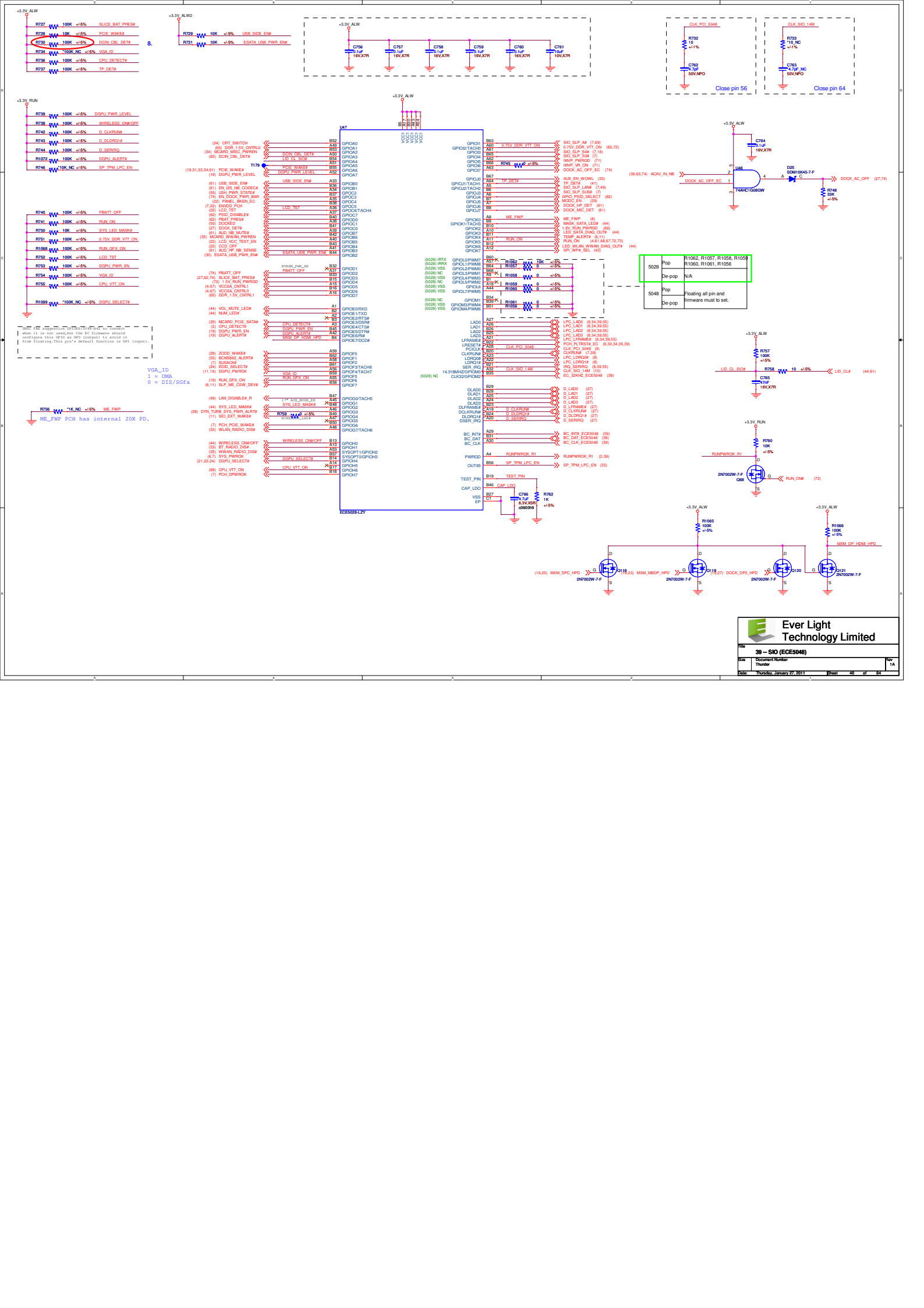


Cap Value (C755)	Resistor Value (R725) +/- 5%	Board Ver
4700PF	240K	SSI (X00)
4700PF	130K	PT (X01)
4700PF	62K/33K	ST (X02)
4700PF	8.2K /4.3K	QT(A00)
4700PF	2K	(X04)
4700PF	1K	

Cap Value (C744)	Resistor Value (R663) +/- 5%	System
4700PF	240K	Brooks 15
4700PF	130K	Brooks 17
4700PF	62K /33K	Brooks 15 10 BIT
4700PF	8.2K /4.3K	Brooks 17 10 BIT
4700PF	2K	
4700PF	1K	



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Title	39 -- SIO (ECE5048)
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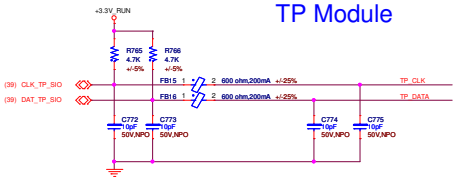
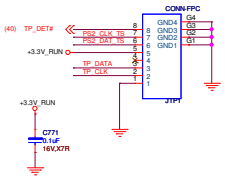
TP Module

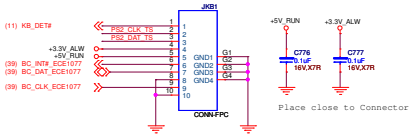


0524GC: CIS OK



Keyboard Module

1116: update to CIS.



Place close to Connector

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Title	40 -- ECE1099+KB+TP		
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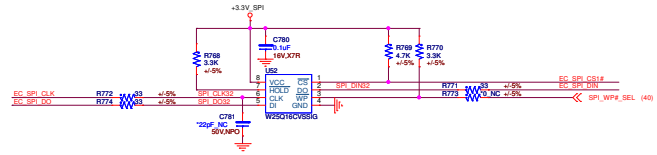
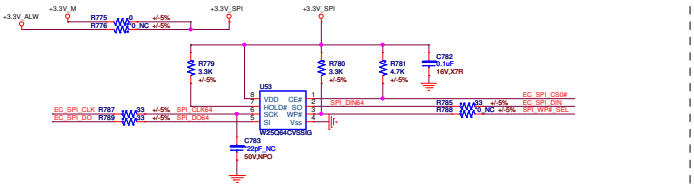
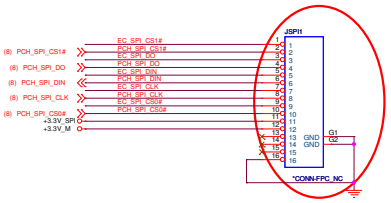
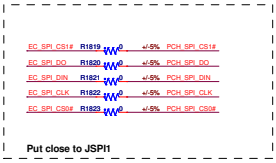
PCH, EC SPI ROM For BIOS (2M Byte)



PCH SPI ROM For iAMT (8M Byte)







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Title	41 -- BIOS ROM(4M+8M)	
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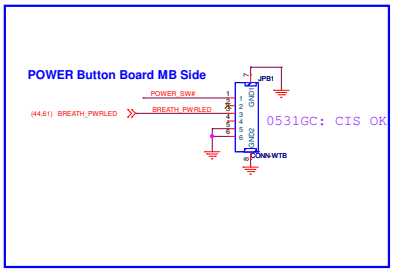

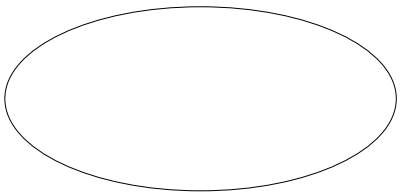

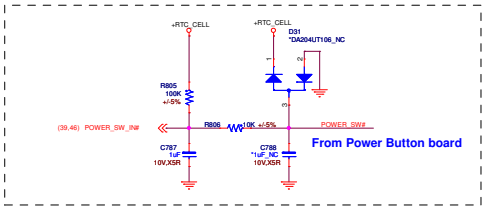

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Title	43 -- DB Connector x 7	
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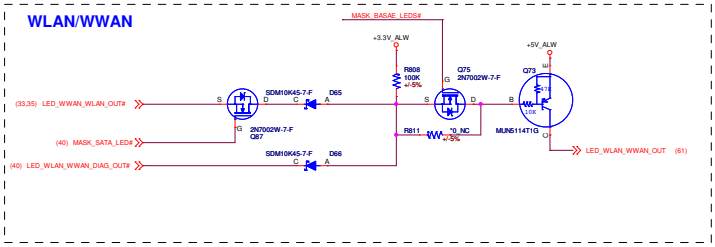
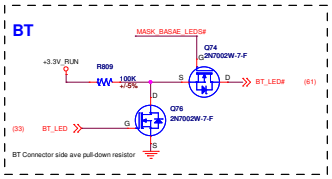
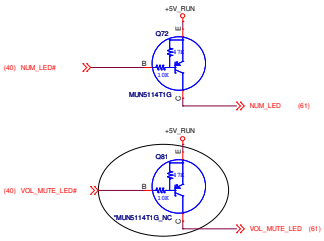
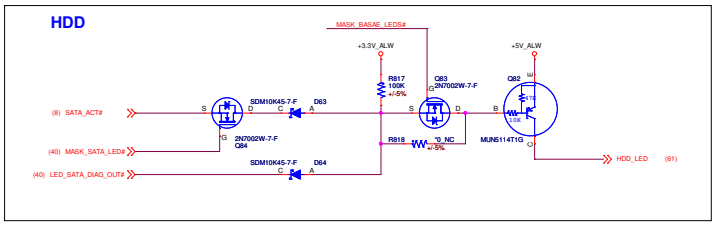
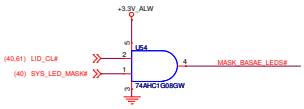
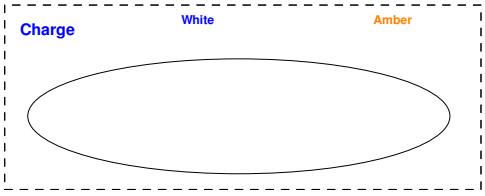

WLAN/WWAN
MASK_BASAE_LEDS#
+3.3V_ALW
+5V_ALW
R808
100K
+/-5%
Q75
2N7002W-7-F
Q73
MUN5114T1G
(33,35) LED_WWAN_WLAN_OUT#
SDM10K45-7-F
D65
2N7002W-7-F
Q87
(40) MASK_SATA_LED#
SDM10K45-7-F
D66
(40) LED_WLAN_WWAN_DIAG_OUT#
R811
*0_NC
+/-5%
LED_WLAN_WWAN_OUT (61)

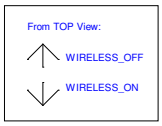

BT
MASK_BASAE_LEDS#
+3.3V_RUN
R809
100K
+/-5%
Q74
2N7002W-7-F
BT_LED# (61)
Q76
2N7002W-7-F
(33) BT_LED
BT Connector side ave pull-down resistor

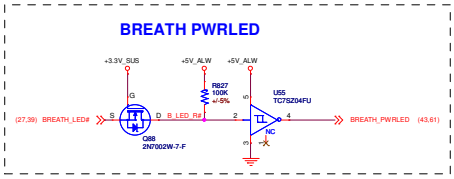

+5V_RUN
Q72
(40) NUM_LED#
MUN5114T1G
NUM_LED (61)
+5V_RUN
Q81
(40) VOL_MUTE_LED#
MUN5114T1G_NC
VOL_MUTE_LED (61)

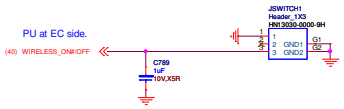

HDD
MASK_BASAE_LEDS#
+3.3V_ALW
+5V_ALW
R817
100K
+/-5%
Q83
2N7002W-7-F
Q82
MUN5114T1G
(8) SATA_ACT#
SDM10K45-7-F
D63
2N7002W-7-F
Q84
(40) MASK_SATA_LED#
SDM10K45-7-F
D64
(40) LED_SATA_DIAG_OUT#
R818
*0_NC
+/-5%
HDD_LED (61)

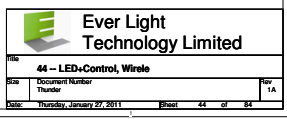

+3.3V_ALW
U54
(40,61) LID_CL#
(40) SYS_LED_MASK#
MASK_BASAE_LEDS#
74AHC1G08GW


Charge
White
Amber


From TOP View:
WIRELESS_OFF
WIRELESS_ON


BREATH PWRLED
+3.3V_SUS
+5V_ALW
+5V_ALW
R827
100K
+/-5%
U55
TC7SZ04FU
Q88
2N7002W-7-F
(27,39) BREATH_LED#
B_LED_R#
BREATH_PWRLED (43,61)


PU at EC side.
JSWITCH1
Header_1X3
HH13033-0000-9H
(40) WIRELESS_ON#/OFF
C789
1uF
10V,X5R
GND1
GND2


Ever Light
Technology Limited
Title
44 -- LED+Control, Wirele
Size
Document Number
Thunder
Rev
1A
Date:
Thursday, January 27, 2011
Sheet
44
of
84

Remove IOL Board

Ever Light Technology Limited

Title	45 -- Hall sensor	
Size	Document Number: Thunder	Rev: 1A
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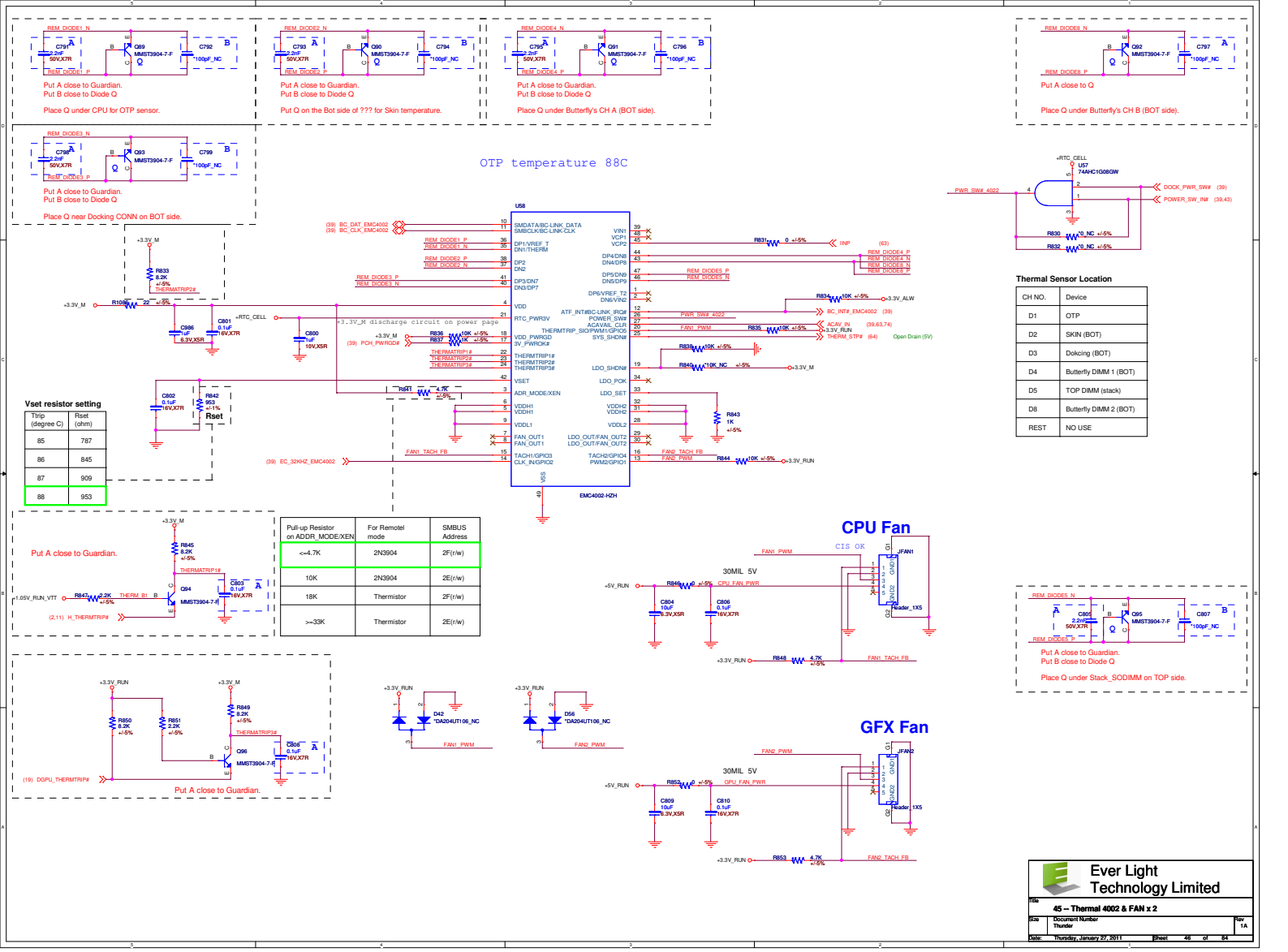
REM_DIODE1_N
C791 2.2nF 50V,X7R
Q89 MMST3904-7-F
C792 *100pF_NC
REM_DIODE1_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under CPU for OTP sensor.
REM_DIODE2_N
C793 2.2nF 50V,X7R
Q90 MMST3904-7-F
C794 *100pF_NC
REM_DIODE2_P
Put A close to Guardian.
Put B close to Diode Q
Put Q on the Bot side of ??? for Skin temperature.
REM_DIODE4_N
C795 2.2nF 50V,X7R
Q91 MMST3904-7-F
C796 *100pF_NC
REM_DIODE4_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Butterfly's CH A (BOT side).
REM_DIODE5_N
C792 *100pF_NC
REM_DIODE5_P
Put A close to Q
Place Q under Butterfly's CH B (BOT side).
REM_DIODE3_N
C798 2.2nF 50V,X7R
Q93 MMST3904-7-F
C799 *100pF_NC
REM_DIODE3_P
Put A close to Guardian.
Put B close to Diode Q
Place Q near Docking CONN on BOT side.
OTP temperature 88C
U58
EMC4002-HZH
+3.3V_M discharge circuit on power page
Vset resistor setting
Trip (degree C) / Rset (ohm)
85 787
86 845
87 909
88 953
Rset
Pull-up Resistor on ADDR_MODE/XEN / For Remotel mode / SMBUS Address
<=4.7K 2N3904 2F(r/w)
10K 2N3904 2E(r/w)
18K Thermistor 2F(r/w)
>=33K Thermistor 2E(r/w)
Put A close to Guardian.
Put A close to Guardian.
CPU Fan
GFX Fan
30MIL 5V
CIS OK
JFAN1
JFAN2
Header_1X5
D42 *DA204UT106_NC
D56 *DA204UT106_NC
U57 74AHC1G08GW
PWR_SW# 4022
DOCK_PWR_SW# (39)
POWER_SW_IN# (39,43)
Thermal Sensor Location
CH NO. / Device
D1 OTP
D2 SKIN (BOT)
D3 Dokcing (BOT)
D4 Butterfly DIMM 1 (BOT)
D5 TOP DIMM (stack)
D8 Butterfly DIMM 2 (BOT)
REST NO USE
REM_DIODE6_N
C805 2.2nF 50V,X7R
Q95 MMST3904-7-F
C807 *100pF_NC
REM_DIODE6_P
Put A close to Guardian.
Put B close to Diode Q
Place Q under Stack_SODIMM on TOP side.
Ever Light Technology Limited
Title: 45 -- Thermal 4002 & FAN x 2
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Move to IOL board

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Technology Limited

Title	47 -- AUDIO(92HD90B)+SPK+JACK	
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Move to IOL board

Ever Light Technology Limited

Title	48 -- AUDIO for Docking+Crystal	
Size	Document Number: Thunder	Rev: 1A
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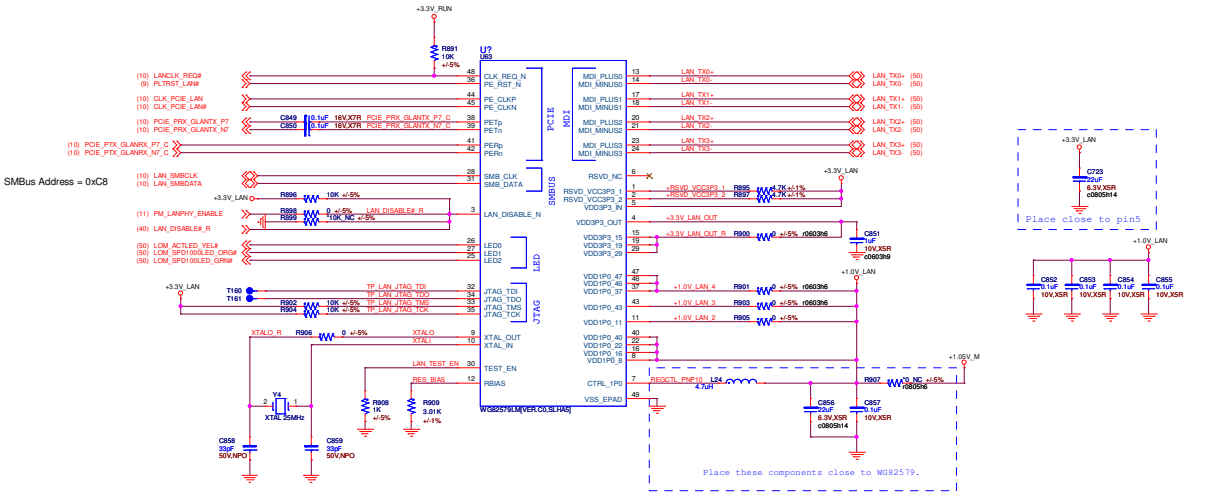
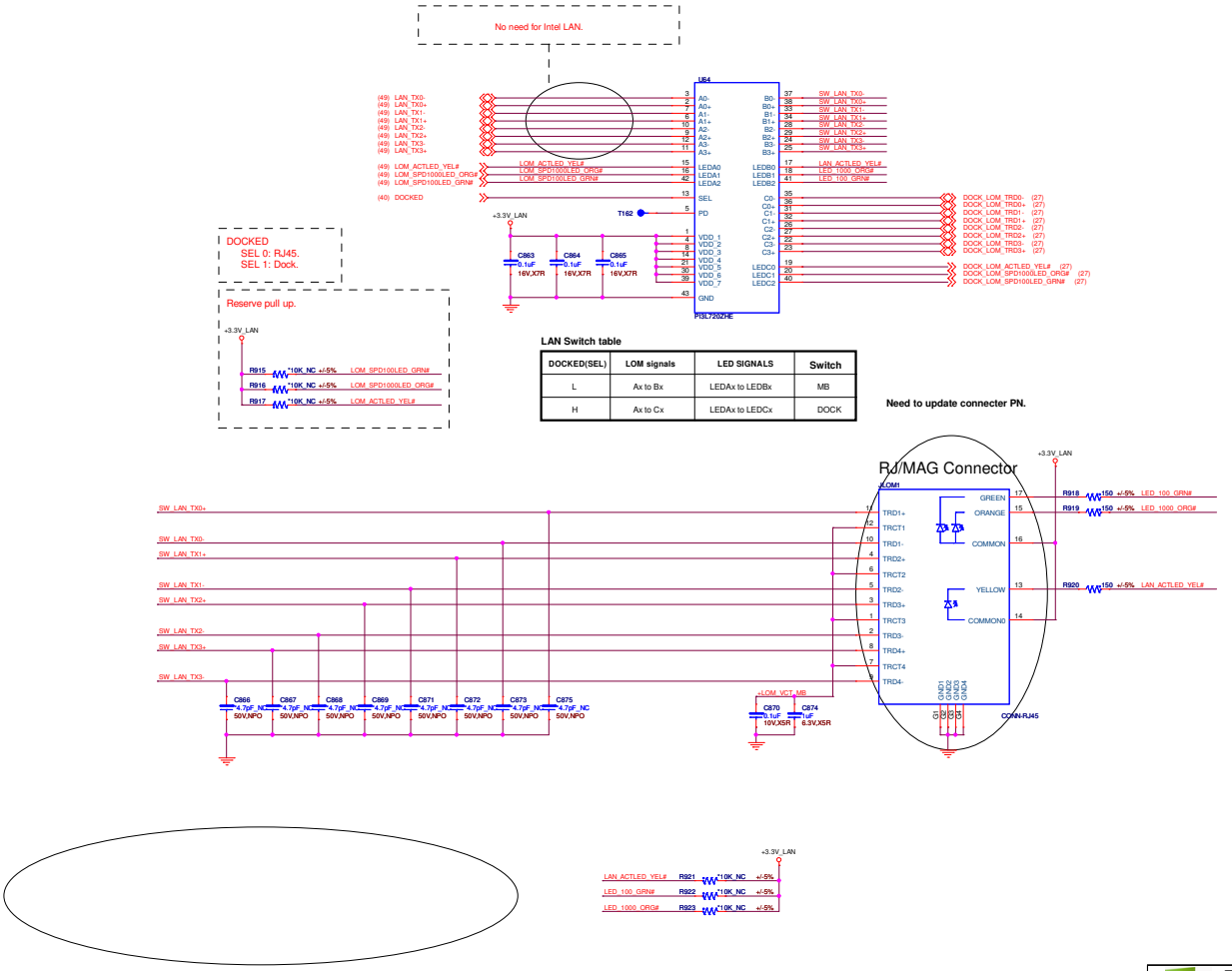


Ever Light Technology Limited	
Title	48 -- LOM 82579
Size	Document Number: Thunder; Rev: 1A
Date: Thursday, January 27, 2011	Sheet 49 of 84



LAN Switch table

DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LEDAx to LEDBx	MB
H	Ax to Cx	LEDAx to LEDCx	DOCK

Need to update connecter PN.

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Title	49 -- RJ45+MID, MUX Switch	
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Title	50 – TPM for China	
Size	Document Number Thunder	Rev 1A
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Move to IOL board

Ever Light Technology Limited

Title	51 -- Card Reader & Conn	
Size	Document Number: Thunder	Rev: 1A
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Move to IOL board

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Title	52 – 15" 1394 Conn	
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Technology Limited

Title	53 – 17" 1394 Conn+ Power	
Size	Document Number Thunder	Rev 1A
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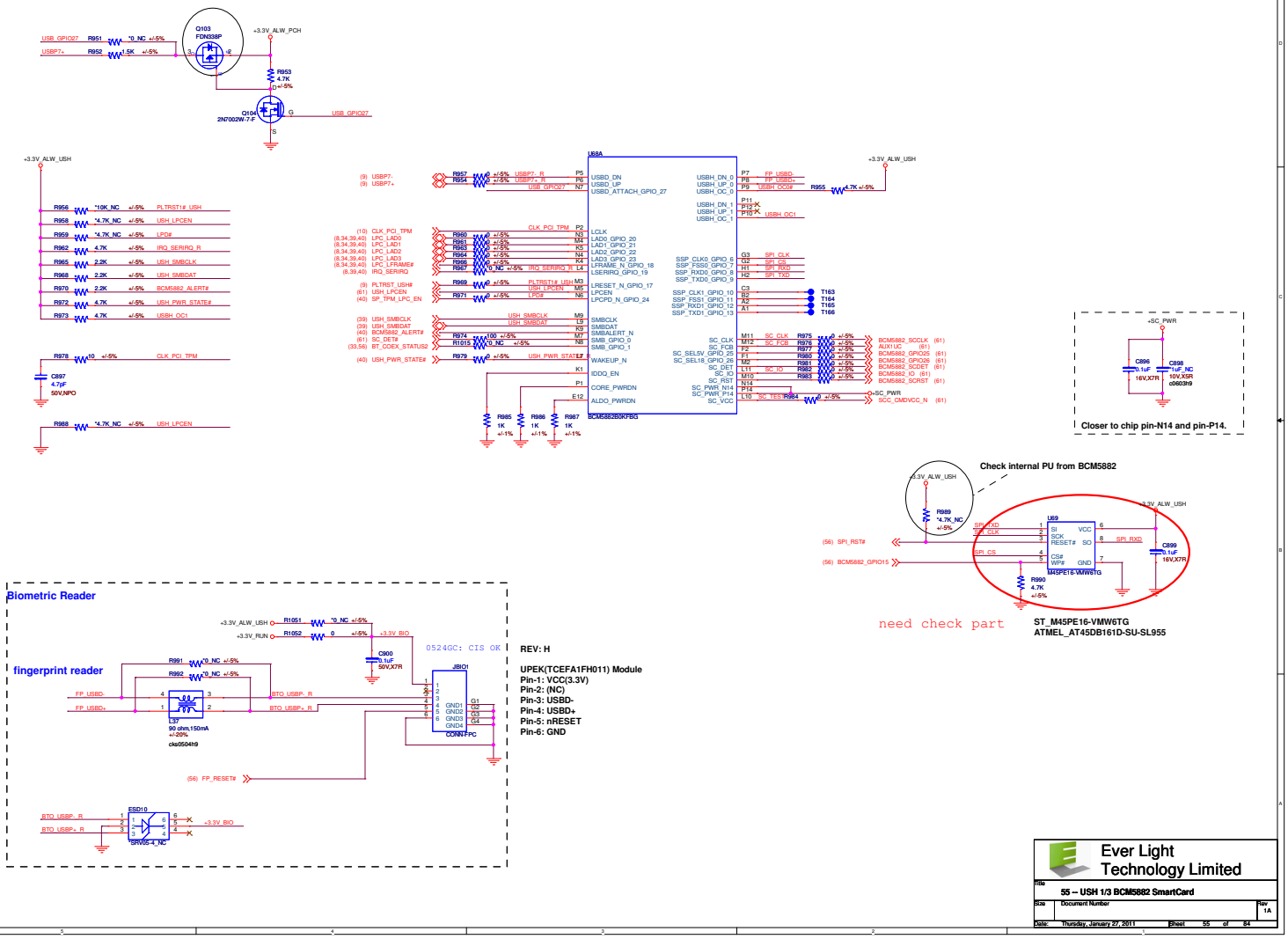
Q103
FDN338P
+3.3V_ALW_PCH
USB_GPIO27
USBP7+
R951 *0_NC +/-5%
R952 1.5K +/-5%
R953 4.7K +/-5%
Q104
2N7002W-7-F
USB_GPIO27
+3.3V_ALW_USH
R956 *10K_NC +/-5% PLTRST1#_USH
R958 *4.7K_NC +/-5% USH_LPCEN
R959 *4.7K_NC +/-5% LPD#
R962 4.7K +/-5% IRQ_SERIRQ_R
R965 2.2K +/-5% USH_SMBCLK
R968 2.2K +/-5% USH_SMBDAT
R970 2.2K +/-5% BCM5882_ALERT#
R972 4.7K +/-5% USH_PWR_STATE#
R973 4.7K +/-5% USBH_OC1
R978 *10 +/-5% CLK_PCI_TPM
C897 4.7pF 50V,NPO
R988 *4.7K_NC +/-5% USH_LPCEN
U68A
BCM5882B0KFBG
USBD_DN
USBD_UP
USBD_ATTACH_GPIO_27
LCLK
LAD0_GPIO_20
LAD1_GPIO_21
LAD2_GPIO_22
LAD3_GPIO_23
LFRAME_N_GPIO_18
LSERIRQ_GPIO_19
LRESET_N_GPIO_17
LPCEN
LPCPD_N_GPIO_24
SMBCLK
SMBDAT
SMBALERT_N
SMB_GPIO_0
SMB_GPIO_1
WAKEUP_N
IDDQ_EN
CORE_PWRDN
ALDO_PWRDN
USBH_DN_0
USBH_UP_0
USBH_OC_0
USBH_DN_1
USBH_UP_1
USBH_OC_1
SSP_CLK0_GPIO_6
SSP_FSS0_GPIO_7
SSP_RXD0_GPIO_8
SSP_TXD0_GPIO_9
SSP_CLK1_GPIO_10
SSP_FSS1_GPIO_11
SSP_RXD1_GPIO_12
SSP_TXD1_GPIO_13
SC_CLK
SC_FCB
SC_SEL5V_GPIO_25
SC_SEL18_GPIO_26
SC_DET
SC_IO
SC_RST
SC_PWR_N14
SC_PWR_P14
SC_VCC
SC_TES
R955 4.7K +/-5%
R957 0 +/-5% USBP7_R
R954 0 +/-5% USBP7+_R
R960 0 +/-5%
R961 0 +/-5%
R963 0 +/-5%
R964 0 +/-5%
R966 0 +/-5%
R967 *0_NC +/-5% IRQ_SERIRQ_R
R969 0 +/-5% PLTRST1#_USH
R971 0 +/-5% LPD#
R974 100 +/-5%
R1015 *0_NC +/-5%
R979 0 +/-5% USH_PWR_STATE#
R985 1K +/-1%
R986 1K +/-1%
R987 1K +/-1%
R975 0 +/-5%
R976 0 +/-5%
R977 0 +/-5%
R980 0 +/-5%
R981 0 +/-5%
R982 0 +/-5%
R983 0 +/-5%
R984 0 +/-5%
T163
T164
T165
T166
+SC_PWR
Closer to chip pin-N14 and pin-P14.
C896 0.1uF 16V,X7R
C898 1uF_NC 10V,X5R c0603h9
Check internal PU from BCM5882
R989 *4.7K_NC +/-5%
U69
M45PE16-VMW6TG
C899 0.1uF 16V,X7R
R990 4.7K +/-5%
need check part
ST_M45PE16-VMW6TG
ATMEL_AT45DB161D-SU-SL955
Biometric Reader
fingerprint reader
R1051 *0_NC +/-5%
R1052 0 +/-5%
+3.3V_BIO
0524GC: CIS OK
C900 0.1uF 50V,X7R
R991 *0_NC +/-5%
R992 *0_NC +/-5%
JBIO1
CONN-FPC
L37
90 ohm,150mA +/-20%
cks0504h9
ESD10
SRV05-4_NC
REV: H
UPEK(TCEFA1FH011) Module
Pin-1: VCC(3.3V)
Pin-2: (NC)
Pin-3: USBD-
Pin-4: USBD+
Pin-5: nRESET
Pin-6: GND
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JTAG_TDI_USH R994 *0_NC +/-5% JTAG_CLK_USH

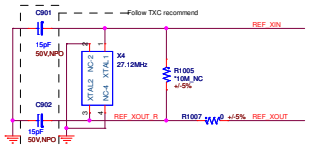
JTAG_TMS_USH R995 *0_NC +/-5% JTAG_TDO_USH

JTCE_USH R996 *0_NC +/-5% JTAG_RST#_USH

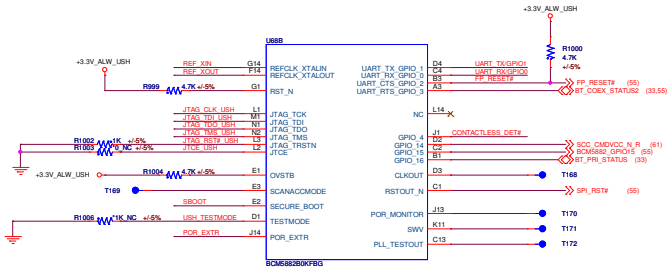
HF_RX_TEST1 R997 *0_NC +/-5% HF_RX_TEST0

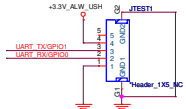
HF_RX_TEST3 R998 *0_NC +/-5% HF_RX_TEST2

27.12Mhz regardless support RFID or not.



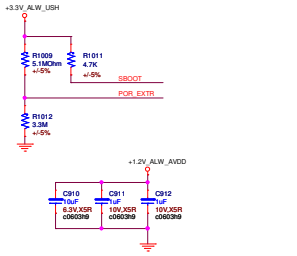
* XTAL CIRCUIT (COMPONENTS + WIRING) SHOULD BE ON TOP LAYER ONLY, TO CONTROL INTERFERENCE

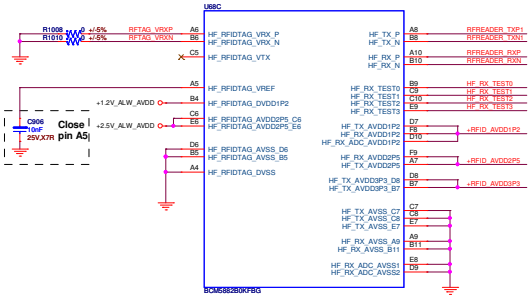


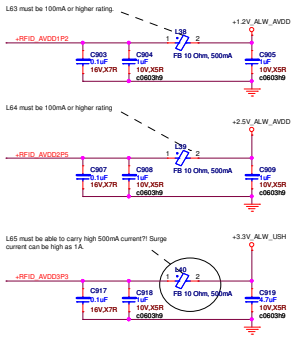


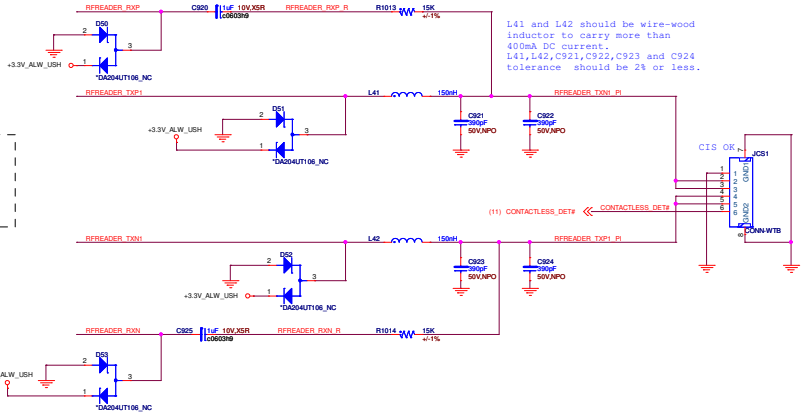
UART_TX/GPIO1, UART_RX_GPIO0, 3.3V_ALW_USH and GND to a connector. This is required for BIOS/FW debugging and EVMCo certification test.

Connector should be placed in place to be easy access by opening cover. Connector can be depop for production.









L41 and L42 should be wire-wood inductor to carry more than 400mA DC current.
L41,L42,C921,C922,C923 and C924 tolerance should be 2% or less.

BRCM : D50, D51, D52, D53 are required for ESD protection, but they could be removed if ODM can guarantee 8kV protection to USH after contacted ESD test.

Note: USH only protect upto 2kV at I/O pins.

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Title	56 -- USH 2/3 BCM5882 RFID	
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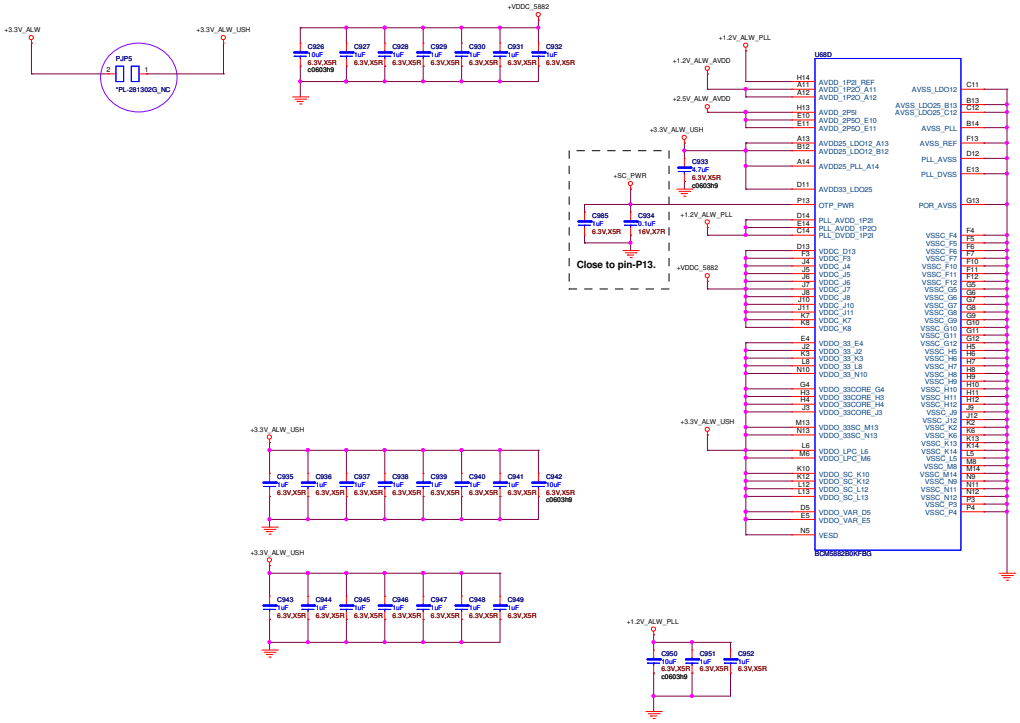

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Title	57 -- USH 3/3 BCM5882 Power	
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Move to IOL board

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Title
58 -- Smart Card IC & Conn

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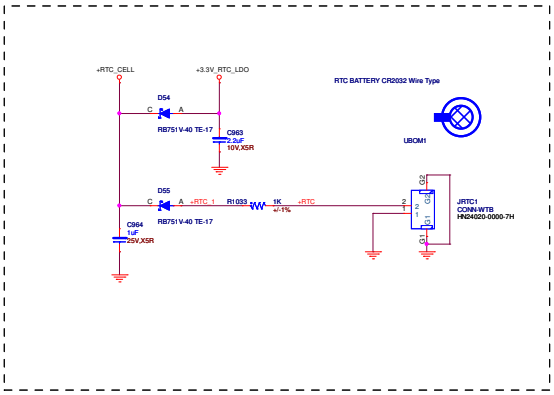

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Title	58 – System Reset, RTC	
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Technology Limited

Title

Blank Page

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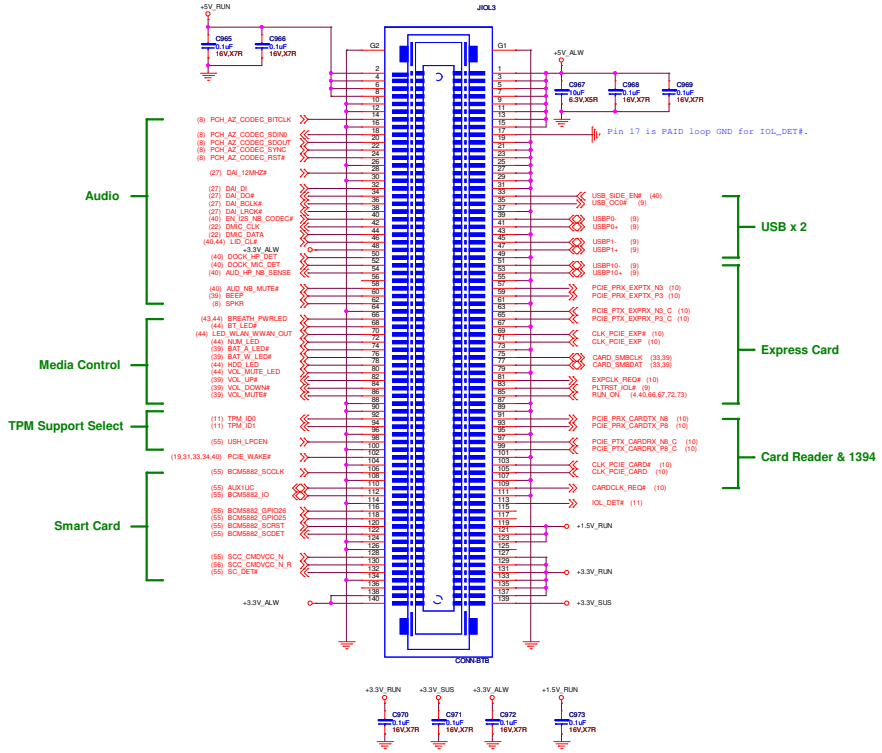
0607GC: CIS OK



Ever Light Technology Limited			
Title	76 -- Blank Page		
Size	Document Number		Rev 1A
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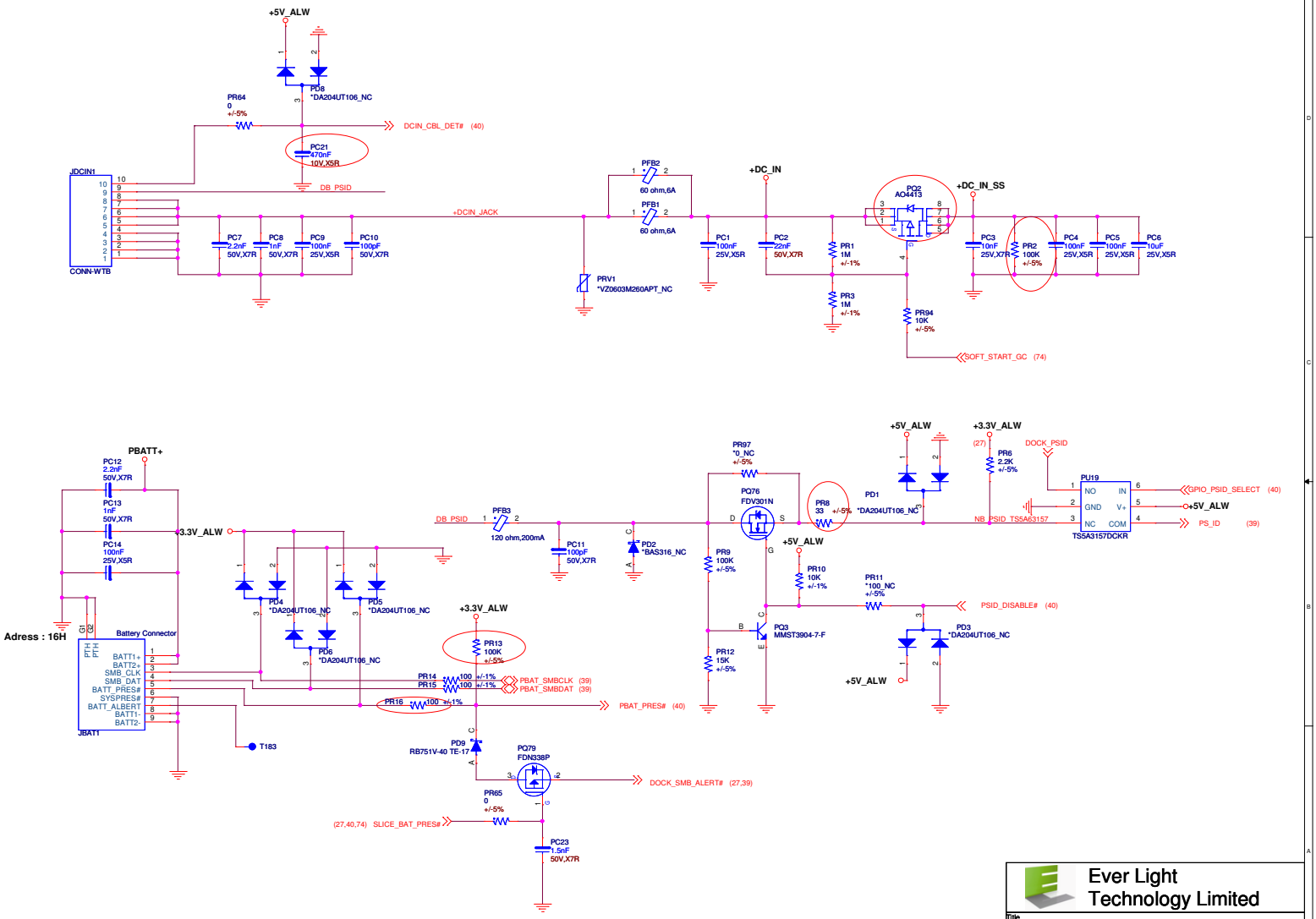

Ever Light Technology Limited	
Title	PW_DCin & Batt
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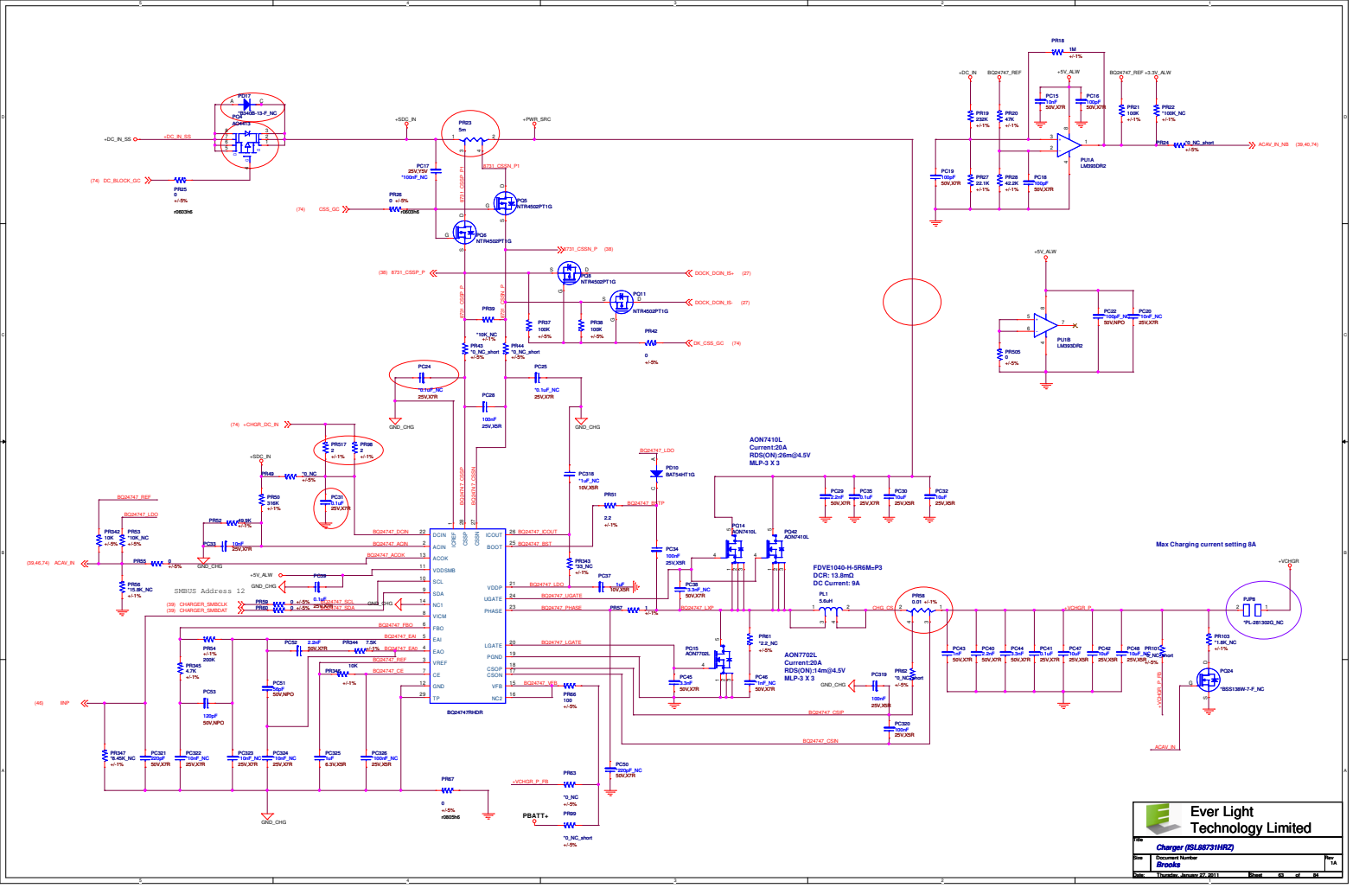
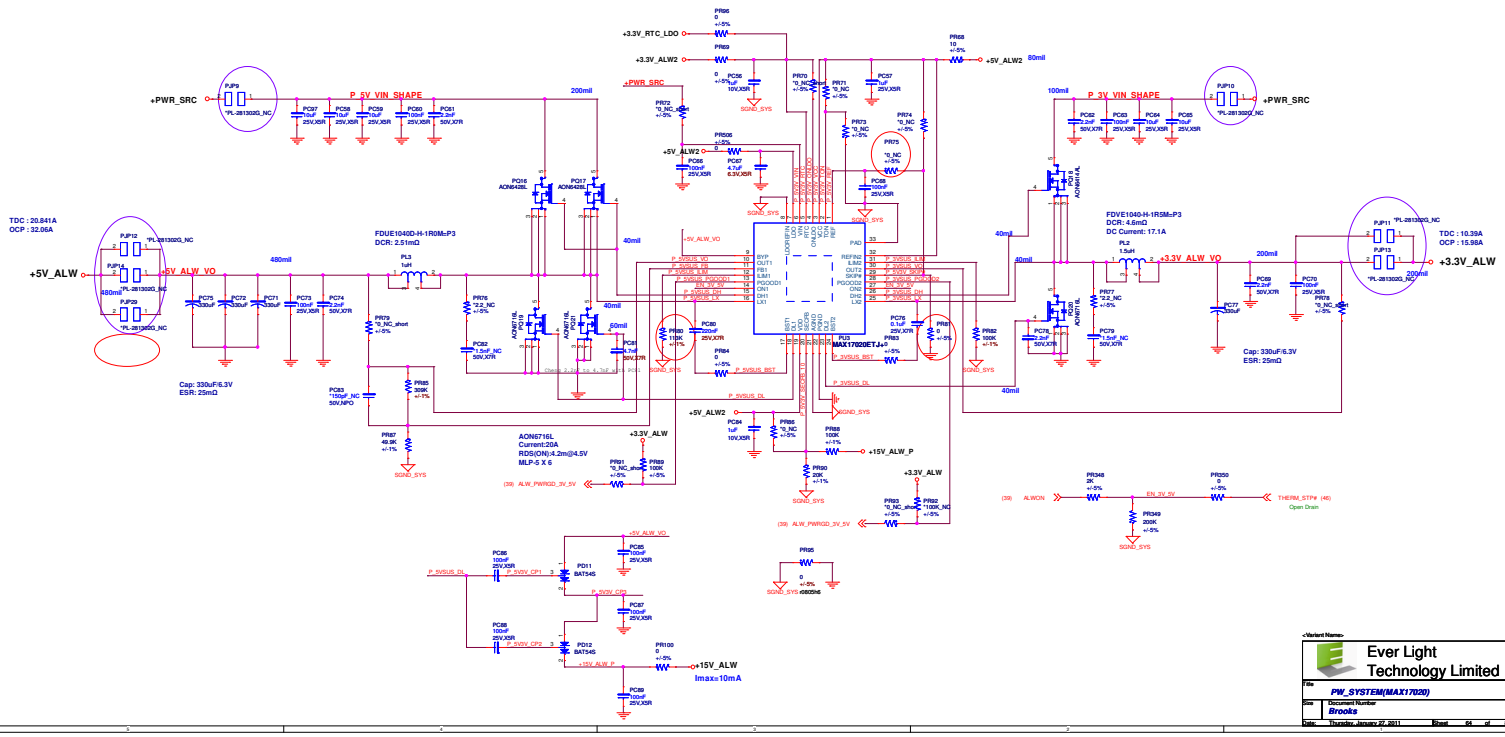

Max Charging current setting 8A
AON7410L
Current:20A
RDS(ON):26m@4.5V
MLP-3 X 3
FDVE1040-H-5R6M=P3
DCR: 13.8mΩ
DC Current: 9A
AON7702L
Current:20A
RDS(ON):14m@4.5V
MLP-3 X 3
SMBUS Address 12
BQ24747RHDR
PBATT+
Ever Light
Technology Limited
Charger (ISL88731HRZ)
Brooks
Thursday, January 27, 2011

+5V_ALW / +3.3V_ALW POWER SUPPLY



<Variant Name>
Ever Light Technology Limited
File: PW_SYSTEM(MAX17020)
Size: Document Number: Brooks
Rev: 1A
Date: Thursday, January 27, 2011
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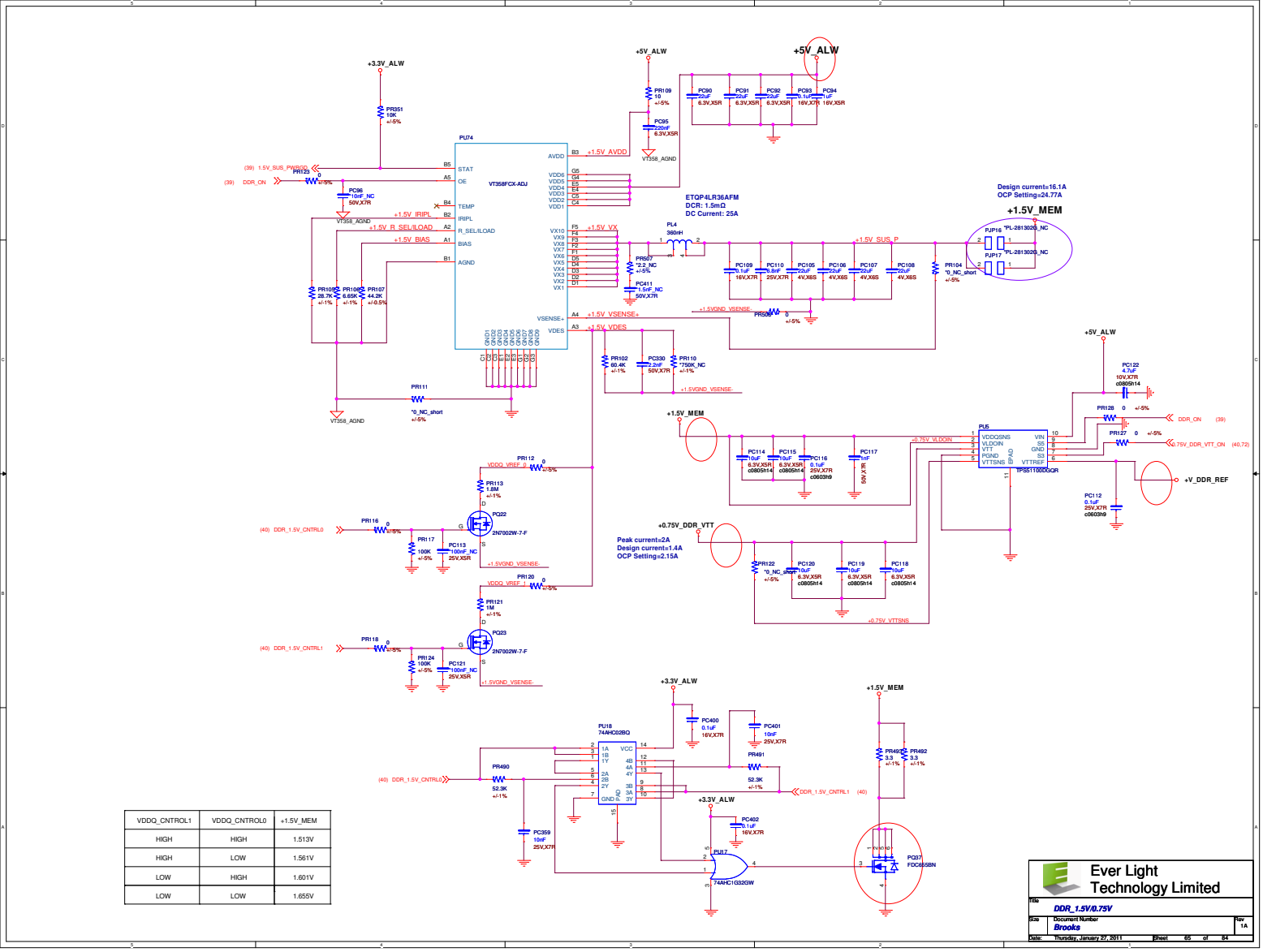

VDDQ_CNTROL1	VDDQ_CNTROL0	+1.5V_MEM
HIGH	HIGH	1.513V
HIGH	LOW	1.561V
LOW	HIGH	1.601V
LOW	LOW	1.655V

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Title	DDR_1.5V/0.75V	
Size	Document Number: Brooks	Rev: 1A
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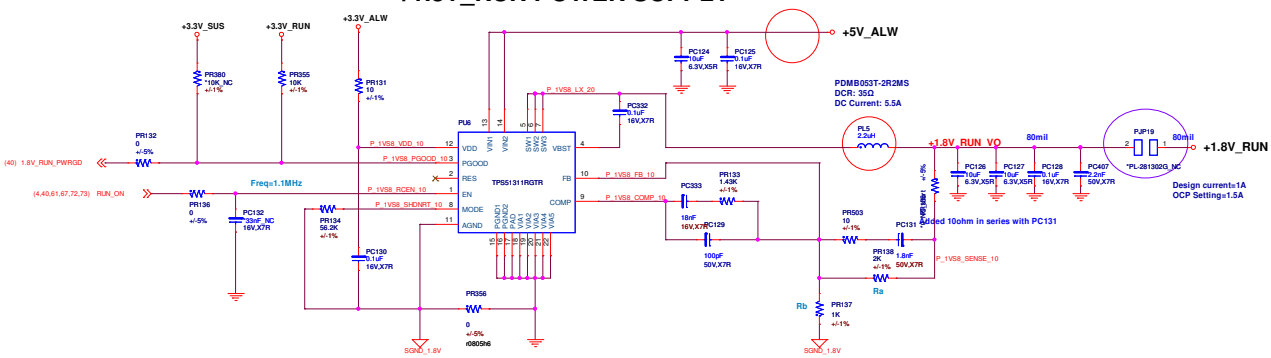
+1.8V_RUN POWER SUPPLY



<Variant Name>

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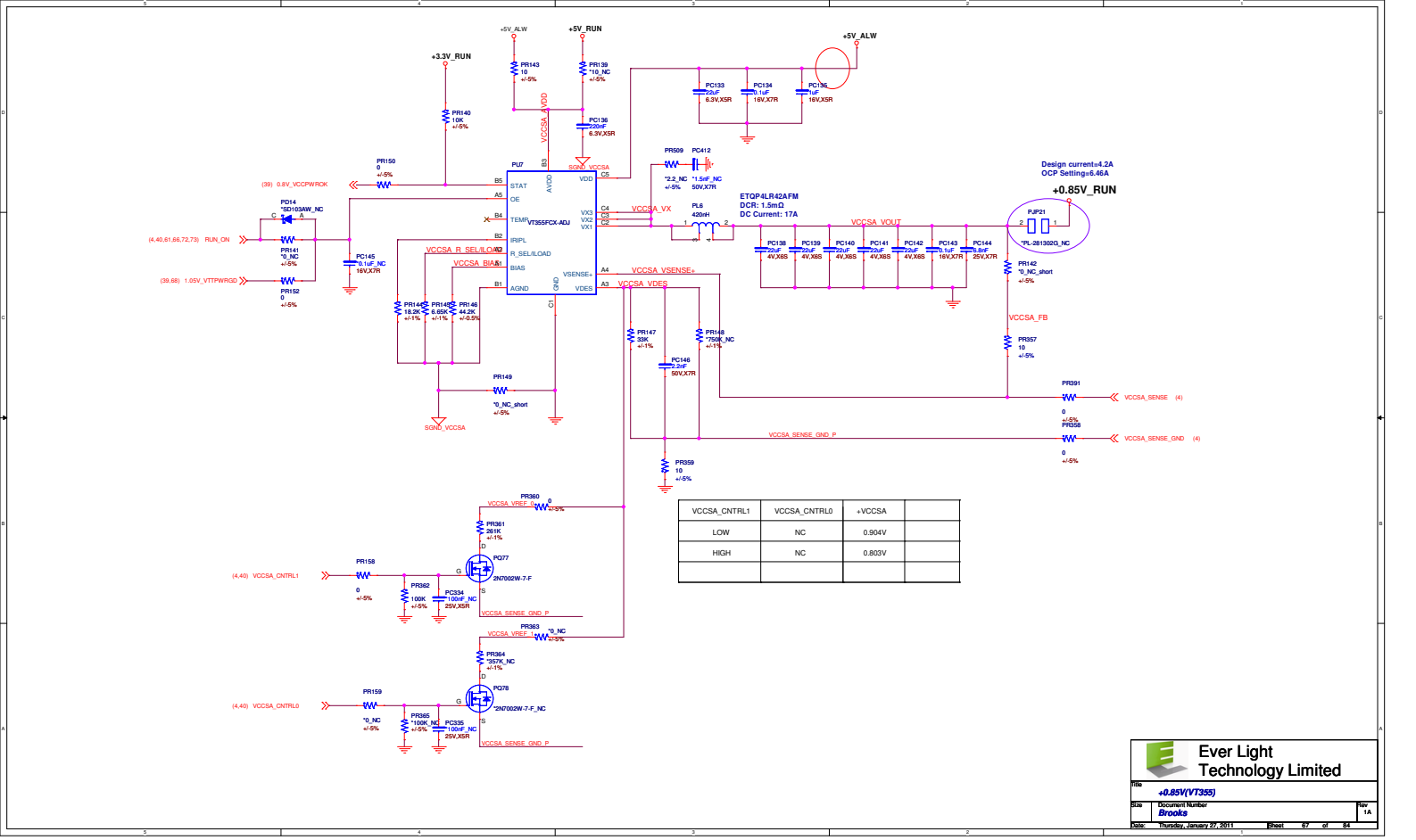
Title	PW_SW_+1.8V(TPS51311)	
Size	Document Number: Brooks	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 66 of 84	



VCCSA_CNTRL1	VCCSA_CNTRL0	+VCCSA	
LOW	NC	0.904V	
HIGH	NC	0.803V	

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Title	+0.85V(VT355)	
Size	Document Number: Brooks	Rev: 1A
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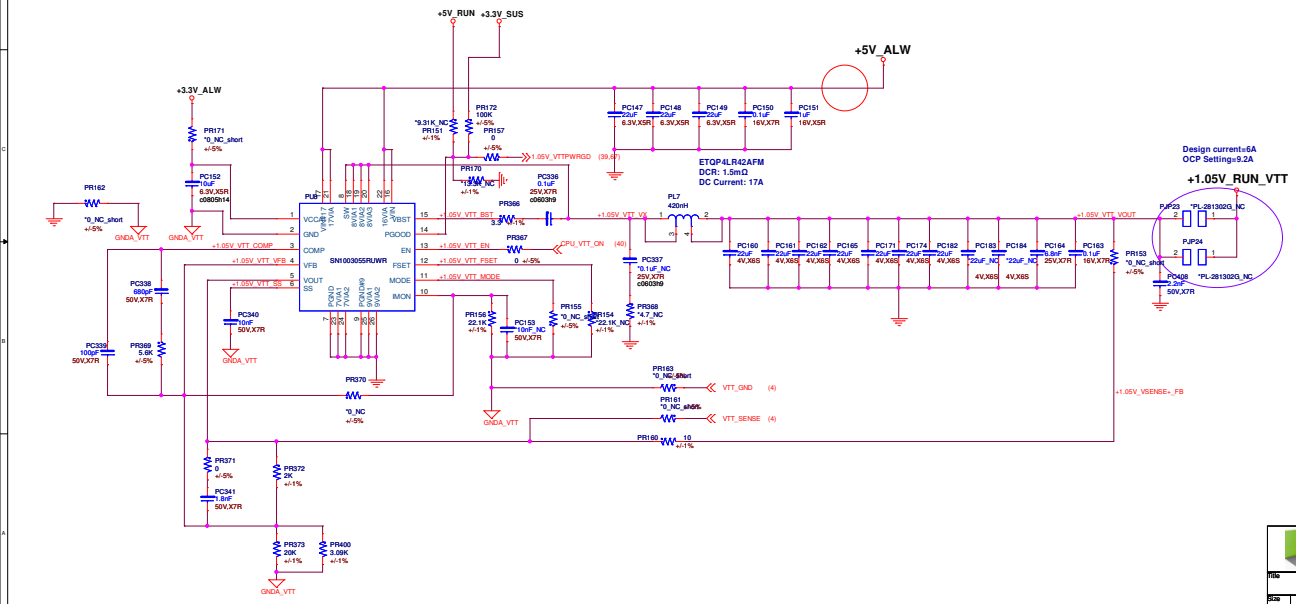

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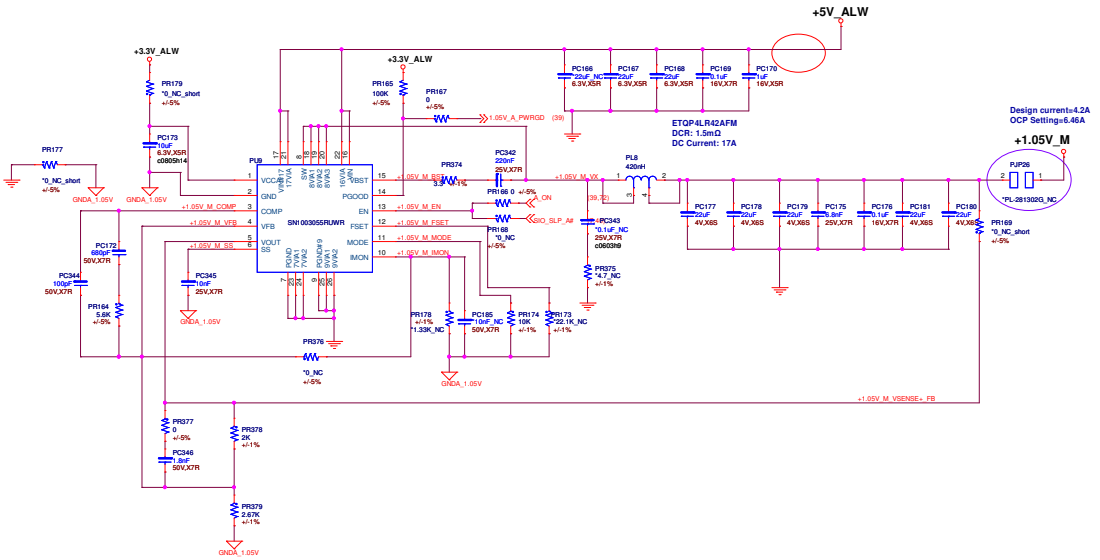
Title	PW_+1.05V_VTT(SN1003055RUWR)	
Size	Document Number: Brooks	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 68 of 84	



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Title	PW_+1.05VM(VT355)	
Size	Document Number: Brooks	Rev: 1A
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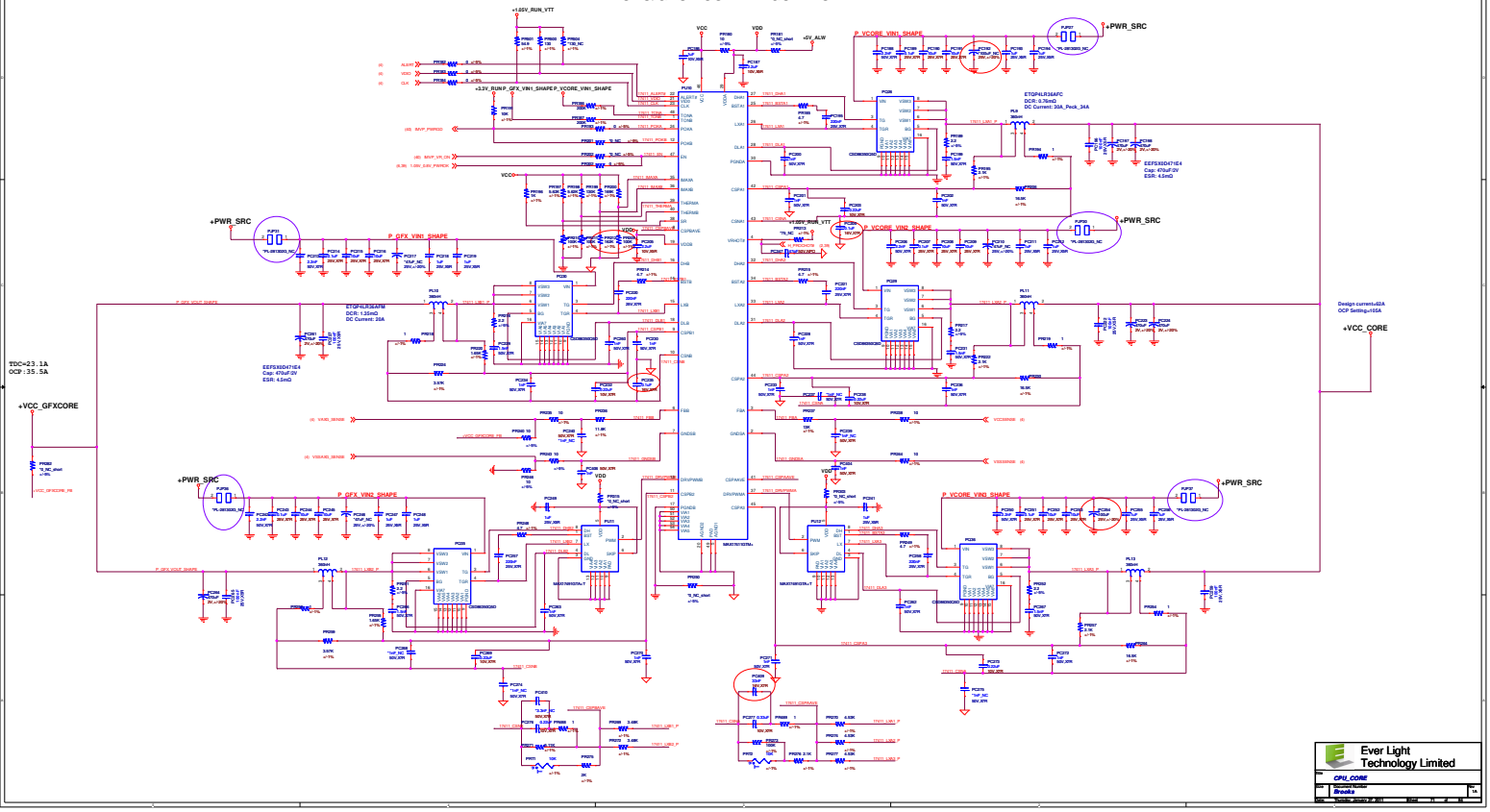
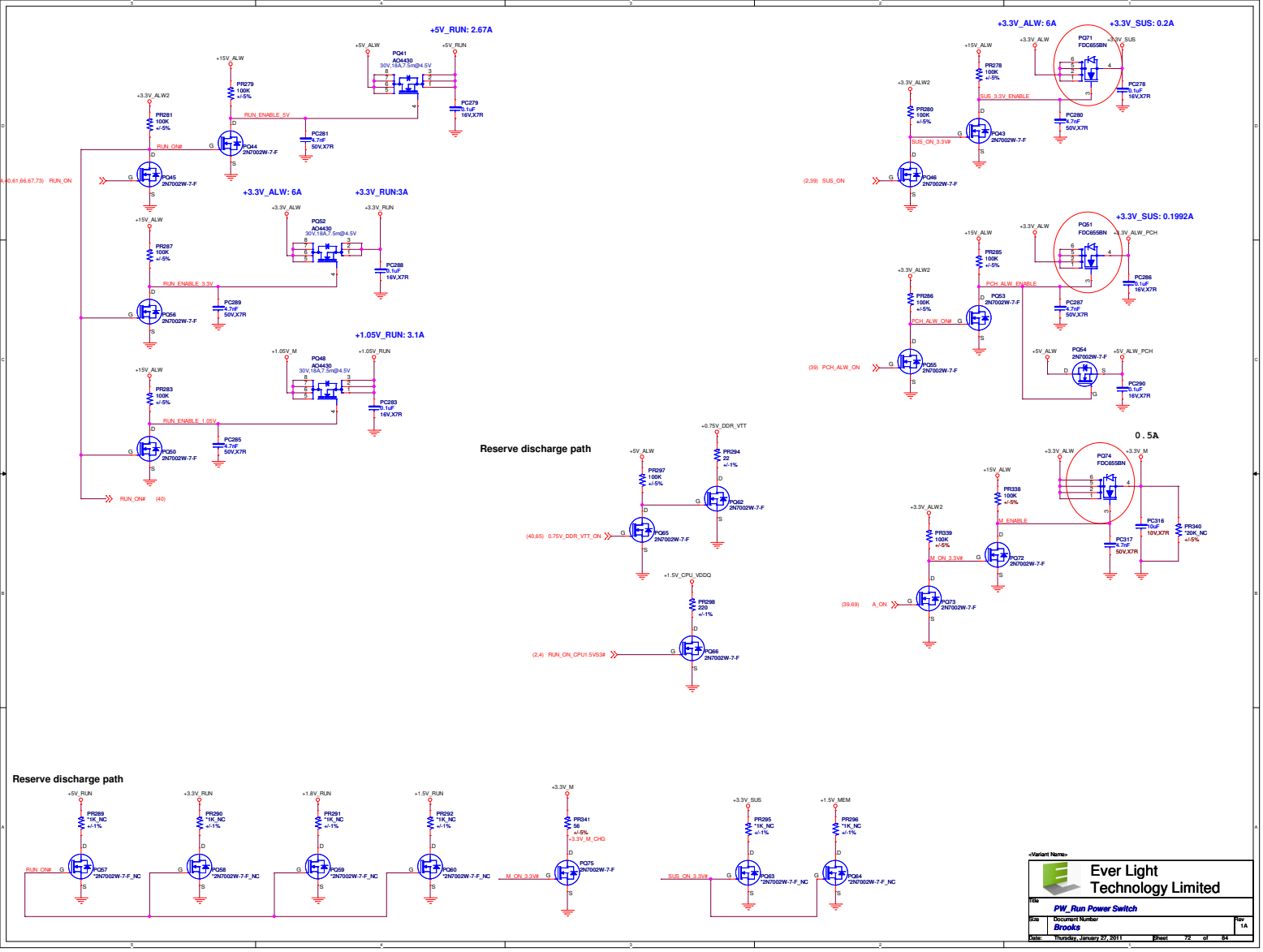
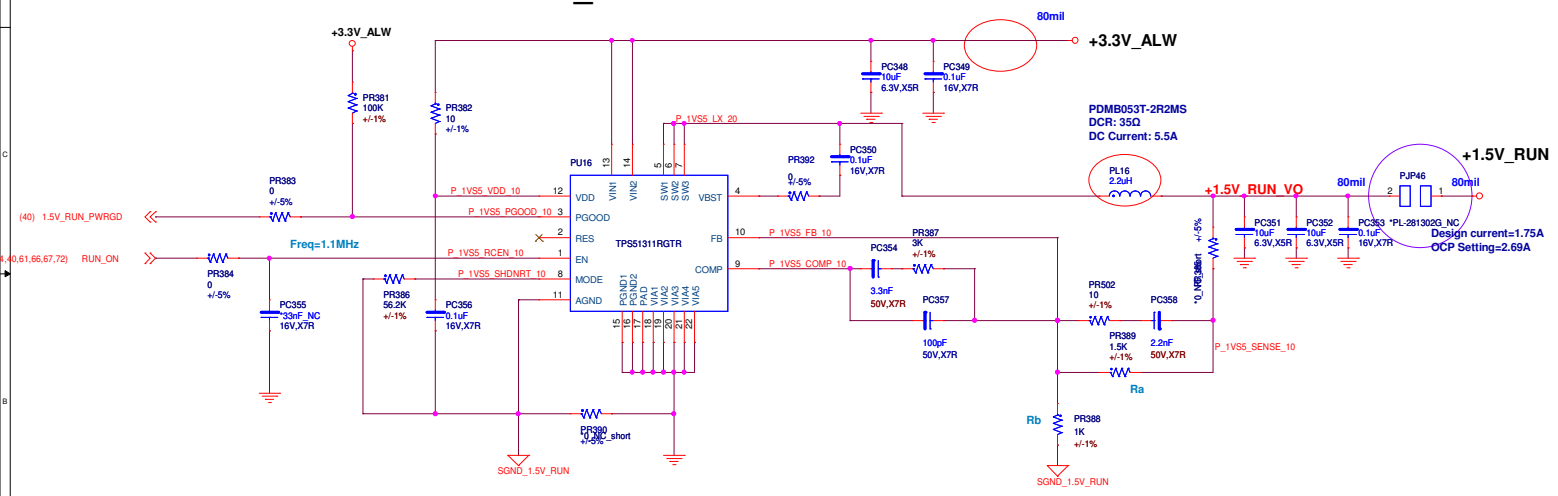
Title	<Title>
Size: A	Document Number: <Doc>
Rev	<RevCo
Date:	Thursday, January 27, 2011
Sheet	70 of 84

IMVP7 CPU/GPU VCORE REGULATOR




+5V_RUN: 2.67A
+3.3V_ALW: 6A
+3.3V_SUS: 0.2A
+3.3V_SUS: 0.1992A
+3.3V_ALW: 6A
+3.3V_RUN:3A
+1.05V_RUN: 3.1A
0.5A
Reserve discharge path
Reserve discharge path
RUN_ON#
RUN_ENABLE_5V
RUN_ENABLE_3.3V
RUN_ENABLE_1.05V
SUS_3.3V_ENABLE
PCH_ALW_ON#
M_ENABLE
SUS_ON_3.3V#
M_ON_3.3V#
+3.3V_M_CHG
RUN_ON
SUS_ON
PCH_ALW_ON
0.75V_DDR_VTT_ON
RUN_ON_CPU1.5VS3#
A_ON
Ever Light Technology Limited
PW_Run Power Switch
Brooks
Thursday, January 27, 2011
72
84

+1.5V_RUN POWER SUPPLY



<Variant Name>

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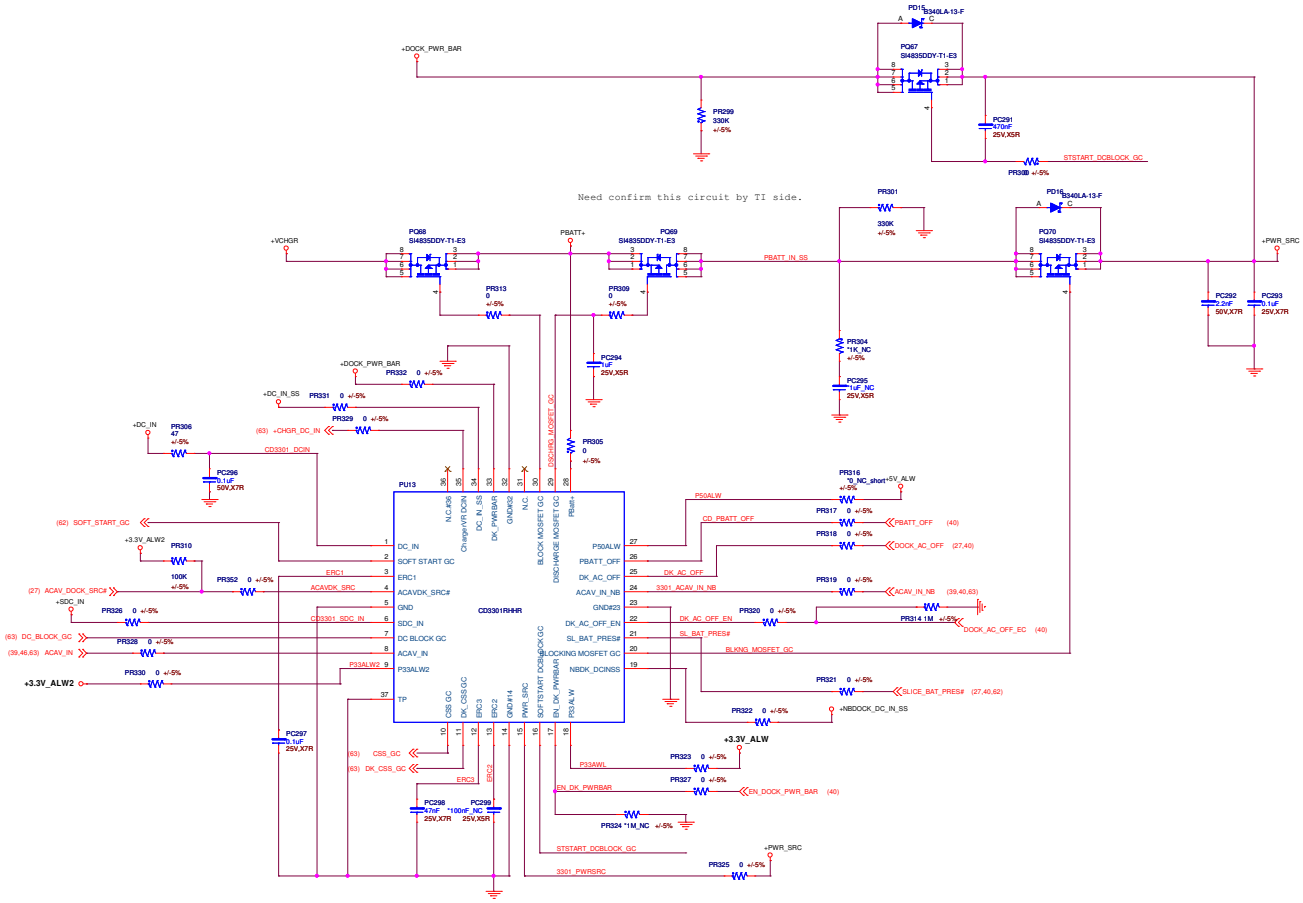
Title	PW_SW_+1.8V(TPS51311)	
Size	Document Number: Brooks	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 73 of 84	



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Title	Docking Selector(CD3301)	
Size	Document Number: Brooks	Rev: 1A
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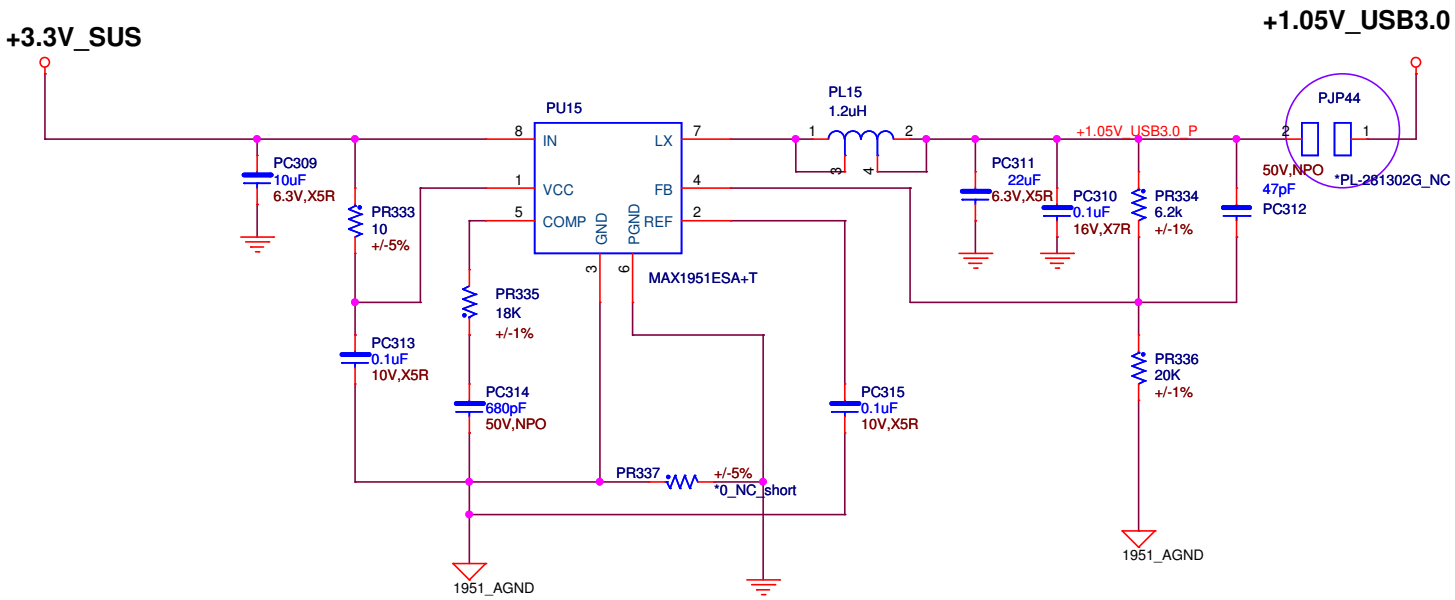
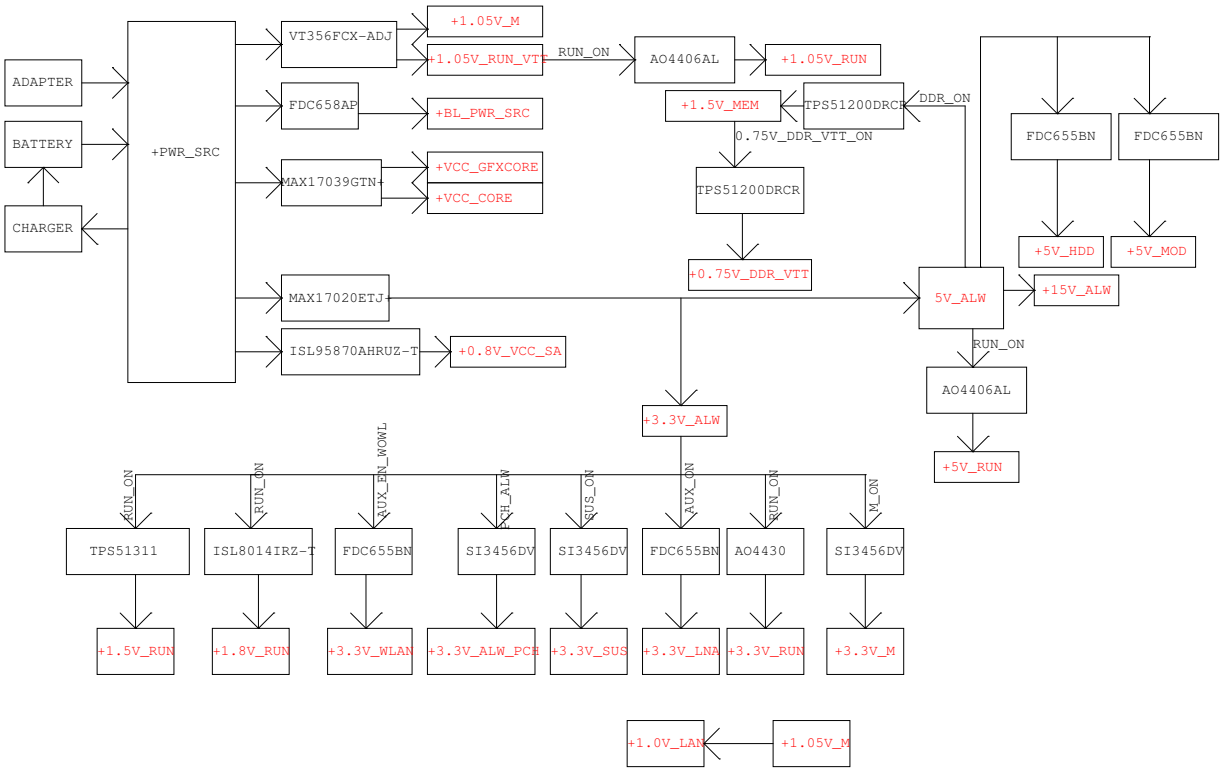
Title	Black	
Size	Document Number: Brooks	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 75 of 84	



Ever Light Technology Limited		
Title	*+1.05V_USB3.0*	
Size	Document Number *Brooks*	Rev 1A
Date: Thursday, January 27, 2011	Sheet 76 of 84	



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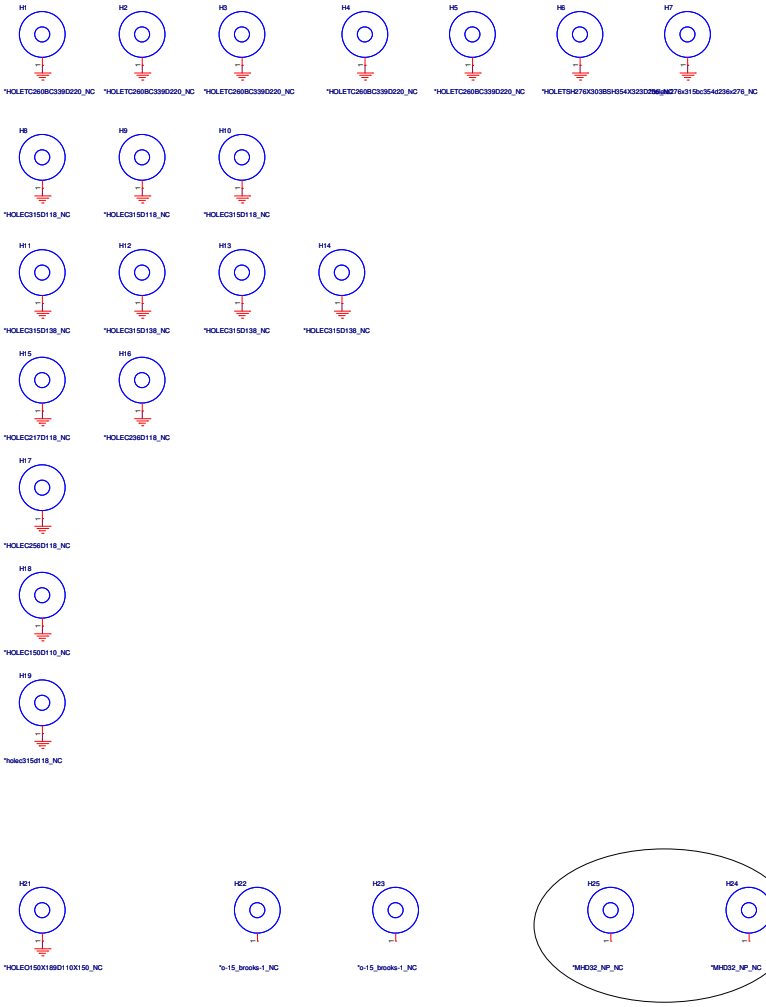
Title	99 -- Media Control	
Size	Document Number	Rev 1A
Date: Thursday, January 27, 2011	Sheet 77 of 84	



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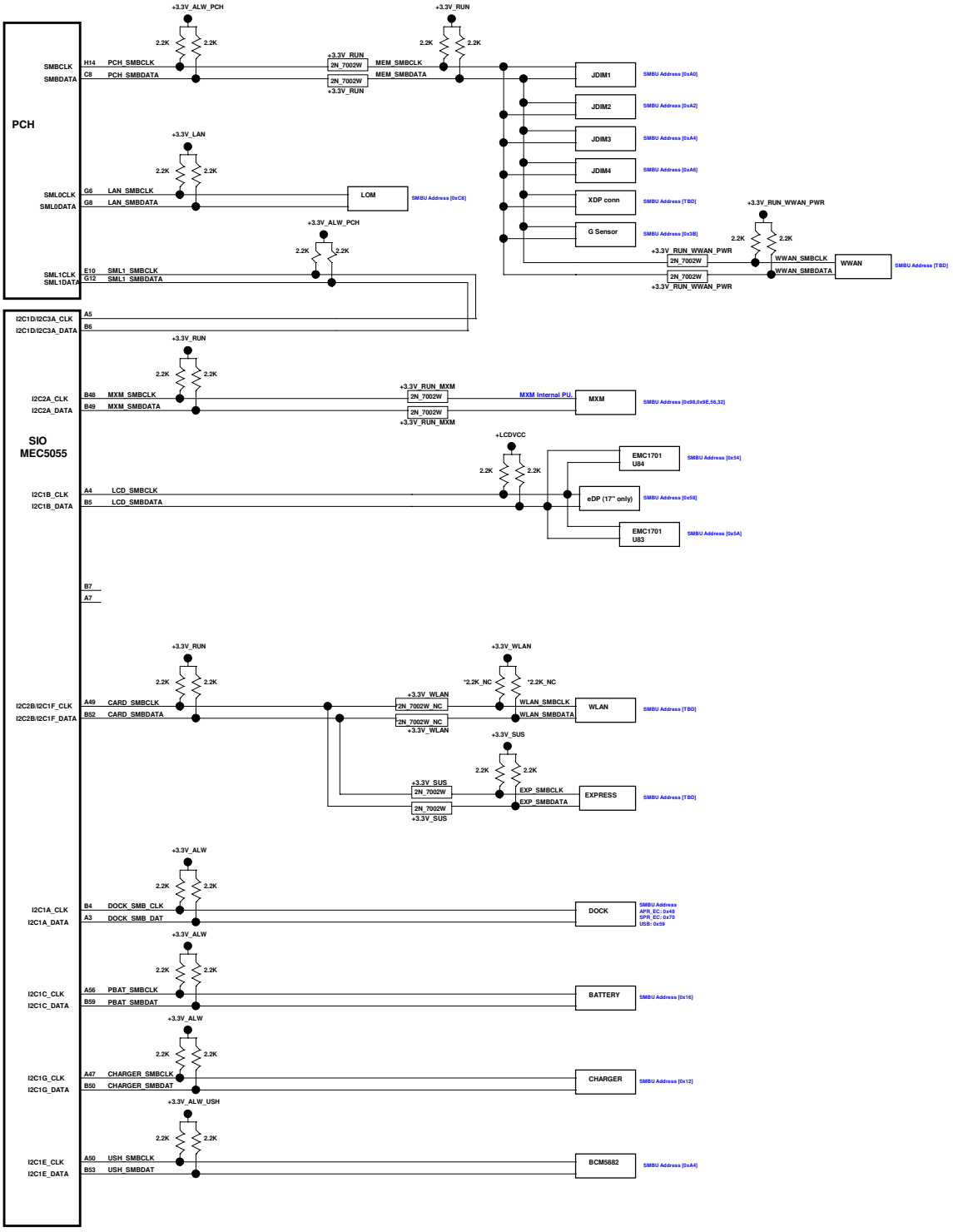
Title	71 -- PAD,SCREW & Stiching CAPs	
Size	Document Number: Thunder	Rev: 1A
Date: Thursday, January 27, 2011	Sheet 75 of 84	



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72 – SMBus Block Diagram

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Title	73 -- Power Sequency Diagram	
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Title	74 -- Power Sequency Timing	
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Change List

Item	Date	Page#	Issue Description
			A00
1.	0112	02	Per Intel DG, eDP_HPD can be NC. NC R57.
2.	0112	02	R39 change from 5.1K to 4.99K.
3.	0112	39	Per Macallan sch, RESET_OUT# PD 8.2K is no necessary. NC R712.
4.	0112	42	JSPI1 NC.
5.	0112	9	PCI_REQ2# PU resistor change from 100K to 10K.
6.	0112	12	Per Intel DG, +PCH_V5REF_SUS C184 change from 1uF to 0.1uF.
7.	0112	39	TOUCH_SCREEN_PD# PD resistor is not necessary. NC R1836.
8.	0112	40	DCIN_CBL_DET# PU resistor change from 10K to 100K.
9.	0112	39	DOCK_SMB_ALERT# PU resistor change from 100K to 10K.
10.	0117	55~57	Update Broadcom 5882 PN from BCM5882TB0KFBG to BCM5882B0KFBG.
11.	0117	27	Change C499 to ESD12 and delete C500. adding ESD13 at DOCK_RST_R# and update to CIS part.
12.	0117	39	Update board ID to A00.
13.	0117	44	Remove volume mute LED, NC Q81.
14.	0117	23	Change F1 from fuse (2411) to Polyswitch type (1206).
15.	0117	23	Adding two NPTH screw hole (MHD32_NP)
16.	0117	22	Populate camera USB common mode choke.
17.	0120	11	Update PCH GPIO28 circuit, delete Q36 and connect SLP_ME_CSW_DEV# to PCH GPIO28 dircetly. Adding 4.7K PU to +3.3V_ALW_PCH.
18.	0120	39	Update board ID value to 8.2K.
19.	0120	25	Brooks 15 change R470 from 5.11k ohms to 5.49k ohms, Brooks 17 change R1927 from 5.11k ohms to 5.6k ohms
20.	0127		Update PCH and LOM PN. 5055 new PN has no available and change to TBD.

POWER SATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0(Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (Soft off) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3(Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	ON	OFF	OFF
S4 (Suspend to HDD) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (Soft off) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power Plane	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
PCH	0	Right Side top
	1	Right Side bot
	2	Back Side
	3	NC
	4	2nd Mini Card (WLAN/WIMAX)
	5	1st Mini Card (WWAN)
	6	3rd Mini Card
	7	USH
	8	DOCKING
	9	DOCKING
	10	Express Card
	11	BlueTooth
	12	Camera
	13	LCD Touch or Nvidia 3D IR

USH	0	BIO
	1	NC

	PCI EXPRESS	DESTINATION
PCH	Lane 1	1st Mini Card WWAN
	Lane 2	2nd Mini Card WLAN
	Lane 3	Express Card
	Lane 4	USB 3.0
	Lane 5	3rd Mini-Card
	Lane 6	4th Mini-Card
	Lane 7	LAN
	Lane 8	Card Reader

	SATA	DESTINATION
PCH	SATA 0	HDD 1st
	SATA 1	HDD 2nd
	SATA 2	MINI CARD
	SATA 3	ODD
	SATA 4	E-SATA
	SATA 5	Docking

	MXM PORT	CONNECTION
MXM Graphics Module	PORT A	MB DP Port
	PORT B	DOCK DP2
	PORT C	DOCK DP1 and MB HDMI
	PORT D	eDP Panel

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Title	99 -- Media Control	
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Change List

Item	Date	Page#	Issue Description
			ST2_power
1.	1229	62	PR2 change from 10K to 100K for E3 levrage
2	1229	64	Change to skip mode: PR75 to NC, PR81 to stuff
3	1230	63	PR58 footprint change from r2512_1h7 to r2512_1h7_mlk
4	1231	63	PD17 no stuff
			A00_power
5	0117	62	PR13 change from 10K to 100K
6	0117	62	PR8 change from 100 to 33 (change from 0603 t0 0402)
7	0117	62	PR8 change from 100 to 33
8	0117	63	PC24 stuff to follow on E3
9	0117		Udpate total 23 jumps
10	0118	62	PR16 move to front of battery connector.
11	0125	63	PC24 no stuff.
12	0125	62	PC21 stuff.
13	0126	71	AL cap change from PC192 to PC254. PC192 no stuff for temp.

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PROJECT : Thunder	DOC. NO. : xxx	REV : M00	
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY:	SHEET 1 OF 1

Title: 75 -- Change List

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